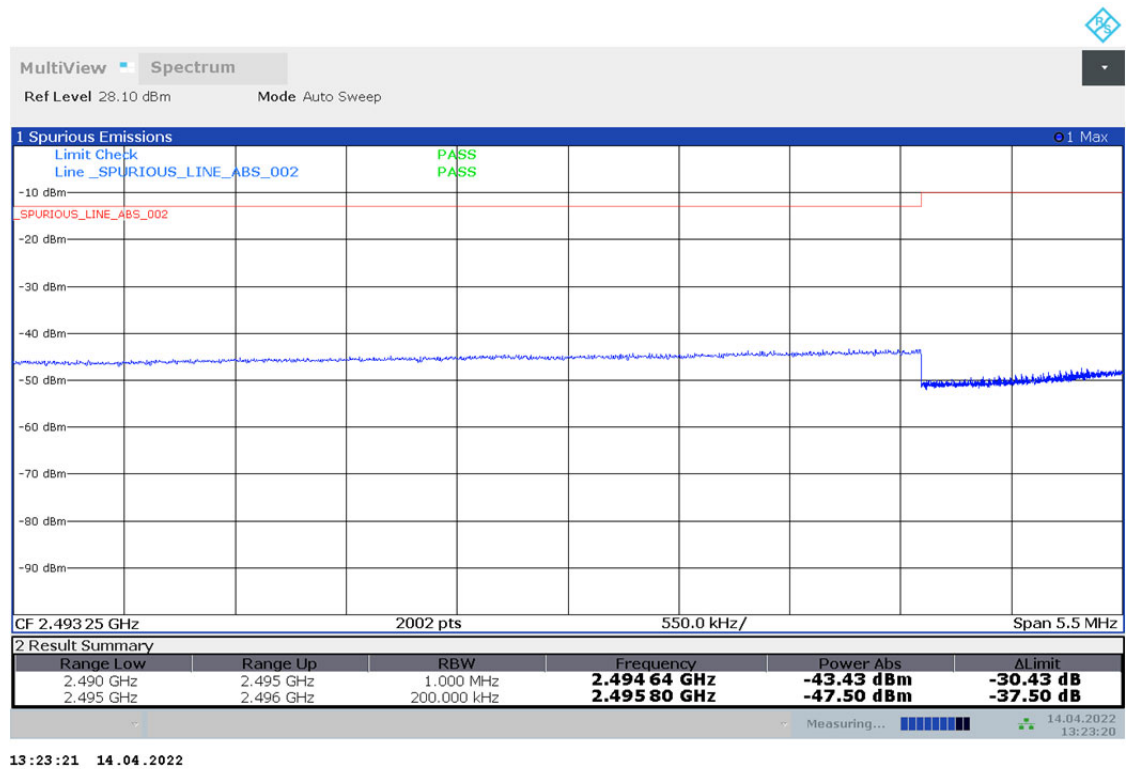
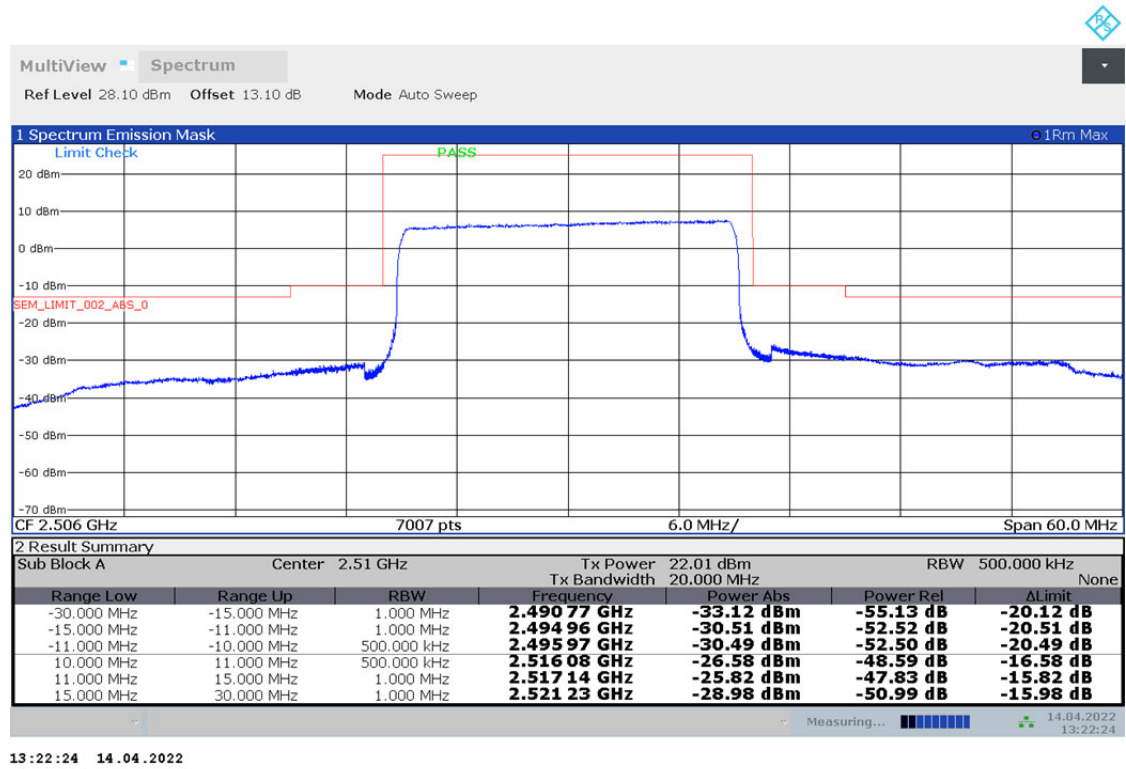
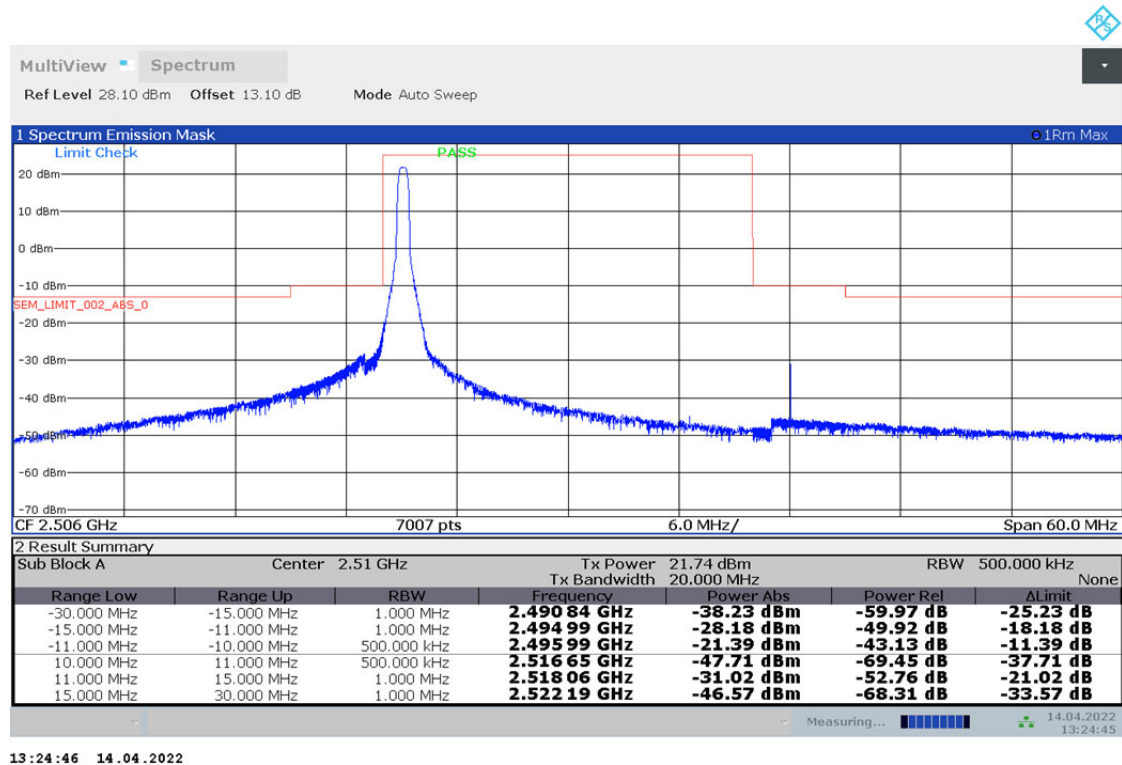


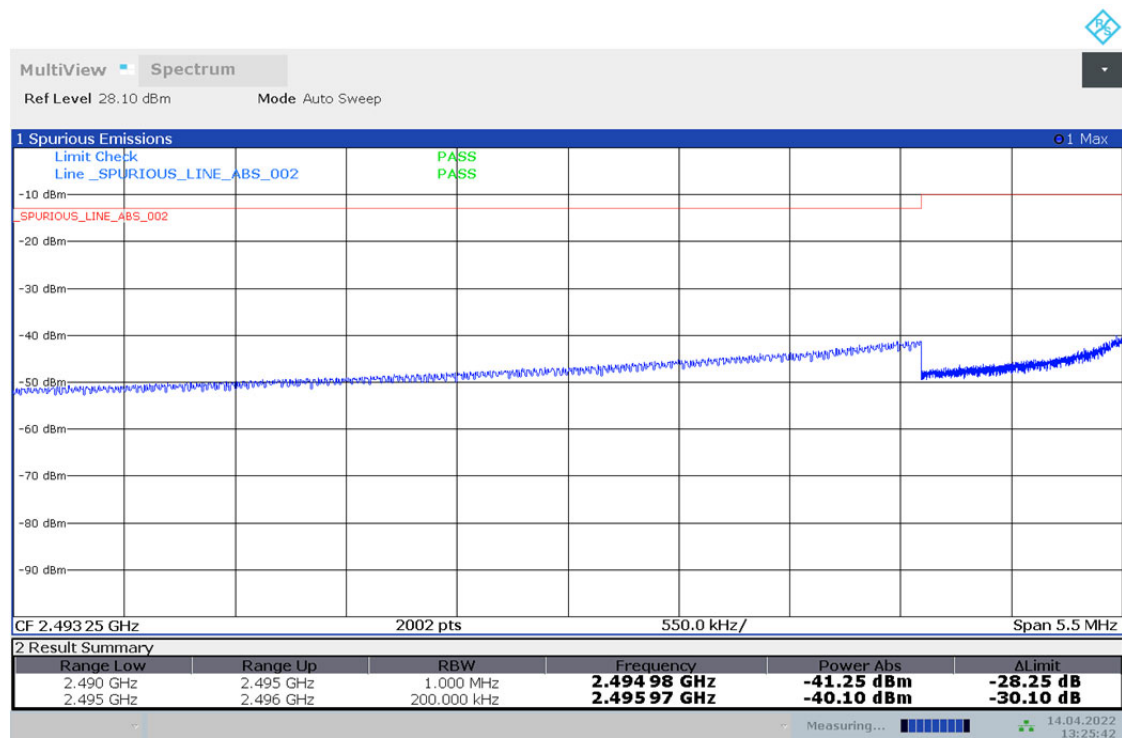
5.2.7 TM1_20MHz_LCH_RB100#0



5.2.8 TM1_20MHz_LCH_RB1#0

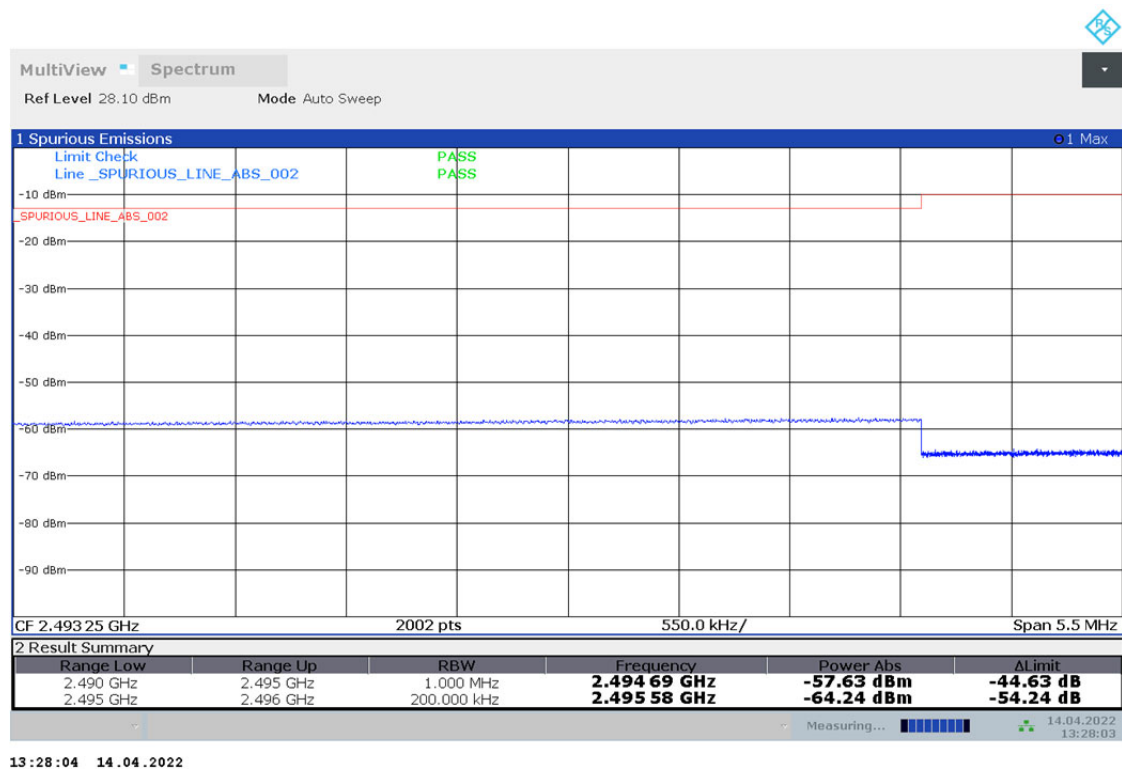
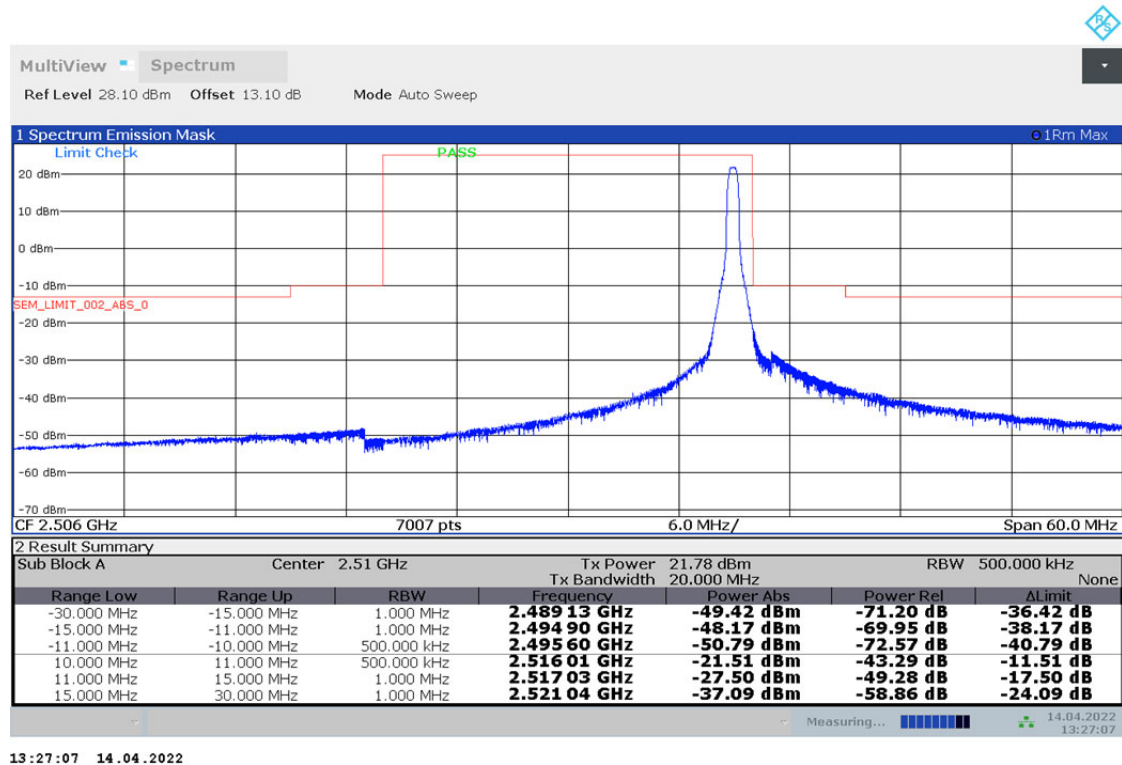


13:24:46 14.04.2022

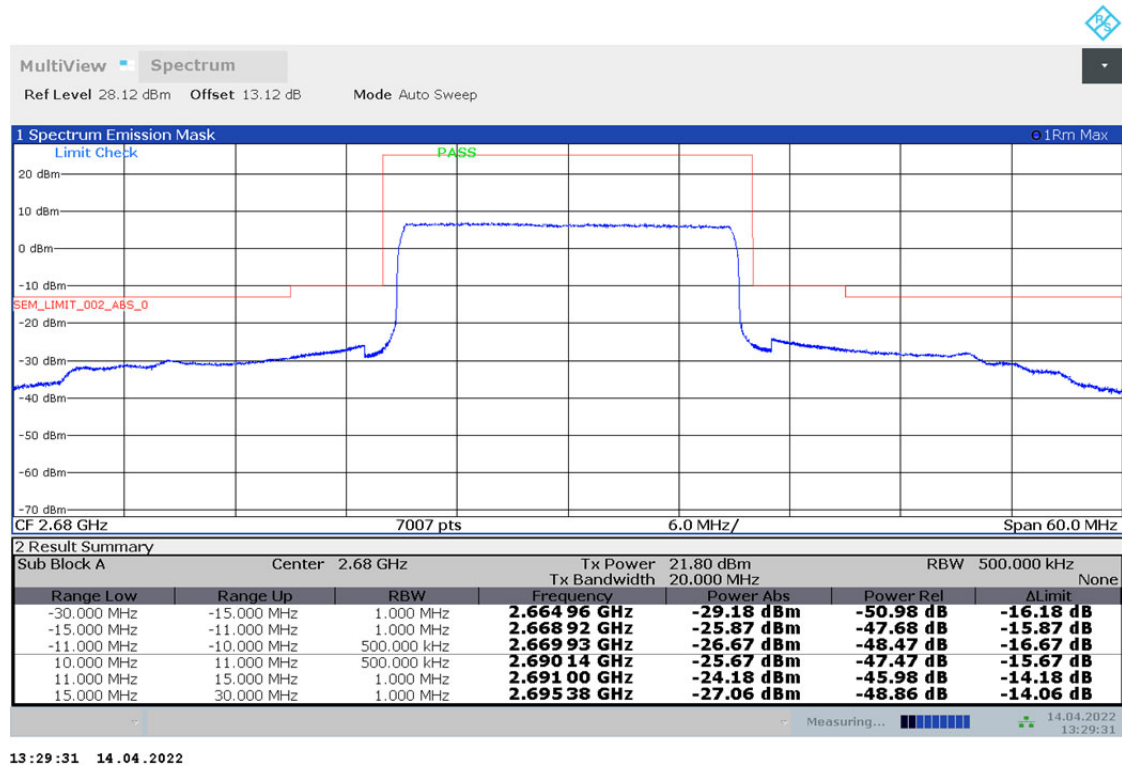


13:25:42 14.04.2022

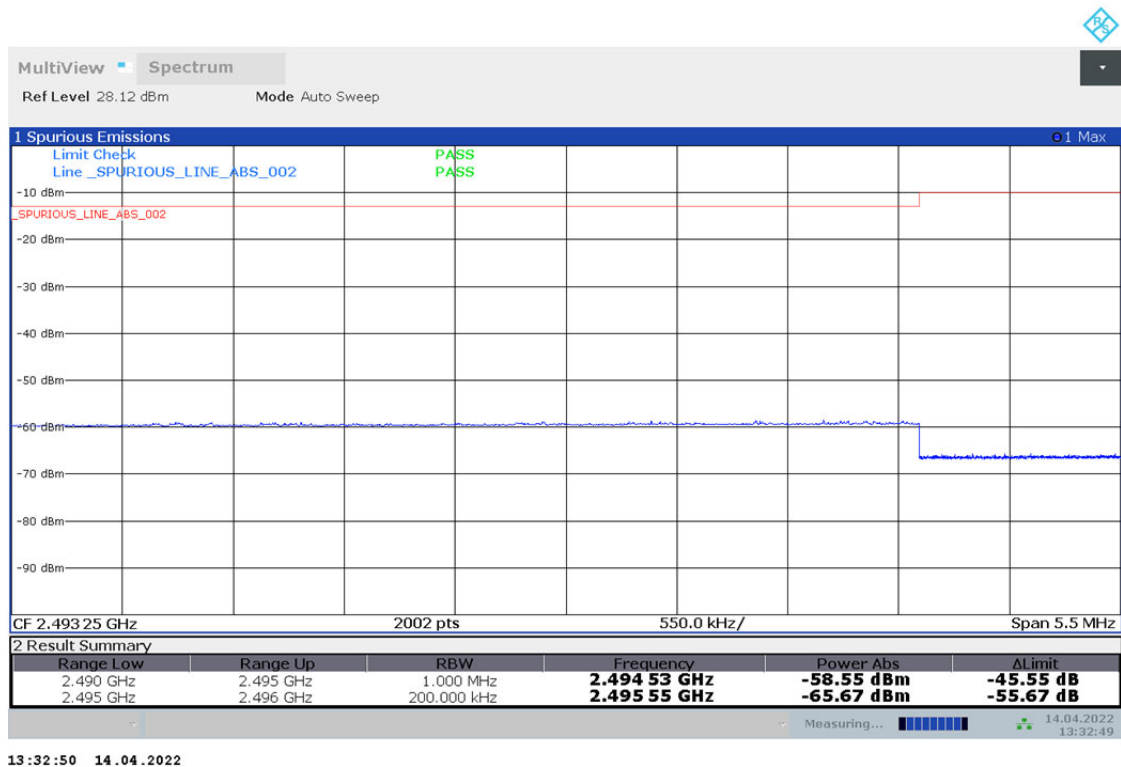
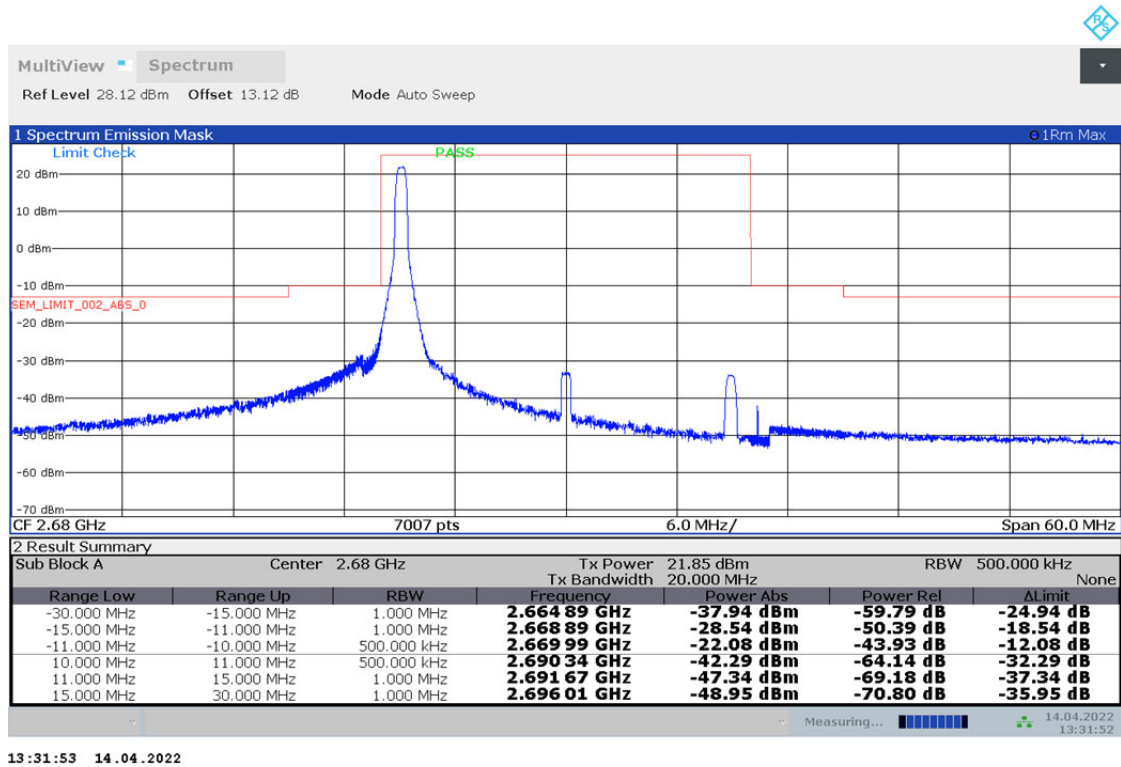
5.2.9 TM1_20MHz_LCH_RB1#99



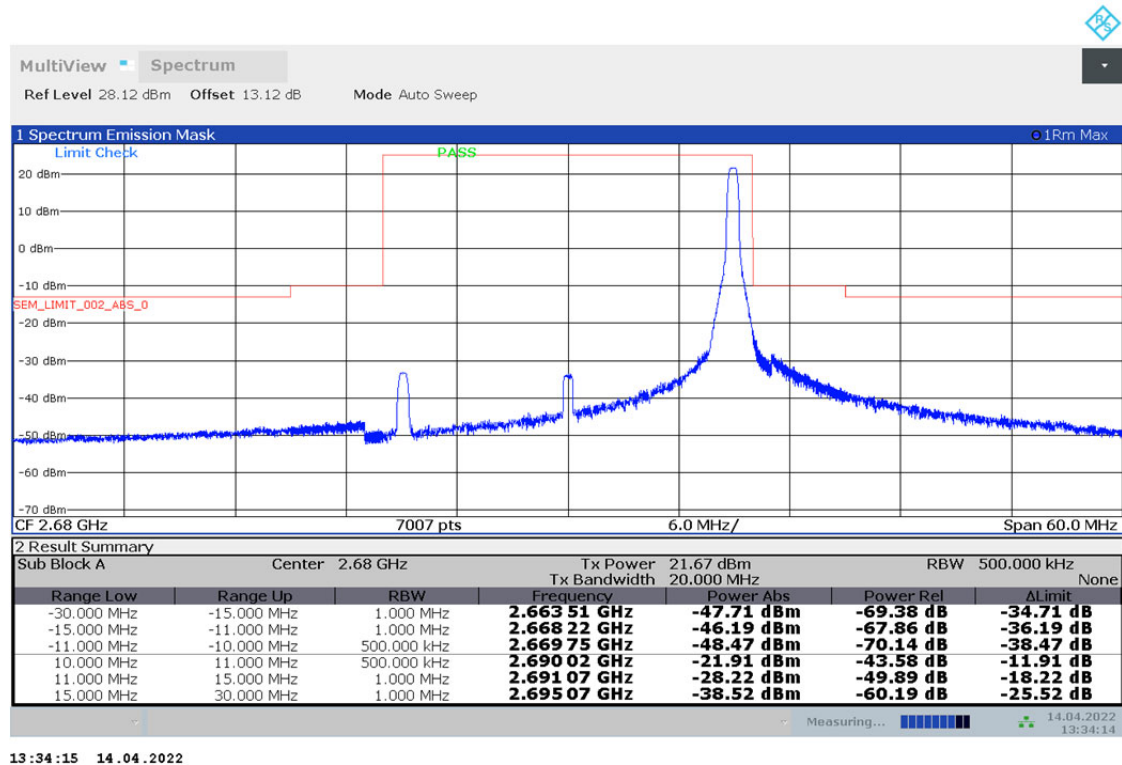
5.2.10 TM1_20MHz_HCH_RB100#0



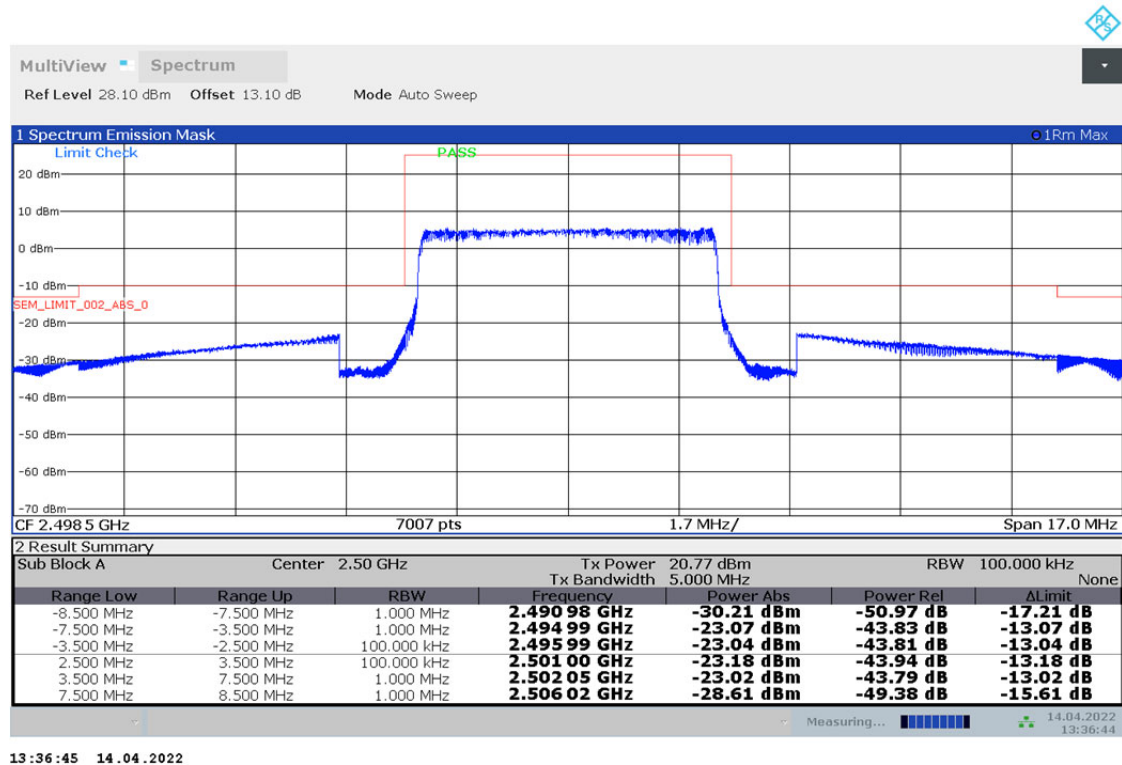
5.2.11 TM1_20MHz_HCH_RB1#0



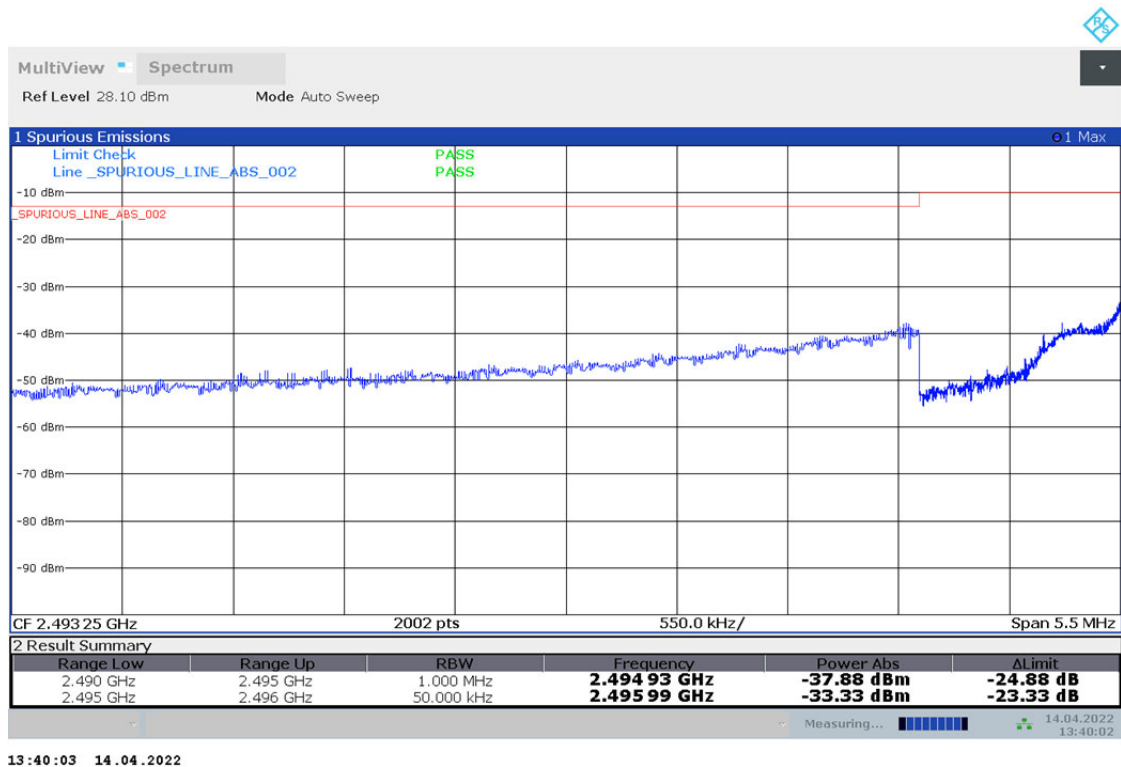
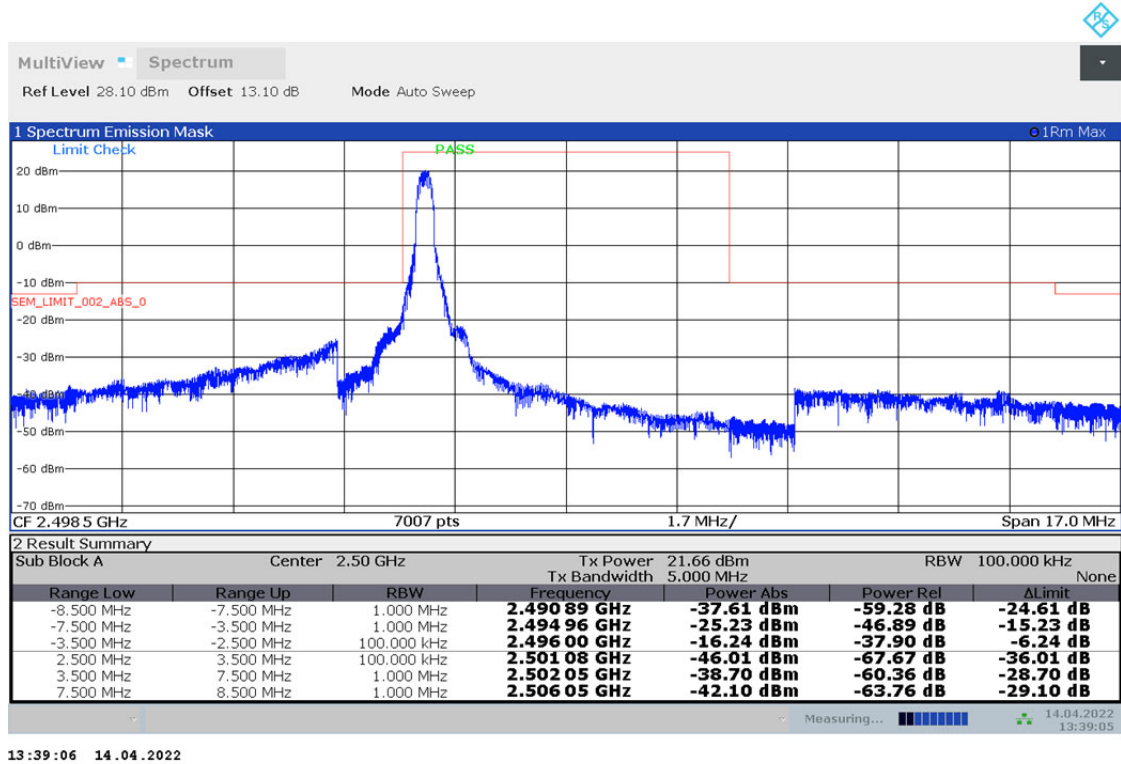
5.2.12 TM1_20MHz_HCH_RB1#99



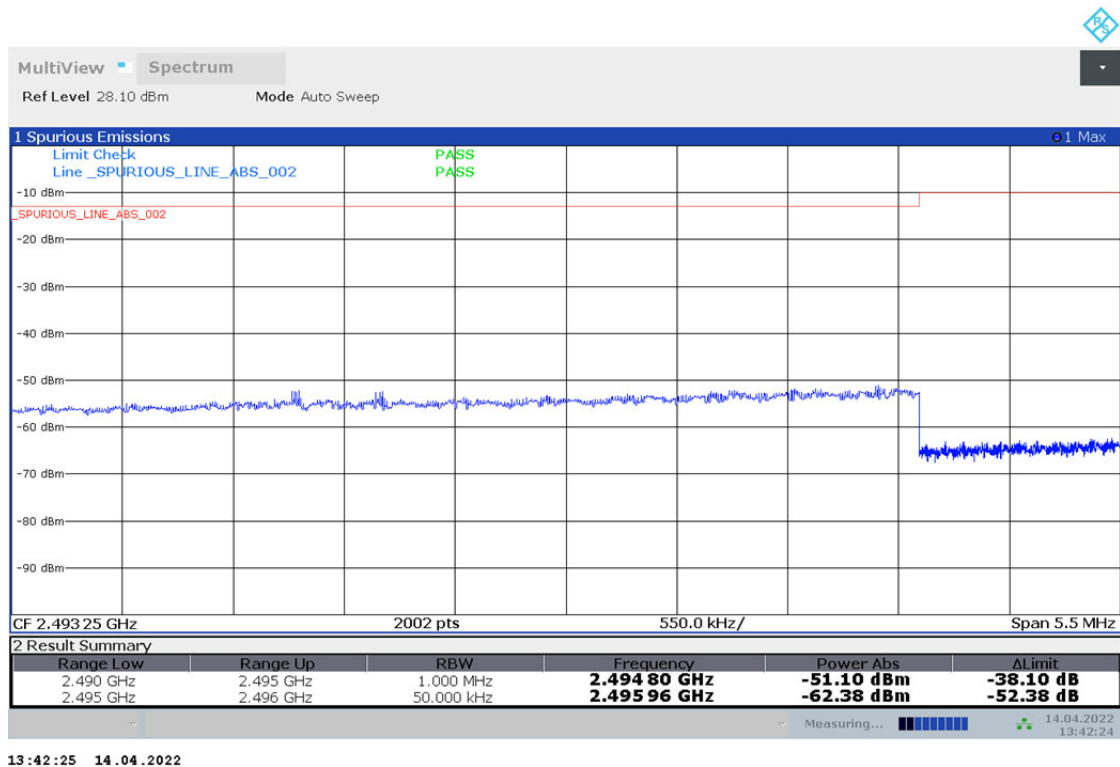
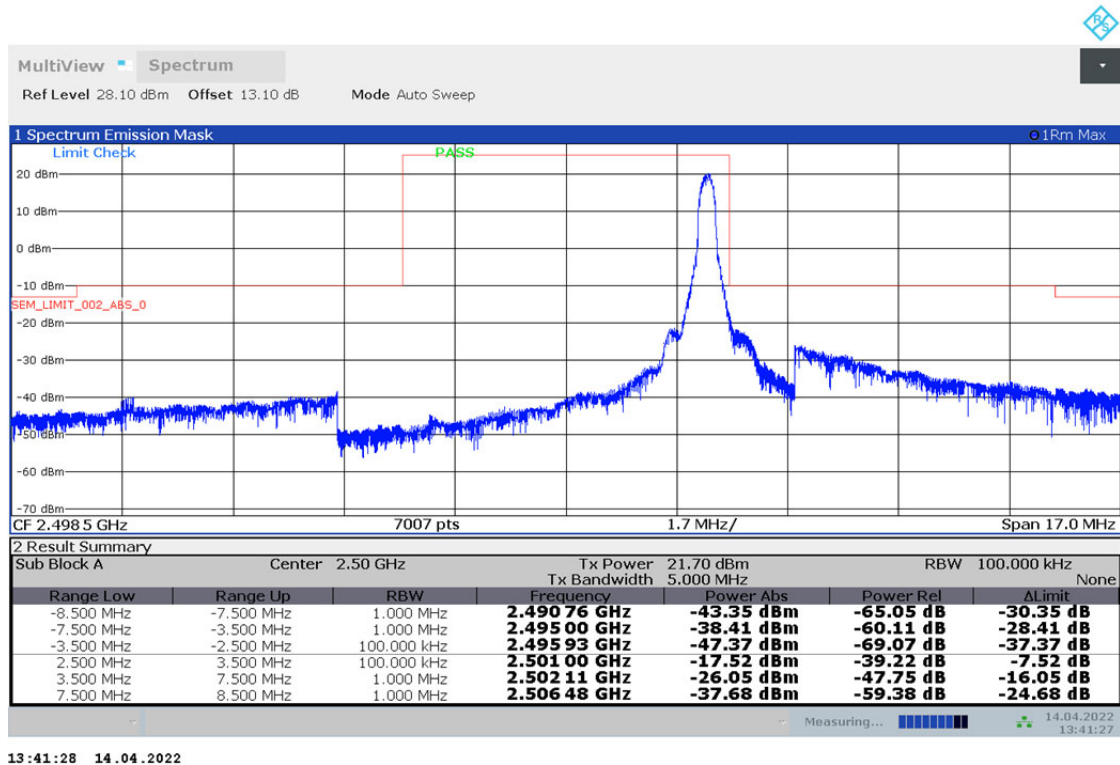
5.2.13 TM2_5MHz_LCH_RB25#0



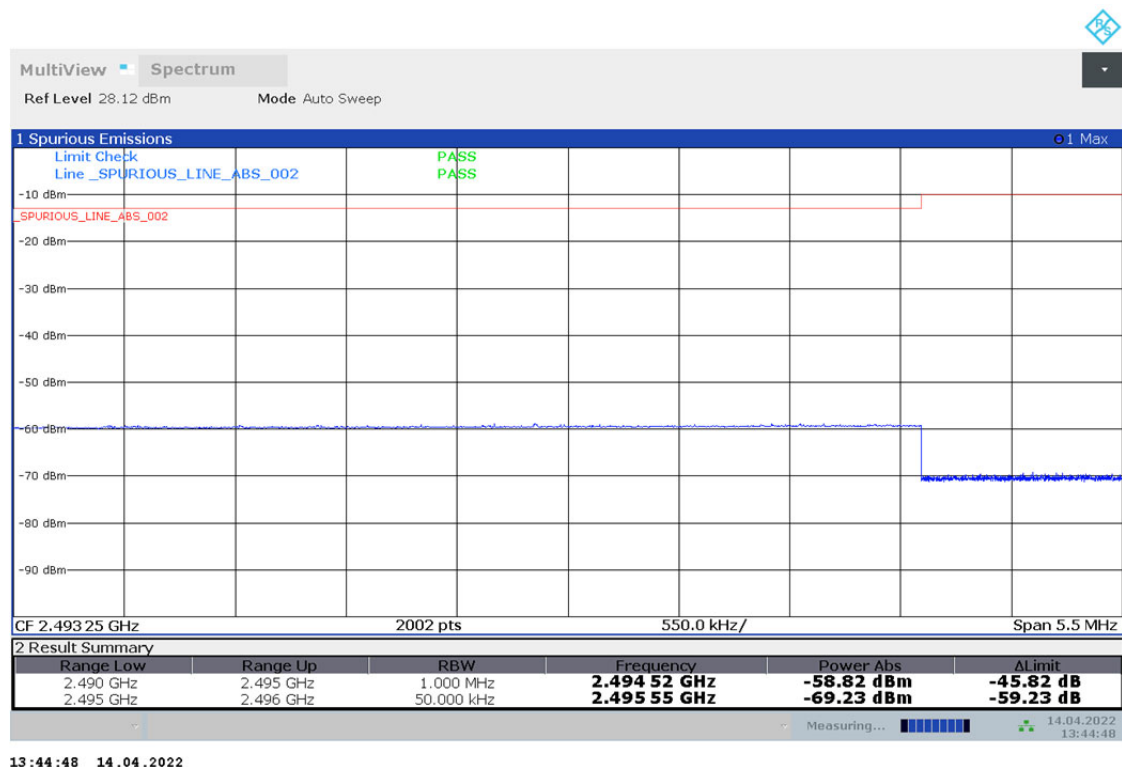
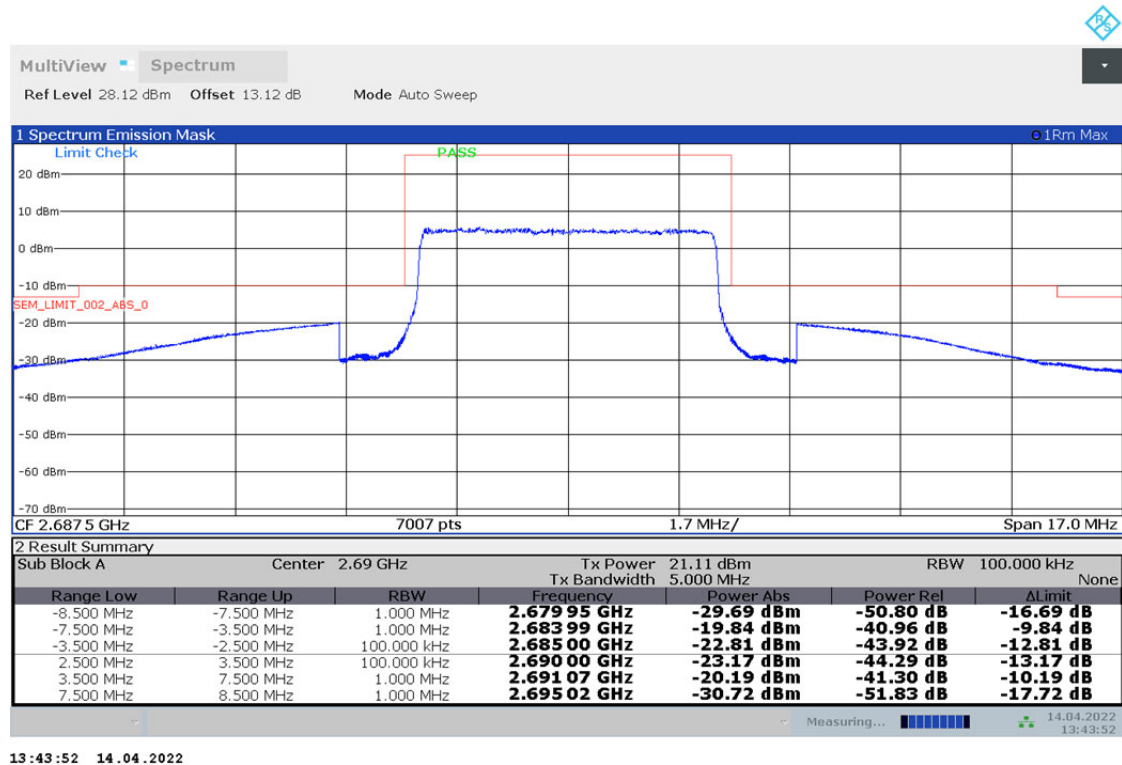
5.2.14 TM2_5MHz_LCH_RB1#0



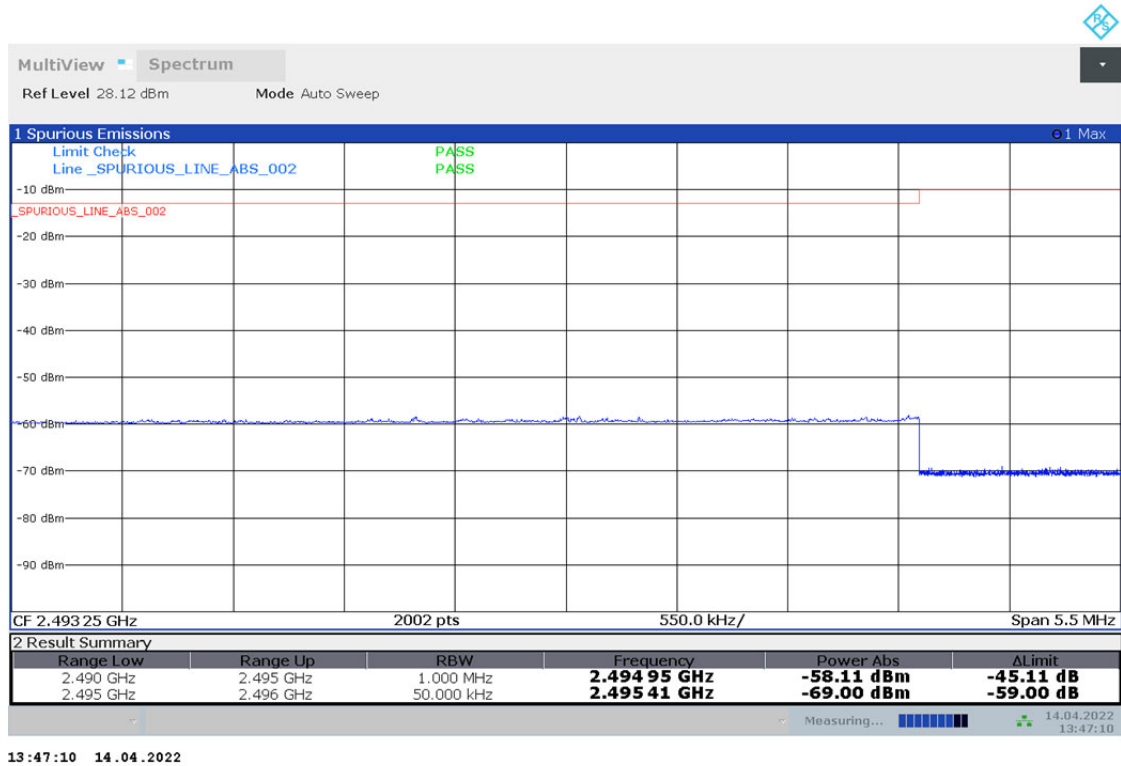
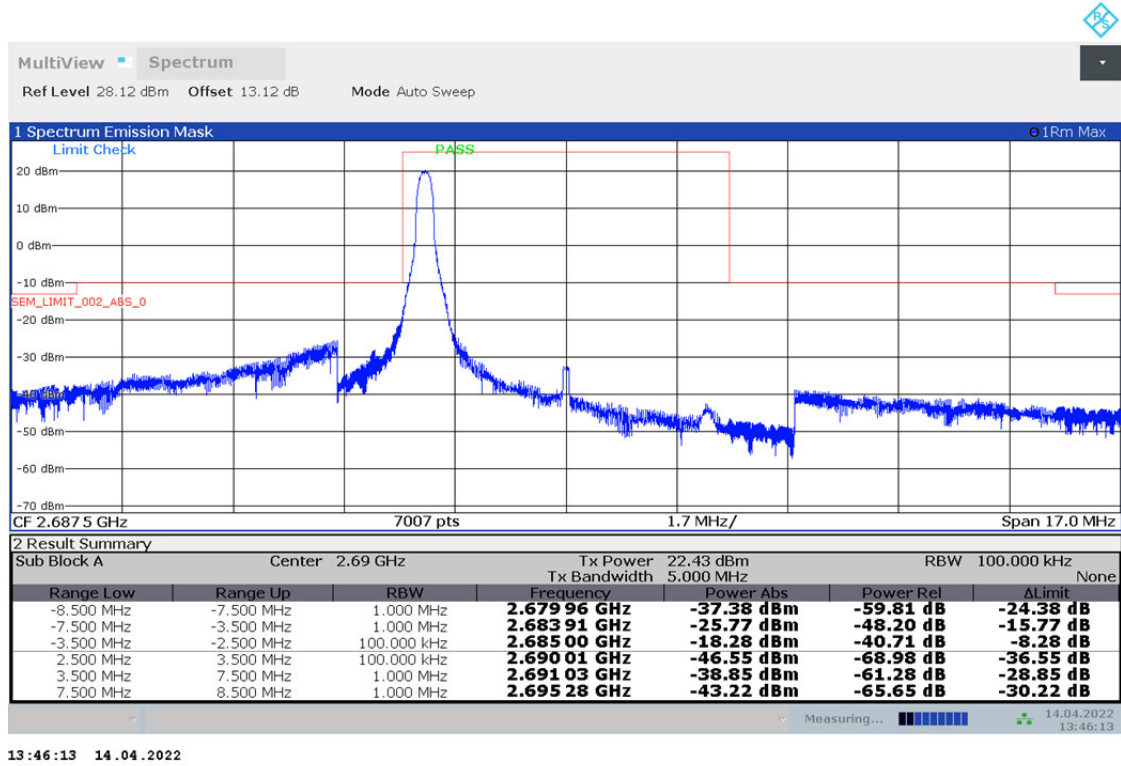
5.2.15 TM2_5MHz_LCH_RB1#24



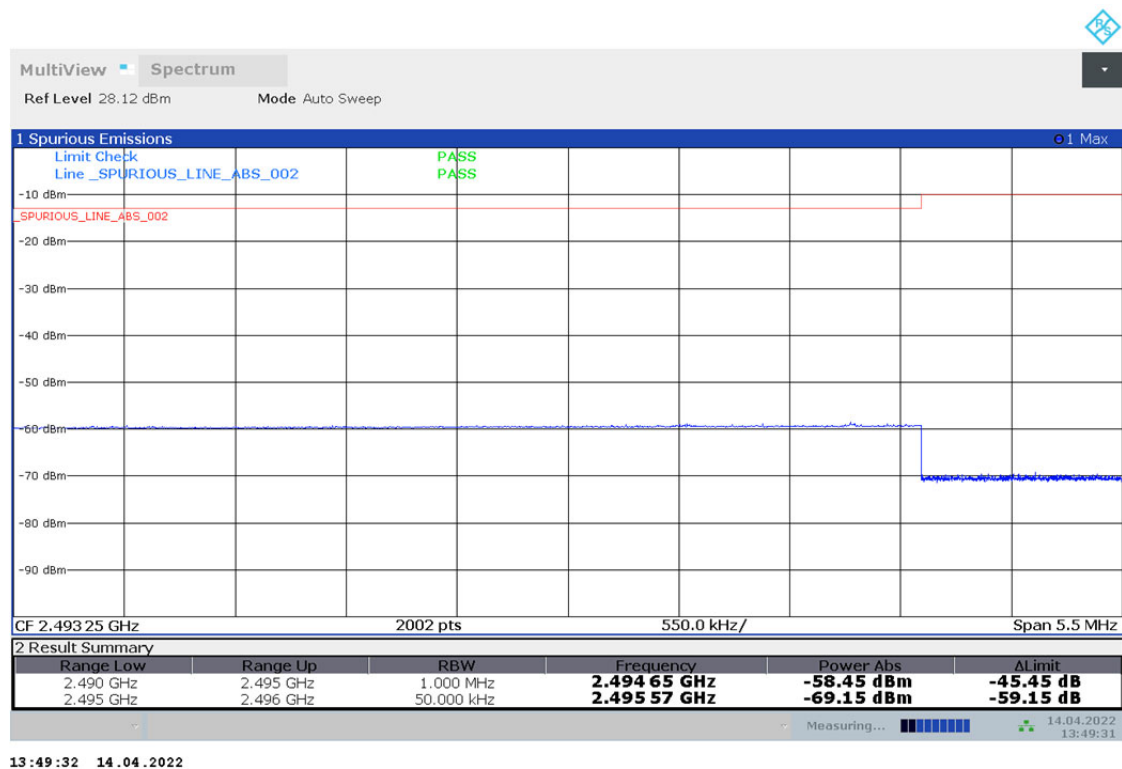
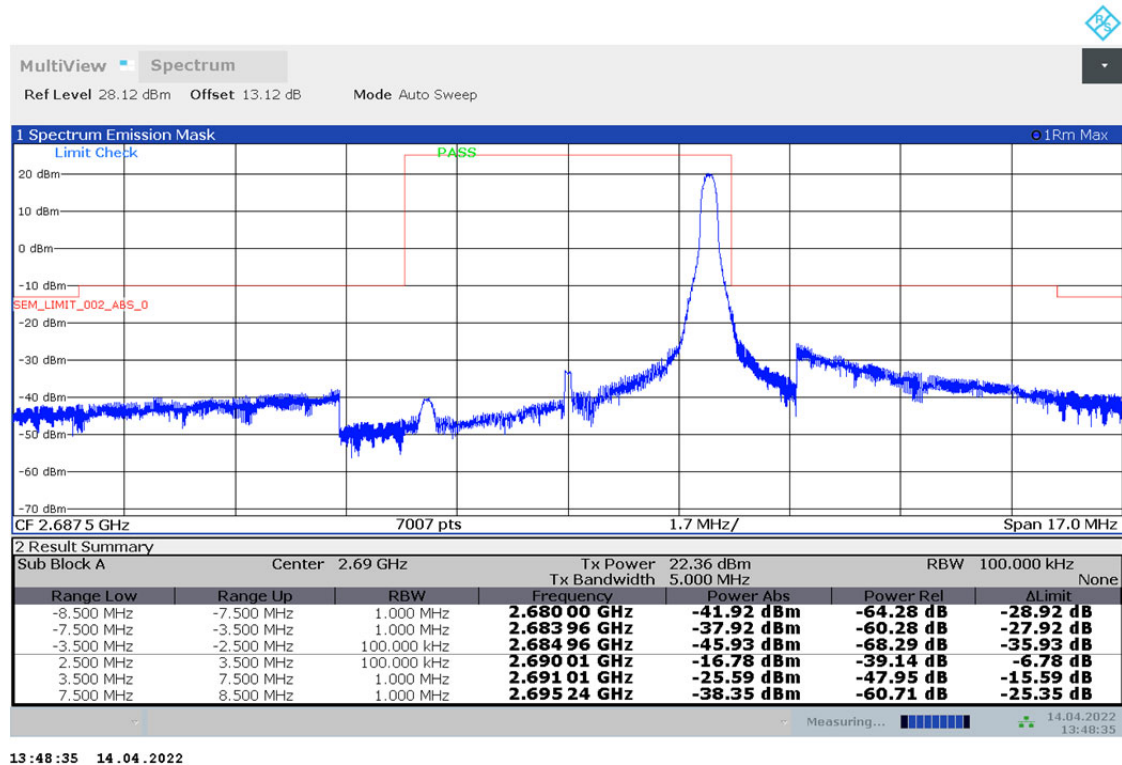
5.2.16 TM2_5MHz_HCH_RB25#0



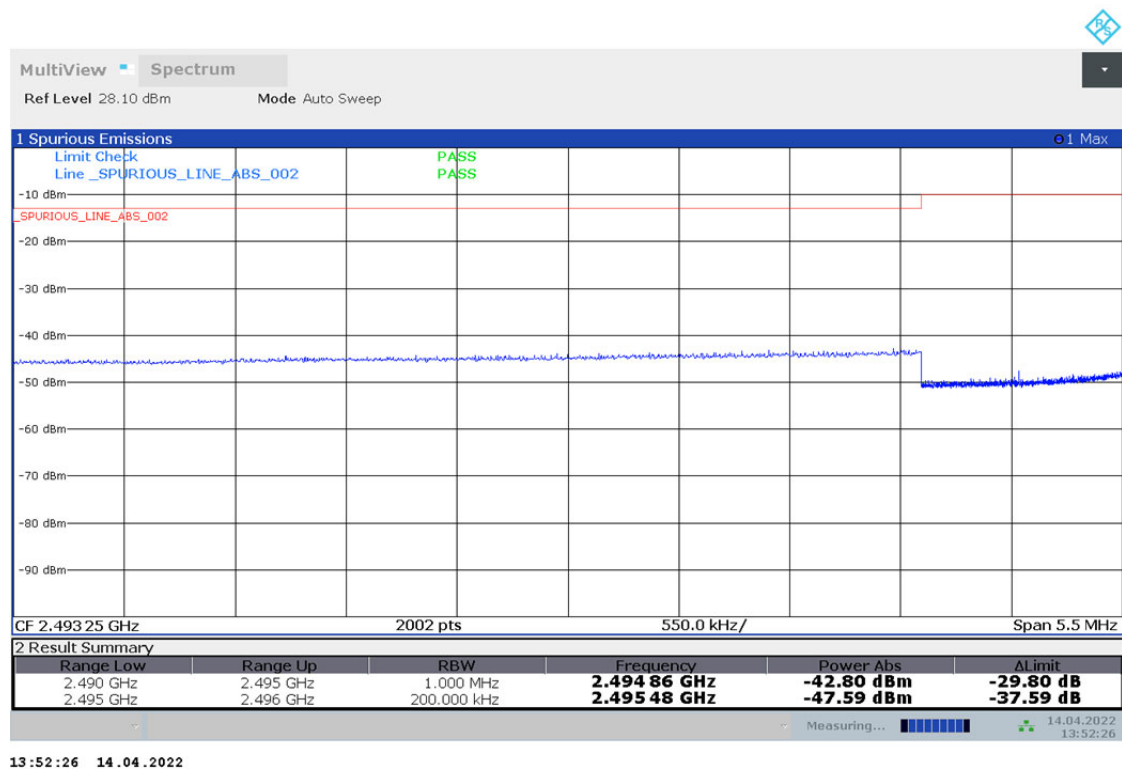
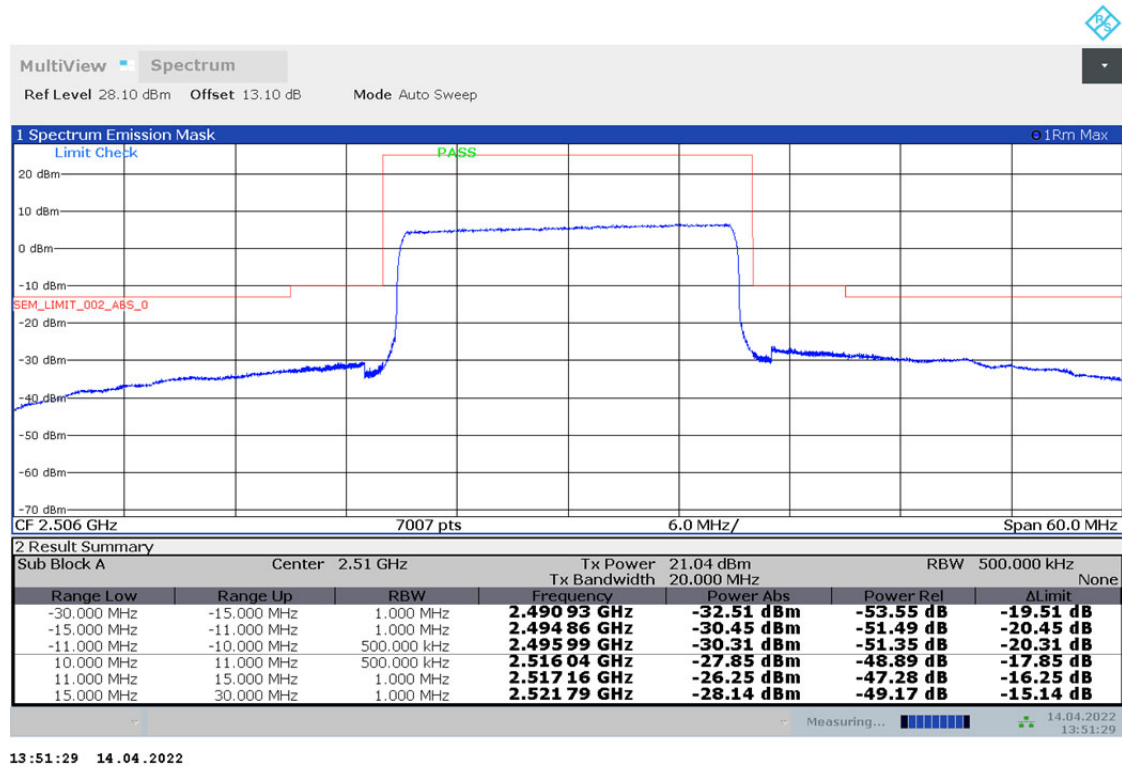
5.2.17 TM2_5MHz_HCH_RB1#0



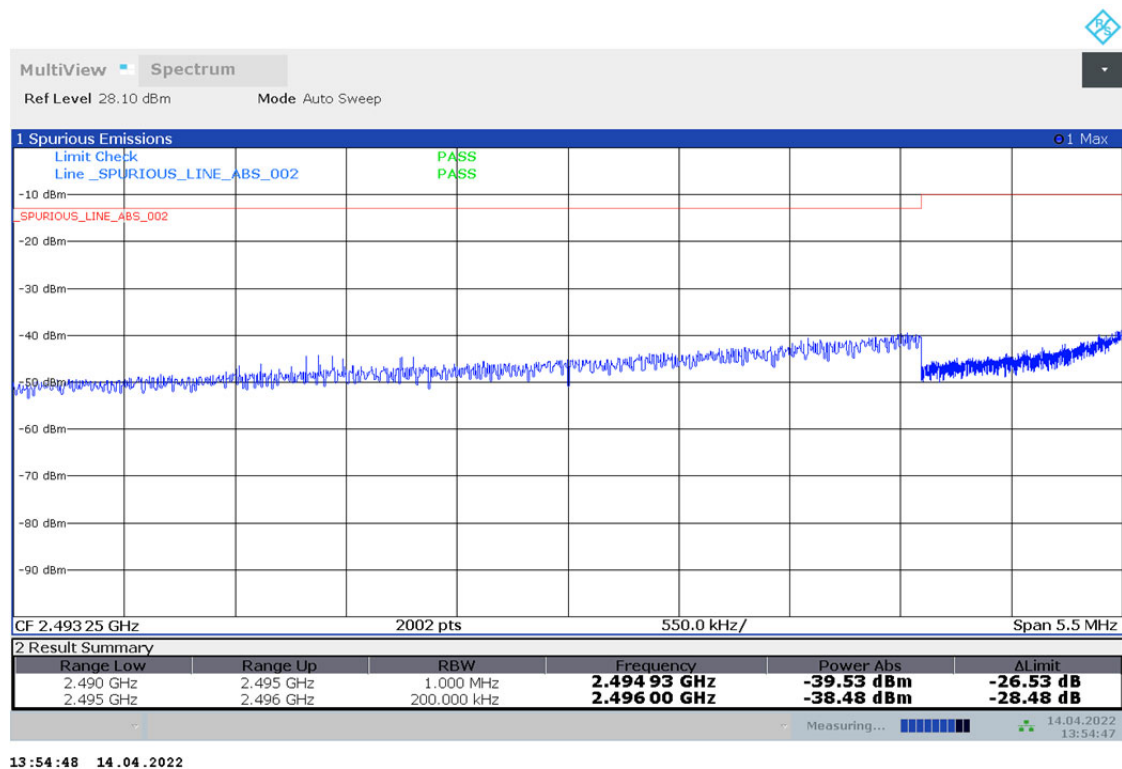
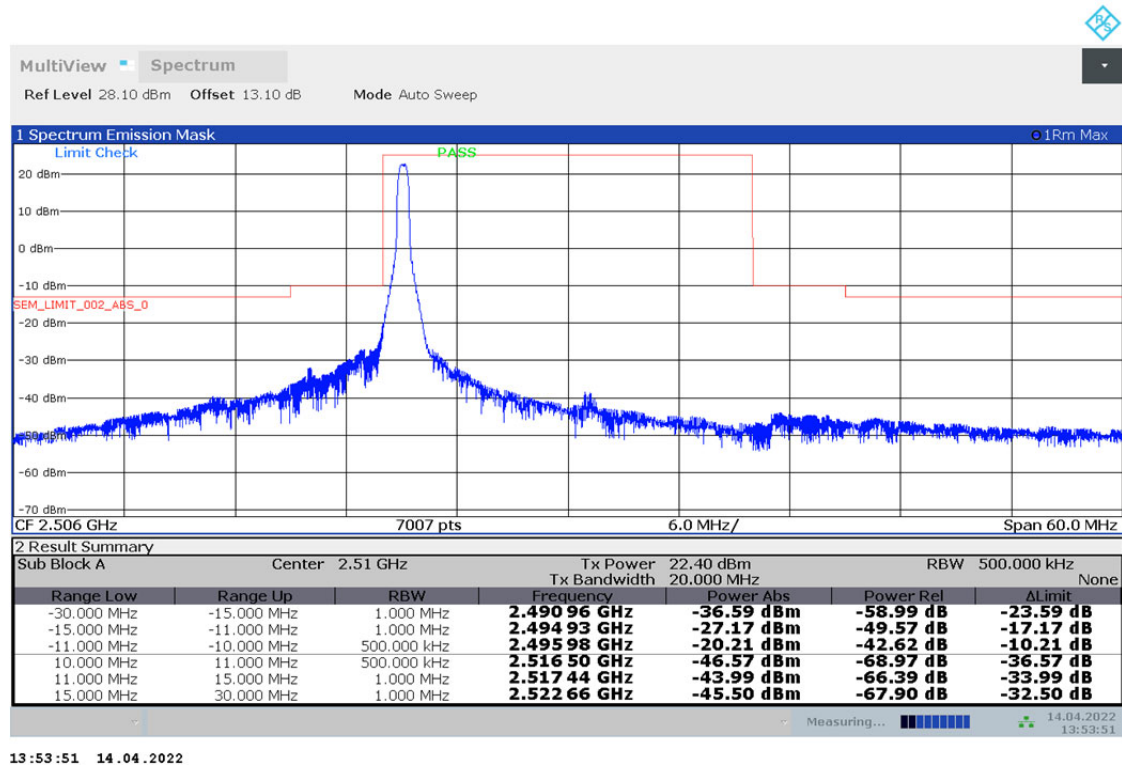
5.2.18 TM2_5MHz_HCH_RB1#24



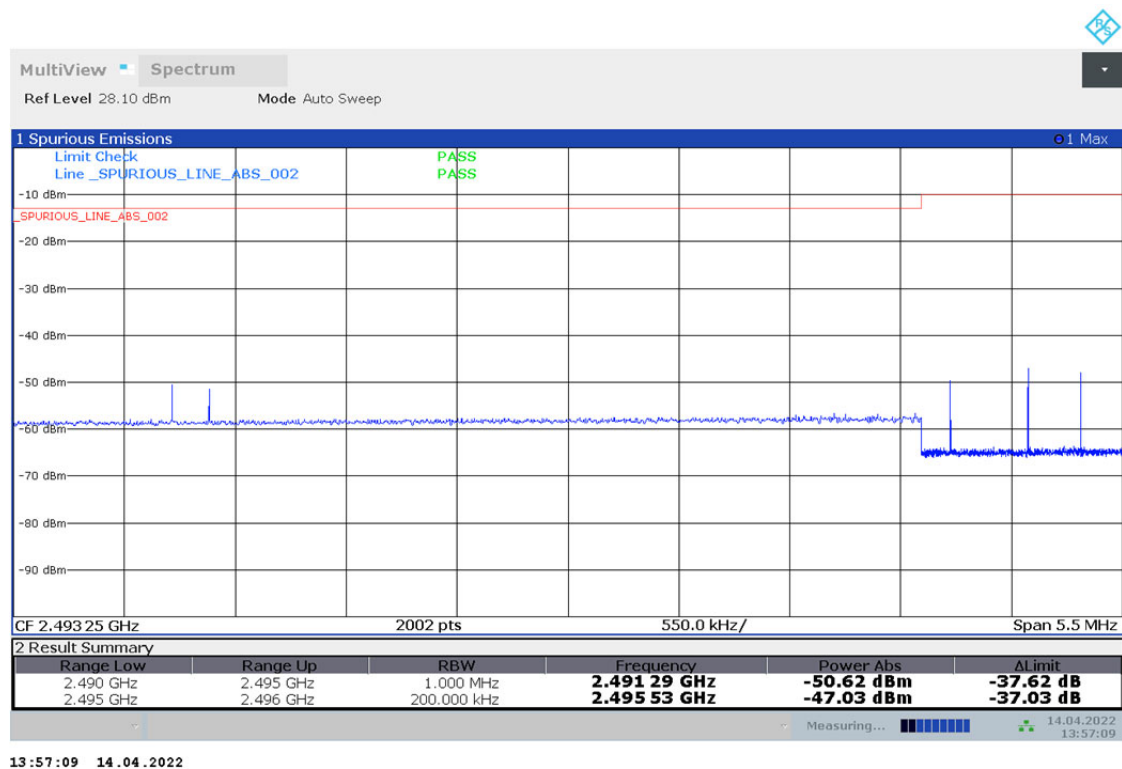
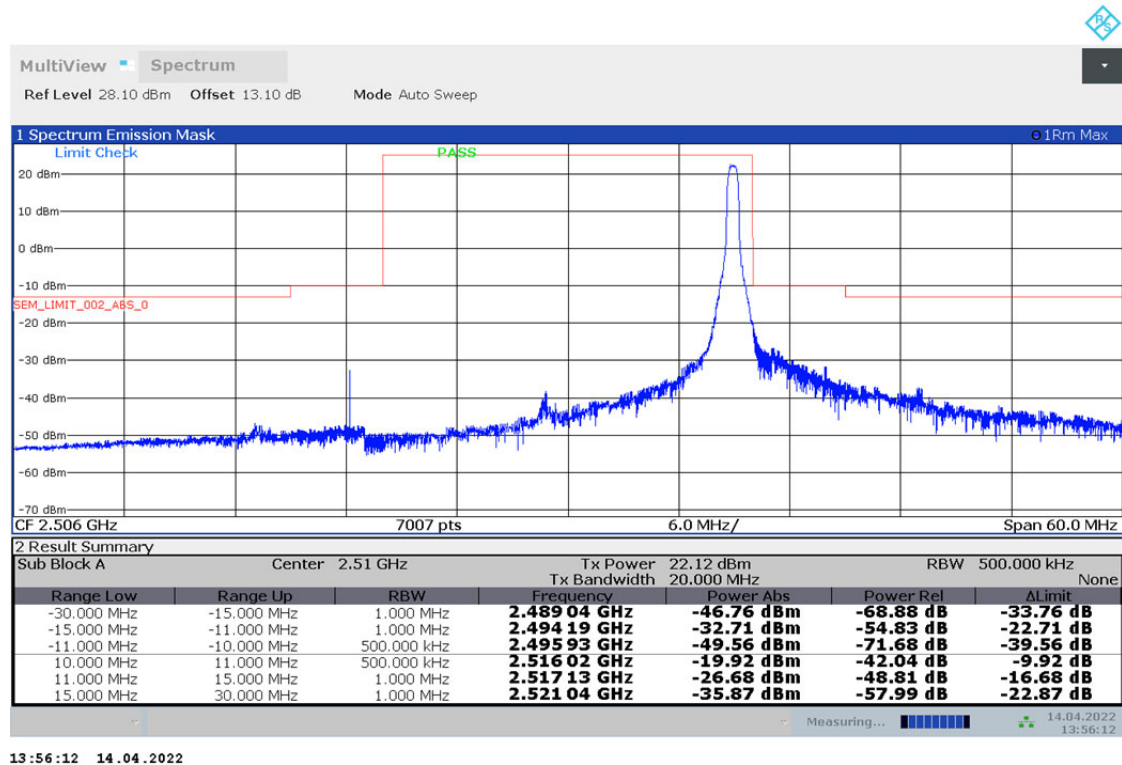
5.2.19 TM2_20MHz_LCH_RB100#0



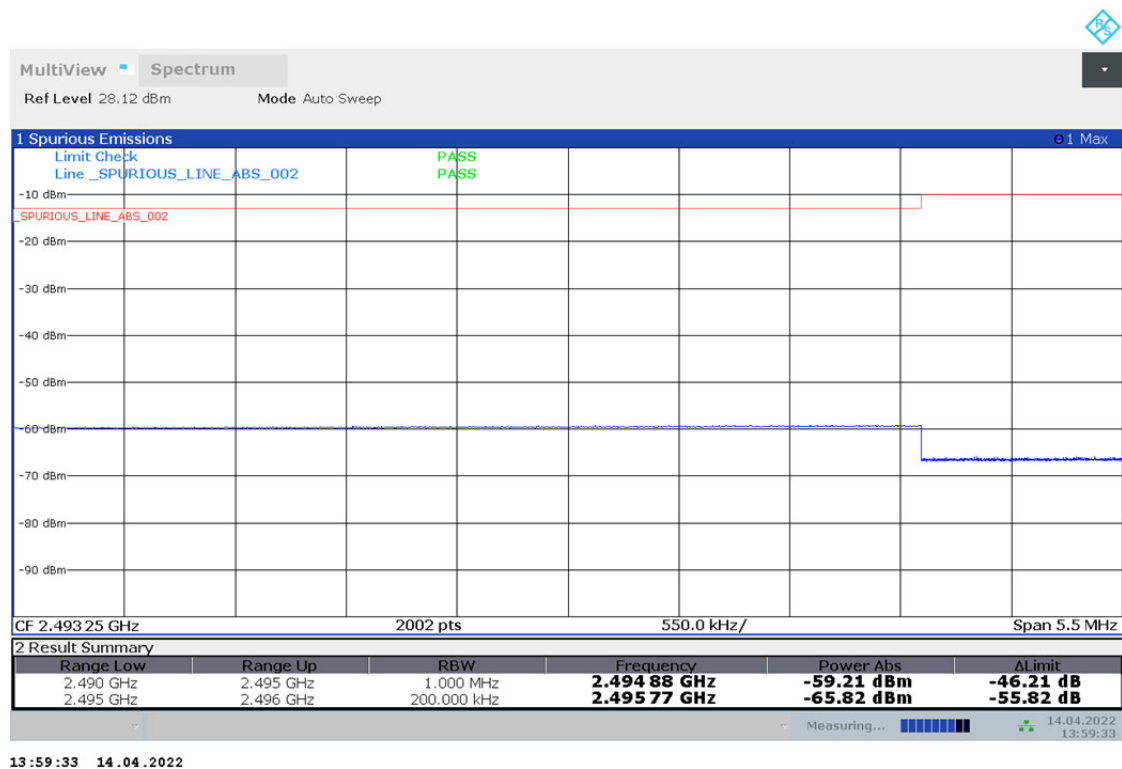
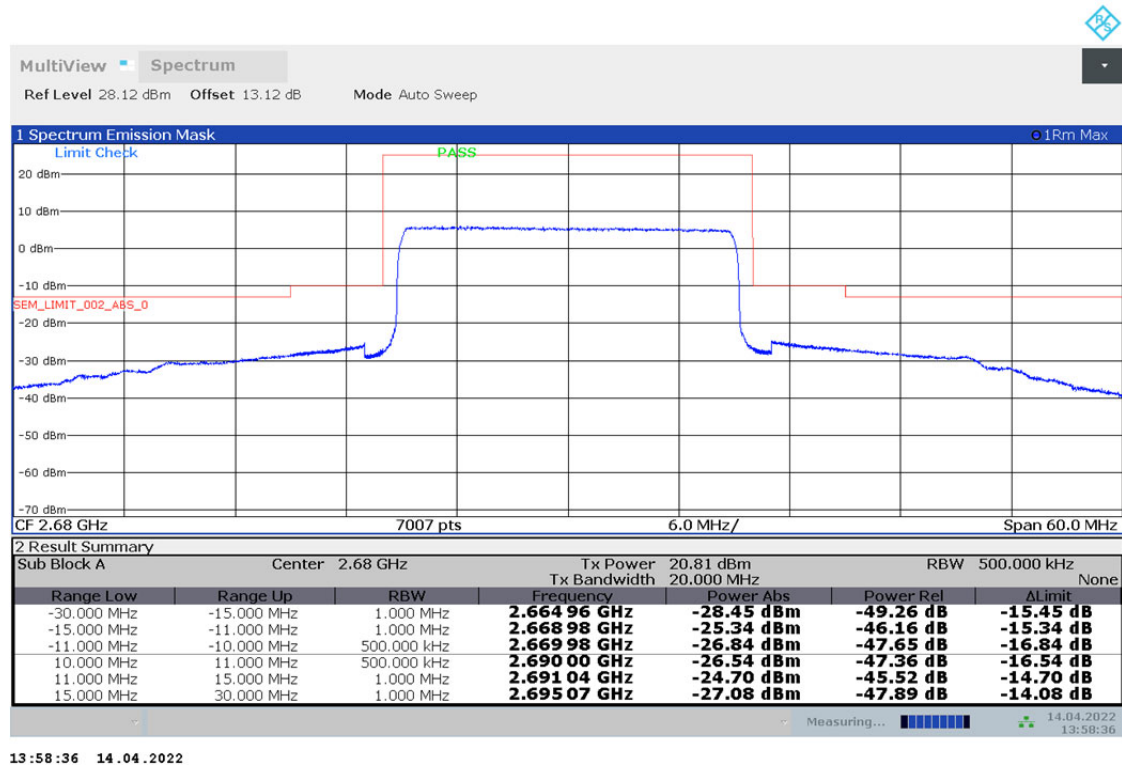
5.2.20 TM2_20MHz_LCH_RB1#0



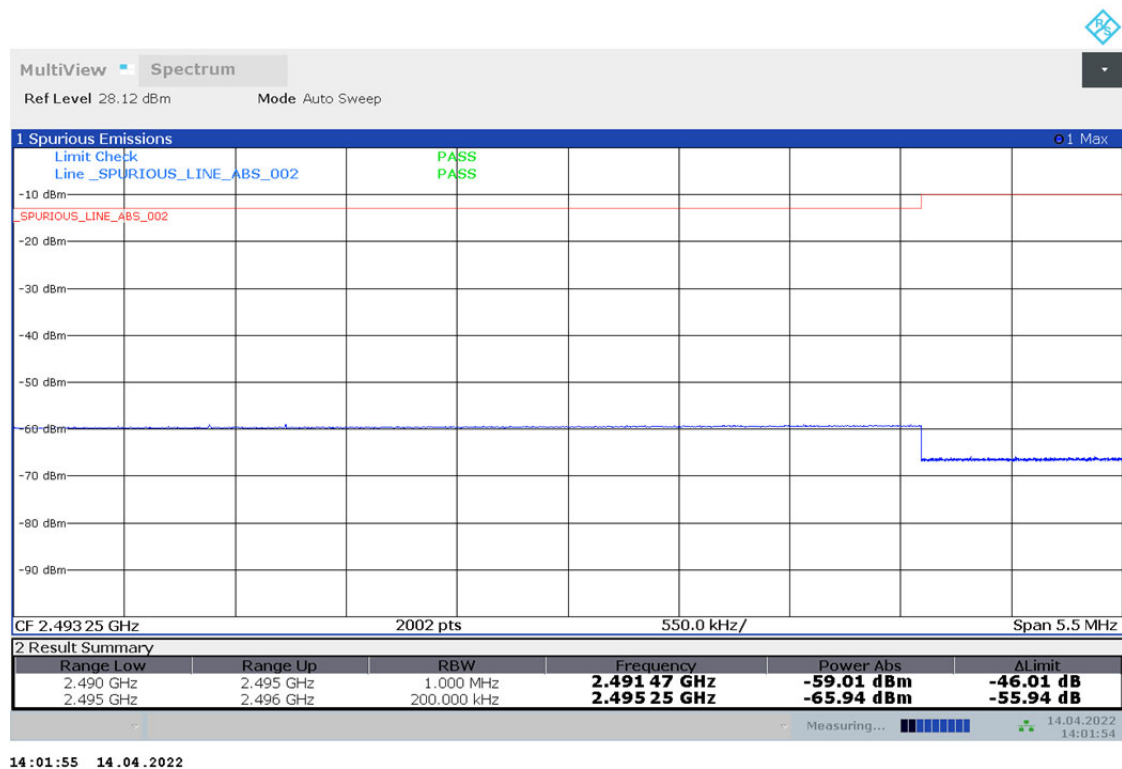
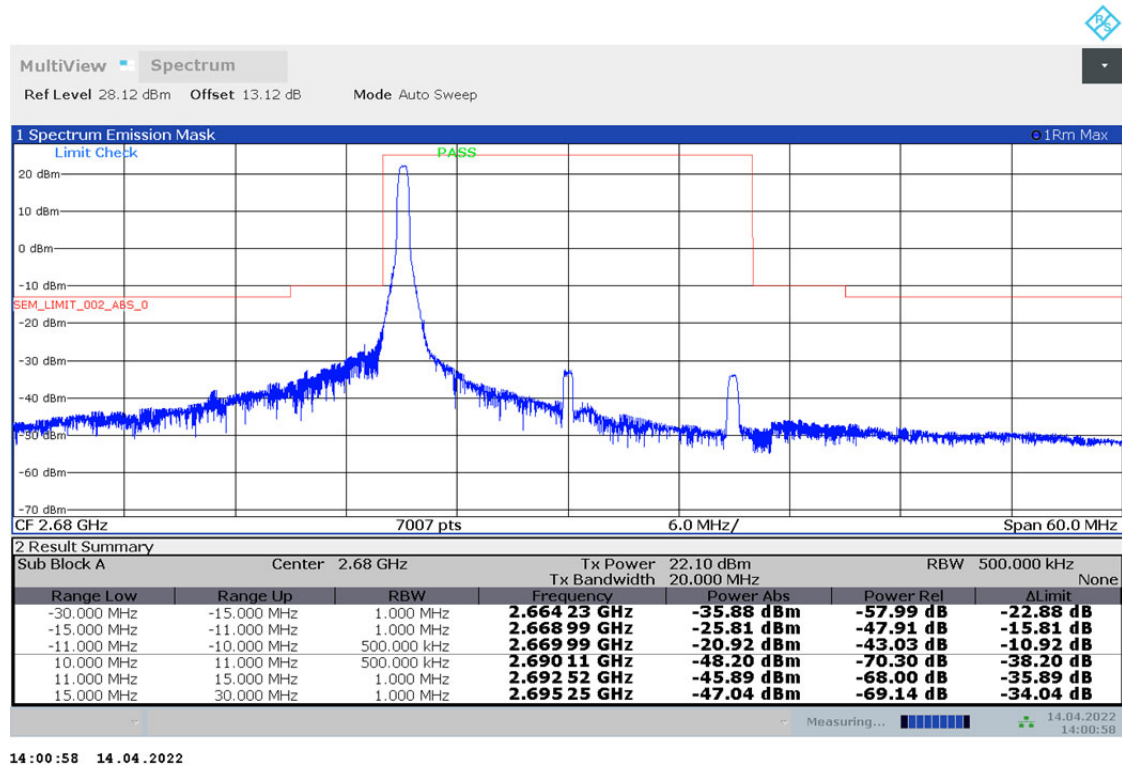
5.2.21 TM2_20MHz_LCH_RB1#99



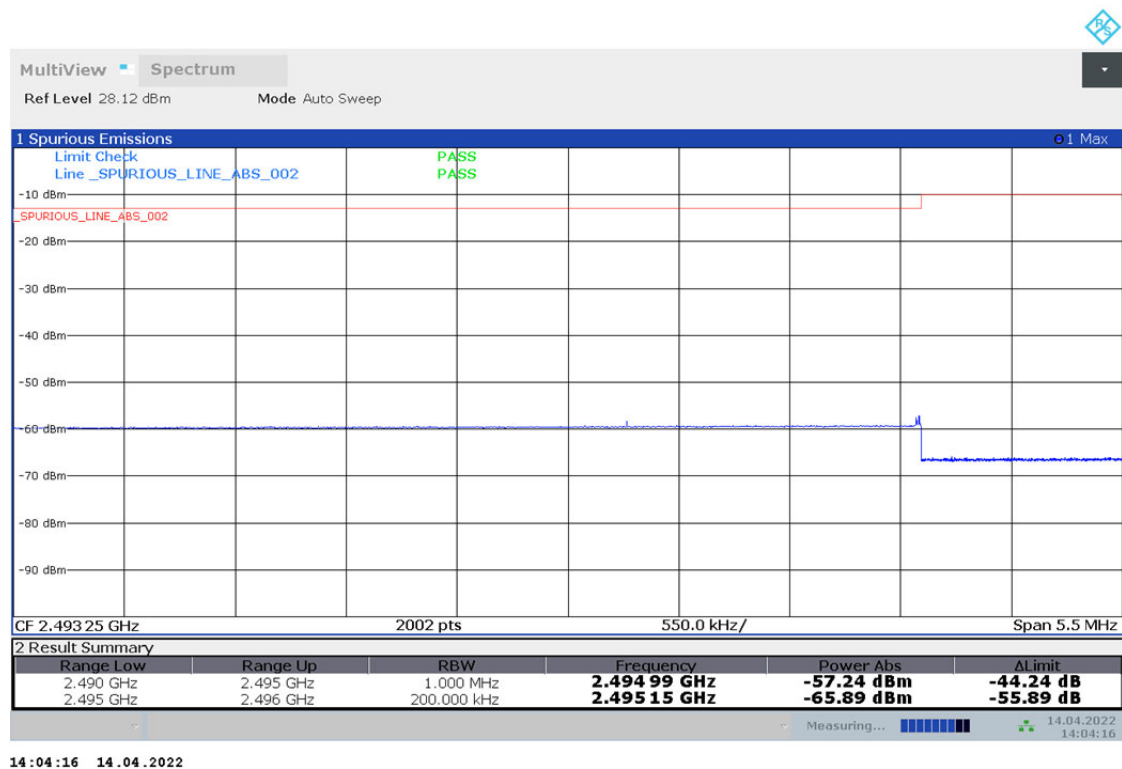
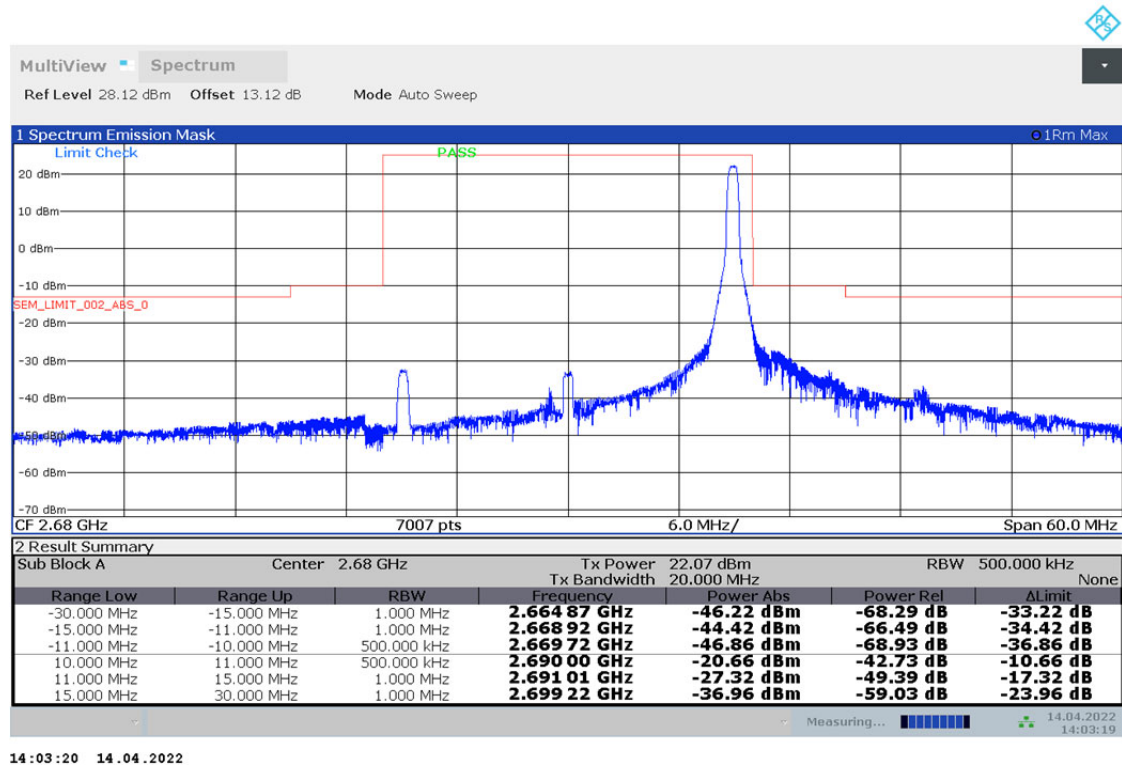
5.2.22 TM2_20MHz_HCH_RB100#0



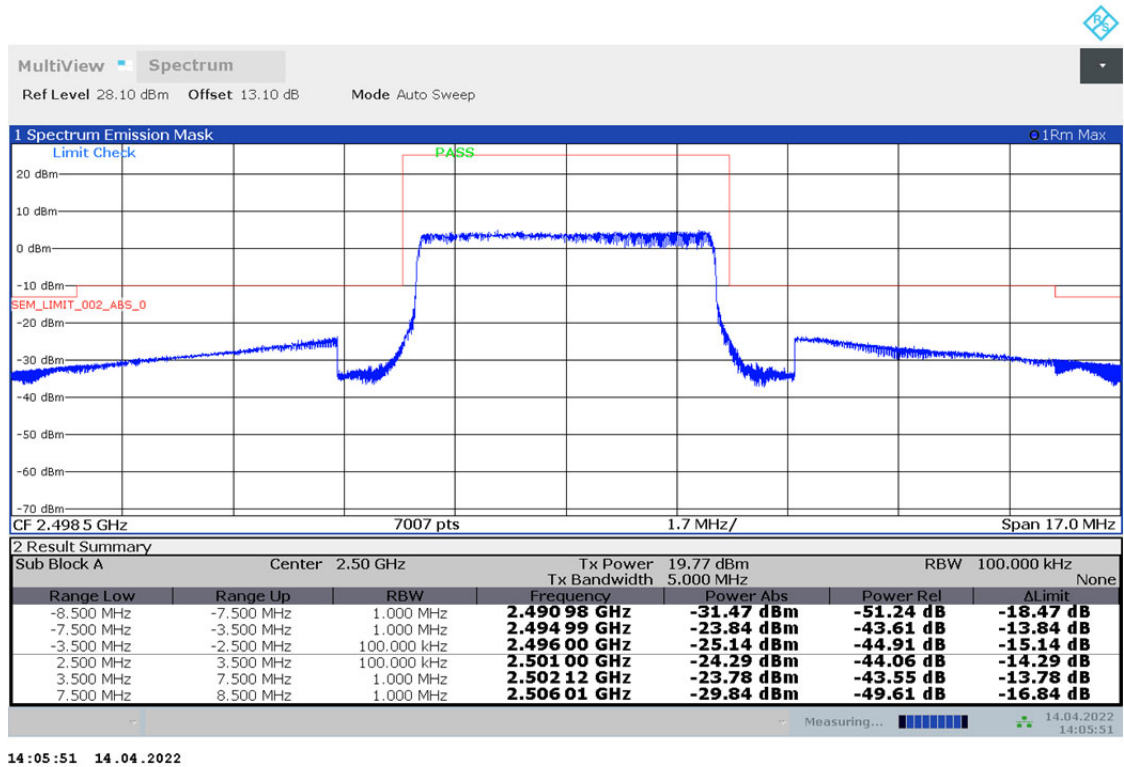
5.2.23 TM2_20MHz_HCH_RB1#0



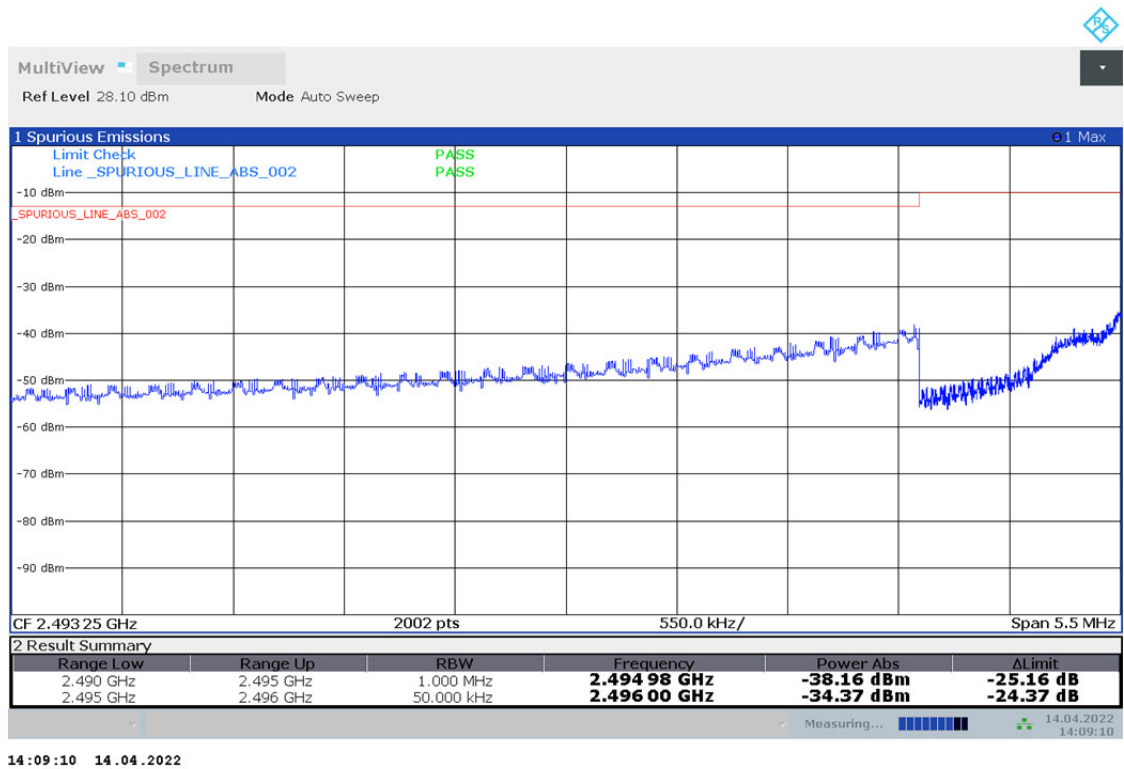
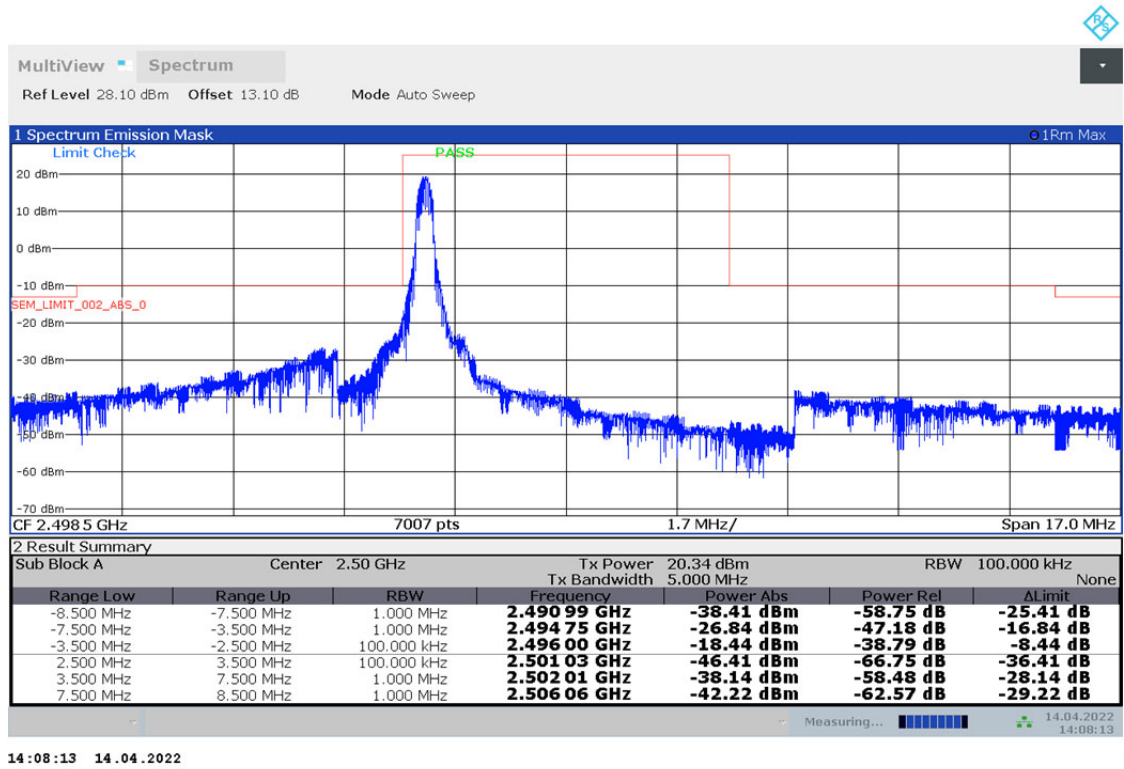
5.2.24 TM2_20MHz_HCH_RB1#99



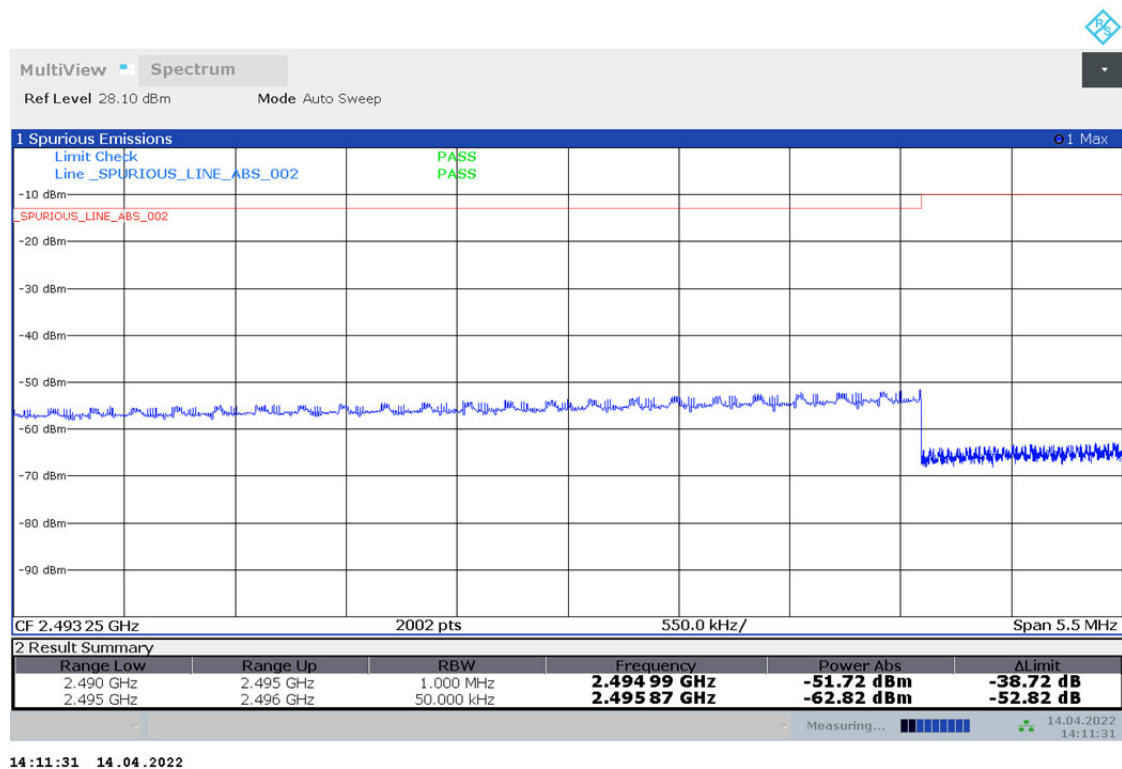
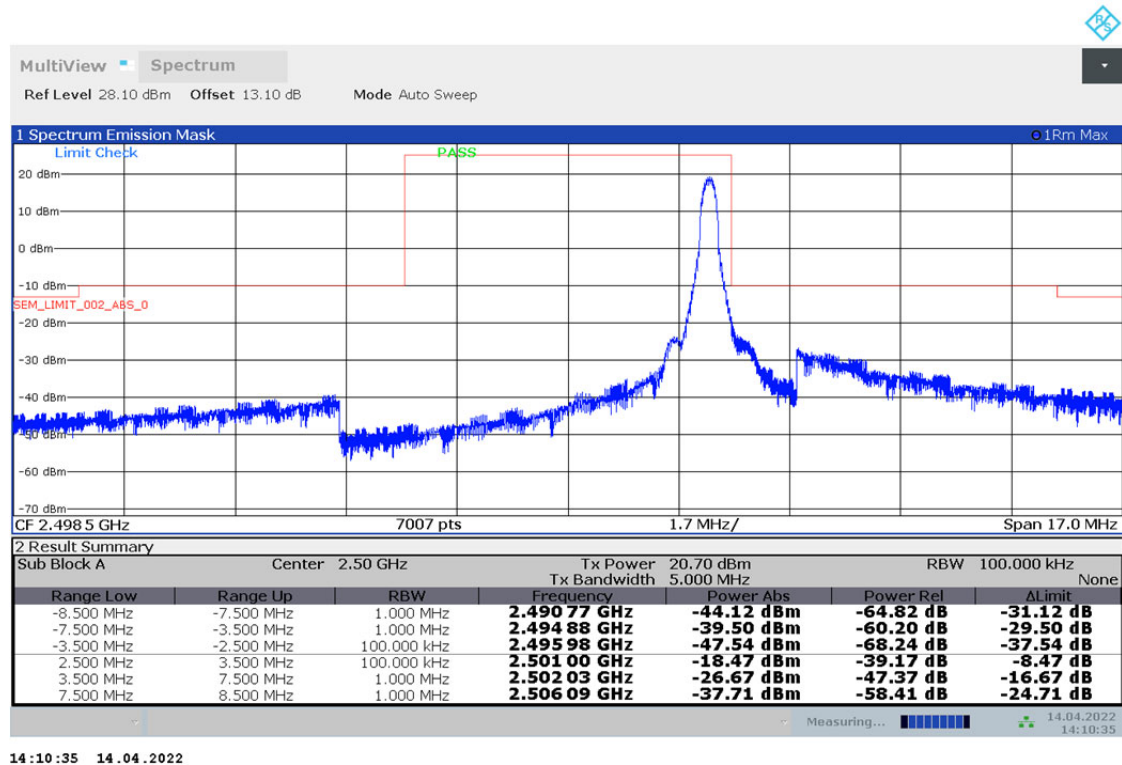
5.2.25 TM3_5MHz_LCH_RB25#0



5.2.26 TM3_5MHz_LCH_RB1#0



5.2.27 TM3_5MHz_LCH_RB1#24



5.2.28 TM3_5MHz_HCH_RB25#0

