LE910Cx

HW Design Guide

Technical Documentation

APPLICABILITY TABLE

This documentation applies to the following products:

PRODUCTS	DESCRIPTION
LE910C1-NA	North America – AT&T with global roaming
LE910C1-NS	North America - Sprint variant
LE910C1-AP	APAC variant CAT1 variant
LE910C4-AP	APAC variant CAT4 variant
LE910C4-EU	Europe CAT4 variant
LE910C1-EU	Europe CAT1 variant
LE910C1-EUX	Europe CAT1 variant
LE910C4-NF	North America CAT4 variant
LE910C1-NF	North America CAT1 variant
LE910C1-SA	North America CAT1 variant – AT&T
LE910C1-SAX	North America CAT1 variant – AT&T
LE910C1-ST	North America CAT1 variant – T Mobile
LE910C1-SV	North America CAT1 variant – Verizon
LE910C1-SVX	North America CAT1 variant – Verizon
LE910C1-LA	Latin America CAT1 variant
LE910C4-LA	Latin America CAT4 variant
LE910C4-CN	China CAT4 variant
LE910C1-WWX	Worldwide CAT1 variant
LE910C4-WWX	Worldwide CAT4 variant

Table 1: Applicability table

Note: ‘X’ means ThreadX OS in LE910C1-EUX, LE910C1-SAX and LE910C1-SVX. The other models which don’t have the letter ‘X’ are Linux OS.

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1. INTRODUCTION

1.1. Scope

This document introduces the EXFO LE910Cx module and presents possible and recommended hardware solutions for the development of a product based on this module. All the features and solutions described in this document are applicable to all LE910Cx variants listed in the applicability table.

If a specific feature is applicable to a specific product only, it will be clearly marked.

Note: LE910Cx refers to all modules listed in the Applicability Table.

This document takes into account all the basic functions of a wireless module; it suggests a valid hardware solution for each function and points out incorrect solutions and common errors to be avoided.

This document cannot include every hardware solution or every product that can be designed. Avoiding invalid solutions must be considered mandatory. Where the suggested hardware configurations are not be considered mandatory, the information provided should be used as a guide and a starting point for the proper development of the product with the EXFO LE910Cx module.

Note: The integration of the GSM/GPRS/EGPRS/WCDMA/HSPA+/LTE LE910Cx cellular module within a user application must be done according to the design rules described in this manual.

1.2. Audience

This document is intended for EXFO customers, especially system integrators, about to implement their applications using the EXFO LE910Cx module.

1.3. Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors, contact EXFO Technical Support at:

- TS-EMEA@EXFO.com
- TS-AMERICAS@EXFO.com
- TS-APAC@EXFO.com

Alternatively, use:

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https://www.EXFO.com/support

For detailed information about where you can buy the EXFO modules or for recommendations on accessories and components visit:

https://www.EXFO.com

To register for product news and announcements or for product questions contact EXFO's Technical Support Center (TTSC).

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

EXFO appreciates feedback from the users of on information.

1.4. Symbol Conventions

The following conventions are used to emphasize specific types of information:

	Danger: This information MUST be followed or catastrophic equipment failure or personal injury may occur.
	Warning: Alerts the user on important steps about the module integration.
	Note/Tip: Provides advice and suggestions that may be useful when integrating the module.
	Electro-static Discharge: Notifies the user to take proper grounding precautions before handling the product.

All dates are in ISO 8601 format, that is YYYY-MM-DD.

1.5. Related Documents

- LE920x4/LE910Cx AT Command User Guide 80490ST10778A
- EXFO EVB HW User Guide 1VV0301249
- LE910Cx Interface Board HW User Guide 1VV0301323

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- LE910/LE920 Digital Voice Interface Application Note 80000NT11246A
- EXFO_LE920A4_LE910Cx_Wi-Fi_Interface_Application_Note_r1 80490NT11511A
- Antenna Detection Application Note 80000NT10002A
- High-Speed Inter-Chip USB Electrical Specification, version 1.0 (a supplement to the USB 2.0 specification, Section 3.8.2)
- ETH_Expansion_board_Application Note 80490NT11622A
- LE910C1/LE910C4 PSM Application Note, 80502NT11758A

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2. GENERAL PRODUCT DESCRIPTION

2.1. Overview

LE910Cx is EXFO's new LTE series for IoT applications.

In its most basic use case, the LE910Cx can be applied as a wireless communication front-end for telematics products, offering GNSS and mobile communication features to an external host CPU through its rich interfaces.

LE910Cx is available in hardware variants as listed in Table 1: Applicability Table.

For differences in the designated RF band sets – refer to Section 2.6.1, RF Bands per Regional Variant.

Note:

(EN) The integration of the LE910Cx cellular module within user application shall be done according to the design rules described in this manual.

(IT) L'integrazione del modulo cellulare LE910Cx all'interno dell'applicazione dell'utente dovrà rispettare le indicazioni progettuali descritte in questo manuale.

(DE) Die Integration des LE910Cx Mobilfunk-Moduls in ein Gerät muß gemäß der in diesem Dokument beschriebenen Kunstruktionsregeln erfolgen.

(SL) Integracija LE910Cx modula v uporabniški aplikaciji bo morala upoštevati projektna navodila, opisana v tem priročniku.

(SP) La utilización del modulo LE910Cx debe ser conforme a los usos para los cuales ha sido deseñado descritos en este manual del usuario.

(FR) L'intégration du module cellulaire LE910Cx dans l'application de l'utilisateur sera faite selon les règles de conception décrites dans ce manuel.

(HE)

האינטגרטור מתבקש ליישם את ההנחיות המפורטות במסמך זה בתהליך האינטגרציה של המודם הסלולארי **LE910Cx** עם המוצר.

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2.2. Applications

LE910Cx can be used for telematics applications where tamper-resistance, confidentiality, integrity, and authenticity of end-user information are required, for example:

- Telematics services
- Road pricing
- Pay-as-you-drive insurance
- Stolen vehicles tracking
- Internet connectivity

2.3. General Functionality and Main Features

The LE910Cx series of cellular modules features an LTE and multi-RAT modem together with a powerful on-chip application processor and a rich set of interfaces.

The major functions and features are listed below:

Function	Features
Modem	Multi-RAT cellular modem for voice and data communication LTE FDD Cat1 and Cat4 (10/5Mbps DL/UL at cat1, 150/50Mbps DL/UL at cat4). Carrier aggregation is not supported GSM/GPRS/EDGE WCDMA up to DC HSPA+, Rel.9 Support for SIM profile switching Regional variants with optimal choice of RF bands for worldwide coverage of countries and MNOs State-of-the-art GNSS solution with GPS/GLONASS/BeiDou/Galileo/QZSS receiver
Digital audio subsystem	PCM/I2S digital audio interface Up to 48 kHz sample rate, 16-bit words
Two USIM ports – dual voltage	Class B and Class C support Hot swap support Clock rates up to 5 MHz
Function	Features

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Application processor	Application processor to run customer application code 32-bit ARM Cortex-A7 up to 1.3 GHz running the Linux operating system Flash + DDR are large enough to allow for customer's own software applications
Interfaces	Rich set of interfaces, including: SD/MMC Card Interface supporting SD3.0 standard SDIO for external WiFi transceiver supporting SDIO3.0 standard SGMII for external Ethernet transceiver Compliant with IEEE802.3 Full duplex operation at 1 Gbps Half/full duplex operation at 10/100 Mbps Support for VLAN tagging Support for IEEE1588, PTP (Precision Time Protocol) USB2.0 – USB port is typically used for: Flashing of firmware and module configuration Production testing Accessing the Application Processor's file system AT command access High-speed WWAN access to external host Diagnostic monitoring and debugging NMEA data to an external host CPU HSIC (Optional) High-speed 480 Mbps (240 MHz DDR) USB transfers are 100% host driver compatible with traditional USB cable connected topologies Bidirectional data strobe signal (STROBE) Bidirectional data signal (DATA) No power consumption unless a transfer is in progress Maximum trace length 10 cm Signals driven at 1.2V standard LVCMOS levels Peripheral Ports – SPI, I2C, UART GPIOs Antenna ports
Form factor	Form factor (28x28mm), accommodating the multiple RF bands in each region variant
Environment and quality requirements	The entire module is designed and qualified by EXFO for satisfying the environment and quality requirements.
Single supply module	The module generates all its internal supply voltages.
RTC	No dedicated RTC supply, RTC is supplied by VBATT
Operating temperature	Range -40 °C to +85 °C (conditions as defined in Section 2.5.1, Temperature Range).

Table 2: Features Table

Note: The following interfaces are unique to the LE910Cx and may not be supported on other (former or future) xE910 family. Special care must be paid when designing the application board if future compatibility is required:

- SGMII for Ethernet connectivity

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- SDIO for WIFI connectivity
- SD/MMC for SD Card connectivity

Warning: LE910C1-EUX, LE910C1-SAX and LE910C1-SVX models which are based on ThreadX OS, does not support the following functions.

- Fastboot
- Wi-Fi / BT
- SD / MMC
- HSIC
- SGMII
- RNDIS over the USB
- NMEA over the USB
- USB Audio
- USB OTG
- Audio playback
- Audio playback during voice call
- Full duplex voice conversation recording (Voice Recording)
- In call music delivery
- AUX PCM interface
- TTY

2.4. Block Diagram

Figure 1 shows an overview of the internal architecture of the LE910Cx module.

It includes the following sub-functions:

- Application processor, Modem subsystem and Location processing with their external interfaces. These three functions are contained in a single SOC.
- RF front end and antenna ports.
- Digital Audio interface for external codec.

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- Rich IO interfaces. Depending on the LE910Cx software features enabled, some of its interfaces exported due to multiplexing may be used internally and therefore may not be usable by the application.
- PMIC with the RTC function inside

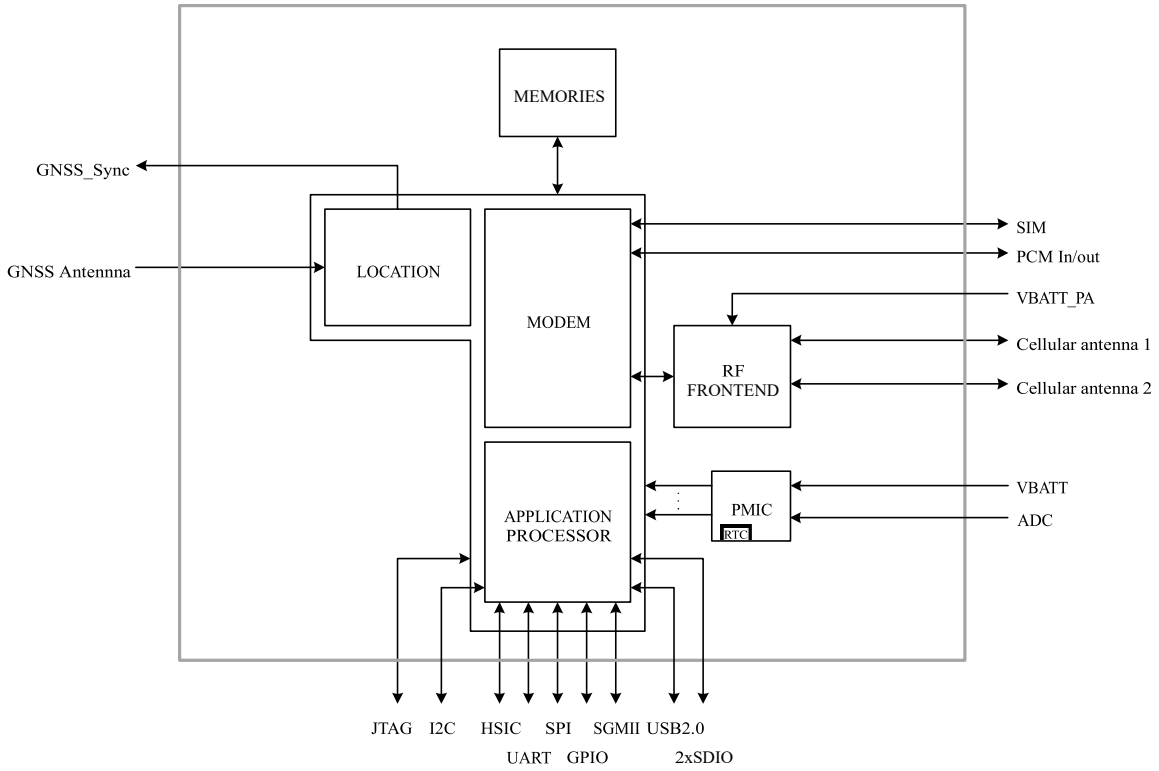

Figure 1: LE910Cx Block Diagram

2.5. Environmental Requirements

2.5.1. Temperature Range

Mode	Temperature	Note

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Operating temperature range	-40 ~ +85°C Ambient. Temperatures outside of the range –20°C ÷ +55°C might slightly deviate from ETSI specifications. The module is fully functional, able to make and receive voice calls, data calls, SMS and GPRS traffic.	Ambient
	–20°C ÷ +55°C	Temperatures outside of this range might slightly deviate from ETSI specifications
Storage and non-operating temperature range	–40°C ~ +90°C	

Table 3: Temperature Range

2.5.2. RoHS Compliance

As a part of the EXFO corporate policy of environmental protection, the LE910Cx complies with the RoHS (Restriction of Hazardous Substances) directive of the European Union (EU directive 2011/65/EU).

2.6. Operating Frequency Bands

The operating frequencies in GSM850, EGSM900, DCS1800, PCS1900, WCDMA & LTE modes conform to the 3GPP specifications.

2.6.1. RF Bands per Regional Variant

Table 4 summarizes all region variants within the LE910Cx family, showing the supported band sets in each variant.

Region Variant	2G	HSPA+	LTE FDD	LTE TDD	TD-SCDMA
LE910C1-NA	2, 3, 5, 8	1, 2, 4, 5, 8	2, 4, 12	-	-
LE910C1-NS	-	-	2, 4, 5, 12, 25, 26	-	-
LE910C1-AP	-	1, 5, 6, 8, 19	1, 3, 5, 8, 9, 18, 19, 26, 28	-	-
LE910C4-AP	-	1, 5, 6, 8, 19	1, 3, 5, 8, 9, 18, 19, 26, 28	-	-
LE910C4-EU	3, 8	1, 3, 8	1, 3, 7, 8, 20, 28A	-	-

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LE910C1-EU	3, 8	1, 3, 8	1, 3, 7, 8, 20, 28A	-	-
LE910C1-EUX	3, 8	1, 3, 8	1, 3, 7, 8, 20, 28A	-	-
LE910C4-NF	-	2, 4, 5	2, 4, 5, 12, 13, 14, 66, 71	-	-
LE910C1-NF	-	2, 4, 5	2, 4, 5, 12, 13, 14, 66, 71	-	-
LE910C1-SA	-	-	2, 4, 12, 14, 66	-	-
LE910C1-SAX	-	-	2, 4, 12, 66	-	-
LE910C1-ST	-	-	2, 4, 12, 66, 71	-	-
LE910C1-SV	-	-	4, 13	-	-
LE910C1-SVX	-	-	4, 13	-	-
LE910C1-LA	2, 3, 5, 8	1, 2, 4, 5	1, 2, 3, 4, 5, 7, 28	-	-
LE910C4-LA	2, 3, 5, 8	1, 2, 4, 5	1, 2, 3, 4, 5, 7, 28	-	-
LE910C4-CN	3, 8	1, 8	1, 3, 5, 8, 38, 39, 40, 41M	-	34, 39
LE910C1-WWX	2, 3, 5, 8	1, 2, 4, 5, 6, 8, 19	1, 2, 3, 4, 5, 7, 8, 9, 12, 13, 14, 18, 19, 20, 25, 26, 28	-	-
LE910C4-WWX	2, 3, 5, 8	1, 2, 4, 5, 6, 8, 19	1, 2, 3, 4, 5, 7, 8, 9, 12, 13, 14, 18, 19, 20, 25, 26, 28	-	-

Table 4: RF Bands per Regional Variant

2.6.2. Reference Table of RF Bands Characteristics

Mode	Freq. Tx (MHz)	Freq. Rx (MHz)	Channels	Tx-Rx Offset
PCS 1900	1850.2 ~ 1909.8	1930.2 ~ 1989.8	512 ~ 810	80 MHz
DCS 1800	1710 ~ 1785	1805 ~ 1880	512 ~ 885	95 MHz
GSM 850	824.2 ~ 848.8	869.2 ~ 893.8	128 ~ 251	45 MHz
EGSM 900	890 ~ 915	935 ~ 960	0 ~ 124	45 MHz
	880 ~ 890	925 ~ 935	975 ~ 1023	45 MHz

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Mode	Freq. Tx (MHz)	Freq. Rx (MHz)	Channels	Tx-Rx Offset
WCDMA 2100 – B1	1920 ~ 1980	2110 ~ 2170	Tx: 9612 ~ 9888 Rx: 10562 ~ 10838	190 MHz
WCDMA 1900 – B2	1850 ~ 1910	1930 ~ 1990	Tx: 9262 ~ 9538 Rx: 9662 ~ 9938	80 MHz
WCDMA 1800 – B3	1710 ~ 1785	1805 ~ 1880	Tx: 937 ~ 1288 Rx: 1162 ~ 1513	95 MHz
WCDMA AWS – B4	1710 ~ 1755	2110 ~ 2155	Tx: 1312 ~ 1513 Rx: 1537 ~ 1738	400 MHz
WCDMA 850 – B5	824 ~ 849	869 ~ 894	Tx: 4132 ~ 4233 Rx: 4357 ~ 4458	45 MHz
WCDMA 900 – B8	880 ~ 915	925 ~ 960	Tx: 2712 ~ 2863 Rx: 2937 ~ 3088	45 MHz
WCDMA 1800 – B9	1750 ~ 1784.8	1845 ~ 1879.8	Tx: 8762 ~ 8912 Rx: 9237 ~ 9387	95 MHz
WCDMA 800 – B19	830 ~ 845	875 ~ 890	Tx: 312 ~ 363 Rx: 712 ~ 763	45 MHz
TDS CDMA 2000 – B34	2010 ~ 2025	2010 ~ 2025	Tx: 10054 ~ 10121 Rx: 10054 ~ 10121	0 MHz
TDS CDMA 1900 – B39	1880 ~ 1920	1880 ~ 1920	Tx: 9404 ~ 9596 Rx: 9404 ~ 9596	0 MHz
LTE 2100 – B1	1920 ~ 1980	2110 ~ 2170	Tx: 18000 ~ 18599 Rx: 0 ~ 599	190 MHz
LTE 1900 – B2	1850 ~ 1910	1930 ~ 1990	Tx: 18600 ~ 19199 Rx: 600 ~ 1199	80 MHz
LTE 1800 – B3	1710 ~ 1785	1805 ~ 1880	Tx: 19200 ~ 19949 Rx: 1200 ~ 1949	95 MHz
LTE AWS – B4	1710 ~ 1755	2110 ~ 2155	Tx: 19950 ~ 20399 Rx: 1950 ~ 2399	400 MHz
LTE 850 – B5	824 ~ 849	869 ~ 894	Tx: 20400 ~ 20649 Rx: 2400 ~ 2649	45 MHz
LTE 2600 – B7	2500 ~ 2570	2620 ~ 2690	Tx: 20750 ~ 21449 Rx: 2750 ~ 3449	120 MHz
LTE 900 – B8	880 ~ 915	925 ~ 960	Tx: 21450 ~ 21799 Rx: 3450 ~ 3799	45 MHz
LTE 1800 – B9	1749.9 ~ 1784.9	1844.9 ~ 1879.9	Tx: 21800 ~ 2149 Rx: 3800 ~ 4149	95 MHz
LTE AWS+ – B10	1710 ~ 1770	2110 ~ 2170	Tx: 22150 ~ 22749 Rx: 4150 ~ 4749	400 MHz
Mode	Freq. Tx (MHz)	Freq. Rx (MHz)	Channels	Tx-Rx Offset

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LTE 700a – B12	699 ~ 716	729 ~ 746	Tx: 23010 ~ 23179 Rx: 5010 ~ 5179	30 MHz
LTE 700c – B13	777 ~ 787	746 ~ 756	Tx: 23180 ~ 23279 Rx: 5180 ~ 5279	-31 MHz
LTE 700PS – B14	788 ~ 798	758 ~ 768	Tx: 23280 ~ 23379 Rx: 5280 ~ 5379	-30 MHz
LTE 700b – B17	704 ~ 716	734 ~ 746	Tx: 23730 ~ 23849 Rx: 5730 ~ 5849	30 MHz
LTE 800 – B19	830 ~ 845	875 ~ 890	Tx: 24000 ~ 24149 Rx: 6000 ~ 6149	45 MHz
LTE 800 – B20	832 ~ 862	791 ~ 821	Tx: 24150 ~ 24449 Rx: 6150 ~ 6449	-41 MHz
LTE 1500 – B21	1447.9 ~ 1462.9	1495.9 ~ 1510.9	Tx: 24450 ~ 24599 Rx: 6450 ~ 6599	48 MHz
LTE 1900+ – B25	1850 ~ 1915	1930 ~ 1995	Tx: 26040 ~ 26689 Rx: 8040 ~ 8689	80 MHz
LTE 850+ – B26	814 ~ 849	859 ~ 894	Tx: 26690 ~ 27039 Rx: 8690 ~ 9039	45 MHz
LTE 700 – B28A	703 ~ 733	758 ~ 788	Tx: 27210 ~ 27510 Rx: 9210 ~ 9510	55 MHz
LTE 700 – B28	703 ~ 748	758 ~ 803	Tx: 27210 ~ 27659 Rx: 9210 ~ 9659	55 MHz
LTE AWS-3 – B66	1710 ~ 1780	2210 ~ 2200	Tx: 131972-132671 Rx: 66436-67335	400 MHz
LTE600 – B71	663 ~ 698	617 ~ 652	Tx: 133122-133471 Rx: 68568-68935	46 MHz
LTE TDD 2600 – B38	2570 ~ 2620	2570 ~ 2620	Tx: 37750 ~ 38250 Rx: 37750 ~ 38250	0 MHz
LTE TDD 1900 – B39	1880 ~ 1920	1880 ~ 1920	Tx: 38250 ~ 38650 Rx: 38250 ~ 38650	0 MHz
LTE TDD 2300 – B40	2300 ~ 2400	2300 ~ 2400	Tx: 38650 ~ 39650 Rx: 38650 ~ 39650	0 MHz
LTE TDD 2500 – B41M	2555 ~ 2655	2555 ~ 2655	Tx: 40265 ~ 41215 Rx: 40265 ~ 41215	0 MHz

Table 5: RF Bands Characteristics

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2.7. RF Parameters

2.7.1. Sensitivity

Typical sensitivity levels are as follows:

Mode	Primary	Diversity	SIMO	3GPP
PCS 1900	-107.5	-	-	-102
DCS 1800	-107.0	-	-	-102
GSM 850	-108.5	-	-	-102
EGSM 900	-107.5	-	-	-102
WCDMA 2100 – B1	-109.0	-110.0	-111.5	-106.7
WCDMA 1900 – B2	-109.5	-110.5	-112	-104.7
WCDMA 1800 – B3	-107.5	-109.5	-109.5	-103.7
WCDMA AWS – B4	-109.5	-110.0	-112	-106.7
WCDMA 850 – B5	-110.0	-111.0	-112.5	-104.7
WCDMA 850 – B6	-110.0	-111.0	-112.5	-106.7
WCDMA 850 – B19	-110.0	-111.0	-112.5	-106.7
WCDMA 900 – B8	-109.5	-110.5	-112	-103.7
TDS CDMA 2000 – B34	-110.0	-	-	-105
TDS CDMA 1900 – B39	-110.0	-	-	-105
LTE 2100 – B1	-98.0	-98.5	-100.5	-96.3
LTE 1900 – B2	-97.0	-99.0	-99	-94.3
LTE 1800 – B3	-97.5	-99.5	-99.5	-93.3
LTE AWS – B4	-98.0	-99.0	-100.5	-96.3
LTE 850 – B5	-99.0	-100.5	-101.5	-94.3
LTE 2600 – B7	-97.5	-97.5	-99.5	-94.3
LTE 900 – B8	-98.5	-99.5	-101	-93.3
LTE 1800 – B9	-98.0	-99.0	-100.5	-95.3
LTE 700a – B12	-98.5	-99.5	-101	-93.3
LTE 700c – B13	-98.5	-99.5	-101	-93.3
Mode	Primary	Diversity	SIMO	3GPP

Not Subject to NDA

LTE 700PS – B14	-98.0	-99.5	-100.5	-93.3
LTE 700b – B18	-99.0	-100.0	-101.5	-96.3
LTE 800 – B19	-99.0	-99.5	-101.5	-96.3
LTE 800 – B20	-99.0	-99.0	-101.5	-93.3
LTE 1900+ – B25	-96.5	-98.5	-98.5	-92.8
LTE 850+ – B26	-99.0	-100.0	-101.5	-93.8
LTE 700 – B28A/B	-98.5	-100.5	-101.5	-94.8
LTE AWS-3 – B66	-98.0	-99.0	-100.5	-95.8
LTE600 – B71	-98.0	-97.5	-100.5	-93.5
LTE TDD 2600 – B38	-98.0	-98.5	-100.5	-96.3
LTE TDD 1900 – B39	-98.5	-99.5	-101	-96.3
LTE TDD 2300 – B40	-97.0	-98.5	-99.5	-96.3
LTE TDD 2500 – B41M	-97.0	-98.0	-99.5	-94.3

Table 6: sensitivity levels

Note: The sensitivity level has a deviation about +/- <2dB each model, device and channel because the level shows typical value.

LTE level is measured at BW 10M

2.7.2. Output power

Typical values for Max output level are as follow:

- 2G (GSM):

LB: Class 4(2W, 33dBm)

Class E2(0.5W,27dBm@EDGE)

HB: Class 1(1W, 30Bm)

Class E2(0.4W, 26dBm@EDGE)

- 3G (WCDMA): Class 3(0.25W, 24dBm)
- TD-SCDMA: Class 3(0.13W, 21dBm)
- 4G (FDD & TDD): Class 3(0.2W, 23dBm@1RB)

2.8. Mechanical Specifications

Not Subject to NDA

2.8.1. Dimensions

The module's overall dimensions are:

- Length: 28.2 mm, +/- 0.15 mm tolerance
- Width: 28.2 mm, +/- 0.15 mm tolerance
- Thickness: 2.2 mm, +/- 0.15 mm tolerance and The LE910Cx-WWX module's overall dimensions are:
- Length: 29.4 mm, +/- 0.15 mm tolerance
- Width: 29.4 mm, +/- 0.15 mm tolerance
- Thickness: 2.2 mm, +/- 0.15 mm tolerance

Note: LE910C1-SV's thickness is only 2.3mm, +/- 0.15 mm tolerance

Note: Consider a typical label thickness of 0.1 mm in addition to the module thickness.

2.8.2. Weight

The nominal weight of the LE910Cx module is 5.0 grams.

Not Subject to NDA

3. MODULE CONNECTIONS

3.1. Pin-out

PAD	Signal	I/O	Function	Type	Comment
USB HS 2.0 Communication Port					
B15	USB_D+	I/O	USB differential Data (+)		
C15	USB_D-	I/O	USB differential Data (-)		
A13	USB_VBUS	AI	Power sense for the internal USB transceiver	Power	
A14	USB_ID	AI	USB ID		See note below
Asynchronous UART					
N15	C103/TXD	I	Serial data input (TXD) from DTE	1.8V	
M15	C104/RXD	O	Serial data output to DTE	1.8V	
L14	C105/RTS	I	Input for Request to send signal (RTS) from DTE	1.8V	
P15	C106/CTS	O	Output for Clear to send signal (CTS) to DTE	1.8V	
P14	C107/DSR	O	Output for Data Set Ready (DSR) to DTE	1.8V	Alternate Fn GPIO_32
M14	C108/DTR	I	Input for Data Terminal Ready (DTR) from DTE	1.8V	Alternate Fn GPIO_34
N14	C109/DCD	O	Output for Data Carrier Detect (DCD) to DTE	1.8V	Alternate Fn GPIO_33
R14	C125/RING	O	Output for Ring Indication (RI) to DTE	1.8V	Alternate Fn GPIO_31
SPI – Serial Peripheral Interface / AUX UART					
F15	SPI_CLK	O	SPI Clock output	1.8V	
E15	SPI_MISO/ RX_AUX	I	SPI data Master Input Slave output / RX_AUX	1.8V	
D15	SPI_MOSI/TX_AUX	O	SPI data Master Output Slave input/ TX_AUX	1.8V	
H14	SPI_CS/GPIO11	O	SPI Chip select output / GPIO11	1.8V	See note below
SD/MMC Card Digital I/O					
J12	SD/MMC_CMD	O	SD Command	1.8/2.95V	
F12	SD/MMC_CLK	O	SD Card Clock	1.8/2.95V	
E12	SD/MMC_DATA0	I/O	SD Serial Data 0	1.8/2.95V	
G12	SD/MMC_DATA1	I/O	SD Serial Data 1	1.8/2.95V	

Not Subject to NDA

PAD	Signal	I/O	Function	Type	Comment
K12	SD/MMC_DATA2	I/O	SD Serial Data 2	1.8/2.95V	
H12	SD/MMC_DATA3	I/O	SD Serial Data 3	1.8/2.95V	
G13	SD/MMC_CD	I	SD card detect input	1.8V	Active Low
F13	VMMC	-	Power supply for MMC card pull-up resistors	1.8/2.95V	
WiFi (SDIO) Interface					
N13	WiFi_SD_CMD	O	Wi-Fi SD Command	1.8V	
L13	WiFi_SD_CLK	O	Wi-Fi SD Clock	1.8V	
J13	WiFi_SD_DATA0	I/O	Wi-Fi SD Serial Data 0	1.8V	
M13	WiFi_SD_DATA1	I/O	Wi-Fi SD Serial Data 1	1.8V	
K13	WiFi_SD_DATA2	I/O	Wi-Fi SD Serial Data 2	1.8V	
H13	WiFi_SD_DATA3	I/O	Wi-Fi SD Serial Data 3	1.8V	
L12	WiFi_SDRST	O	Wi-Fi Reset / Power enable control	1.8V	
M11	WLAN_SLEEP_CLK	O	Wi-Fi Sleep clock output	1.8V	
L4	WOW	I	Wake On WLAN	1.8V	Active Low
LTE-WiFi Coexistence					
M8	WCI_TX	O	Wireless coexistence interface TXD	1.8V	
M9	WCI_RX	I	Wireless coexistence interface RXD	1.8V	
SIM Card Interface 1					
A6	SIMCLK1	O	External SIM 1 signal – Clock	1.8/2.85V	
A7	SIMRST1	O	External SIM 1 signal – Reset	1.8/2.85V	
A5	SIMIO1	I/O	External SIM 1 signal - Data I/O	1.8/2.85V	Internally PU 10 kΩ to SIMVCC1
A4	SIMIN1	I	External SIM 1 signal - Presence	1.8V	Active low
A3	SIMVCC1	-	External SIM 1 signal – Power supply for SIM 1	1.8/2.85V	
SIM Card Interface 2					
C1	SIMCLK2	O	External SIM 2 signal – Clock	1.8/2.85V	
D1	SIMRST2	O	External SIM 2 signal – Reset	1.8/2.85V	
C2	SIMIO2	I/O	External SIM 2 signal – Data I/O	1.8/2.85V	Internally PU 10kΩ to SIMVCC2
G4	SIMIN2	I	External SIM 2 signal – Presence	1.8V	Active low

PAD	Signal	I/O	Function	Type	Comment

Not Subject to NDA

D2	SIMVCC2	-	External SIM 2 signal – Power supply for SIM 2	1.8/2.85V	
Digital Voice Interface (DVI)					
B9	DVI_WAO	O	Digital Voice interface (WAO master output)	1.8V	
B6	DVI_RX	I	Digital Voice interface (Rx)	1.8V	
B7	DVI_TX	O	Digital Voice interface (Tx)	1.8V	
B8	DVI_CLK	O	Digital Voice interface (CLK master output)	1.8V	
B12	REF_CLK	O	Reference clock for external Codec	1.8V	See Note below
General Purpose Digital I/O					
C8	GPIO_01	I/O	GPIO_01 / STAT_LED	1.8V	Alternate Fn I2C
C9	GPIO_02	I/O	GPIO_02	1.8V	Alternate Fn I2C
C10	GPIO_03	I/O	GPIO_03	1.8V	Alternate Fn I2C
C11	GPIO_04	I/O	GPIO_04	1.8V	Alternate Fn I2C
B14	GPIO_05	I/O	GPIO_05	1.8V	Alternate Fn I2C
C12	GPIO_06	I/O	GPIO_06	1.8V	Alternate Fn I2C
C13	GPIO_07	I/O	GPIO_07	1.8V	Alternate Fn I2C
K15	GPIO_08	I/O	GPIO_08 / SW_RDY	1.8V	Alternate Fn I2C
L15	GPIO_09	I/O	GPIO_09	1.8V	Alternate Fn I2C
G15	GPIO_10	I/O	GPIO_10	1.8V	Alternate Fn I2C
RF Section					
K1	Antenna	I/O	GSM/EDGE/UMTS/LTE Main antenna (50 Ohm)	RF	
F1	ANT_DIV	I	UMTS/LTE antenna diversity input (50 Ohm)	RF	
GPS Section					
R9	ANT_GPS	I	GPS antenna (50 Ohm)	RF	

Not Subject to NDA

PAD	Signal	I/O	Function	Type	Comment
R7	GPS_LNA_EN	O	Enables the external regulator for GPS LNA	1.8V	
N9	GPS_SYNC	O	GPS sync signal for Dead Reckoning	1.8V	
Miscellaneous Functions					
R12	ON_OFF_N	I	Power ON / Power OFF input		Active low
R13	HW_SHUTDOWN_N	I	Unconditional Shutdown input		Active low
R11	VAUX/PWRMON	O	Supply output for external accessories / Power ON monitor	1.8V	
E13	VIO_1V8	O	IO voltage for internal ICs This power rail is always on while LE910Cx is working.	1.8V	
B1	ADC_IN1	AI	Analog/Digital Converter Input 1	Analog	
H4	ADC_IN2	AI	Analog/Digital Converter Input 2	Analog	
D7	ADC_IN3	AI	Analog/Digital Converter Input 3	Analog	
SGMII Interface					
E4	SGMII_RX_P	AI	SGMII receive – plus	PHY	
F4	SGMII_RX_M	AI	SGMII receive – minus	PHY	
D5	SGMII_TX_P	AO	SGMII transmit – plus	PHY	
D6	SGMII_TX_M	AO	SGMII transmit - minus	PHY	
HSIC Interface					
A12	HSIC_DATA	I/O	High-speed inter-chip interface - data	1.2V	Optional
A11	HSIC_STB	I/O	High-speed inter-chip interface - strobe	1.2V	Optional
I2C Interface					
B11	I2C_SCL	I/O	I2C clock	1.8V	Internally PU 2.2kΩ to 1.8V
B10	I2C_SDA	I/O	I2C Data	1.8V	Internally PU 2.2kΩ to 1.8V
Power Supply					
M1	VBATT	-	Main Power Supply (Digital Section)	Power	
M2	VBATT	-	Main Power Supply (Digital Section)	Power	
N1	VBATT_PA	-	Main Power Supply (RF Section)	Power	
N2	VBATT_PA	-	Main Power Supply (RF Section)	Power	

Not Subject to NDA

PAD	Signal	I/O	Function	Type	Comment
P1	VBATT_PA	-	Main Power Supply (RF Section)	Power	
P2	VBATT_PA	-	Main Power Supply (RF Section)	Power	
A2	GND	-	Ground		
B13	GND		Ground		
D4	GND	-	Ground		
E1	GND	-	Ground		
E2	GND	-	Ground		
E14	GND	-	Ground		
F2	GND	-	Ground		
G1	GND	-	Ground		
G2	GND	-	Ground		
G7	GND	-	Ground		
G8	GND	-	Ground		
G9	GND	-	Ground		
H1	GND	-	Ground		
H2	GND	-	Ground		
H7	GND	-	Ground		
H8	GND	-	Ground		
H9	GND	-	Ground		
J1	GND	-	Ground		
J2	GND	-	Ground		
J7	GND	-	Ground		
J8	GND	-	Ground		
J9	GND	-	Ground		
K2	GND	-	Ground		
L1	GND	-	Ground		
L2	GND	-	Ground		
M3	GND	-	Ground		
M4	GND	-	Ground		
M12	GND	-	Ground		
N3	GND	-	Ground		
N4	GND	-	Ground		

Not Subject to NDA

PAD	Signal	I/O	Function	Type	Comment
N5	GND	-	Ground		
N6	GND	-	Ground		
P3	GND	-	Ground		
P4	GND	-	Ground		
P5	GND	-	Ground		
P6	GND	-	Ground		
P8	GND	-	Ground		
P9	GND	-	Ground		
P10	GND	-	Ground		
P13	GND	-	Ground		
R2	GND	-	Ground		
R3	GND	-	Ground		
R5	GND	-	Ground		
R6	GND	-	Ground		
R8	GND	-	Ground		
R10	GND	-	Ground		
Reserved					
A8	Reserved	-	Reserved		
A9	Reserved	-	Reserved		
A10	Reserved	-	Reserved		
B2	Reserved	-	Reserved		
B3	Reserved	-	Reserved		
B4	Reserved	-	Reserved		
B5	Reserved	-	Reserved		
C3	Reserved	-	Reserved		
C4	Reserved	-	Reserved		
C5	Reserved	-	Reserved		
C6	Reserved	-	Reserved		
C7	Reserved	-	Reserved		
C14	Reserved	-	Reserved		
D3	Reserved	-	Reserved		
D8	Reserved	-	Reserved		

Not Subject to NDA

PAD	Signal	I/O	Function	Type	Comment
D9	Reserved	-	Reserved		
D10	Reserved	-	Reserved		
D11	Reserved	-	Reserved		
D12	Reserved	-	Reserved		
D13	Reserved	-	Reserved		
D14	Reserved	-	Reserved		
E3	Reserved	-	Reserved		
F3	Reserved	-	Reserved		
F14	Reserved	-	Reserved		
G3	Reserved	-	Reserved		
G14	Reserved	-	Reserved		
H3	Reserved	-	Reserved		
H15	Reserved	-	Reserved		
J3	Reserved	-	Reserved		
J4	Reserved	-	Reserved		
J14	Reserved	-	Reserved		
J15	Reserved	-	Reserved		
K3	Reserved	-	Reserved		
K4	Reserved	-	Reserved		
K14	Reserved	-	Reserved		
L3	Reserved	-	Reserved		
M5	Reserved	-	Reserved		
M6	Reserved	-	Reserved		
M7	Reserved	-	Reserved		
M10	Reserved	-	Reserved		
N7	Reserved	-	Reserved		
N8	Reserved	-	Reserved		
N10	Reserved	-	Reserved		
N11	Reserved	-	Reserved		
N12	Reserved	-	Reserved		
P7	Reserved	-	Reserved		
P11	Reserved	-	Reserved		

Not Subject to NDA

PAD	Signal	I/O	Function	Type	Comment
P12	Reserved	-	Reserved		
Reserved for future use					
R4	RFU	-	Reserved for future use. Not connected internally		Can be tied to GND

Table 7: Pin-out

Note: When the UART signals are used as the communication port between the host and the modem, the RTS must be connected to GND (on the module side) if flow control is not used.

If the UART port is not used, all UART signals can be left disconnected.

Note: Unless otherwise specified, RESERVED pins must be left unconnected (floating).

Note: The following pins are unique for the LE910Cx and may not be supported on other (former or future) xE910 family modules. Special care must be taken when designing the application board if future compatibility is required.

REF_CLK

SPI_CS

USB_ID

I2C_SCL

I2C_SDA

ADC_IN2
ADC_IN3

Note: The pin out of LE910Cx-WWX's is perfectly same as LE910Cx even if the demission is a little bigger than others.

Not Subject to NDA

3.2. Signals That Must Be Connected

Table 8 lists the LE910Cx signals that must be connected even if not used by the end application:

PAD	Signal	Notes
M1, M2, N1, N2, P1, P2	VBATT & VBATT_PA	
A2, B13, D4, E1, E2, E14, F2, G1, G2, G7, G8, G9, H1, H2, H7, H8, H9, J1, J2, J7, J8, J9, K2, L1, L2, M3, M4, M12, N3, N4, N5, N6, P3, P4, P5, P6, P8, P9, P10, P13, R2, R3, R5, R6, R8, R10	GND	
R12	ON/OFF	Main power on off signal
R13	HW_SHUTDOWN_N	Emergency power off
B15	USB_D+	If not used, connect to a Test Point or an USB connector
C15	USB_D-	If not used, connect to a Test Point or an USB connector
A13	USB_VBUS	If not used, connect to a Test Point or an USB connector
N15	C103/TXD	If not used, connect to a Test Point
M15	C104/RXD	If not used, connect to a Test Point
L14	C105/RTS	If flow control is not used, connect to GND
P15	C106/CTS	If not used, connect to a Test Point
D15	TX_AUX	If not used, connect to a Test Point
E15	RX_AUX	If not used, connect to a Test Point
K1	Antenna	MAIN antenna
F1	ANT_DIV	DIV antenna
R9	ANT_GPS	GPS antenna
C4, C5, C6, C7, D3, E3, G3, P11	Reserved	Connect to a Test Point for EXFO internal use
L15	GPIO_09	If not used, connect to a Test Point
M9	WCI_RX	If not used, connect to a Test Point

Table 8: Mandatory Signals

Not Subject to NDA

3.3. LGA Pads Layout

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
1		ADC_IN1	SIMCLK2	SIMRST2	GND	ANT_DIV	GND	GND	GND	ANT_MAIN	GND	VBATT	VBATT_PA	VBATT_PA		1
2	GND	RES	SIMIO2	SIMVCC2	GND	GND	GND	GND	GND	GND	GND	VBATT	VBATT_PA	VBATT_PA	GND	2
3	SIMVCC	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	GND	GND	GND	GND	3
4	SIMIN	RES	RES	GND	SGMII_RX_P	SGMII_RX_M	SIMIN2	ADC_IN2	RES	RES	WOW	GND	GND	GND	RFU	4
5	SIMIO	RES	RES	SGMII_TX_P								RES	GND	GND	GND	5
6	SIMCLK	DVI_RX	RES	SGMII_TX_M								RES	GND	GND	GND	6
7	SIMRST	DVI_TX	RES	ADC_IN3			GND	GND	GND			RES	RES	RES	GPS_LNA_EN	7
8	RES	DVI_CLK	GPIO_01	RES			GND	GND	GND			WCI_TXD TGPIO24	RES	GND	GND	8
9	RES	DVI_WAO	GPIO_02	RES			GND	GND	GND			WCI_RXD TGPIO25	GPS_SYNC	GND	ANT_GPS	9
10	RES	I2C_SDA	GPIO_03	RES								RFCLK2_QCA	RES	GND	GND	10
11	HSIC_STB	I2C_SCL	GPIO_04	RES								WLAN_SLEEP_CLK	RES	RES	VAUX/PWRMON	11
12	HSIC_DATA	REF_CLK	GPIO_06	RES	MMC_DAT0	MMC_CLK	MMC_DAT1	MMC_DAT3	MMC_CMD	MMC_DAT2	WIFI_SD RST	GND	RES	RES	ON_OFF*	12
13	VUSB	GND	GPIO_07	RES	VIO_1V8	VMMC	MMC_CD	WIFI_SD3	WIFI_SD0	WIFI_SD2	WIFI_SD CLK	WIFI_SD1	WIFI_SD CMD	GND	HW_SHUTDOWN*	13
14	USB_ID	GPIO_05	RES	RES	GND	RES	RES	SPI_CS/ GPIO_11	RES	RES	C105/RTS	C108/DTR	C109/DCD	C107/DSR	C125/RING	14
15		USB_D+	USB_D-	SPI_MOSI /TX_AUX	SPI_MISO /RX_AUX	SPI_CLK	GPIO_10	RES	RES	GPIO_08	GPIO_09	C104/RXD	C103/TXD	C106/CTS		15

Figure 2: LGA Pads Layout

3.4. Backward Compatibility to xE910 Family

The LE910Cx is a new series in the xE910 form factor

The LE910Cx is fully backward compatible with the previous xE910 in terms of:

- Mechanical dimensions
- Package and pin-map

To support the extra features and additional interfaces, the LE910Cx introduces more pins than the xE910.

The extra pins of the LE910Cx can be considered as optional if not needed and can be left unconnected (floating) if not used.

Not Subject to NDA

In this case, the new LE910Cx can be safely mounted on existing carrier boards designed for the previous xE910.

The additional pins of the LE910Cx are shown in Figure 3 (marked Green)

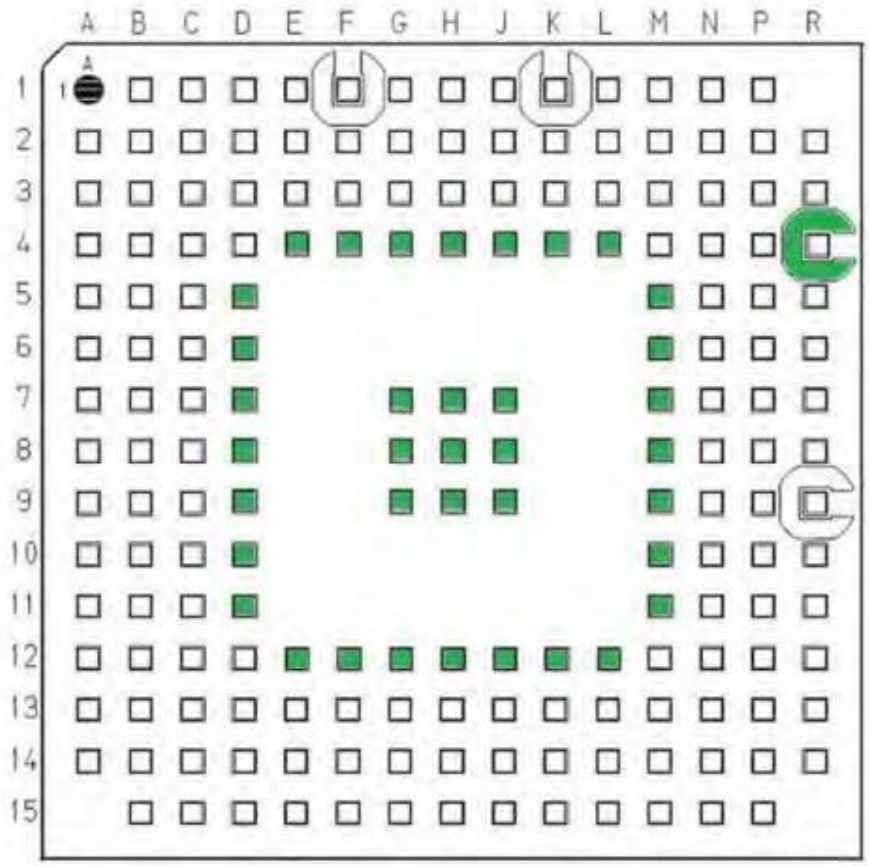

Figure 3: LE910Cx vs. LE910 Pin-out Comparison (top view)

Not Subject to NDA

4. ELECTRICAL SPECIFICATIONS

4.1. Absolute Maximum Ratings – Not Operational

Warning: A deviation from the value ranges listed below may harm the LE910Cx module.

Symbol	Parameter	Min	Max	Unit
VBATT	Battery supply voltage on pin VBATT	-0.5	+6.0	[V]
VBATT TRANSIENT	Transient voltage on pin VBATT (< 10 ms)	-0.5	+7.0	[V]
VBATT_PA	Battery supply voltage on pin VBATT_PA	-0.3	+6.0	[V]

Table 9: Absolute Maximum Ratings – Not Operational

4.2. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_{amb}	Ambient temperature	-40	+25	+85	[°C]
VBATT	Battery supply voltage on pin VBATT	3.4	3.8	4.2	[V]
VBATT_PA	Battery supply voltage on pin VBATT_PA	3.4	3.8	4.2	[V]
$I_{BATT_PA} + I_{BATT}$	Peak current to be used to dimension decoupling capacitors on pin VBATT_PA	-	80	2000	[mA]

Table 10: Recommended Operating Conditions

Not Subject to NDA

4.3. Logic Level Specifications

Unless otherwise specified, all LE910Cx interface circuits are 1.8V CMOS logic. Only few specific interfaces (such as MAC, USIM and SD Card) are capable of dual voltage I/O.

The following tables show the specifications of the logic level used in the LE910Cx interface circuits.

Note: Do not connect LE910Cx digital logic signals directly to OEM digital logic signals with a level higher than 2.7V for 1.8V CMOS signals.

4.3.1. 1.8V Pads - Absolute Maximum Ratings

Parameter	Min	Max
Input level on any digital pin when on	-0.3V	+2.16V
Input voltage on analog pins when on	-0.3V	+2.16 V

Table 11: Absolute Maximum Ratings - Not Functional

4.3.2. 1.8V Standard GPIOs

Pad	Parameter	Min	Max	Unit	Comment
V_{IH}	Input high level	1.25V	--	[V]	
V_{IL}	Input low level	--	0.6V	[V]	
V_{OH}	Output high level	1.4V	--	[V]	
V_{OL}	Output low level	--	0.45V	[V]	
I_{IL}	Low-level input leakage current	-1	--	[uA]	No pull-up
I_{IH}	High-level input leakage current	--	+1	[uA]	No pull-down
R_{PU}	Pull-up resistance	30	390	[kΩ]	
R_{PD}	Pull-down resistance	30	390	[kΩ]	
C_i	Input capacitance	--	5	[pF]	

Table 12: Operating Range – Interface Levels (1.8V CMOS)

Not Subject to NDA

Note: Pull-Up and Pull-Down resistance of GPIO3, GPIO7 and GPIO8 is different from the one mentioned above.

GPIO3 pull resistance is specified as 10KΩ to 50KΩ

4.3.3. 1.8V SD Card Pads

Pad	Parameter	Min	Max	Unit	Comment
V_{IH}	Input high level	1.27V	2V	[V]	
V_{IL}	Input low level	-0.3V	0.58V	[V]	
V_{OH}	Output high level	1.4V	--	[V]	
V_{OL}	Output low level	0	0.45V	[V]	
I_{IL}	Low-level input leakage current	-2	-	[uA]	No pull-up
I_{IH}	High-level input leakage current	-	2	[uA]	No pull-down
R_{PU}	Pull-up resistance	10	100	[kΩ]	
R_{PD}	Pull-down resistance	10	100	[kΩ]	
C_i	Input capacitance		5	[pF]	

Table 13: Operating Range – SD Card Pads Working at 1.8V

4.3.4. 1.8V SIM Card Pads

Pad	Parameter	Min	Max	Unit	Comment
V_{IH}	Input high level	1.35V	2V	[V]	
V_{IL}	Input low level	-0.3V	0.43V	[V]	
V_{OH}	Output high level	1.35V	1.875V	[V]	
V_{OL}	Output low level	0V	0.4V	[V]	
I_{IL}	Low-level input leakage current	-2	-	[uA]	No pull-up
I_{IH}	High-level input leakage current	-	2	[uA]	No pull-down
R_{PU}	Pull-up resistance	10	100	[kΩ]	

Not Subject to NDA

Pad	Parameter	Min	Max	Unit	Comment
R_{PD}	Pull-down resistance	10	100	[kΩ]	
C_i	Input capacitance		5	[pF]	

Table 14: Operating Range – SIM Pads Working at 1.8V

4.3.5. Dual Voltage Pads - Absolute Maximum Ratings

Parameter	Min	Max
Input level on any digital pin when on	-0.3V	+3.6V
Input voltage on analog pins when on	-0.3V	+3.6 V

Table 15: Absolute Maximum Ratings - Not Functional

4.3.6. SD Card Pads @ 2.95V

Pad	Parameter	Min	Max	Unit	Comments
V_{IH}	Input high level	1.9V	3.1V	[V]	
V_{IL}	Input low level	-0.3V	0.7V	[V]	
V_{OH}	Output high level	2.1V	3.05V	[V]	
V_{OL}	Output low level	0V	0.4V	[V]	
I_{IL}	Low-level input leakage current	-10		[uA]	No pull-up
I_{IH}	High-level input leakage current		10	[uA]	No pull-down
R_{PU}	Pull-up resistance	10	100	[kΩ]	
R_{PD}	Pull-down resistance	10	100	[kΩ]	
C_i	Input capacitance		5	[pF]	

Table 16: Operating Range – For SD Card Pads Operating at 2.95V

4.3.7. SIM Card Pads @2.95V

Pad	Parameter	Min	Max	Unit	Comment
V_{IH}	Input high level	2.1V	3.1V	[V]	
V_{IL}	Input low level	-0.3V	0.55V	[V]	

Not Subject to NDA

Pad	Parameter	Min	Max	Unit	Comment
V_{OH}	Output high level	2.25V	3.1V	[V]	
V_{OL}	Output low level	0V	0.4V	[V]	
I_{IL}	Low-level input leakage current	-10		[uA]	No pull-up
I_{IH}	High-level input leakage current		10	[uA]	No pull-down
R_{PU}	Pull-up resistance	10	100	[kΩ]	
R_{PD}	Pull-down resistance	10	100	[kΩ]	
C_i	Input capacitance		5	[pF]	

Table 17: Operating Range – For SIM Pads Operating at 2.95V

Not Subject to NDA

5. HARDWARE COMMANDS

5.1. Turning on the LE910Cx Module

To turn on the LE910Cx module, the ON_OFF_N pad must be asserted low for at least 1 second and then released.

The maximum current that can be drained from the ON/OFF # pad is 0.1 mA. This pin is pulled up internally; customers should expect to see ~ 800 mV on the output.

Figure 4 illustrates a simple circuit to power on the module using an inverted buffer output.

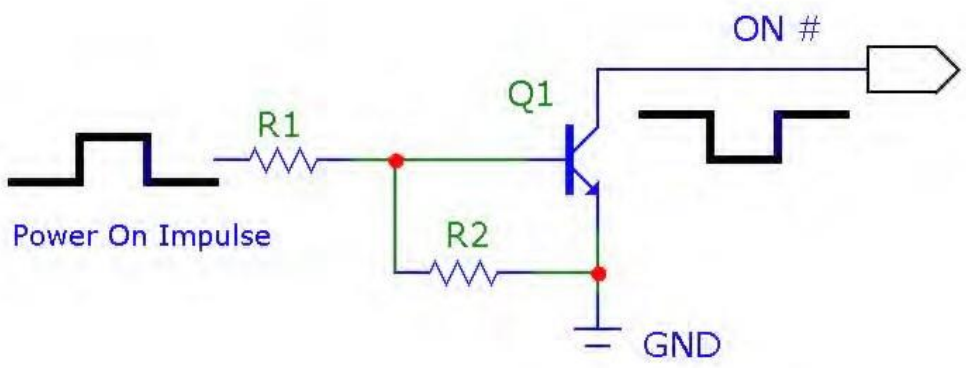

Figure4:Power-onCircuit

Note: Recommended values R2 = 47 kΩ, R1 = 10 kΩ.

5.2. Initialization and Activation State

After turning on the LE910Cx module, a predefined internal boot sequence performs the HW and SW initialization of the module, which takes some time to complete. During this process, the LE910Cx is not accessible.

As shown in Figure 5, the LE910Cx becomes operational at least 20 seconds after the assertion of ON_OFF.

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Note: During the Initialization state, the AT commands are not available. The DTE host must wait for the Activation state before communicating with the LE910Cx

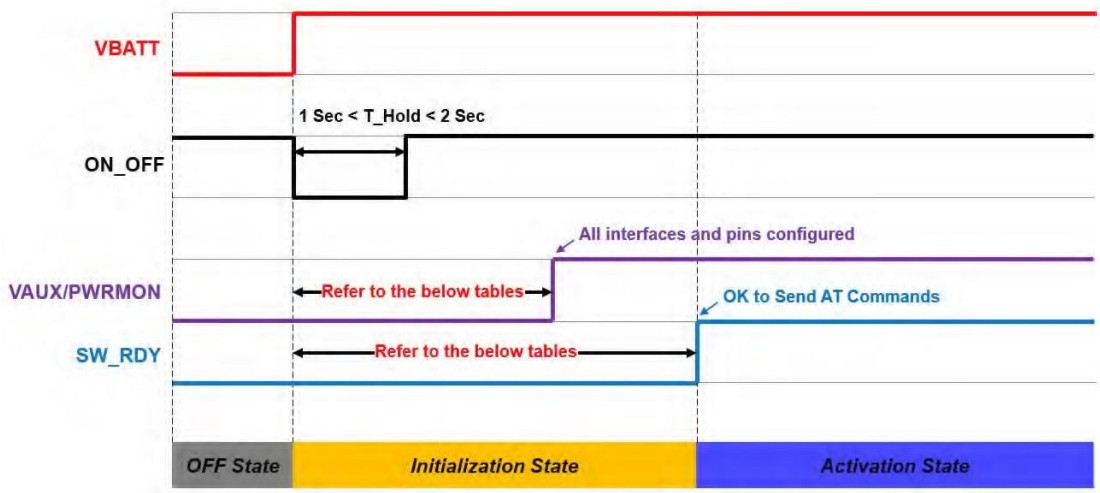

Figure5:LE910CxInitializationandActivation

A flow chart showing the proper turn on procedure is displayed below:

Not Subject to NDA

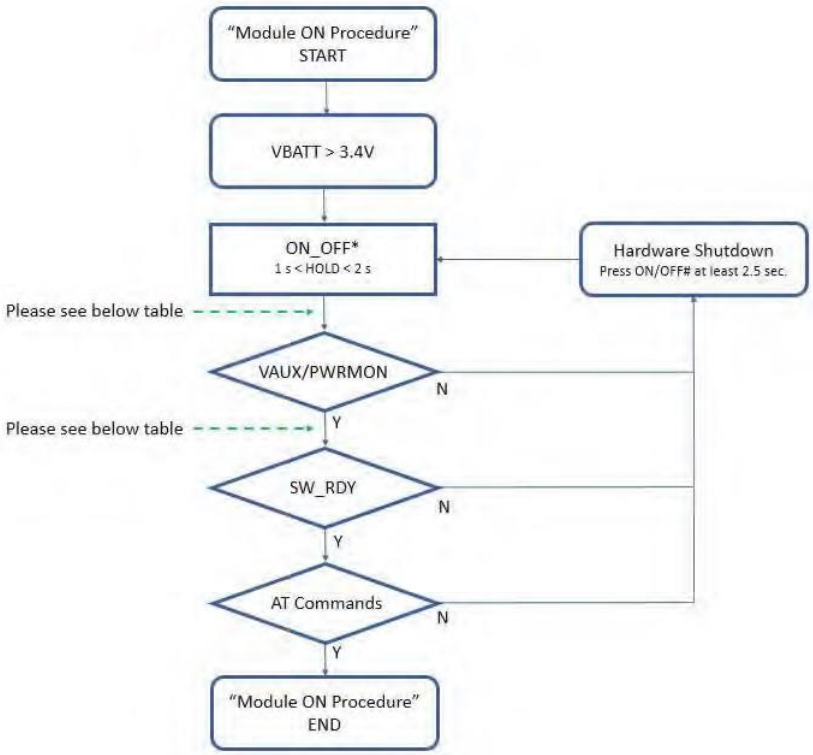

Figure 6: Turn-on Procedure

Timing of VAUX/PWRMON and SW_RDY

Models	ON ↔ VAUX/PWRMON	ON ↔ SW_RDY
LE910C1-NA	Typ. 21 sec	Typ. 28 Sec
LE910C4-NS		
LE910C1-AP		
LE910C4-AP		
LE910C1-EU		
LE910C4-EU		
LE910C1-NF		
LE910C4-NF		
LE910C1-LA		
LE910C4-LA		
LE910C4-CN		

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Models	ON ↔ VAUX/PWRMON	ON ↔ SW_RDY
LE910C1-SA	Typ. 13 Sec	Typ. 16 Sec
LE910C1-ST		
LE910C1-SV		
LE910C1-EUX	Typ. 10 Sec	Typ. 20 Sec
LE910C1-SAX		
LE910C1-SVX		

Table 18: Timing of VAUX/PWRMON and SW_RDY

Note: SW_RDY signal is available on GPIO_08 (by default GPIO_08 functions as SW_RDY)

Note: To check whether the LE910Cx has completely powered on, monitor the SW_RDY hardware line. When SW_RDY becomes high, the module is completely powered on and is ready to accept AT commands.

Note: During the SW initialization of the LE910Cx, the SW configures all pads and interfaces to the desired mode. When PWRMON goes high, this indicates that the initialization of all I/O pads is completed.

Note: Do not use any pull-up resistor on the ON_OFF_N line as it is pulled up internally. Using a pull-up resistor may cause latch-up problems on the LE910Cx power regulator and improper powering on/off of the module. The ON_OFF_N line must be connected only in an open-collector configuration.

Note: For systems not requiring controlled power ON/OFF, automatic power on can be supported by shorting the ON_OFF signal directly to GND

Not Subject to NDA

In this case, the module will start power on sequence immediately after VBATT supply is applied

Note: Active low signals are labeled with a name that ends with "#" or with "_N"

Note: To avoid a back-powering effect, it is recommended to prevent any HIGH logic level signal from being applied to the module's digital pins when it is powered OFF or during an ON/OFF transition.

A flow chart showing the AT commands managing procedure is displayed below:

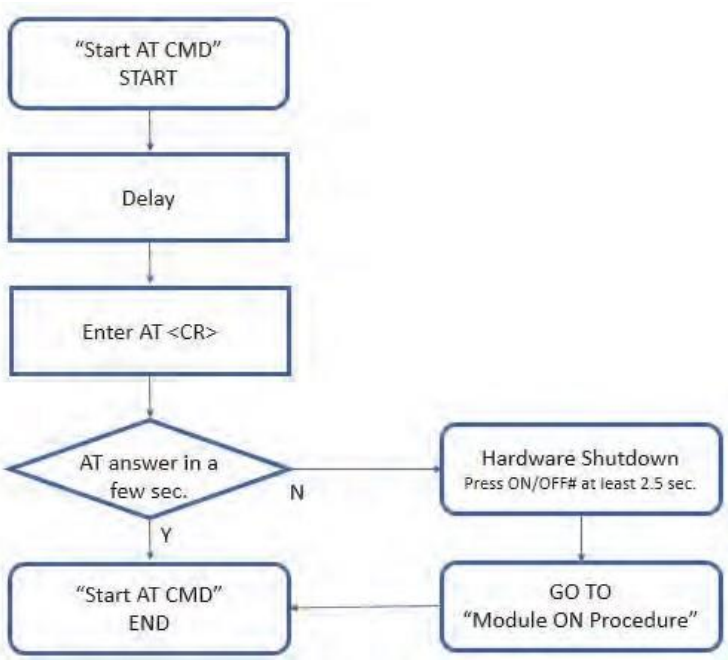

Figure 7: AT commands managing procedure

Note: Waiting time for the AT commands answer can vary between different LE910Cx variants, between 2-6 sec.

Not Subject to NDA

5.3. Turning off the LE910Cx Module

Turning off the device can be done in the following different ways:

- Shutdown by software using the AT#SHDN software command
- Hardware shutdown using ON_OFF_N pad
- Hardware Unconditional Shutdown using the SHDN_N pad

When the device is shut down by a software command or hardware shutdown, it issues a detach request to the network, informing the network that the device will no longer be reachable.

Note: To check if the device has powered off, monitor the PWRMON/SW_RDY hardware line. When PWRMON/SW_RDY goes low, it means the device has powered off.

Note: To avoid a back-powering effect, it is recommended to prevent any HIGH logic level signal from being applied to the module's digital pins when it is powered OFF or during an ON/OFF transition.

5.3.1. Shutdown by Software Command

The LE910Cx module can be shut down by a software command.

When a shutdown command is sent, LE910Cx enters the Finalization state and at the end of the finalization process shuts down PWRMON/SW_RDY .

The duration of the Finalization state may vary according to the current situation of the module, so it is not possible to define a value.

Usually, it will take more than 10 seconds from sending a shutdown command until a complete shutdown is achieved. The DTE host should monitor the PWRMON/SW_RDY status to observe the actual power-off.

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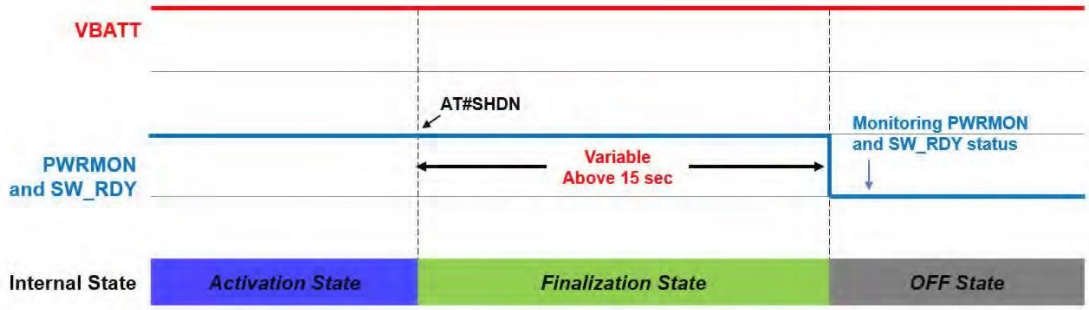

Figure 8: Shutdown by Software Command

Note: To check whether the device has powered off, monitor the PWRMON/SW_RDY hardware line. When PWRMON/SW_RDY goes low, the device has powered off.

5.3.2. Hardware Shutdown

To turn off the LE910Cx module, the ON_OFF_N pad must be asserted low for at least 2.5 seconds and then released. Use the same circuitry and timing for power-on.

When the ON/OFF# hold time is above 2.5 seconds, the LE910Cx enters the Finalization state and eventually shuts down PWRMON/SW_RDY .

The duration of the Finalization state can differ according to the current module situation, so a value cannot be defined.

Usually, it will take more than 15 seconds from sending a shutdown command until a complete shutdown is achieved. The DTE host should monitor the status of PWRMON/SW_RDY to observe the actual power-off.

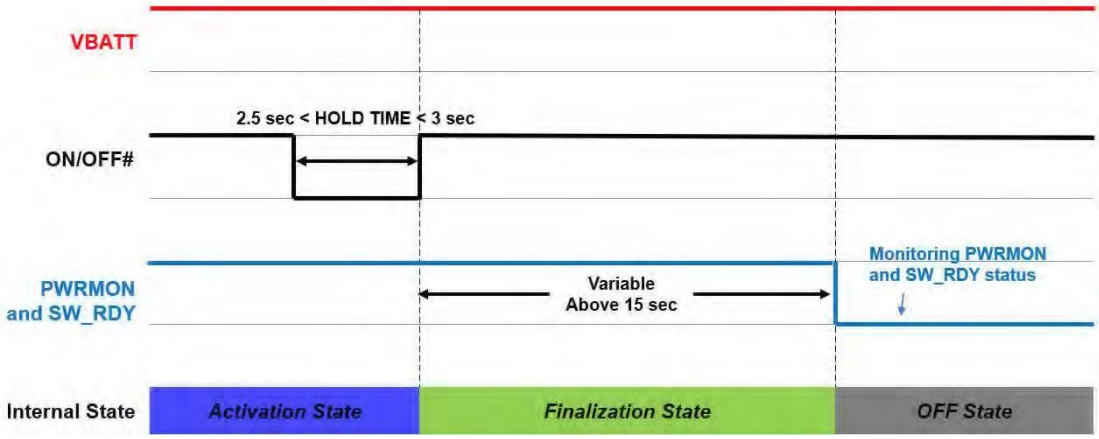

Figure 9: Hardware Shutdown

Not Subject to NDA

Note: To check whether the device has powered off, monitor the PWRMON/SW_RDY hardware line. When PWRMON/SW_RDY or goes low, the device has powered off.

5.3.3. Unconditional Hardware Shutdown

To unconditionally shut down the LE910Cx module, the HW_SHUTDOWN_N pad must be tied low for at least 200 milliseconds and then released.

Figure 10 shows a simple circuit for applying an unconditional shutdown.

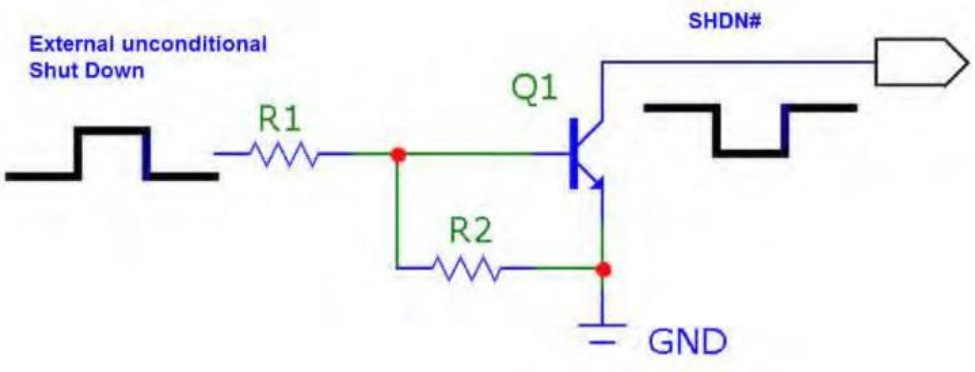

Figure 10: Circuit for Unconditional Hardware Shutdown

Figure 11 shows the system power-down timing when using HW_SHUTDOWN_N.

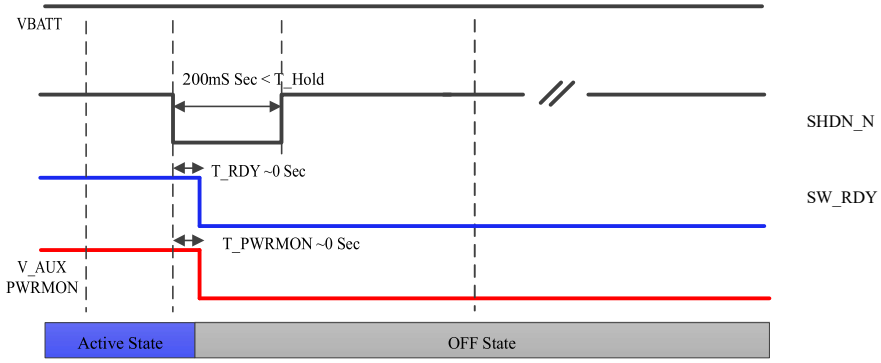

Figure 11: Power down timing using HW_SHUTDOWN_N

Note: Recommended values are as follows: R2 = 47kΩ, R1 = 10kΩ.

Not Subject to NDA

Note: Do not use any pull-up resistor on the HW_SHUTDOWN_N line or any totem pole digital output. Using a pull-up resistor may cause latch-up problems on the LE910Cx power regulator and improper functioning of the module. The HW_SHUTDOWN_N line must be connected only in an open-collector configuration.

Note: The Unconditional Hardware Shutdown must always be implemented on the boards, but this function must use it only as an emergency exit procedure, and not as a normal power-off operation.

5.4. Powering OFF the Module

Powering OFF the module should be done gracefully allowing the module to complete all ongoing and pending tasks while properly handling all memory buffers.

In a complete power supply shut down is needed, the below procedure must be followed: 1. Perform a HW shutdown as described in Section 5.3.1

2. Wait for the HW Shutdown procedure to complete (monitor the PWRMON/SW_RDY pin).
3. Turn OFF power supply to the module

Warning: Carefully follow the recommended procedure for shut down and power off.

Failure to follow the recommended shut-down and power off procedures might damage the device and consequently void the warranty.

5.5. Fast Power Down

The gentle power down procedure is described in chapter 5.3.1 and 5.3.2. It normally takes more than 15 seconds to de-attach network and make LE910Cx internal filesystem properly closed.

In the event of an unwanted power supply loss, LE910Cx can be switched off without any risk of filesystem data corruption by implementing Fast Power Down feature.

The Fast Power Down feature permits to reduce the current consumption and the timeto-power off to minimum values.

Not Subject to NDA

Note: Refer to LE910Cx series AT command reference guide (Fast power down - #FASTSHDN) in order to set up detailed AT command.

5.5.1. Fast Shut Down by Hardware

The Fast Shut Down is triggered by a GPIO. Customers wishing to implement the Fast Shut Down should configure a GPIO as the trigger pin for the Fast Shut Down through AT command. The high-to-low transition of a GPIO triggers the Fast Shut Down and then the LE910Cx module turns off within 30ms.

Below is the example hardware configuration for the Fast Shut Down.

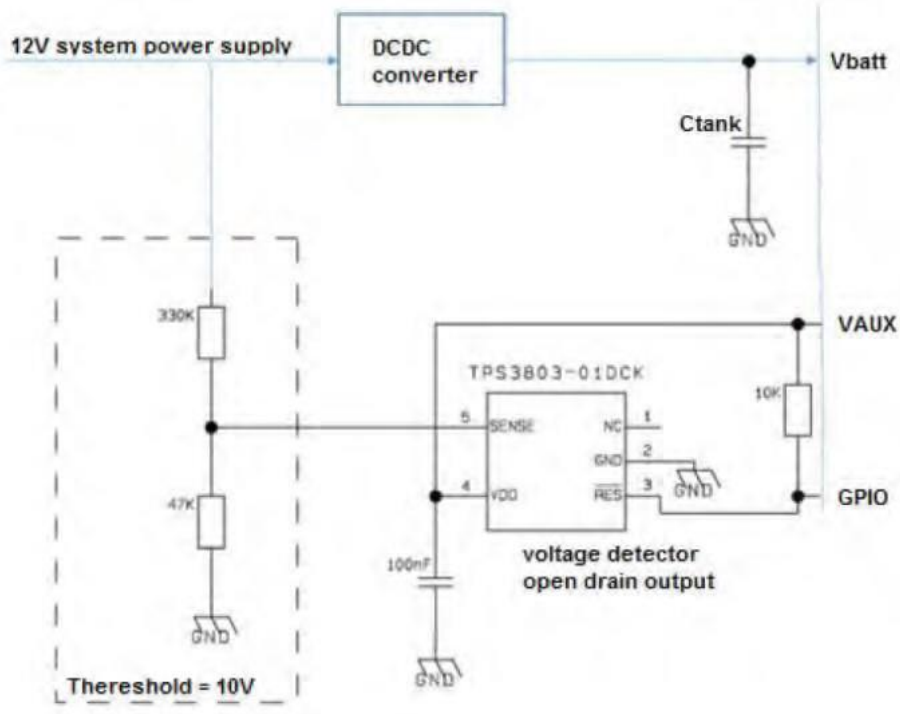

Figure 12: Example for Fast Shut Down circuit

Note: Consider the voltage drop under max current conditions when defining the voltage detector threshold in order to avoid unwanted shutdown.

Not Subject to NDA

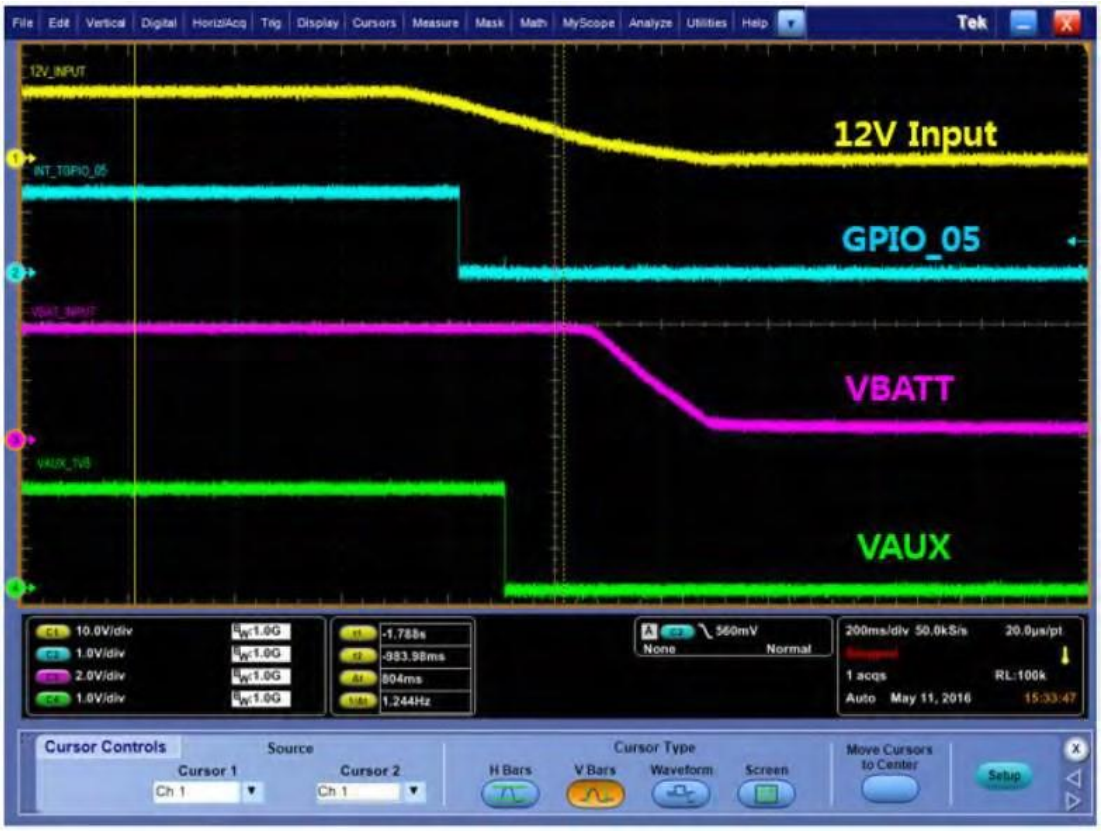

Figure 13: Example of Timing diagram for Fast Shut Down

The most important thing is that a system should give enough energy. The LE910Cx turns off safely for 30ms after the Fast Shut Down is triggered. Otherwise, unwanted memory corruption may occur. The VAUX pin can be used to check if the LE910Cx is turned off. If VUAX is low, LE910Cx is turned off.

The following formula can be used to calculate Ctank value to provide the LE910Cx with sufficient energy during the Fast Shut Down.

$$C = I \frac{\Delta t}{\Delta V}$$

The LE910Cx consumes up to 800mA and 30ms is the typical time to perform shutdown and 1V is the minimum voltage margin from the threshold of LE910Cx hardware reset. Based on the formula, more than 24mF is needed for the Fast Shut Down.

But the Ctank value should be optimized depending on the detection voltage and load current LE910Cx consumes in the customer's system.

Note: Make the same plot during system verification to check timing and voltage levels.

Not Subject to NDA

Warning: C_{tank} associated with low ESR requires current limiting feature in the DCDC converter to avoid inrush current side effects.

5.5.2. Fast Shut Down by Software

The Fast Power Down can be triggered directly by the AT command.

Not Subject to NDA

6. POWER SUPPLY

The power supply circuitry and board layout are very important parts of the full product design, with a critical impact on the overall performance of the product. Please read the following requirements and guidelines carefully to ensure a good and proper design.

6.1. Power Supply Requirements

The LE910Cx power requirements are as follows:

Power Supply	Value
Nominal supply voltage	3.8V
Supply voltage range	3.4V – 4.2V
Max ripple on module input supply	30 mV

Table19:PowerSupplyRequirements

Note: For PTCRB approval on the final products, the power supply is required to be within the range of the "Normal Supply voltage ranger".

6.2. Power Consumption

Table 20 provides typical current consumption values of LE910Cx for the various available modes.

Mode		Average (Typ.)	Mode Description
Switched Off			
Switched off		10µA	Module supplied but switched Off (RTC On)
Idle Mode (Standby Mode; No Call in Progress)			
AT+CFUN=1		15.0 mA	Module full functionality with power saving disabled
AT+CFUN=4		14.0 mA	Tx and Rx disabled; module is not registered on the network (Flight mode)
Multi Variant			
DRX AT+CFUN=5	GSM	2.2 mA	DRx2
		1.6 mA	DRx5
	WCDMA	1.6 mA	DRx7
		1.4 mA	DRx8
	LTE	1.9mA	Paging cycle #128 frames (1.28 sec DRx cycle)

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Mode		Average (Typ.)	Mode Description
		1.6mA	Paging cycle #256 frames (2.56 sec DRx cycle)
Single Variant / ThreadX			
DRX AT+CFUN=5	LTE	1.7mA	Paging cycle #128 frames (1.28 sec DRx cycle)
		1.4mA	Paging cycle #256 frames (2.56 sec DRx cycle)
Operative Mode (LTE)			
LTE (max power)		860mA	LTE CAT 1/CAT 4 channel BW 10 MHz, RB=12, Tx = Max power
		890mA	LTE CAT 1/CAT 4 channel BW 20 MHz, RB=Full RB, Tx = Max power With FTP TpT session LTE to USB 10Mbps DL/5Mbps UL (CAT 1) 150Mbps DL/50Mbps UL (CAT 4)
LTE (0dBm)		270mA	LTE CAT 1/CAT 4 channel BW 10 MHz, RB=12, Tx = 0 dBm
		300mA	LTE CAT 1/CAT 4 channel BW 20 MHz, RB=Full RB, Tx = 0 dBm With FTP TpT session LTE to USB 10Mbps DL/5Mbps UL (CAT 1) 150Mbps DL/50Mbps UL (CAT 4)
Operative Mode (WCDMA)			
WCDMA Voice		330mA	WCDMA voice call (Tx = 10 dBm)
WCDMA HSDPA (0 dBm)		220mA	WCDMA data call (Cat 14, Tx = 0 dBm, Max throughput)
WCDMA HSDPA (22 dBm)		640mA	WCDMA data call (Cat 14, Tx = 22 dBm, Max throughput)
Operative Mode (GSM)			
GSM Tx and Rx mode			
GSM900 PL5		330 mA	GSM voice call
DCS1800 PL0		220mA	
GPRS 2 Tx + 1 Rx			
GSM 900 PL5		510mA	GPRS Sending Data mode (CS-4)
DCS 1800 PL0		340mA	
Operative Mode (GPS/GNSS)			
GPS/GNSS tracking		40mA	LTE connection is idle
PSM Mode			
AT+CPSMS=1		10uA	No current source or sink by any connected pin

Table 20: LE910Cx Current Consumption

* Worst/best case current values depend on the network configuration, not under module control.

Not Subject to NDA

* The above currents in idle are measured when Status LED, which is controlled by AT#SLED, is turned off. See the AT Command User Guide for details about the AT#SLED section.

Note: The current consumption of CFUN=0 mode could be 300uA higher than CFUN=5 mode to support the wake-up by RTS pin. For more details, please see the AT Command User Guide of AT+CFUN section.

Note: Regarding the eDRX mode, please refer to 80502NT11758A, LE910C1/LE910C4 PSM Application Note.

Note: The electrical design for the power supply must ensure a peak current output of at least 2.0A.

Note: In GSM/GPRS mode, the RF transmission is not continuous, but is packed into bursts at a base frequency of approximately 216 Hz with relative current peaks up to about 2.0A. Therefore, the power supply must be designed to withstand these current peaks without large voltage drops. This means that both the electrical design and the board layout must be designed for this current flow.

If the PCB layout is not well designed, a strong noise floor is generated on the ground. This will be reflected on all audio paths producing an annoying audible noise at 216 Hz.

If the voltage drops during the peaks, the current absorption is too high. The device may even shut down as a consequence of the supply voltage drop.

6.3. General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- Electrical design
- Thermal design
- PCB layout

Not Subject to NDA

6.3.1. Electrical Design Guidelines

The electrical design of the power supply strongly depends on the power source where this power is drained. Power sources can be divided into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

6.3.1.1. + 5V Input Source Power Supply – Design Guidelines

- The desired output for the power supply is 3.8V. So, the difference between the input source and the desired output is not great and therefore a linear regulator can be used. A switching power supply is preferred to reduce power consumption.
- When using a linear regulator, a proper heat sink must be provided to dissipate the generated power.
- A bypass low ESR capacitor of adequate capacity must be provided to cut the current absorption peaks near the LE910Cx module. A 100 µF tantalum capacitor is usually suitable on both VBATT and VBATT_PA power lines.
- Make sure that the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode must be placed near the power input to protect the LE910Cx module from power polarity inversion.

Figure 14 shows an example of a linear regulator with 5V input.

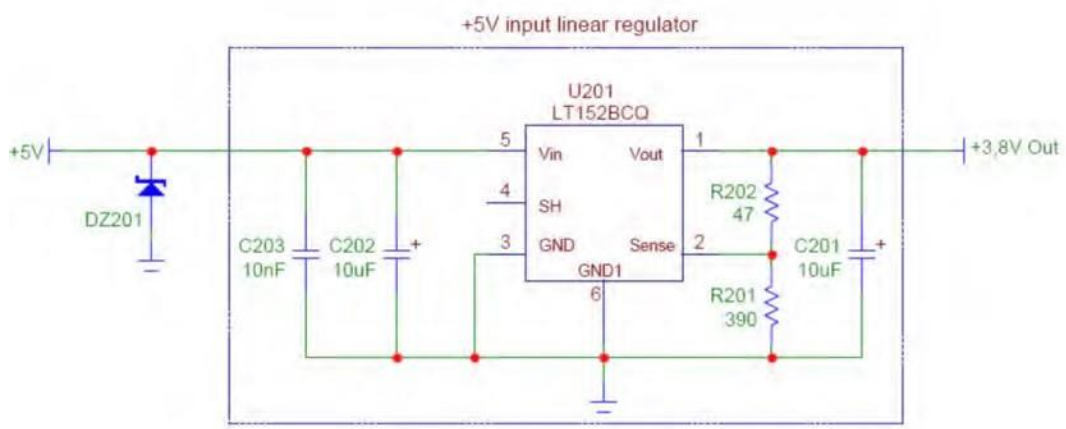


Figure 14: Example of Linear Regulator with 5V Input

Not Subject to NDA

6.3.1.2. + 12V Input Source Power Supply – Design Guidelines

- The desired output for the power supply is 3.8V. Due to the huge difference between the input source and the desired output, a linear regulator is unsuitable and must not be used. A switching power supply is preferable for its better efficiency, especially with the 2A peak current load expected during GSM Tx.
- When using a switching regulator, a 500-kHz or higher switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case, the selection of the frequency and switching design is related to the application to be developed as the switching frequency can also generate EMC interference.
- For car batteries (lead-acid accumulators) the input voltage can rise up to 15.8V. This must be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A bypass low ESR capacitor of adequate capacity must be provided to cut the current absorption peaks. A 100µF tantalum capacitor is usually suitable on VBATT & VBATT_PA power lines.
- Make sure that the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- For automotive applications, a spike protection diode must be inserted close to the power input to clean the supply of spikes.
- A protection diode must be inserted close to the power input to protect the LE910Cx module from power polarity inversion. This can be the same diode as for spike protection.

Figure 13 and Figure 14 show an example of switching regulator with 12V input.

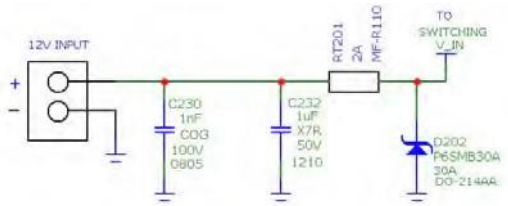


Figure 15: Example of Switching Regulator with 12V Input – Part 1

Not Subject to NDA

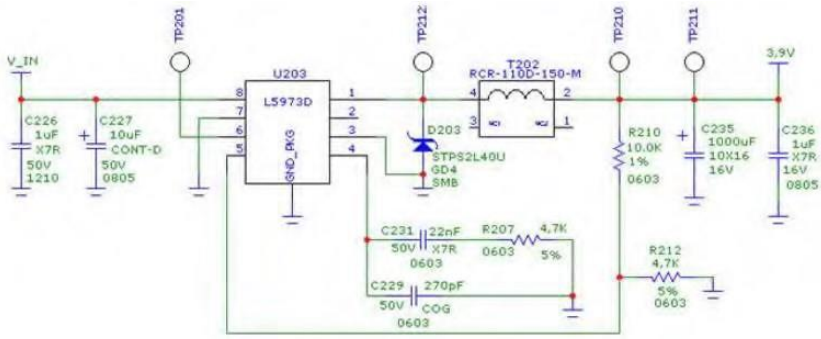


Figure 16: Example of Switching Regulator with 12V Input – Part 2

6.3.1.3. Battery Source Power Supply – Design Guidelines

- The desired nominal output for the power supply is 3.8V, and the maximum voltage allowed is 4.2V. Hence, a single 3.7V Li-Ion cell battery type is suitable for supplying the power to the LE910Cx module.

Note: Do not use any Ni-Cd, Ni-MH, and Pb battery types directly connected to the LE910Cx module. Their use can lead to overvoltage on the LE910Cx and damage it. Use only Li-Ion battery types.

- A bypass low ESR capacitor of adequate capacity must be provided to cut the current absorption peaks; a 100µF tantalum capacitor is usually suitable.
- Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input to protect the LE910Cx module from power polarity inversion. Otherwise, the battery connector should be done in a way to avoid polarity inversions when connecting the battery.
- The battery capacity must be at least 500 mAh to withstand the current peaks of 2A.

6.3.2. Thermal Design Guidelines

The thermal design for the power supply heat sink must be done with the following specifications:

- Average current consumption during RF transmission @PWR level max in LE910Cx as shown in Table 20: LE910Cx Current Consumption
- Average current consumption during Class10 GPRS transmission @PWR level max as shown in Table 20: LE910Cx Current Consumption

Not Subject to NDA

- Average GPS current consumption during GPS tracking (LTE @ idle): mA (40mA).

Note: The average consumption during transmission depends on the power level at which the device is requested to transmit via the network. Therefore, the average current consumption varies significantly.

Note: The thermal design for the power supply must be made keeping an average consumption at the max transmitting level during calls of (LTE/HSPA)/GPRS plus average consumption in GPS Tracking mode.

Considering the very low current during Idle, especially if the Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs significant current only during an Active Call or Data session.

For the heat generated by the LE910Cx module, consider it to be 2W max during transmission at Class10 GPRS upload.

In LTE/WCDMA/HSPA mode, the LE910Cx emits RF signals continuously during transmission. Therefore, special attention must be paid to how to dissipate the heat generated.

The LE910Cx is designed to conduct heat flow from the module IC's towards the bottom of the PCB across GND metal layers

The generated heat is mainly conducted to the ground plane under the LE910Cx module. The application board should be properly designed to dissipate this heat.

Application board design must ensure that the area under the LE910Cx module is as large as possible. Make sure that the LE910Cx is mounted to the large ground area of the application board and provide plenty of ground vias to dissipate heat.

Although the peak current consumption in GSM mode is higher than in LTE/WCDMA/HSPA, considerations for the heat sink are more important in the case of WCDMA due to the continuous transmission conditions.

Not Subject to NDA

6.3.3. Power Supply PCB Layout Guidelines

As seen on the guidelines for electrical design, the power supply shall have a low ESR capacitor on the output to cut the current peaks and a protection diode on the input to protect the supply from spikes and polarity inversion. The placement of these components is crucial for the correct operation of the circuitry. A misplaced component can be useless or can even decrease the power supply performances.

- The bypass low ESR capacitor must be placed close to the LE910Cx power input pads or, if the power supply is of a switching type, it can be placed close to the inductor to cut the ripple, provided the PCB trace from the capacitor to LE910Cx is wide enough to ensure a drop-less connection even during the 2A current peaks.
- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure that no voltage drops occur during the 2A current peaks.
- Note that this is not done in order to avoid RF power loss but to avoid voltage drops on the power line at the current peaks frequency of 216 Hz that will reflect on all the components connected to this supply (also introducing the noise floor at the burst base frequency)
- For this reason, while a voltage drop of 300-400 mV may be acceptable from the RF power loss point of view, the same voltage drop may not be acceptable from the noise point of view. If the application does not have an audio interface but only uses the data feature of the LE910Cx, this noise is not so disturbing, and the power supply layout design can be more forgiving.
- The PCB traces to LE910Cx and the bypass capacitor must be wide enough to ensure that no significant voltage drops occur when the 2A current peaks are absorbed. This is needed for the same above-mentioned reasons. Try to keep these traces as short as possible.
- The PCB traces connecting the switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode very close to the power switching IC (only for the switching power supply). This is done to reduce the radiated field (noise) at the switching frequency (usually 100500 kHz).
- Use a good common ground plane.
- Place the power supply on the board to ensure that the high current return paths in the ground plane do not overlap any noise sensitive circuitry, such as the microphone amplifier/buffer or earphone amplifier.

Not Subject to NDA

- The power supply input cables must be kept separate from noise sensitive lines, such as microphone/earphone cables.

Not Subject to NDA

7. ANTENNA(S)

Antenna connection and board layout design are the most important parts in the full product design, and they have a strong influence on the overall performance of the product. Read carefully and follow the requirements and guidelines for a good and proper design.

7.1. GSM/WCDMA/TD-SCDMA/LTE Antenna Requirements

The antenna for the LE910Cx device must meet the following requirements:

Item	Value
Frequency range	The customer must use the most suitable antenna bandwidth to cover the frequency bands provided by the network operator and supported by the OEM while using the EXFO module. The bands supported by each variant of the LE910Cx module family are provided in Section 2.6.1, RF Bands per Regional Variant.
Gain	Gain < 3 dBi
Impedance	50 Ohm
Input power	> 33 dBm(2 W) peak power in GSM > 24 dBm average power in WCDMA & LTE
VSWR absolute max	<= 10:1 (limit to avoid permanent damage)
VSWR recommended	<= 2:1 (limit to fulfill all regulatory requirements)

Table 21: Primary Antenna Requirements

Since there is no antenna connector on the LE910Cx module, the antenna must be connected to the LE910Cx antenna pad (AD1) by a transmission line implemented on the PCB.

If the antenna is not directly connected to the antenna pad of the LE910Cx, a PCB line is required to connect to it or to its connector.

This transmission line must meet the following requirements:

Item	Value
Characteristic impedance	50 Ohm
Max attenuation	0.3 dB
Avoid coupling with other signals.	
Cold End (Ground Plane) of the antenna must be equipotential to the LE910Cx ground pads.	

Table 22: Antenna Line on PCB Requirements

Not Subject to NDA

Furthermore, if the device is developed for the US and/or Canadian market, it must comply with FCC and/or IC approval requirements:

This equipment complies with FCC and ISED RSS-102 radiation exposure limits set forth for an uncontrolled environment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. In order to avoid the possibility of exceeding the FCC and ISED RSS-102 radio frequency exposure limits, this equipment should be installed and operated with minimum distance 20 cm (7.9 inches) between the antenna and your body during normal operation. Users must follow the specific operating instructions for satisfying RF exposure compliance.
Cet équipement est conforme aux limites d'exposition aux rayonnements FCC et ISED CNR-102 établies pour un environnement non contrôlé. Cet émetteur ne doit pas être installé ou utilisé en conjonction avec une autre antenne ou un autre émetteur. Afin d'éviter la possibilité de dépasser les limites d'exposition aux radiofréquences FCC et ISED, cet équipement doit être installé et utilisé avec une distance minimale de 20 cm (7.9 pouces) entre l'antenne et votre corps pendant le fonctionnement normal. Les utilisateurs doivent suivre les instructions spécifiques d'utilisation pour respecter la conformité à l'exposition aux RF.

7.2. GSM/WCDMA/TD-SCDMA/LTE Antenna – PCB Line Guidelines

- Make sure that the transmission line's characteristic impedance is 50 Ohm.
- Keep the line on the PCB as short as possible since the antenna line loss should be less than around 0.3 dB.
- Line geometry should have uniform characteristics, constant cross sections, and avoid meanders and abrupt curves.
- Any suitable geometry/structure can be used to implement the printed transmission line affecting the antenna.
- If a ground plane is required in the line geometry, this plane must be continuous and sufficiently extended so the geometry can be as similar as possible to the related canonical model.
- Keep, if possible, at least one layer of the PCB used only for the Ground plane. If possible, use this layer as reference Ground plane for the transmission line.
- Surround the PCB transmission line with ground (on both sides). Avoid that other signal tracks face directly the antenna line track.
- Avoid crossing any un-shielded transmission line footprint with other tracks on different layers.
- The ground surrounding the antenna line on the PCB must be strictly connected to the main Ground plane by means of via-holes (once per 2 mm at least) placed close to the ground edges facing the line track.
- Place EM-noisy devices as far as possible from LE910Cx antenna line.
- Keep the antenna line far away from the LE910Cx power supply lines.

Not Subject to NDA

- If EM-noisy devices are present on the PCB hosting the LE910Cx, such as fast switching ICs, take care to shield them with a metal frame cover.
- If EM-noisy devices are not present around the line, geometries like Micro strip or Grounded Coplanar Waveguide are preferred because they typically ensure less attenuation if compared to a Strip line of the same length.

7.3. GSM/WCDMA/LTE Antenna – Installation Guidelines

- Install the antenna in a location with access to the network radio signal.
- The antenna must not be installed inside metal cases.
- The antenna must be installed according to the antenna manufacturer's instructions.

7.4. Antenna Diversity Requirements

This product includes an input for a second Rx antenna to improve radio sensitivity. The function is called Antenna Diversity.

Item	Value
Frequency range	The customer must use the most suitable antenna bandwidth to cover the frequency bands provided by the network operator and supported by the OEM while using the EXFO module. The bands supported by each variant of the LE910Cx module family are provided in Section 2.6.1, RF Bands per Regional Variant
Impedance	50Ω
VSWR recommended	≤ 2:1 (limit to fulfill all regulatory requirements)

Table 23: Antenna Diversity Requirements

Since there is no antenna connector on the LE910Cx module, the antenna must be connected to the LE910Cx antenna pad by means of a transmission line implemented on the PCB.

If the antenna is not connected directly to the LE910Cx (F1) antenna pad, a PCB line is required to connect to it or to its connector.

The second Rx antenna must not be placed in the immediate vicinity of the main antenna. To improve diversity gain and isolation and to reduce mutual interaction, the two antennas should be placed at the as far apart as possible, taking into consideration the available space within the application.

Not Subject to NDA

Note: If Rx Diversity is not used/connected, perfectly disable the Diversity functionality using the AT#RXDIV command (refer to Ref 1: LE910Cx AT Command User Guide) and connect the Diversity pad F1 to a 50 Ohm termination or floating

7.5. GNSS Antenna Requirements

LE910Cx supports an active antenna.

It is recommended to use antennas as follow:

- An external active antenna (17dB typ. Gain, GPS only)
- An external active antenna plus GNSS pre-filter (17dB typ. Gain)

Note: 80502ST10950A_LE910Cx AT_Commands_Reference_Guide document must be referred to install passive or active GNSS ANT configuration by customer.

Note: If the GNSS is not used/connected, please disable the GNSS functionality perfectly using the AT$GPSP command (refer to Ref 1: LE910Cx AT Command User Guide) and connect the GNSS pad R9 to a 50 Ohm termination or floating.

Note: The external GNSS pre-filter is required for the GLONASS application. The GNSS pre-filter must meet the following requirements:

Source and load impedance = 50 Ohm
Insertion loss (1575.42–1576.42 MHz) = 1.4 dB (Max)
Insertion loss (1565.42–1585.42 MHz) = 2.0 dB (Max)

Insertion loss (1597.5515–1605.886 MHz) = 2.0 dB (Max)

Note: It is recommended to add a DC block to the customer's GPS application to prevent damage to the LE910Cx module due to unwanted DC voltage.

Not Subject to NDA

Note: It is recommended to add PI matching network near the GPS connector on the application board in case that RF matching is needed.

7.5.1. Combined GNSS Antenna

The use of a combined RF/GNSS antenna is NOT recommended. This solution can generate extremely poor GNSS reception. Furthermore, the combination of antennas requires an additional diplexer, which adds significant power loss in the RF path.

7.5.2. Linear and Patch GNSS Antenna

The use of this type of antenna introduces a loss of at least 3 dB compared to a circularly polarized (CP) antenna. Having a spherical gain response instead of a hemispherical gain response can aggravate multipath behaviour and create poor position accuracy.

7.5.3. Front End Design Considerations

Since there is no antenna connector on the LE910Cx module, the antenna must be connected to the LE910Cx through the PCB to the antenna pad.

If the antenna is not directly connected at the antenna pad of the LE910Cx, a PCB line is required.

This line of transmission must meet the following requirements:

Item	Value
Characteristic impedance	50 Ohm
Max attenuation	0.3 dB
Avoid coupling with other signals.	
Cold End (Ground Plane) of the antenna must be equipotential to the LE910Cx ground pads.	

Table 24: Antenna Line on PCB Requirements

Furthermore, if the device is developed for the US and/or Canada market, it must comply with the FCC and/or IC requirements.

This device is to be used only for mobile and fixed application.

Not Subject to NDA

7.5.4. GNSS Antenna – PCB Line Guidelines

- Ensure that the antenna line impedance is 50 Ohm.
- Keep the line on the PCB as short as possible to reduce the loss.
- The antenna line must have uniform characteristics, constant cross section, avoiding meanders and abrupt curves.
- Keep one layer of the PCB used only for the Ground plane; if possible.
- Surround (on the sides, top and bottom) the antenna line on the PCB with Ground. Avoid having other signal tracks directly facing the antenna line track.
- The Ground around the antenna line on the PCB must be strictly connected to the main Ground plane by placing vias at least once per 2mm.
- Place EM-noisy devices as far away from the LE910Cx antenna line as possible.
- Keep the antenna line far away from the LE910Cx power supply lines.
- If there are EM-noisy devices, such as fast switching ICs, around the PCB hosting the LE910Cx, ensure shielding the antenna line by burying it inside the layers of PCB and surrounding it with Ground planes; or shield it with a metal frame cover.
- If you do not have EM-noisy devices around the PCB of LE910Cx, use a Micro strip line on the surface copper layer for the antenna line. The line attenuation will be lower than a buried one.

7.5.5. GNSS Antenna – Installation Guidelines

- The LE910Cx, due to its sensitivity characteristics, is able to perform a fix inside buildings. (In any case, the sensitivity could be affected by the characteristics of the building, that is shielding.)
- The antenna must not be co-located or operating in conjunction with any other antennas or transmitters.
- The antenna must not be installed inside metal cases.
- The antenna must be installed according to the antenna manufacturer's instructions.

Not Subject to NDA

8. HARDWARE INTERFACES

Table 25 summarizes all the hardware interfaces of the LE910Cx module.

Interface	LE910Cx
SGMII	For Ethernet support
HSIC	x1 (Optional)
SD/MMC	x1 dual voltage interface for supporting SD/MMC card
SDIO	For WIFI support (1.8V only)
USB	USB2.0, OTG support on LE910C1-LA, LE910C4-LA and LE910C4-CN
SPI	Master only, up to 50 MHz
I2C	For sensors, audio control
UART	2 HS-UART (up to 4 Mbps)
Audio I/F	I2S/PCM, Analog I/O
GPIO	10 ~ 27 (10 dedicated + 17 multiplexed with other signals)
USIM	x2, dual voltage each (1.8V/2.85V)
ADC	Up to x3
Antenna ports	2 for Cellular, 1 for GNSS

Table 25: LE910Cx Hardware Interfaces

8.1. USB Port

The LE910Cx module includes a Universal Serial Bus (USB) transceiver, which operates at USB high-speed (480Mbits/sec). It can also operate with USB full-speed hosts (12Mbits/sec).

It is compliant with the USB 2.0 specification and can be used for control and data transfer as well as for diagnostic monitoring and firmware update.

The USB port is typically the main interface between the LE910Cx module and OEM hardware.

Note: The USB_D+ and USB_D- signals have a clock rate of 480 MHz. The signal traces must be routed carefully. Minimize trace lengths, number of vias, and capacitive loading. The impedance value should be as close as possible to 90 Ohms differential.

Not Subject to NDA

Table 26 lists the USB interface signals.

Signal	Pad No.	Usage
USB_VBUS	A13	Power and cable detection for the internal USB transceiver. Acceptable input voltage range 2.5V – 5.5V @ max 5 mA consumption
USB_D-	C15	Minus (-) line of the differential, bidirectional USB signal to/from the peripheral device
USB_D+	B15	Plus (+) line of the differential, bidirectional USB signal to/from the peripheral device
USB_ID	A14	Used for USB OTG to determine host or client mode

Table 26: USB Interface Signals

Note: USB_VBUS input power is used internally to detect the USB port and start the enumeration process.

It is a power supply pin with a maximum consumption of 5 mA.

Do not use pull up or a voltage divider for sourcing this supply

Note: Even if USB communication is not used, it is still highly recommended to place an optional USB connector on the application board.

At least USB signal test points are required as USB physical communication is needed in the case of SW update.

Note: USB OTG feature is supported by default.

If the USB_ID pin asserted to ‘low’, USB OTG is enabled.
Please note that LE910Cx doesn’t supply 5V power to OTG devices therefore an external 5V power is required on an application board to provide 5V power to OTG devices.

Not Subject to NDA

8.2. HSIC Interface (Optional)

The application processor exposes a High-Speed Inter-Chip (HSIC). HSIC eliminates the analog transceiver from a USB interface for lower voltage operation and reduced power dissipation.

Further details will be provided in a future release of this document.

8.3. SGMII Interface

The SOC includes an integrated Ethernet MAC with an SGMII interface, with the following key features:

- This interface can be directly connected to external Ethernet devices which use SGMII interface.
- When enabled, an additional network interface will be available to the Linux kernel.
- Further details can be found at Ref 8: ETH_Expansion_board_Application Note

8.3.1. Ethernet Control interface

When using an external PHY for Ethernet connectivity, the LE910Cx also includes the control interface for managing the external PHY

Table 27 lists the signals for controlling the external PHY

PAD	Signal	I/O	Function	Type	Comment
C2	MAC_MDC	O	MAC to PHY Clock	2.85V	Logic Level Specifications are shown in Section 0, Table 16: Operating Range – For SD Card Pads Operating at 2.95V SIM Card Pads @2.95V, Table 17
C1	MAC_MDIO	I/O	MAC to PHY Data	2.85V	
D1	ETH_RST_N	O	Reset to Ethernet PHY	2.85V	
G4	ETH_INT_N	I	Interrupt from Ethernet PHY	1.8V	Logic Level Specifications are shown in Table 12

Table27:EthernetControlInterfaceSignals

Note: The Ethernet control interface is shared with USIM2 port!

When Ethernet PHY is used, USIM2 port cannot be used (and vice versa).

Not Subject to NDA

Note: ETH_INT_N is a 1.8V input. It has an internal pull up to 1.8V inside the module thus it should be connected to an open drain interrupt pin of the Ethernet PHY. In case the PHY does not support 1.8V I/O, proper level shifter needs to be used.

8.4. Serial Ports

The serial port is typically a secondary interface between the LE910Cx module and OEM hardware. The following serial ports are available on the module:

- Modem Serial Port 1 (Main)
- Modem Serial Port 2 (Auxiliary)

Several serial port configurations can be designed for the OEM hardware. The most common are:

- RS232 PC com port
- Microcontroller UART @ 1.8V (Universal Asynchronous Receive Transmit)
- Microcontroller UART @ 3.3V/5V or other voltages different from 1.8V

Depending on the type of serial port on the OEM hardware, level translator circuits may be required to operate the system. The only configuration that does not need level translation is the 1.8V UART.

The LE910Cx UART has CMOS levels as described in Section 4.3, Logic Level Specifications.

8.4.1. Modem Serial Port 1 Signals

On the LE910Cx, Serial Port 1 is a +1.8V UART with 7 RS232 signals. It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels. Table 28 lists the signals of LE910Cx Serial Port 1.

RS232 Pin#	Signal	Pad No.	Name	Usage
1	DCD - DCD_UART	N14	Data Carrier Detect	Output from LE910Cx that indicates carrier presence
2	RXD - TX_UART	M15	Transmit line *see Note	Output transmit line of LE910Cx UART

Not Subject to NDA

RS232 Pin#	Signal	Pad No.	Name	Usage
3	TXD -RX_UART	N15	Receive line *see Note	Input receive line of LE910Cx UART
4	DTR - DTR_UART	M14	Data Terminal Ready	Input to LE910Cx that controls the DTE READY condition
5	GND	A2, B13, D4…	Ground	Ground
6	DSR - DSR_UART	P14	Data Set Ready	Output from LE910Cx that indicates that the module is ready
7	RTS - RTS_UART	L14	Request to Send	Input to LE910Cx controlling the Hardware flow control
8	CTS - CTS_UART	P15	Clear to Send	Output from LE910Cx controlling the Hardware flow control
9	RI - RI_UART	R14	Ring Indicator	Output from LE910Cx indicating the Incoming call condition

Table28:ModemSerialPort1Signals

Note: DCD, DTR, DSR, RI signals that are not used for UART functions can be configured as GPIO using AT commands.

Note: To avoid a back-powering effect, it is recommended to prevent any HIGH logic level signal from being applied to the module's digital pins when it is powered OFF or during an ON/OFF transition.

Note: For minimum implementations, only the TXD and RXD lines need be connected. The other lines can be left open provided a software flow control is implemented.

Not Subject to NDA

Note: According to V.24, Rx/Tx signal names refer to the application side; therefore, on the LE910Cx side, these signal are in the opposite direction: TXD on the application side will be connected to the receive line (here named TXD/ RX_UART) of the LE910Cx serial port and vice versa for Rx.

Note: The DTR pin is used to control the UART and system sleep

Pulling the DTR pin down prevents the UART and the entire module from entering low power mode.

DTR can be left floating if not used (DTR is internally pulled high).

8.4.2. Modem Serial Port 2

On the LE910Cx, Serial Port 2 is a +1.8V UART with Rx and Tx signals only.

The UART functionality is shared with SPI, thus simultaneous use of SPI and UART is not supported.

Table 29 lists the signals of the LE910Cx Serial Port 2.

PAD	Signal	I/O	Function	Type	Comment
D15	TXD_AUX	O	Auxiliary UART (Tx Data to DTE)	1.8V	Shared with SPI_MOSI
E15	RXD_AUX	I	Auxiliary UART (Rx Data to DTE)	1.8V	Shared with SPI_MISO

Table 29: Modem Serial Port 2 Signals

Note: To avoid a back-powering effect, it is recommended to prevent any HIGH logic level signal from being applied to the module's digital pins when it is powered OFF or during an ON/OFF transition.

Note: The Auxiliary UART is used as the SW main debug console. It is required to place test points on this interface even if not used.

Not Subject to NDA

8.4.3. RS232 Level Translation

To interface the LE910Cx with a PC COM port or an RS232 (EIA/TIA-232) application, a level translator is required. This level translator must perform the following actions:

- Invert the electrical signal in both directions
- Change the level from 0/1.8V to +15/-15V

The RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required.

The easiest way to translate the levels and invert the signal is by using a single chip-level translator. There are a multitude of them, differing in the number of drivers and receivers and in the levels (make sure to get a true RS232 level translator, not a RS485 or other standards).

By convention, the driver is the level translator from the 0-1.8V UART to the RS232 level. The receiver is the translator from the RS232 level to 0-1.8V UART. To translate the whole set of control lines of the UART, the following is required:

- 2 drivers
- 2 receivers

Warning: The digital input lines, operating at 1.8V CMOS levels, have an absolute maximum input voltage of 2.0V. The level translator IC outputs on the module side (i.e. LE910Cx inputs) will cause damage to the module inputs if the level translator is powered with +3.8V power.

So, the level translator IC must be powered by a dedicated +1.8V power supply.

As an example, RS232 level adaption circuitry could use a MAXIM transceiver (MAX218).

In this case, the chipset is capable of translating directly from 1.8V to the RS232 levels (example on 4 signals only).

Not Subject to NDA

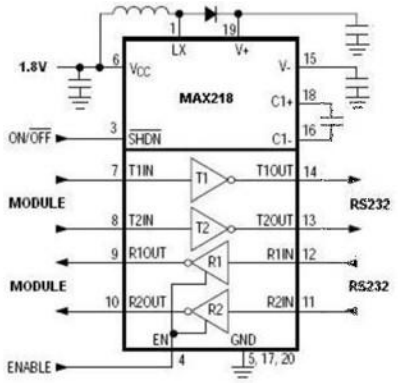


Figure 17: RS232 Level Adaption Circuitry Example

Note: In this case, the length of the lines on the application must be taken into account to avoid problems in the case of high-speed rates on RS232.

The RS232 serial port lines are usually connected to a DB9 connector as shown in Figure 18. Signal names and directions are named and defined from the DTE point of view.

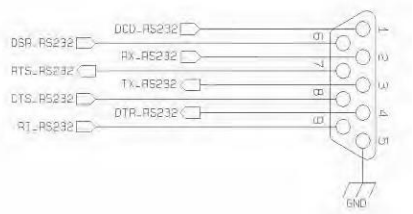


Figure 18: RS232 Serial Port Lines Connection Layout

8.5. Peripheral Ports

In addition to the LE910Cx serial ports, the LE910Cx supports the following peripheral ports:

- SPI – Serial Peripheral Interface
- I2C - Inter-integrated circuit
- SD/MMC Card Interface
- SDIO Interface

8.5.1. SPI – Serial Peripheral Interface

The LE910Cx SPI supports the following:

- Master Mode only

Not Subject to NDA

- 1.8V CMOS level
- Up to 50 MHz clock rate

Note: The LE910Cx module supports Master mode only and cannot be configured as Slave mode.

PAD	Signal	I/O	Function	Type	Comment
F15	SPI_CLK	O	SPI clock output	1.8V	
E15	SPI_MISO	I	SPI data Master input Slave output	1.8V	Shared with RX_AUX
D15	SPI_MOSI	O	SPI data Master output Slave input	1.8V	Shared with TX_AUX
H14	SPI_CS	O	SPI chip-select output	1.8V	

Table 30: SPI Signals

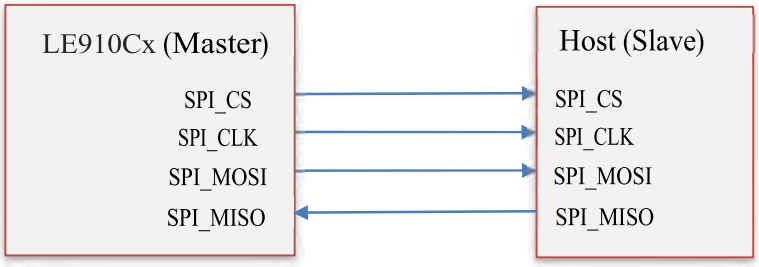


Figure 19: SPI Signal Connectivity

8.5.2. I2C - Inter-integrated Circuit

The LE910Cx supports an I2C interface on the following pins:

- B11 - I2C_SCL
- B10 - I2C_SDA

The I2C can also be used externally by the end customer application.

In addition, SW emulated I2C functionality can be used on GPIO pins 1-10. Any GPIO (among GPIO 1-10) can be configured as SCL or SDA.

LE910Cx only supports I2C Master Mode.

Not Subject to NDA

Note: SW emulated I2C on GPIO lines is only supported from the modem side. For more information, refer to Ref 1: LE910Cx AT Command User Guide for command settings..

Note: To keep backward compatibility with previous LE910 products, it is recommended to keep using the SW emulated I2C available on GPIO's 1-10.

8.5.3. SD/MMC Card Interface

The LE910Cx provides an SD port supporting the SD3.0 specification, which can be used to support standard SD/MMC memory cards with the following features:

- Interface with SD/MMC memory cards up to 32 GB
- Max clock @ 2.95V - 50 MHz SDR
- Max Data: 25 MB/s
- SD standard: HS-SDR25 at 2.95V
- Max clock @ 1.8V - 200 MHz SDR
- Max Data: 100 MB/s
- SD standard: UHS-SDR104 at 1.8 V
- Max clock @ 1.8V - 50 MHz DDR
- Max Data: 50 MB/s
- SD standard: UHS-DDR50 at 1.8 V

Table 31 lists the LE910Cx SD card signals.

PAD	Signal	I/O	Function	Type	Comments
J12	SD/MMC_CMD	O	SD command	1.8/2.95V	
F12	SD/MMC_CLK	O	SD card clock	1.8/2.95V	
E12	SD/MMC_DATA0	I/O	SD Serial Data 0	1.8/2.95V	
G12	SD/MMC_DATA1	I/O	SD Serial Data 1	1.8/2.95V	
K12	SD/MMC_DATA2	I/O	SD Serial Data 2	1.8/2.95V	
H12	SD/MMC_DATA3	I/O	SD Serial Data 3	1.8/2.95V	
G13	SD/MMC_CD	I	SD card detect input	1.8V	Active Low

Not Subject to NDA

PAD	Signal	I/O	Function	Type	Comments
F13	VMMC	-	Power supply for MMC card pull-up resistors	1.8/2.95V	Max Current is 50mA

Table 31: SD Card Signals

Figure 20 shows the recommended connection diagram of the SD interface.

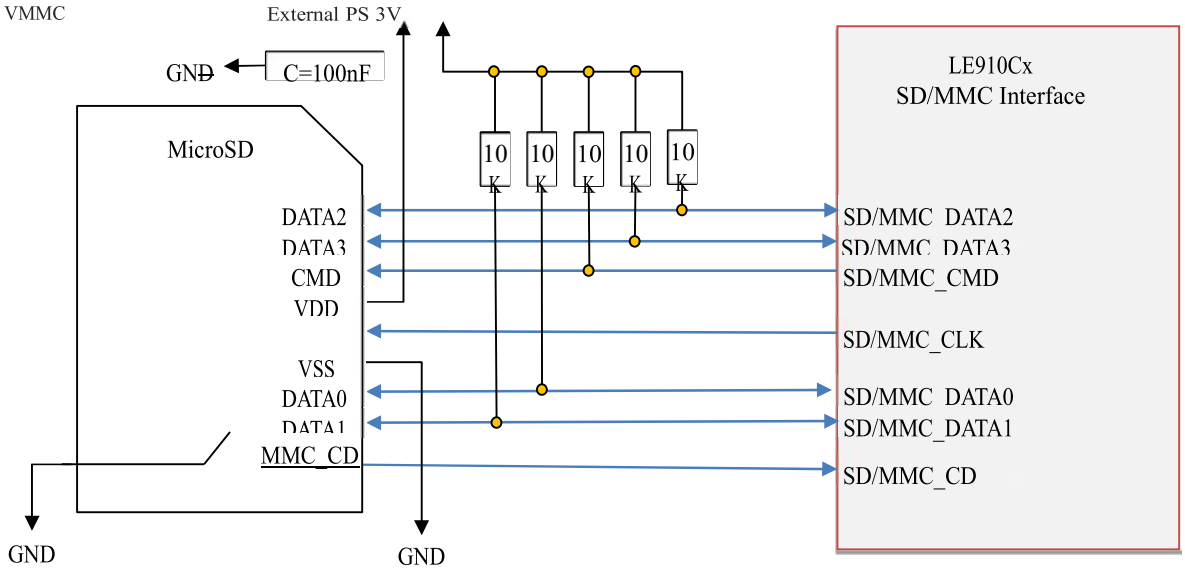


Figure 20: SD/MMC Interface Connectivity

Note: SD/MMC is only supported on the Linux side.

The power supply to the SD/MMC card must be supplied from the Host application board. The LE910Cx does not provide a dedicated power supply for the SD/MMC card.

The VMMC Supply is limited to 50mA so it can only supply the MMC card external pull-up resistors.

The Pull-up resistors must be placed on the host application board.

The card detection input has an internal pull-up resistor.

VMMC can be used to enable the external power supply (LDO Enable signal)

8.5.4. WiFi SDIO Interface

The LE910Cx provides an SDIO port supporting the SDIO3.0 specification, which can be used to interface with a WiFi chipset (Qualcomm QCA65x4 chipset or other WiFi solutions). The LE910Cx module includes an integrated SW driver to support the Qualcomm QCA6574 chipset.

Not Subject to NDA

Note: Qualcomm QCA9377 WiFi chipset may be supported on some of the LE910Cx variants.
Please contact your EXFO representative for more details.

The LE910Cx SDIO port supports the SDIO 3.0 specification at 1.8V CMOS only, so it cannot be used as an external SD/MMC card connection.

The LE910Cx module supports an LTE/WiFi coexistence mechanism via the WCI (Wireless Coexistence Interface) port, which connects between the module and the external WiFi IC.

For a detailed explanation, refer to Ref 5:

EXFO_LE920A4_LE910Cx_WiFi_Interface_Application_Note_r1.

PAD	Signal	I/O	Function	Type	Comments
N13	WIFI_SD_CMD	O	WiFi SD Command	1.8V	
L13	WIFI_SD_CLK	O	WiFi SD Clock	1.8V	200 MHz max.
J13	WIFI_SD_DATA0	I/O	WiFi SD Serial Data 0	1.8V	
M13	WIFI_SD_DATA1	I/O	WiFi SD Serial Data 1	1.8V	
K13	WIFI_SD_DATA2	I/O	WiFi SD Serial Data 2	1.8V	
H13	WIFI_SD_DATA3	I/O	WiFi SD Serial Data 3	1.8V	
L12	WIFI_SDRST	O	WiFi Reset / Power enable control	1.8V	Active Low
M8	WCI_TX	O	Wireless coexistence interface TXD	1.8V	
M9	WCI_RX	I	Wireless coexistence interface RXD	1.8V	

Table 32: WiFi SDIO Interface Signals

8.6. Audio Interface

The LE910Cx module supports a digital audio interface.

8.6.1. Digital Audio

The LE910Cx module can be connected to an external codec through the digital interface.

The product provides Digital Audio Interface (PCM/I2S) on the following pins:

Not Subject to NDA

PAD	Signal	I/O	Function	Type	Comments
B9	DVI_WA0	O	Digital Audio Interface (WA0)	B-PD 1.8V	PCM_SYNC I2S_WS
B6	DVI_RX	I	Digital Audio Interface (RX)	B-PD 1.8V	PCM_DIN I2S_DIN
B7	DVI_TX	O	Digital Audio Interface (TX)	B-PD 1.8V	PCM_DOUT I2S_DOUT
B8	DVI_CLK	O	Digital Audio Interface (CLK)	B-PD 1.8V	PCM_CLK I2S_CLK
B12	REF_CLK	O	Audio Master Clock	B-PD 1.8V	MCLK

Table 33: Digital Audio Interface Signals (PCM/I2S)

LE910Cx DVI has the following characteristics:

PCM

- PCM Master and slave modes using short or long frame sync modes
- 16-bit linear PCM format
- PCM clock rates of 128kHz, 256 kHz, 512 kHz, 1024 kHz and 2048 kHz (Default), 4096kHz
- Frame size of 8, 16, 32, 64, 128 & 256 bits per frame
- Sample rates of 8 kHz and 16 kHz

I2S

- Sample rate 8KHz, 16KHz, 48KHz
- Sample-width is 16bit only.
- Supported I2S standard only - Phillips I2S Bus Specifications revised June 5, 1996

In addition to the DVI port, the LE910Cx module provides a master clock signal (REF_CLK on Pin B12) which can either provide a reference clock to an external codec or form an PCM/I2S interface together with the DVI port where the REF_CLK acts as the MCLK.

The REF_CLK default frequency is 12.288 MHz.

When using the DVI with REF_CLK as PCM/I2S interface, 12.288 MHz is 256 x fs (where fs = 48 kHz)

Not Subject to NDA

8.6.1.1. Short Frame Timing Diagrams

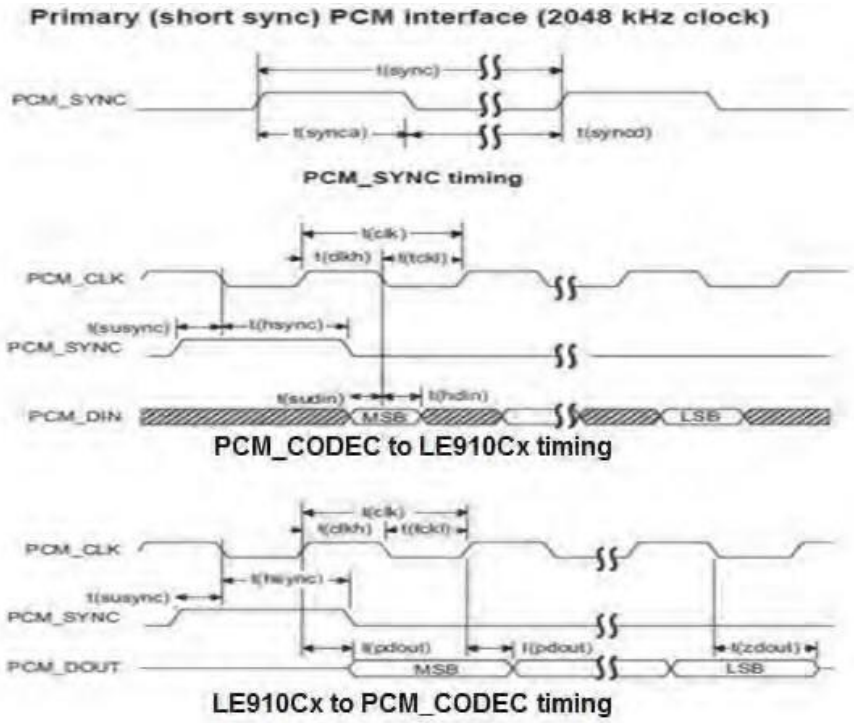


Figure 21: Primary PCM Timing

Parameter		Comments	Min	Typ	Max	Unit
t(sync)	PCM_SYNC cycle time		-	125	-	µs
t(synca)	PCM_SYNC asserted time		-	488	-	ns
t(syncd)	PCM_SYNC de-asserted time		-	124.5	-	µs
t(clk)	PCM_CLK cycle time		-	488	-	ns
t(clkh)	PCM_CLK high time		-	244	-	ns
t(clkl)	PCM_CLK low time		-	244	-	ns
t(sync_offset)	PCM_SYNC offset time to PCM_CLK falling		-	122	-	ns
t(sudin)	PCM_DIN setup time to PCM_CLK falling		60	-	-	ns
t(hdin)	PCM_DIN hold time after PCM_CLK falling		60	-	-	ns
t(pdout)	Delay from PCM_CLK rising to PCM_DOUT valid		-	-	60	ns
t(zdout)	Delay from PCM_CLK falling to PCM_DOUT HIGH-Z		-	-	60	ns

Table 34: PCM_CODEC Timing Parameters

Not Subject to NDA

8.6.1.2. Long Frame Timing Diagrams

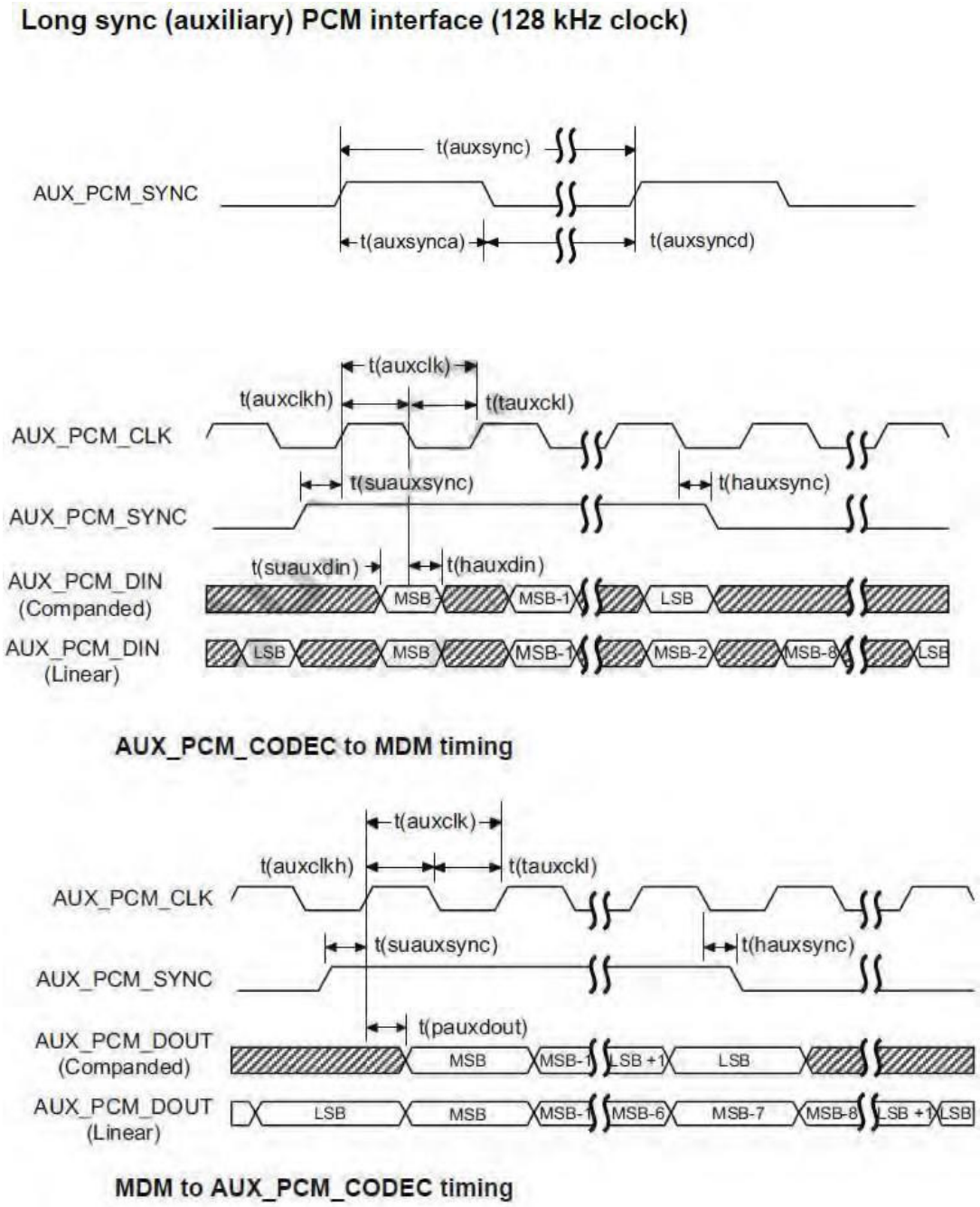


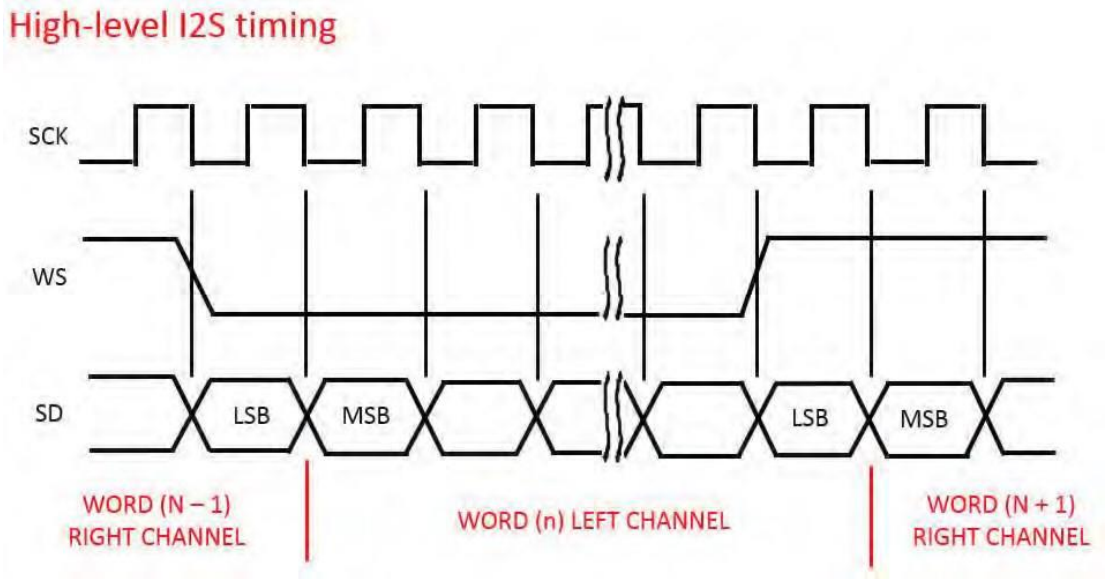
Figure 22: Auxiliary PCM Timing

Not Subject to NDA

Parameter		Comments	Min	Typ	Max	Unit
t(auxsync)	AUX_PCM__SYNC cycle time		-	125	-	µs
t(auxsynca)	AUX_PCM_SYNC asserted time		62.4	62.5	-	µs
t(auxsyncd)	AUX_PCM_SYNC de-asserted time		62.4	62.5	-	µs
t(auxclk)	AUX_PCM_CLK cycle time		-	7.8	-	µs
t(auxclkh)	AUX_PCM_CLK high time		3.8	3.9	-	µs
t(auxclkl)	AUX_PCM_CLK low time		3.8	3.9	-	µs
t(suauxsync)	AUX_PCM_SYNC setup time to AUX_PCM_CLK rising		1.95	-	-	ns
t(hauxsync)	PCM_DIN hold time after AUX_PCM_CLK rising		1.95	-	-	ns
t(suauxdin)	AUX_PCM_DIN setup time to AUX_PCM_CLK falling		70	-	-	ns
t(hauxdin)	AUX_ PCM_DIN hold time after AUX_PCM_CLK falling		20	-	-	ns
t(pauxdout)	Delay from AUX_PCM_CLK to AUX_PCM_DOUT valid		-	-	50	ns

Table 35: AUX_PCM_CODEC Timing Parameters

8.6.1.3. I2S Digital Audio Diagram



Not Subject to NDA

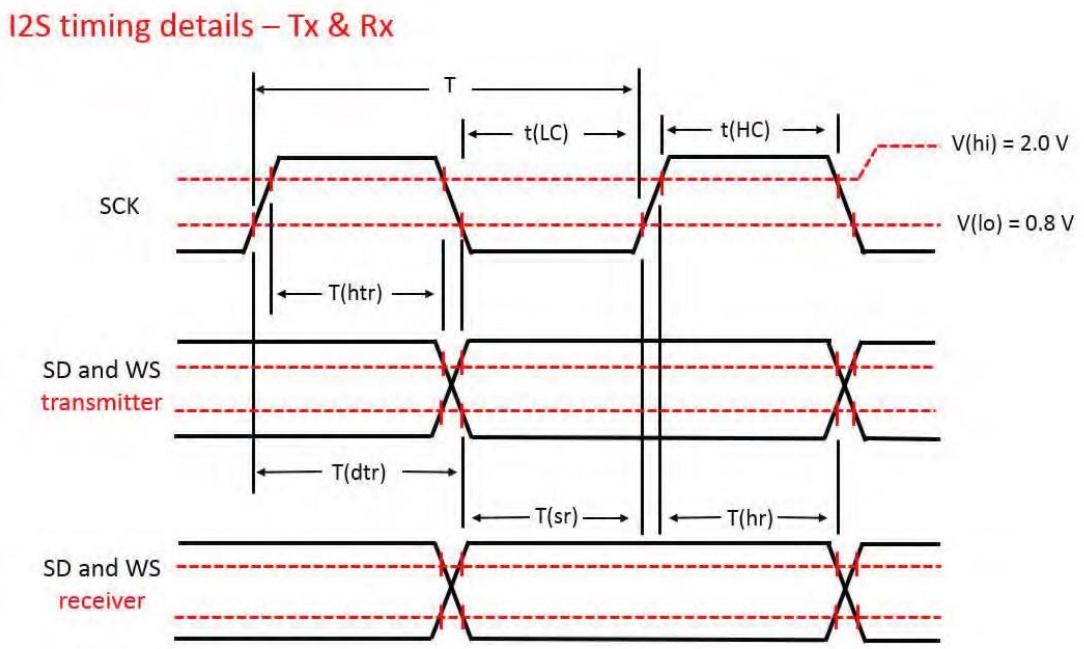


Figure 23: I2S timing diagram

Note LE910Cx family supports both PCM/I2S.

Parameter		Comments	Min	Typ	Max	Unit
Using internal SCK						
	Frequency		-	-	12.288	MHz
T	Clock period		81.380	-	-	ns
t(HC)	Clock high		0.45*T	-	0.55*T	ns
t(LC)	Clock low		0.45*T	-	0.55*T	ns
t(sr)	SD and WS input setup time		16.276	-	-	ns
t(hr)	SD and WS input hold time		0	-	-	ns
t(dtr)	SD and WS output delay		-		65.100	ns
t(htr)	SD and WS output hold time		0	-	-	ns
Using external SCK						
	Frequency		-	-	12.288	MHz
T	Clock period		81.380	-	-	ns
t(HC)	Clock high		0.45*T	-	0.55*T	ns
t(LC)	Clock low		0.45*T	-	0.55*T	ns

Not Subject to NDA

Parameter		Comments	Min	Typ	Max	Unit
t(sr)	SD and WS input setup time		16.276	-	-	ns
t(hr)	SD and WS input hold time		0	-	-	ns
t(dtr)	SD and WS output delay		-		65.100	ns
t(htr)	SD and WS output hold time		0	-	-	ns

Table 36: Interface timing

8.7. General Purpose I/O

The general-purpose I/O pads can be configured to act in three different ways:

- Input
- Output
- Alternative function (internally controlled)

The Input pads can only be read, reporting the digital values (high / low) present on the pad at the time of reading. The Output pads can only be written or queried and set values on the pad output. Pads with alternative function can be internally controlled by the LE910Cx firmware and act according to the implementation.

The following GPIOs are always available as a primary function on the LE910Cx.

PAD	Signal	I/O	Function	Type	Note
C8	GPIO_01	I/O	Configurable GPIO	CMOS 1.8V	*
C9	GPIO_02	I/O	Configurable GPIO	CMOS 1.8V	
C10	GPIO_03	I/O	Configurable GPIO	CMOS 1.8V	
C11	GPIO_04	I/O	Configurable GPIO	CMOS 1.8V	
B14	GPIO_05	I/O	Configurable GPIO	CMOS 1.8V	*
C12	GPIO_06	I/O	Configurable GPIO	CMOS 1.8V	*
C13	GPIO_07	I/O	Configurable GPIO	CMOS 1.8V	*
K15	GPIO_08	I/O	Configurable GPIO	CMOS 1.8V	*
L15	GPIO_09	I/O	Configurable GPIO	CMOS 1.8V	*
G15	GPIO_10	I/O	Configurable GPIO	CMOS 1.8V	

Table 37: Primary GPIOs

Warning: GPIO's marked with (*) must not be pulled high externally (from the carrier board) during module power on procedure. Pulling these pads high during module power up might lead to unwanted/non-operational boot mode.

Not Subject to NDA

The additional GPIOs below can be used in case their initial functionality is not used:

PAD	Signal	I/O	Initial Function	Alternate Function	Type	Note
L12	GPIO_13	I/O	WIFI_SDRST	Configurable GPIO	CMOS 1.8V	*
N13	GPIO_14	I/O	WIFI_SDIO_CMD	Configurable GPIO	CMOS 1.8V	
J13	GPIO_15	I/O	WIFI_SDIO_D0	Configurable GPIO	CMOS 1.8V	
M13	GPIO_16	I/O	WIFI_SDIO_D1	Configurable GPIO	CMOS 1.8V	
K13	GPIO_17	I/O	WIFI_SDIO_D2	Configurable GPIO	CMOS 1.8V	
H13	GPIO_18	I/O	WIFI_SDIO_D3	Configurable GPIO	CMOS 1.8V	
L13	GPIO_19	I/O	WIFI_SDIO_CLK	Configurable GPIO	CMOS 1.8V	
M8	GPIO_24	I/O	WCI_TXD	Configurable GPIO	CMOS 1.8V	*
M9	GPIO_25	I/O	WCI_RXD	Configurable GPIO	CMOS 1.8V	*
R14	GPIO_31	I/O	UART_RI	Configurable GPIO	CMOS 1.8V	
P14	GPIO_32	I/O	UART_DSR	Configurable GPIO	CMOS 1.8V	
N14	GPIO_33	I/O	UART_DCD	Configurable GPIO	CMOS 1.8V	
M14	GPIO_34	I/O	UART_DTR	Configurable GPIO	CMOS 1.8V	
F15	GPIO_35	I/O	SPI_CLK	Configurable GPIO	CMOS 1.8V	
E15	GPIO_36	I/O	SPI_MISO	Configurable GPIO	CMOS 1.8V	
D15	GPIO_37	I/O	SPI_MOSI	Configurable GPIO	CMOS 1.8V	
H14	GPIO_11	I/O	SPI_CS	Configurable GPIO	CMOS 1.8V	

Table 38: Additional GPIOs

Warning: GPIO's marked with (*) should not be pulled high externally (from the carrier board) during module power on procedure. Pulling these pads high during module power up might lead to unwanted/non-operational boot mode.

Note: LE910Cx GPIOs 1~10 can also be used as alternate I2C function. Refer to Section 8.5.2, I2C - Inter-integrated Circuit.

Not Subject to NDA

8.7.1. Using a GPIO Pad as Input

GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided that this device has interface levels compatible with the 1.8V CMOS levels of the GPIO.

If the digital output of the device is connected to the GPIO input, the pad has interface levels other than 1.8V CMOS. It can be buffered with an open collector transistor with a 10 kΩ pull-up resistor to 1.8V.

8.7.2. Using a GPIO Pad as an interrupt / Wakeup source

GPIO pads used as inputs can also be used as an interrupt source for software. In general, all GPIO pads can also be used as an interrupt. However, not all GPIO's can be used as a wakeup source of the module (wakeup from sleep).

Only the following GPIO's can be used for waking up the system from sleep:

- GPIO1
- GPIO4
- GPIO5
- GPIO8

8.7.3. Using a GPIO Pad as Output

The GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output, and therefore the pullup resistor can be omitted.

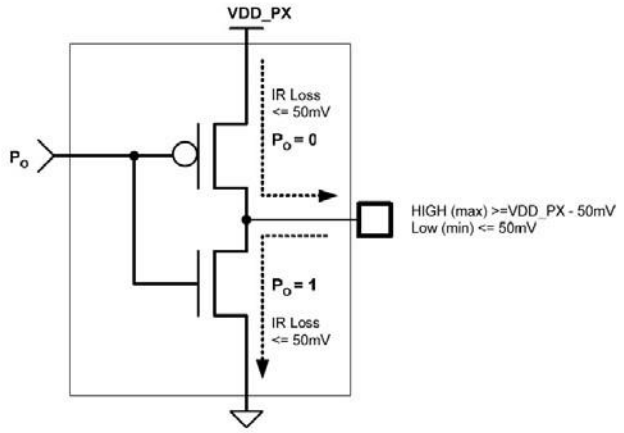


Figure 24: GPIO Output Pad Equivalent Circuit

Not Subject to NDA

9. MISCELLANEOUS FUNCTIONS

9.1. Indication of Network Service Availability

The STAT_LED pin status shows information on the network service availability and call status. In the LE910Cx module, the STAT_LED usually needs an external transistor to drive an external LED.

The STAT_LED does not have a dedicated pin. The STAT_LED functionality is available on GPIO_01 pin (by default GPIO_01 functions as STAT_LED)

See the AT Command User Guide for details about the AT#SLED section.

LED status		Device Status
Permanently off		Device off
Blinking	Blinking 1s on and 2s off	Registered in idle
	Blinking time depends on network condition in order to minimize power consumption	Registered in idle with power saving
Permanently on		Not registered

Table 39: Network Service Availability Indication

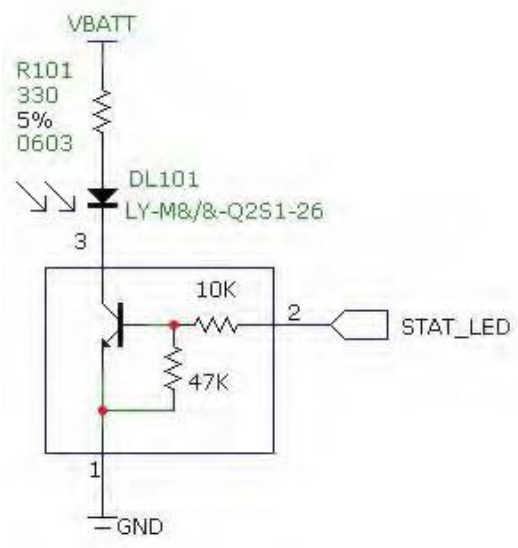


Figure 25: Status LED Circuit Example

Not Subject to NDA

9.2. Indication of Software Ready

The SW_RDY signal provides indication on the module's ability to receive commands. As long as the SW_RDY is asserted low, it indicates that the LE910Cx has not finished booting yet. Once the SW_RDY is asserted high, it indicates that the LE910Cx is ready to receive commands.

The SW_RDY does not have a dedicated pin. The SW_RDY functionality is available on GPIO_08 pin (by default GPIO_08 functions as SW_RDY).

9.3. RTC – Real Time Clock

The RTC within the LE910Cx module does not have a dedicated RTC supply pin. The RTC block is supplied by the VBATT supply.

If the battery is removed, the RTC is not maintained so if it is necessary to maintain an internal RTC , VBATT must be supplied continuously.

In Power OFF mode, the average current consumption is ~25uA.

9.4. VAUX Power Output

A regulated power supply output is provided to supply small devices from the module.

This output is active when the module is ON and turns OFF when the module is shut down. The operating range characteristics of the supply are as follows:

Item	Min	Typical	Max
Output voltage	1.75V	1.80V	1.85V
Output current			100 mA
Output bypass capacitor (within the module)			1 µF

Table 40: Operating Range – VAUX Power Supply

9.5. ADC Converter

9.5.1. Description

The LE910Cx module provides three on-board 8-bit Analog to Digital converters. Each

ADC reads the voltage level applied on the relevant pin, converts it and stores it into an 8-bit word.

Not Subject to NDA

Item	Min	Max	Units
Input voltage range	0.1	1.7	Volt
AD conversion	-	8	bits
Resolution	-	< 6.6	mV

Table 41: ADC Parameters

9.5.2. Using the ADC Converter

An AT command is available to use the ADC function.

The command is AT#ADC=1,2. The read value is expressed in mV.

Refer to Ref 1: LE910Cx AT Command User Guide for the full description of this function.

9.6. Using the Temperature Monitor Function

The Temperature Monitor supports temperature monitoring by providing periodic temperature indications, to perform some functions in extreme conditions. When properly set (see the #TEMPMON command in Ref 1: LE910Cx AT Command User Guide), it raises a GPIO to High Logic level when the maximum temperature is reached.

9.7. GNSS Characteristics

Table 42 specifies the GNSS characteristics and expected performance. The values are related to typical environment and conditions.

Parameters		Typical Measurement	Notes
Sensitivity	Standalone or MS Based Tracking Sensitivity	-160.0 dBm	
	Acquisition	-147.0 dBm	
	Cold Start Sensitivity	-145.0 dBm	
TTFF	Hot	1.1s	GPS+GLONASS Simulator test
	Warm	22.1s	GPS+GLONASS Simulator test
	Cold	29.94s	GPS+GLONASS Simulator test
Accuracy		< 2.0 m	GPS+GLONASS Simulator test @ CEP50
Min Navigation update rate		1Hz	
Dynamics		2g	
Operation limits		515 m/sec	
A-GPS		Supported	

Table 42: GNSS Characteristics

Not Subject to NDA

Note: The sensitivity level has a deviation about +/- <2dB each model and device

Not Subject to NDA

10. MOUNTING THE MODULE ON YOUR BOARD

10.1. General

The LE910Cx module is designed to be compliant with a standard lead-free soldering process.

10.2. Finishing & Dimensions

The below figure shows the mechanical dimensions of the LE910Cx module.

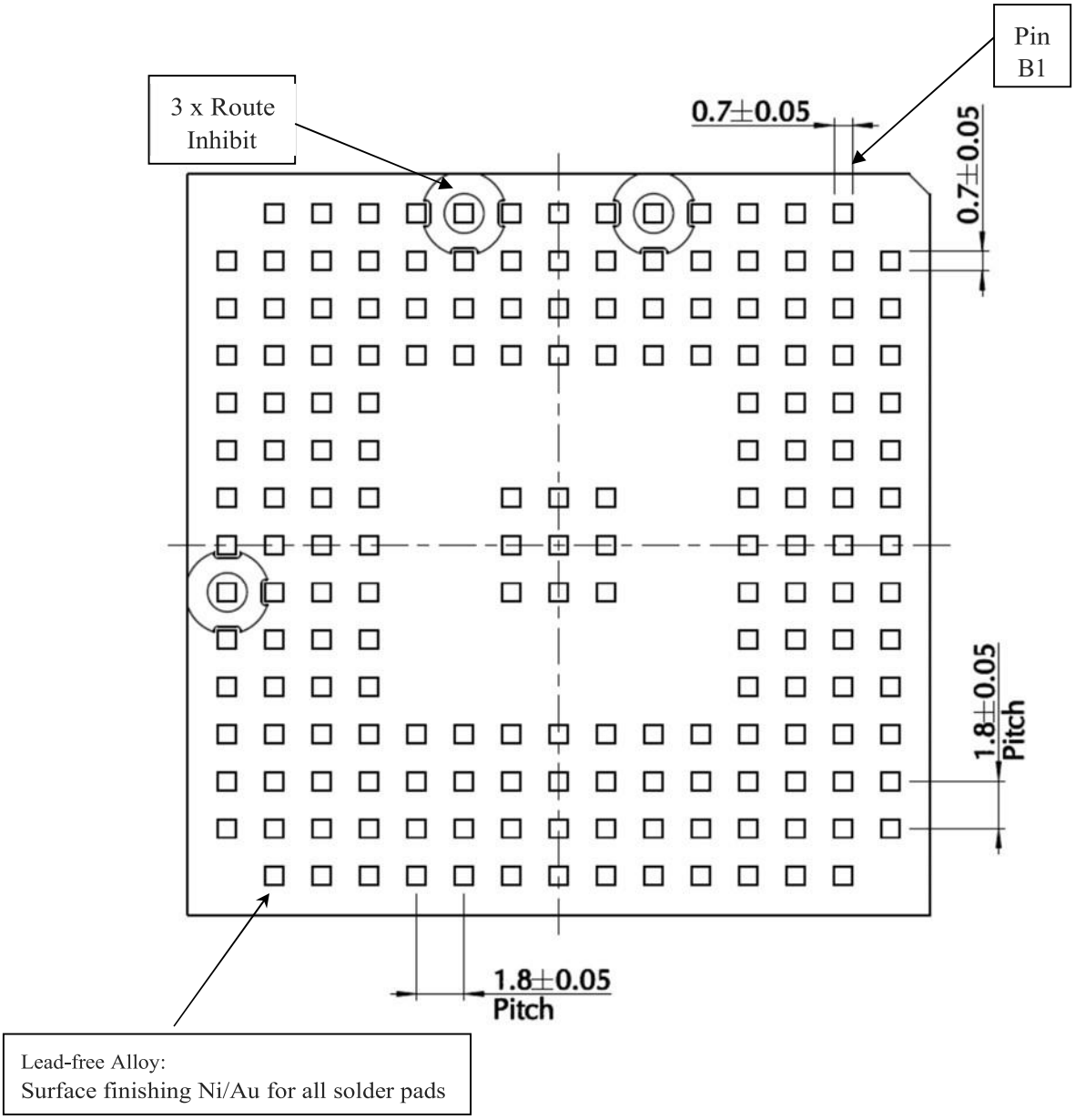


Figure 26: LE910Cx Mechanical Dimensions (Bottom View) except for LE910Cx-WWX

Not Subject to NDA

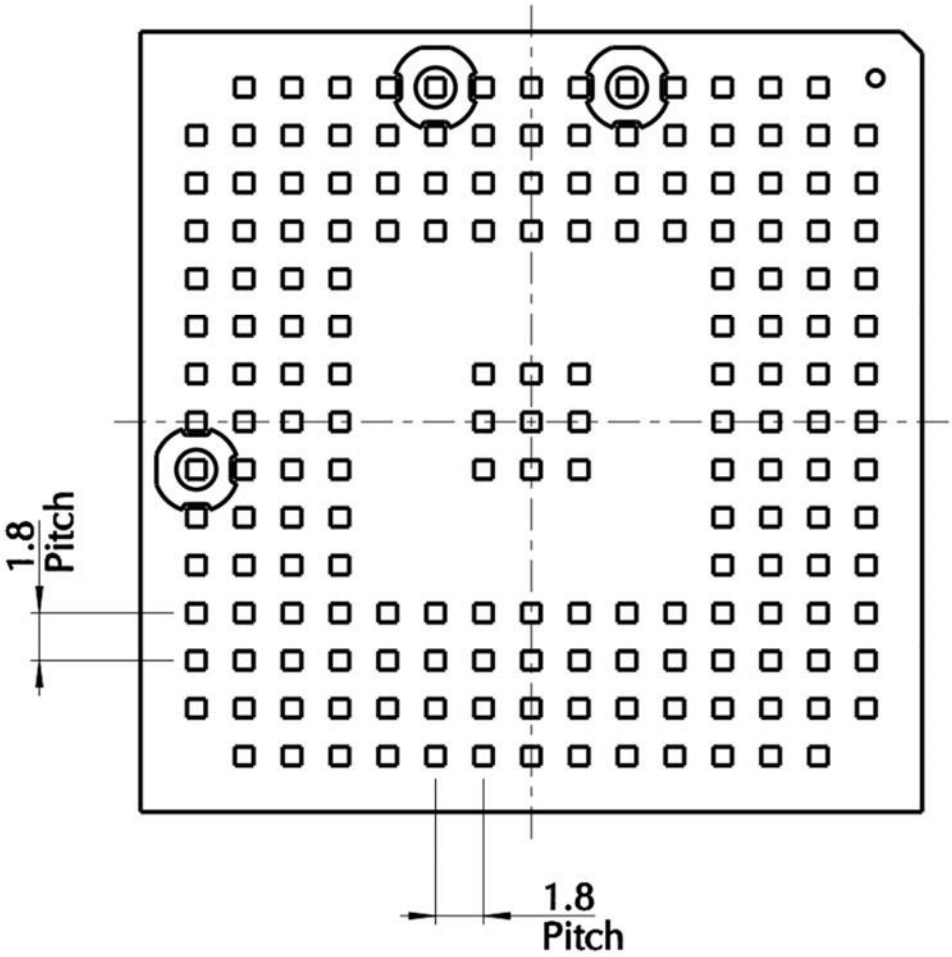


Figure 26-1: LE910Cx-WWX Mechanical Dimensions (Bottom View)

Note: LE910Cx-WWX mechanical dimension is bigger than other LE910Cx variants

Please, refer to 10.3 section for detail information.

Not Subject to NDA

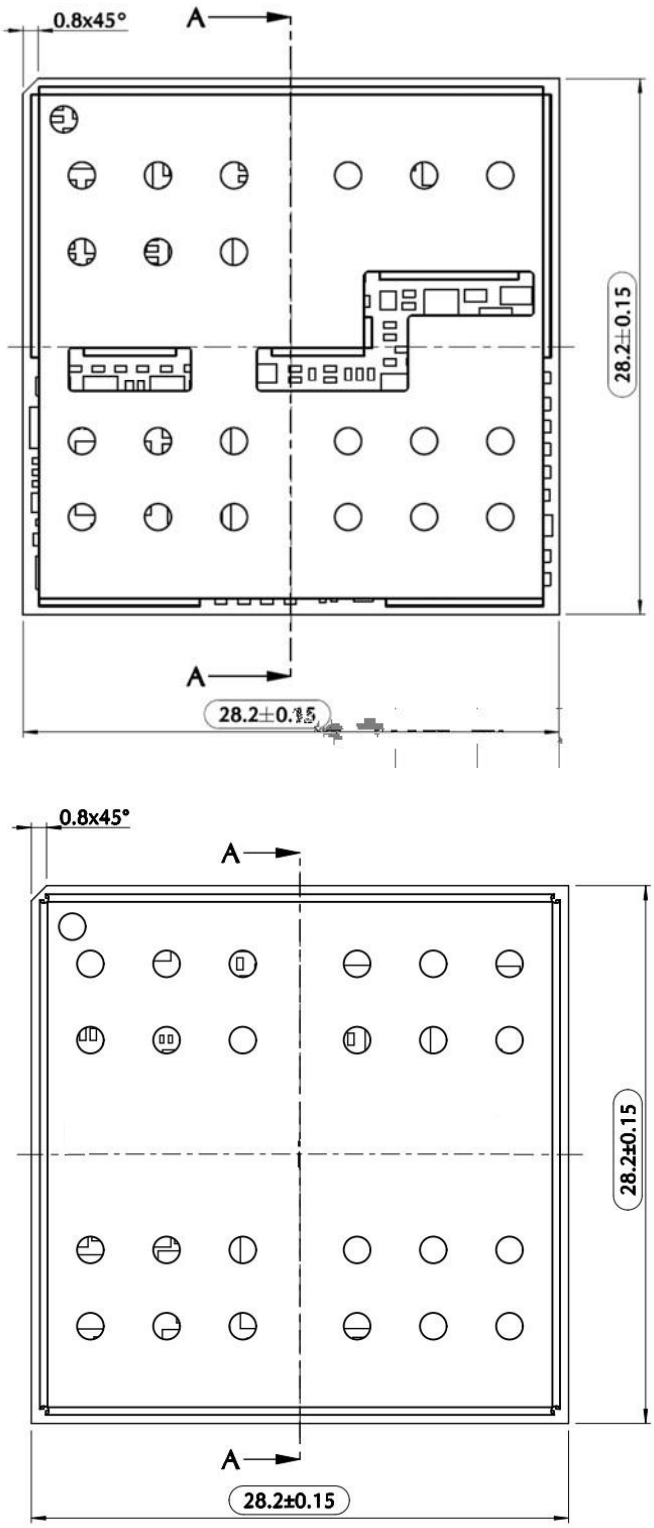


Figure 27: LE910Cx Mechanical Dimensions (Top view) with two kinds of shield design except for LE910Cx-WWX

Not Subject to NDA

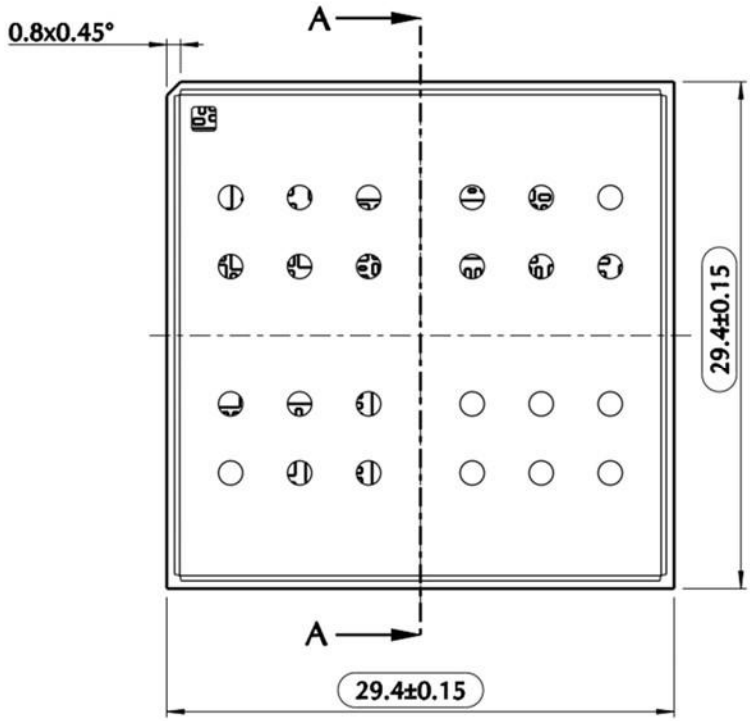


Figure 28: LE910Cx-WWX Mechanical Dimensions (Top view)

Note: LE910Cx-AP/NA/NS/EU/NF/ST/SA has two sheild design and LE910Cx-SV/SVX/LA/CN/EUX/SAX/WWX has one shield design.

Not Subject to NDA

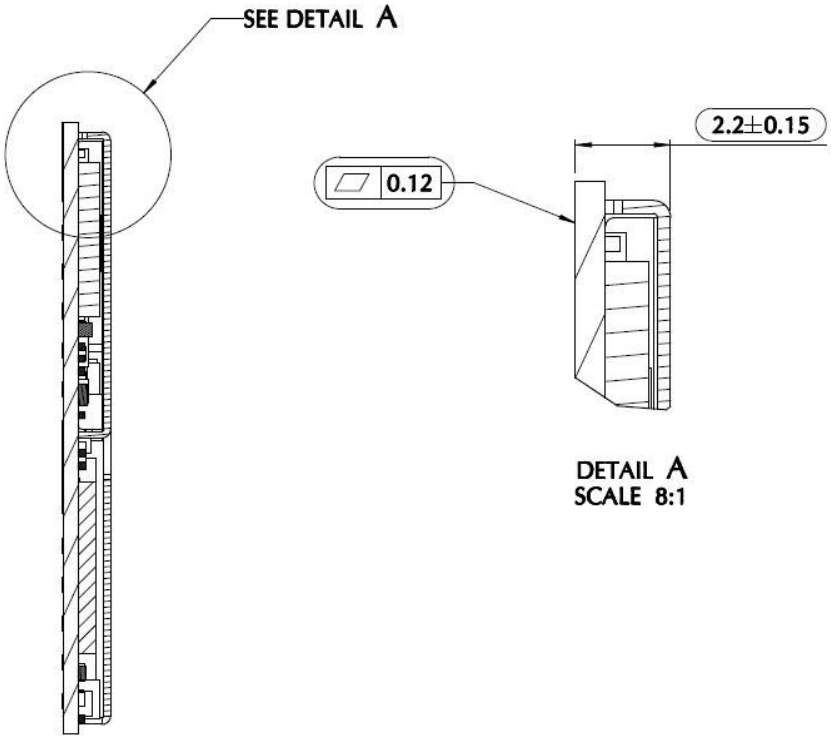


Figure 29: LE910Cx Mechanical Dimensions (Side view) except for LE910C1-SV and -SVX

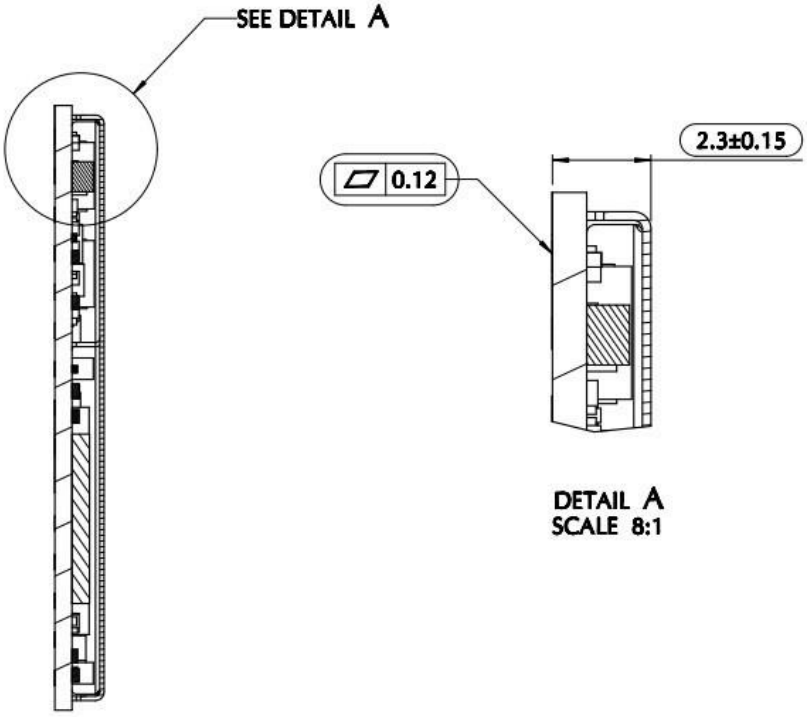


Figure 30: LE910C1-SV and SVX Mechanical Dimensions (Side view)

Not Subject to NDA

10.3. Recommended Footprint for the Application

Figure 31 and 31-1 shows the recommended footprint for the application board (dimensions are in mm).

To facilitate the replacement of the LE910Cx module if necessary, it is suggested to design the application board with a 1.5 mm placement inhibit area around the module.

It is also suggested, as a common rule for an SMT component, to avoid having a mechanical part of the application board in direct contact with the module.

Note: In the customer application, the region marked as INHIBIT WIRING in Figure 31 and 31-1 must be clear of signal wiring or ground polygons.

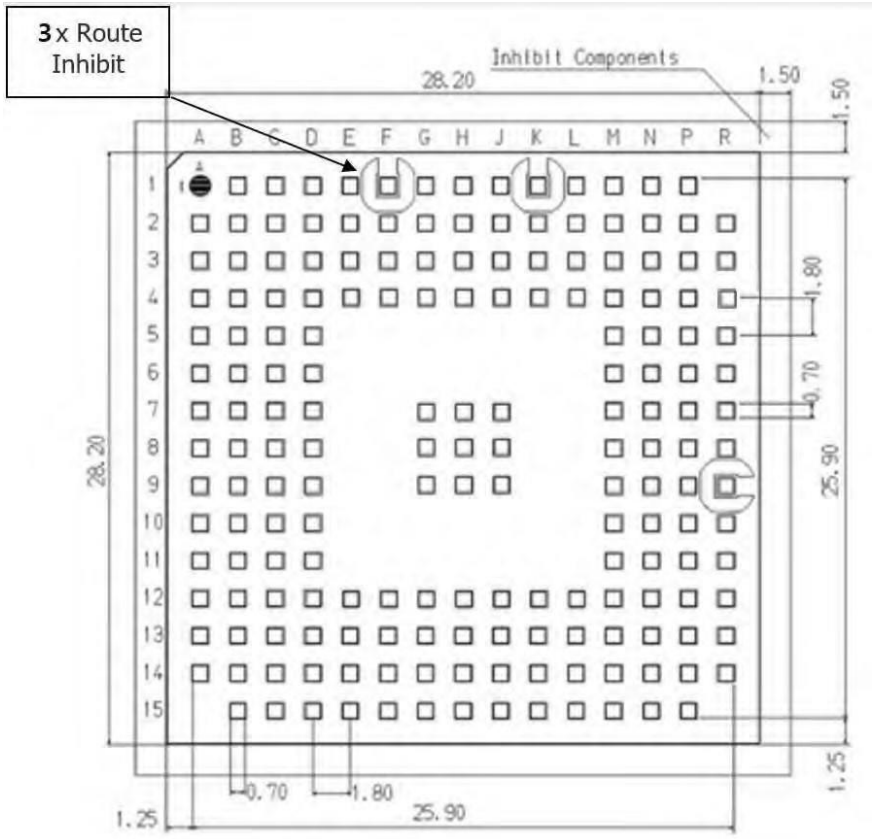


Figure 31: Recommended Footprint - Top View, 181 pads for LE910Cx variants except for LE910Cx-WWX

Not Subject to NDA

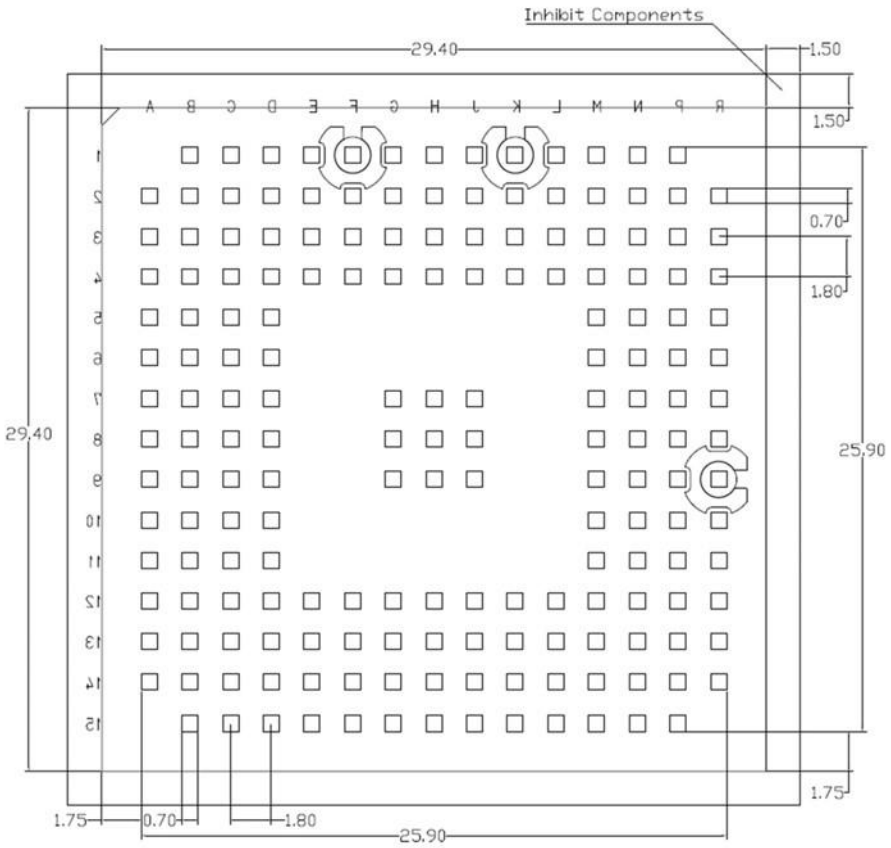


Figure 32-1: Recommended Footprint - Top View, 181 pads for LE910Cx-WWX only

Note: LE910Cx-WWX footprint is same as LE910Cx variants but PCB size is differenct others.

Please, refer to above dimension for LE910Cx-WWX.

Not Subject to NDA

10.4. Stencil

The layout of the stencil openings can be the same as the recommended footprint (1:1).
The suggested thickness of stencil foil is greater than 120 µm.

10.5. PCB Pad Design

The solder pads on the PCB are recommended to be of the Non-Solder Mask Defined (NSMD) type.

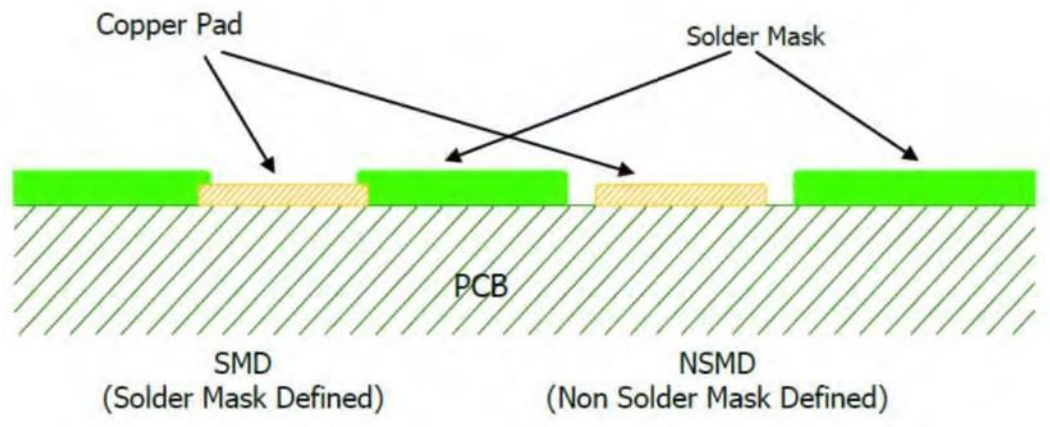


Figure 33: PCB Pad Design

10.6. Recommendations for PCB Pad Dimensions (mm)

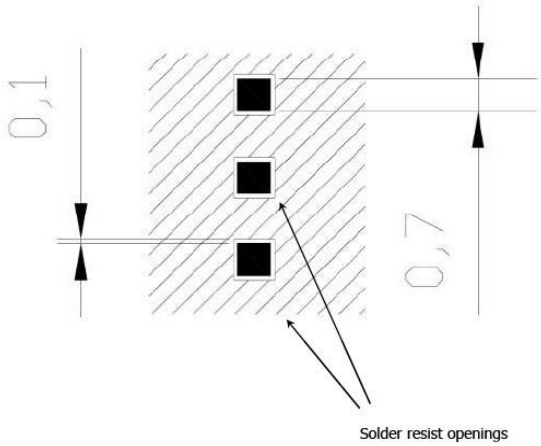


Figure 34: PCB Pad Dimensions

Not Subject to NDA

It is not recommended to place a via or micro-via not covered by solder resist around the pads in an area of 0.15 mm unless it carries the same signal as the pad itself. Micro vias inside the pads are allowed.

Holes in pad are only allowed for blind holes and not for through holes.

Finish	Layer Thickness (um)	Properties
Electro-less Ni / Immersion Au	3-7 / 0.05-0.15	Good solder ability protection, high shear force values

Table 43: Recommendations for PCB Pad Surfaces

The PCB must be able to resist the higher temperatures, which occur during the leadfree process. This issue should be discussed with the PCB-supplier. In general, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.

10.7. Solder Paste

We recommend using only “no clean” solder paste to avoid the cleaning of the modules after assembly.

10.7.1. Solder Reflow

Figure 35 shows the recommended solder reflow profile.

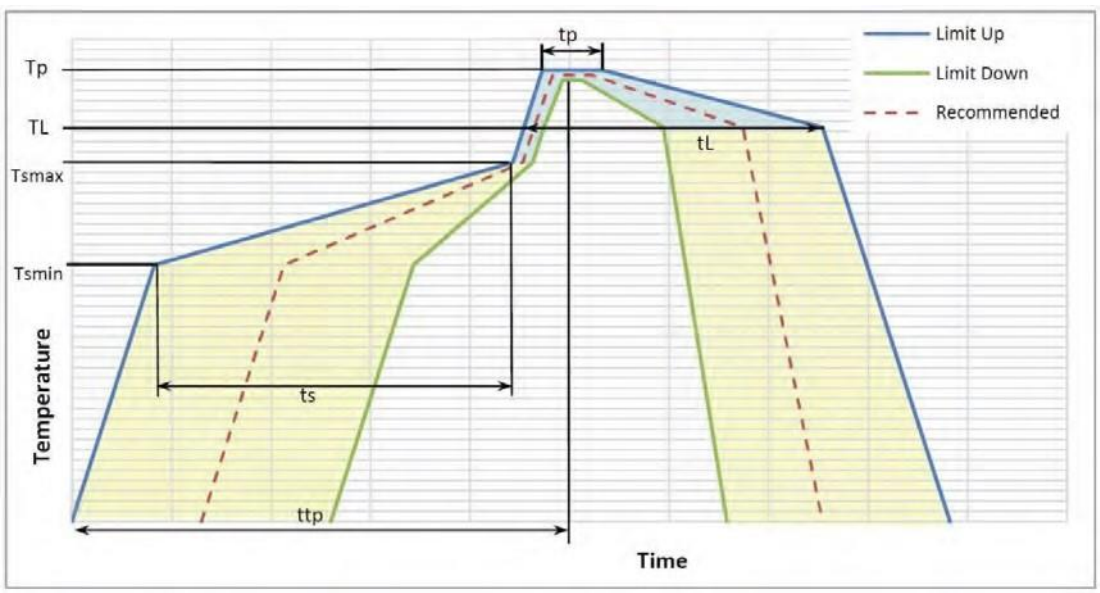


Figure 35: Solder Reflow Profile

Not Subject to NDA

Warning: The above solder reflow profile represents the typical SAC reflow limits and does not guarantee adequate adherence of the module to the customer application throughout the temperature range. Customer must optimize the reflow profile depending on the overall system taking into account such factors as thermal mass and warpage

Profile Feature	Pb-Free Assembly
Average ramp-up rate (TL to TP)	3°C/second max
Preheat – Temperature min (Tsmin) – Temperature max (Tsmax) – Time (min to max) (ts)	150°C 200°C 60-180 seconds
Tsmax to TL – Ramp-up rate	3°C/second max
Time maintained above: – Temperature (TL) – Time (tL)	217°C 60-150 seconds
Peak temperature (Tp)	245 +0/-5°C
Time within 5°C of actual peak Temperature (tp)	10-30 seconds
Ramp-down rate	6°C/second max
Time 25°C to peak temperature	8 minutes max

Table44:SolderProfileCharacteristics

Note: All temperatures refer to the top side of the package, measured on the package body surface.

Warning: The LE910Cx module withstands one reflow process only.

10.7.2. Cleaning

In general, cleaning the module mounted on the carrier board is not recommended.

- Residues between the module and the host board cannot be easily removed with any cleaning method.

Not Subject to NDA

- Cleaning with water or any organic solvent can lead to capillary effects where the cleaning solvent is absorbed into the gap between the module and the host board or even leaks inside the module (due to the gap between the module shield and PCB). The combination of soldering flux residues and encapsulated solvent could lead to short circuits between conductive parts. The solvent could also damage the module label.
- Ultrasonic cleaning could damage the module permanently. Especially for crystal oscillators where the risk of damaging is very high.

Not Subject to NDA

11. APPLICATION GUIDE

11.1. Debug of the LE910Cx Module in Production

To test and debug the mounting of the LE910Cx module, we strongly recommend adding several test pads on the application board design for the following purposes:

- Check the connection between the LE910Cx itself and the application
- Test the performance of the module by connecting it to an external computer

Depending on the customer's application, these test pads include, but are not limited to the following signals:

- TXD
- RXD
- ON/OFF
- HW_SHUTDOWN_N
- GND
- VBATT
- TX_AUX
- RX_AUX
- USB_VBUS
- USB_D+
- USB_D- GPIO_09
- WCI_RX

In addition, the following signals are also recommended (but not mandatory):

- PWRMON
- GPIO_01 (STAT_LED)
- GPIO_08 (SW_RDY)

11.2. Bypass Capacitor on Power Supplies

When there is a sudden voltage step to or a cut from the power supplies, the steep transition causes some reactions such as overshoot and undershoot. This abrupt voltage transition can affect the device causing it to fail or malfunction.

Not Subject to NDA

Bypass capacitors are needed to alleviate this behaviour. The behaviour can appear differently depending on the various applications. Customers need to pay special attention to this issue when designing their application board. The length and width of the power lines must be carefully considered, and the capacitance of the capacitors must be selected accordingly. The capacitor will also prevent power supplies ripple and switching noise caused in TDMA systems, such as GSM.

Especially, a suitable bypass capacitor must be mounted on the following lines on the application board:

- VBATT & VBATT_PA (M1, M2, N1, N2, P1, P2)
- USB_VBUS (Pad A13) Recommended values are:
- 100uF for both VBATT and VBATT_PA together
- 4.7uF for USB_VBUS (including the 1uF capacitor inside the module)

Customers must still consider that the capacitance mainly depends on the conditions of their application board.

Generally, more capacitance is required when the power line is longer.

11.3. SIM Interface

This section presents the recommended schematics for the design of SIM interfaces on the application boards. The LE910Cx supports two external SIM interfaces.

11.3.1. SIM Schematic Example

Figure 36 illustrates in particular how to design the application side and what values to assign the components.

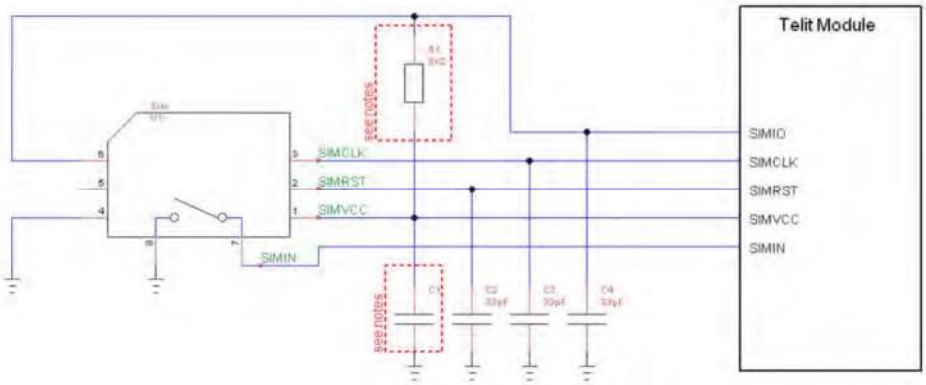


Figure 36: SIM Schematics

Not Subject to NDA

Note: The resistor value on SIMIO pulled up to SIMVCC must be defined to be compliant with the 3GPP specification for USIM electrical testing.

The LE910Cx module contains an internal pull-up resistor of 10K Ω on SIMIO.
However, the un-mounted R1 option in the application can be used to tune SIMIO timing if necessary.

Table 45 lists the values of C1 to be adopted with the LE910Cx product:

Product P/N	C1 Range (nF)
LE910Cx	100 nF

Table 45: SIM Interface – C1 Range

11.4. EMC Recommendations

All LE910Cx signals are provided with some EMC protection. However, the accepted level differs according to the specific pin.

Human body model (HBM) rating: 2000 V, JESD22-A114

Charged device model (CDM) rating: 500 V, JESD22-C101

Appropriate series resistors must be considered to protect the input lines from overvoltage.

11.5. Download and Debug Port

Choose one of the following options in the design of the host system to download or upgrade the EXFO software and debug the LE910Cx module when it is already mounted on a host system.

- UART and USB interfaces.
- Users who use both UART and USB interfaces to communicate with the LE910Cx module must implement a USB download method in the host system to upgrade the LE910Cx when it is mounted.
- USB interface only.
- Users who use a USB interface only to communicate with the LE910Cx module must arrange for a USB port in the host system to debug or upgrade the LE910Cx when it is mounted.
- UART interface only.

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- Users who use a UART interface only to communicate with the LE910Cx module must arrange for a UART port in the host system to debug or upgrade the LE910Cx when it is mounted.

11.5.1. Fast Boot mode

Fast boot mode is normally used by EXFO SW to enter SW download mode

Fast boot is triggered by GPIO_09 (PAD L15). Asserting this signal high (1.8V) during boot will force the system into Fast boot

11.5.2. Recovery Boot Mode

Emergency boot download mode is used in case of corrupted boot image has been flashed into the device or in case all other recovery modes failed to work

The emergency download mode is triggered by WCI_RX signal (PAD M9). Asserting this signal high (1.8V) during boot will force the system into Emergency download.

Note: The application board must support accessible test pads on GPIO_09 and WCI_RX signal to enable the download recovery modes mentioned above.

Not Subject to NDA

12. PACKING SYSTEM

12.1. Packing System – Tray

The LE910Cx modules are packaged on trays of 36 pieces each as shown in Figure 37.

These trays can be used in SMT processes for pick & place handling.

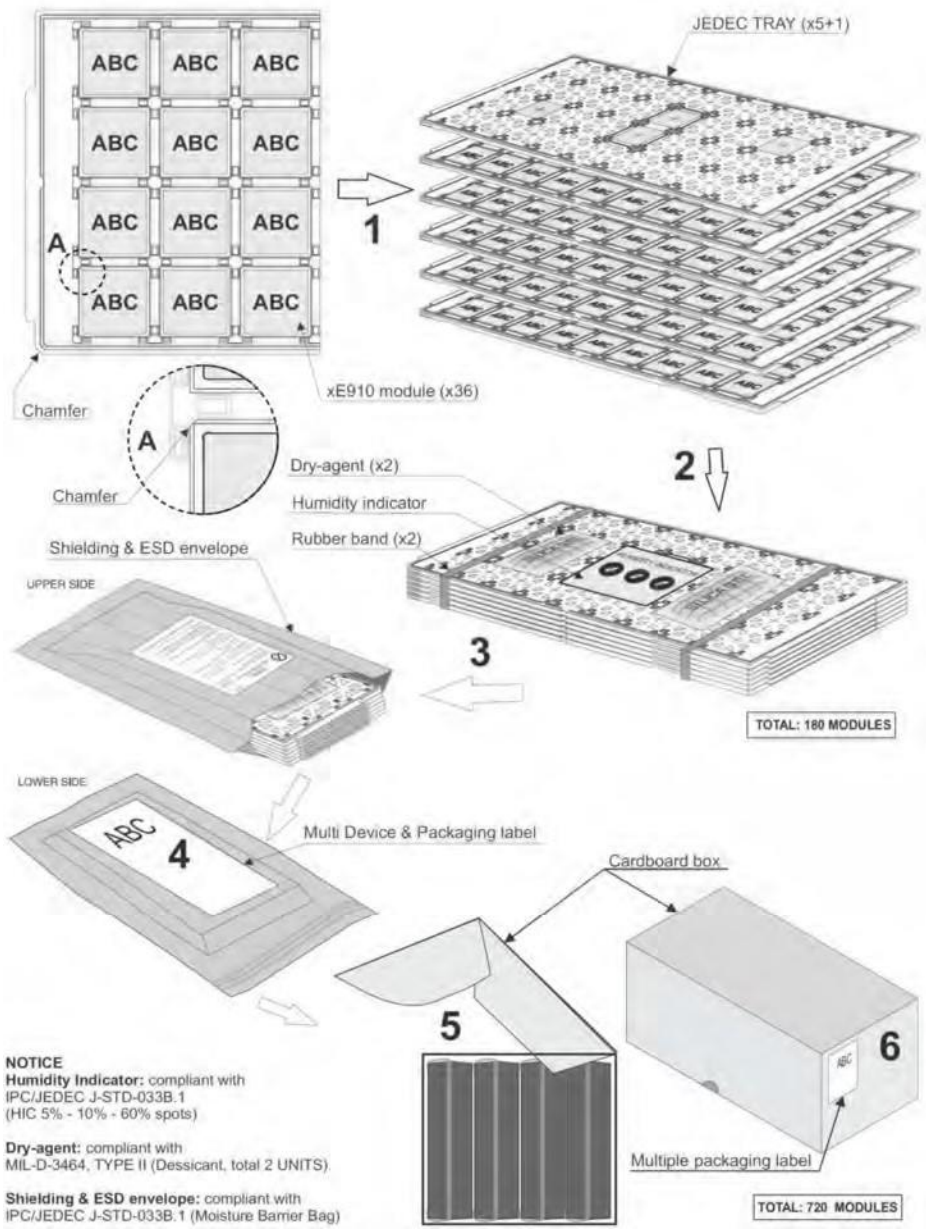

Figure 37: Packing

Not Subject to NDA

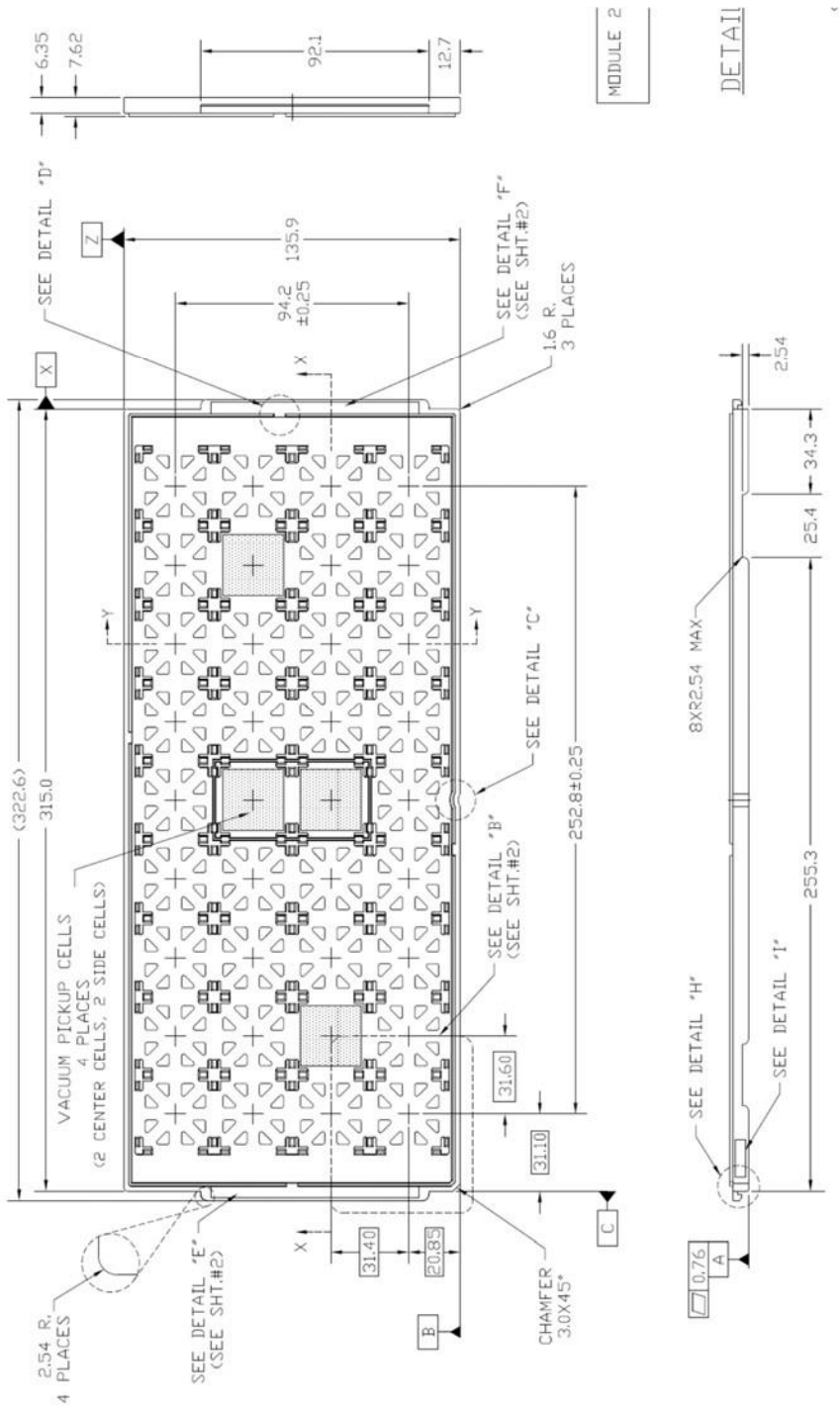

Figure 38: Tray Drawing

Not Subject to NDA

12.2. Tape & Reel

The LE910Cx can be packaged on reels of 200 pieces each.

See figure for module positioning into the carrier.

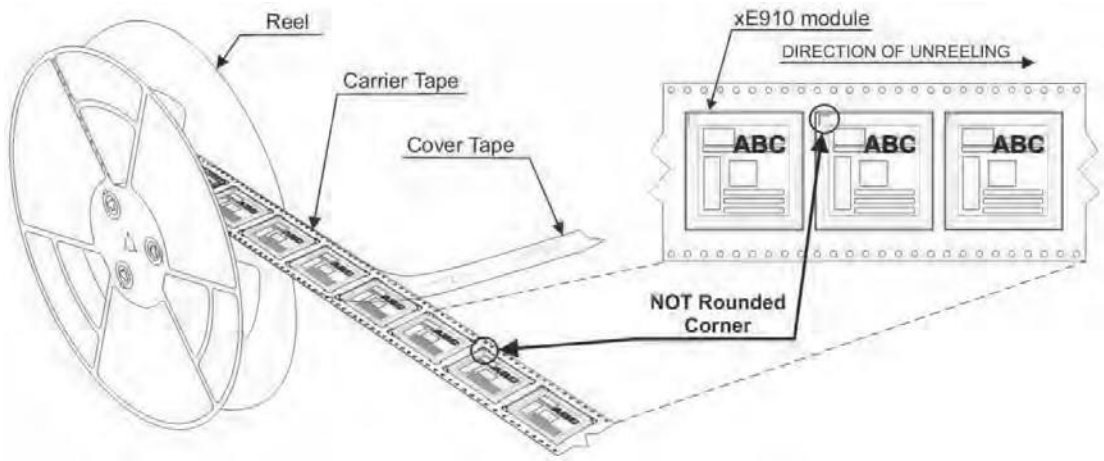

Figure 39: Module Positioning into the Carrier

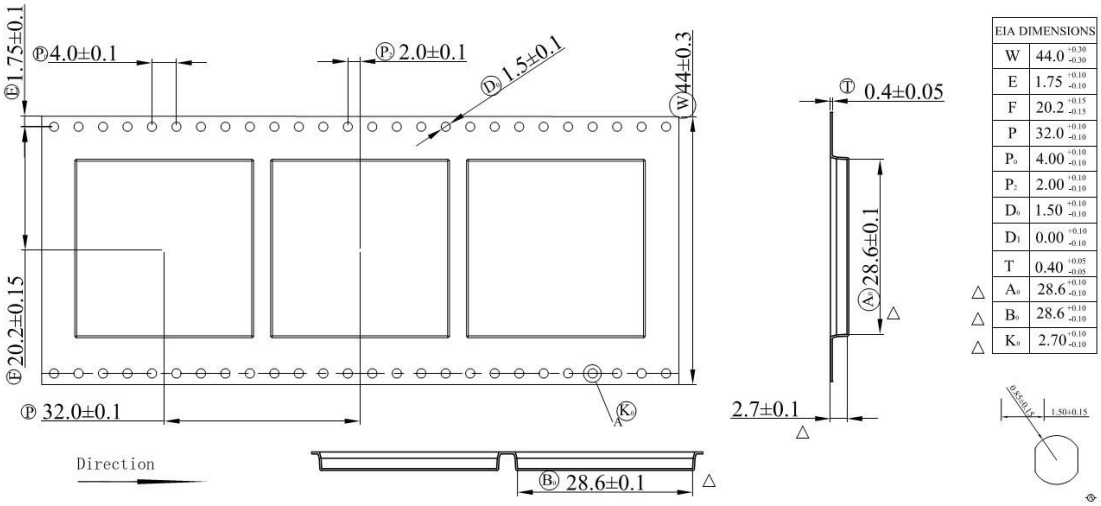

Figure 40: Carrier Tape Detail

Not Subject to NDA

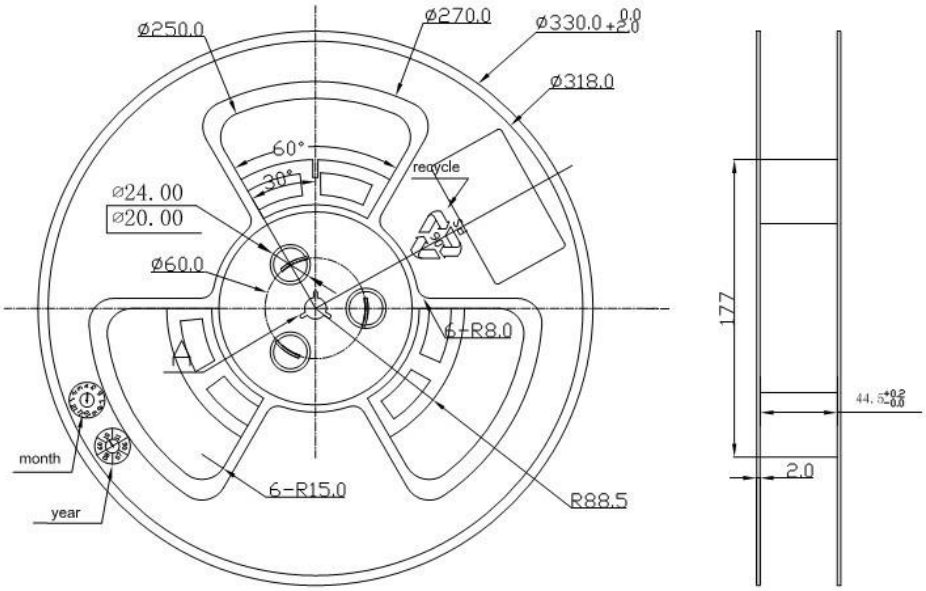

Figure 41: Reel Detail

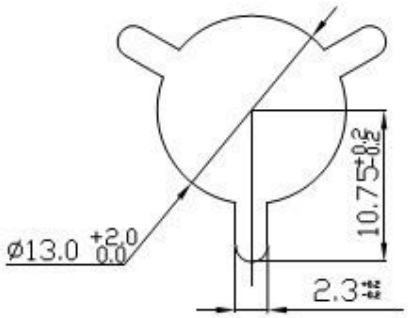

Figure 42: Detail

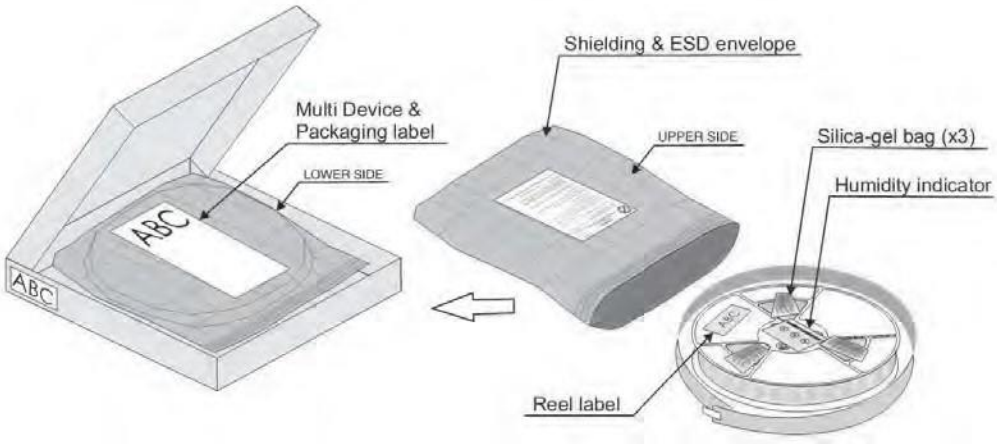

Figure 43: Reel Box Detail

Not Subject to NDA

12.3. Moisture Sensitivity

The LE910Cx module is a Moisture Sensitive Device Level 3, in accordance with standard IPC/JEDEC J-STD-020. Comply with all the requirements for using this kind of components.

Not Subject to NDA

13. CONFORMITY ASSESSMENT ISSUES

13.1. FCC/ISED Regulatory Notices

Information for the OEMs and Integrators

The following statement must be included with all versions of this document supplied to an OEM or integrator but should not be distributed to the end user.

1. This device is intended for OEM integrators only.
2. Please see the full Grant of Equipment document for other restrictions

Manual Information To the End User

The OEM integrator should be aware not to provide information to the end user on how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warming as shown in this manual

Modular approval RF Exposure

The product complies with FCC, ISED and EU Specific Absorption Rate (SAR) limits applicable to devices approved for use in uncontrolled environments (general public use) when used as directed in this user documentation.

Le produit est conforme aux limites de débit d'absorption spécifique (DAS) de la FCC, de l'ISDE et de l'UE applicables aux appareils approuvés pour une utilisation dans des environnements non contrôlés (utilisation par le grand public) lorsqu'il est utilisé conformément aux instructions.

Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only authorized by the FCC for the specific rule parts (for example, FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed. The end product with an embedded module may also need to pass the FCC Part 15 unintentional emission testing requirements and be properly authorized per FCC Part 15

Not Subject to NDA

Trace antenna designs

See 7.2 GSM/WCDMA/TD-SCDMA/LTE Antenna - PCB Line Guidelines

Summary of the specific operational use conditions

See apart 7.1 GSM/WCDMA/TD-SCDMA/LTE Antenna - Antenna requirements

Modification Statement

EXFO has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

EXFO n'approuve aucune modification apportée à l'appareil par l'utilisateur, quelle qu'en soit la nature. Tout changement ou modification peuvent annuler le droit d'utilisation de l'appareil par l'utilisateur.

Interference Statement (if it is not placed in the device)

This device complies with Part 15 of the FCC Rules and Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Wireless Notice

This device complies with FCC/ISED radiation exposure limits set forth for an uncontrolled environment and meets the FCC radio frequency (RF) Exposure Guidelines and RSS-102 of the ISED radio frequency (RF) Exposure rules. Antenna gain must be below:

Not Subject to NDA

Frequency Band	Freq [MHz]	LE910C1 -NA Gain [dBi]	LE910C1 -NS Gain [dBi]	LE910C1/C4 -NF Gain [dBi]	LE910C1 -SV Gain [dBi]	LE910C1/C4 -LA Gain [dBi]	LE910C1 -SA Gain [dBi]	LE910C1 - SAX Gain [dBi]	LE910C1 -ST Gain [dBi]	LE910C1/C4 -WWX Gain [dBi]
850 MHz	850	3.64	6.08	6.12	NA	3.5	NA	NA	NA	3.62
1900 MHz	1900	2.51	8.01	8.01	NA	9.5	8.01	8.00	8.01	8.51
1700 MHz	1700	5.00	5.00	5.00	6.00	13.0	5.00	5.00	5.00	5.50
900 MHz	900	5.00	N/A	N/A	N/A	N/A	NA	NA	NA	7.38
700 MHz	700	5.63	5.63	5.94	6.44	N/A	5.63	5.60	5.63	6.64
600 MHz	600	N/A	N/A	5.63	N/A	N/A	NA	NA	5.63	N/A
2600 MHz	2600	N/A	N/A	N/A	N/A	13.0	NA	NA	NA	9.01

Table 46: Antenna gain from FCC/ISED

Note: These are the max gain usable considering all the technologies featured, for more details please refer to FCC Grant for each project.

Le présent appareil est conforme à l'exposition aux radiations FCC / ISED définies pour un environnement non contrôlé et répond aux directives d'exposition de la fréquence de la FCC radiofréquence (RF) et RSS-102 de la fréquence radio (RF) ISED règles d'exposition. Gain de l'antenne doit être ci-dessous:

Frequency Band	Freq [MHz]	LE910C1 -NA Gain [dBi]	LE910C1 -NS Gain [dBi]	LE910C1/C4 -NF Gain [dBi]	LE910C1 -SV Gain [dBi]	LE910C1/C4 -LA Gain [dBi]	LE910C1 -SA Gain [dBi]	LE910C1 - SAX Gain [dBi]	LE910C1 -ST Gain [dBi]	LE910C1/C4 -WWX Gain [dBi]
850 MHz	850	3.64	6.08	6.12	NA	3.5	NA	NA	NA	3.62
1900 MHz	1900	2.51	8.01	8.01	NA	9.5	8.01	8.00	8.01	8.51
1700 MHz	1700	5.00	5.00	5.00	6.00	13.0	5.00	5.00	5.00	5.50
900 MHz	900	5.00	N/A	N/A	N/A	N/A	NA	NA	NA	7.38
700 MHz	700	5.63	5.63	5.94	6.44	N/A	5.63	5.60	5.63	6.64
600 MHz	600	N/A	N/A	5.63	N/A	N/A	NA	NA	5.63	N/A
2600 MHz	2600	N/A	N/A	N/A	N/A	13.0	NA	NA	NA	9.01

Table 47: Antenna gain from FCC/ISED

Not Subject to NDA

FCC Class B Digital Device Notice

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Labelling Requirements for the Host device

The host device shall be properly labelled to identify the modules within the host device. The certification label of the module shall be clearly visible at all times when installed in the host device, otherwise the host device must be labelled to display the FCC ID and IC of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as follows:

LE910C1/C4 WWX

Contains FCC ID: 2AYQH-LE910CXWWX

Contains IC: 26882-LE910CXWWX

CAN ICES-3 (B) / NMB-3 (B)

Not Subject to NDA

L'appareil hôte doit être étiqueté comme il faut pour permettre l'identification des modules qui s'y trouvent. L'étiquette de certification du module donné doit être posée sur l'appareil hôte à un endroit bien en vue en tout temps. En l'absence d'étiquette, l'appareil hôte doit porter une étiquette donnant le FCC ID et le IC du module, précédé des mots « Contient un module d'émission », du mot « Contient » ou d'une formulation similaire exprimant le même sens, comme suit:

LE910C1/C4 WWX

Contains FCC ID: 2AYQH-LE910CXWWX

Contains IC: 26882-LE910CXWWX

CAN ICES-3 (B) / NMB-3 (B)

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de classe B est conforme à la norme canadienne ICES-003.

Not Subject to NDA

13.2. JTBL Regulatory Notices

Antenna

According to Japan regulatory rule, module certification is valid only with the specific antennas registered to and approved by JRL certified body in relation to module certification. Customers who are going to use modules under Japan Radio Law, are responsible to contact EXFO technical support or sales to get the list of these antennas.

Dial Function

The JTBL Module Certification for “LE910C1-AP” is for “non-Auto Redial Function” device.

In case customer implement “Auto Redial” function into Application Device by controlling LE910C1-AP, the customer cannot utilize LE910C1-AP JTBL certification, and they must apply JTBL as “Application Device” System.

13.3. NCC Regulatory Notices

According to NCC Taiwan requirements, the module and the packaging shall be identified as described in the following lines. Shall be added also the specified safety warning statement.

Brand name: EXFO

Model name: LE910C1-AP

Product name: WWAN module

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NCC logo:

NCC ID: CCAF19Z10050T8

NCC safety warning statement: “減少電磁波影響，請妥適使用”

13.4. ANATEL Regulatory Notices

"Este equipamento não tem direito à proteção contra interferência prejudicial e não pode causar interferência em sistemas devidamente autorizados"

"This equipment is not entitled to protection against harmful interference and must not cause interference in duly authorized systems" LE910C1-LA Homologation # 05818-19-02618

LE910C1-AP Homologation # 04679-18-02618

LE910C4-LA Homologation # 07669-19-02618

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14.3. Safety Recommendations

Make sure the use of this product is allowed in your country and in the environment required. The use of this product may be dangerous and has to be avoided in areas where:

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- it can interfere with other electronic devices, particularly in environments such as hospitals, airports, aircrafts, etc.
- there is a risk of explosion such as gasoline stations, oil refineries, etc. It is the responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conformed to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible for the functioning of the final product. Therefore, the external components of the module, as well as any project or installation issue, have to be handled with care. Any interference may cause the risk of disturbing the GSM network or external devices or having an impact on the security system. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed carefully in order to avoid any interference with other electronic devices.

The equipment must be supplied by an external specific limited power source in compliance with the standard EN 62368-1:2014.

The European Community provides some Directives for the electronic equipment introduced on the market. All of the relevant information is available on the European Community website:

https://ec.europa.eu/growth/sectors/electrical-engineering_en

Not Subject to NDA

15. GLOSSARY

ADC	Analog-to-digital converter
AE	Application-enabled
CABC	Content Adaptive Backlight Control
DAC	Digital-to-analog converter
DTE	Data Terminal Equipment
FDD	Frequency division duplex
GLONASS	Global orbiting navigation satellite system
GNSS	Global navigation satellite system
GPIO	General-purpose input/output
GPRS	General packet radio services
GPS	Global positioning system
GSM	Global system for mobile communications
HSIC	High-speed inter-chip
I2C	Inter-integrated circuit
LTE	Long term evolution
RGMII	Reduced Gigabit media-independent interface
SD	Secure digital
SGMII	Serial Gigabit media-independent interface
SIM	Subscriber identity module
SMX	SmartMX
SOC	System-on-Chip
SPI	Serial peripheral interface
UART	Universal asynchronous receiver transmitter
UMTS	Universal mobile telecommunications system
USB	Universal serial bus
WCDMA	Wideband code division multiple access
WCI	Wireless Coexistence Interface

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16. DOCUMENT HISTORY

Revision	Date	Changes
34	2021-07-09	Table 48: GNSS Characteristics updated 13.1. FCC/ISED Regulatory Notices updated for LE910Cx-WWX
33	2021-07-01	Section 1.5 – Updated Related Documents Section 5.1 – Added flow chart for turn on and AT command managing procedure Section 6.2 – Added note for eDRX Section 8.6 – Update Audio Interface (ThreadX OS support PCM) Section 10-3 - Recommended Footprint for the Application updated for LE910Cx-WWX Table 49: LE910Cx Current Consumption updated Section 10.x – Dimension and Mechanical design updated
32	2021-03-23	Section 5.3.3 – Fixed Typo in Note of Section. Section 8.6 – Update PCM CLK rate.
31	2021-02-05	Table 1: Applicability Table updated Table4: RF Bands per Regional Variant updated 2.8.1 Dimensions updated 3.1 Note added
30	2021-01-29	Section 2.3 – Added not supported function only based on TreadX OS models Section 8.5.1 – Updated Note
29	2021-01-12	Updated Section 8.6 – updated I2S diagram
28	2020-12-08	Updated APPLICABILITY TABLE and added notes Section 3.1 – Updated Pin-out Section 5.2 – Updated Initialization and Activation figure and added timing table Section 5.3 – Updated figures Section 14.1 - Updated FCC/ISED Regulatory Notices Updated Table 50: RF Bands per Regional Variant
27	2020-07-31	Section 11.4 – Updated EMC Recommendations
26	2020-07-22	7.4 Antenna Diversity Requirements – Note comment changed to AT#RXDIV 14.4 ANATEL Regulatory Notices - Updated
25	2020-06-15	Section 8 – Hardware Interfaces; USB part updated Section 8.1 – Note Updated Table 45 and 4 - EUX variant added Table 46 – CAT 4 DL/UL Tput swapped

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Revision	Date	Changes
		Section 14.1 ANATEL Regulatory Notices – Homologation No. fixed Section 2.7.1 Sensitivity – Sensitivity Table added Section 2.2. Applications – E-call comment deleted Table 47 – Sensitivity level changed Sections 7.4 Antenna Diversity Requirements – Note comment changed Section 7.5 GNSS Antenna Requirements – Note added Table 39 – Sensitivity table changed and note added
24	2020-04-29	Section 8.3 – SGMII interface updated
23	2020-04-20	Section 6.2 – Power Consumption updated
22	2020-04-02	Section 7.4 – Diversity ANT PAD changed
21	2020-03-30	Section 2.8.2 – Weight updated
20	2020-01-23	Section 3.1 – WOW pin updated Section 3.2 – Table updated Section 3.3 – LGA Pads Layout updated Section 8.7 – GPIOs table updated
19	2019-11-27	Section 14.4 – Added ANATEL Regulatory notices
18	2019-11-21	Section 8.5.3 – SD/MMC Card interface updated
17	2019-10-29	Section 9.1 – STATUS LED control updated
16	2019-10-22	Section 2.7.2 – Output power updated
15	2019-10-15	Section 3.1 – Warning comment removed Table 34, 35 – note updated Table 18 – Updated Idle mode current consumption Section 14.3 – Added NCC (TW) requirement section
14	2019-09-03	Table 18 – Updated the current consumption of LTE max power Table 6 – Updated the description of E13 pin-out 14.1 FCC/ISED Regulatory Notices updated for LE910C1/C4-LA 14.1 FCC/ISED Regulatory Notices updated Table 5 – LTE B2 fixed Section 2.7.1 – Sensitivity updated Section 7.5 – Note added for passive or active ANT installation Table 36 – Network Service Availability Indication updated
13	2019-05-14	Table 1 and 4 LE910C1-xx bis Variants removed Section 3.2 and 7– Note for C1 bis variants removed

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Revision	Date	Changes
12	2019-04-23	Table 1, 4 – Added variants Table 19,21 – Added comment
11	2019-03-22	Section 10.7.1 – Warning comment added
10	2019-03-13	Section 2.8.1 – Note added for C1-SV variant Section 3.1 – Updated E13 Pin-out Section 3.3 – Updated figure 2. LGA Pads Layout Added Fast Power Down Section 5.5 Table 18 – Updated Idle mode current consumption Section 10.2 – Picture added for Cx-SV/LA variants Section 14.2 – Japan Radio Law comment added
9	2019-03-06	Table 1 and 4 Variants updated Section 2.7 - RF Parameters updated Section 3.2 – Note added for C1 bis variants Section 6.2 – Power consumption update Section 7 – Note added for C1 bis variants
8	2018-12-12	14.1 FCC/ISED Regulatory Notices updated for LE910C1-SA and LE910C1-ST
7	2018-11-19	14.1 FCC/ISED Regulatory Notices updated for LE910C1-SV
6	2018-10-25	Table 1 & 4 – Added -SA, ST, SV and LA variants. Table 5 – Added B14 Section 2.5.1 – Updated Temperature Range
5	2018-09-16	Section 14 – Adding Antenna gain and FCC ID & IC numbers for LE910C1/C4 NF. Section 5.2 – Fixed typo related to power up timing.
4	2018-08-20	Table 1 & 4 - Added LE910C4-EU variant Section 2.3 – Updated SIM interface max speed Declared HSIC interface as optional throughout the document Section 2.6.2 – Updated RF frequency table Section 6.2 – Added clarification related to DRX and CFUN=5 Section 8.1 - Corrected Typo related to USB_VBUS pad number Section 8.4.1- Clarified note about DTR pin
3	2018-07-18	Section 2.8.1 - Fixed typo related to module size General - Align cross reference links across the document
2	2018-06-14	Template update and pagination update Section 1.5 – Updated AT Command UG reference

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Revision	Date	Changes
		Section 2.6.1 - Updated Band support table Section 6.3.2 - Updated Thermal design guidelines Section 8.3 - Removed “optional” term from Ethernet interface
1.13	2018-05-17	Added new variant LE910C1-NF Section 2.6.1 - Added band 66 support for LE910Cx-NF Section 2.6.2 - Added band 66 and band 71 to frequency table Section 3.1 - Updated value of SIM internal pullup Section 8.3 – added clarification regarding Ethernet control interface logic levels Section 8.5.4 – Removed note related to WIFI_SDRST Section 9.7 - Updated GNSS characteristics
1.12	2018-03-18	Replaced LE910C1 with LE910Cx throughout the document Section 2.6.1 and Table 1 - Added LE910C1-EU and LE910C4-NF variants Section 8.7 – Added notes related to GPIO pullups Section 10.7.2 - Added clarification related to flux cleaning
1.11	2018-02-22	Section 5.3.2 – Updated section name Section 5.4 – Added section for clarifying power down and power off procedures Section 8.6.1 – Update for PCM slave mode
1.10	2017-12-27	General spelling and grammar edits throughout the document Section 2.3 – Updated features list table. Section 2.4 - Fixed typo in section and inside block diagram.
1.09	2017-12-07	Section 14.1 – Updated LE910C1 NA 850MHz Max antenna gain. Section 6.2.2 – Corrected Class12 to Class10.
1.08	2017-11-14	Section 2.6.2 - Changed B41 to B41M Section 2.7 – Renamed from Sensitivity to RF parameters and added TX output power section (2.7.2) Section 2.8 – Added note regarding label thickness Section 3.1 - Removed duplication of description related to USB_VBUS. Section 5.2 – Added clarification regarding ON_OFF. Section 7.5 – Added note related to GPS port. Section 8.1 – Added clarification regarding VBUS supply. Section 8.1.1 – Added clarification regarding OTG. Section 8.3.1 – Added clarification regarding ETH_INT_N pin.
1.07	2017-07-23	Adding a note for power supply section
1.06	2017-07-10	Renaming the product from LE910Cx to LE910C1
1.05	2017-06-18	Section 6.1 – Updated power consumption tables

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Revision	Date	Changes
1.04	2017-05-25	Section 14.1 – Added Labelling Requirements for the Host device
1.03	2017-04-23	Section 11.4: Updated ESD values Updated Reference document table Section 8.3 - Updated Ethernet control interface information Section 8.5.2 – Added note related to I2C Section 2.6.2 – Updated table 4 with B25 information. Section 14.1: Added LE910C1 NS Max antenna gain. Added LE910C1 NS FCC ID & IC number.
1.02	2017-04-03	Section 14.1 – updated column “Band” to “Frequency Band” in Wireless notice table Section 8.4.1 - Added note regarding DTR
1.01	2017-02-16	Adding Section 14: FCC/ISED Regulatory notices Changing Document History section from 14 to 15
1.0	2016-12-22	Section 1.5 - Updated “Related Documents” table Section 5.3.4 – Added Figure for SHDN_N power down timing Section 8.5.3 – Added clarification about VMMC Section 9.7 - Added GNSS characteristics
0.6	2016-12-07	Remove all China variant related information
0.5	2016-12-02	Added section 9.2 to better describe SW_RDY signal Minor modifications per typos and improved description Renaming of SHDN_N pin
0.4	2016-11-30	Updated band support table Updated WIFI application note doc info Added note related to future compatibility related to few pins Updated section 3.2 - Signals That Must Be Connected Updated pinout and pin description Updated pinout layout (Figure 2) Remove HW RESET description section Updated serial port 2 section Updated SPI port section Updated 1.8V pads pull info Updated AUX UART section Updated GPIO section

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Revision	Date	Changes
		Updated mechanical drawing (Cosmetic)
0.3	2016-11-13	Added information for GPIO usage as Interrupt Added clarification for AUX_UART location and backward compatibility
0.2	2016-09-05	Minor edits
0.1	2016-08-30	First Draft

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