EG800Q Series

Hardware Design

LTE Standard Module Series

Version: 1.1

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, CTVZN assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-08-05	Chan CHEN/ Gary WANG	Creation of the document
1.0	2023-02-07	Maffie ZHANG/ Emma WU	First official release
1.1	2023-06-29	Maffie ZHANG/ Emma WU/ Lem JIN/ Sean FANG	1. Added an applicable module EG800Q-NA. 2. Added the information about Wi-Fi scan function (Table 3 & Figure 1). 3. Updated the USB serial driver; Added the baud rates and functions of auxiliary UART; Updated the maximum category supported by LTE (Table 4). 4. Updated the DC characteristics of STATUS, NET_STATUS, USIM_DET, MAIN_DCD, MAIN_RI and MAIN_DTR; Added the DC characteristics of PSM_IND and PSM_INT (Table 6). 5. Added the characteristics of WAKEUP, AGPIO and AGPIOWU pins (Table 7). 6. Added the baud rates and functions of auxiliary UART; Added the notifications of the connection between the module' UART and the external device (Chapter 4.3). 7. Updated the note of the ADC design (Chapter 4.6). 8. Updated the power consumption (Chapter 6.3). 9. Updated the digital I/O characteristics (Chapter 6.4). 10. Added the mounting direction (Chapter 8.3.3).

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Introduction

This document defines EG800Q series module and describes its air interface and hardware interfaces, which are connected with your applications.

This document provides a quick insight into EG800Q series module interface specifications, electrical and mechanical details, as well as other related information of the module. Coupled with application notes and user guides, the document makes it easy to design and set up mobile applications with the module.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.

Product Overview

The module is an SMD type module engineered to meet the demanding requirements in M2M applications, such as asset management, commercial telematics, payment, RMAC (Remotely Managed Access Control), security and automation, smart metering and smart grid.

Table 2: Basic Information

EG800Q SERIES	
Packaging	LGA
Pin counts	109
Dimensions	(15.8 ±0.2) mm × (17.7 ±0.2) mm × (2.4 ±0.2) mm
Weight	approx. 2.0 g
Wireless network function	LTE

Frequency Bands and Functions

Table 3: Frequency Bands and Functions Supported by EG800Q Series

Mode	EG800Q-EU	EG800Q-NA
LTE-FDD	B1/B3/B5/B7/B8/B20/B28	B2/B4/B5/B12/B13/B66
Wi-Fi Scan（RX）	√	√

NOTE

√: Supported.

Key Features

Table 4: Key Features

Features	Details
Power Supply	● 3.3–4.3 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
USIM Interface	USIM card: 1.8 V, 3.0 V
PCM Interface*	● Digital audio interface: PCM interface ● Used for audio function with external Codec
I2C Interface	● One I2C interface ● Compliant with I2C bus specification
USB Interface	● Compliant with USB 2.0 specifications (only supports slave mode) ● Data rate: up to 480 Mbps ● Used for AT command communication, data transmission, software debugging, firmware upgrading and outputting logs ● USB Serial Driver: USB serial driver for Windows 7/8/8.1/10/11, Linux 2.6–5.18, Android 4.x–13.x
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate: 115200 bps by default ● RTS and CTS hardware flow control **Debug UART:** ● Used for outputting partial logs ● Baud rate: 115200 bps and 3000000 bps **AUX UART:** ● Used for AT command communication and data transmission ● Baud rate: 115200 bps by default
Network Indication	NET_STATUS to indicate network connectivity status
AT Commands	● Compliant with *3GPP TS 27.007, 3GPP TS 27.005* ● Compliant with CTVZN enhanced AT commands
Antenna Interface	● Main antenna interface (ANT_MAIN) ● 50 Ω impedance
LTE Features	● 3GPP Rel-14 FDD ● Max. LTE category: Cat 1 bis ● 1.4/3/5/10/15/20 MHz RF bandwidth

	● UL modulation: QPSK, 16QAM ● DL modulation: QPSK, 16QAM and 64QAM ● LTE-FDD: Max. 10 Mbps (DL)/ 5 Mbps (UL)
Internet Protocol Features	● TCP/UDP/NTP/NITZ/FTP/HTTP/PING/HTTPS/FTPS/SSL/MQTT/CMUX/PPP/FILE/MMS*/SMTP/SMTPS protocols ● PAP and CHAP for PPP connections
Temperature Range	● Operating temperature range [1]: -35 °C to +75 °C ● Extended temperature range [2]: -40 °C to +85 °C ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	Via USB interface or DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

[1] Within the operating temperature range, the module meets 3GPP specifications.
[2] Within the extended temperature range, the module retains the ability to establish and maintain functions such as SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

Pin Assignment

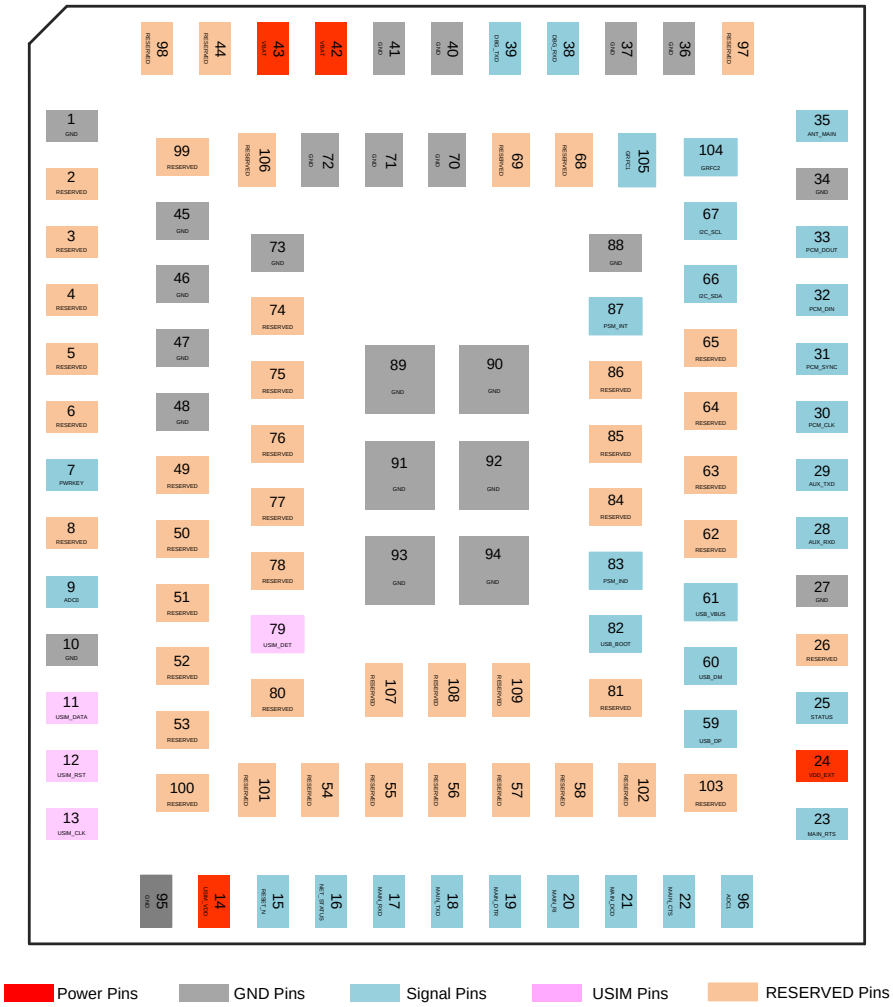


Figure 1: Pin Assignment (Top View)

NOTE

1. Do the following only if the module should be put into emergency download mode: pull USB_BOOT (pin 82) to low level before the module successfully starts up.
2. In sleep mode, some pins of the main UART interface (pins 17, 18, 22, 23), auxiliary UART interface (pins 28, 29), debug UART interface (pins 38, 39), USB_BOOT (pin 82), PCM* and I2C interfaces (pins 30–33, 66, 67), GRFC interface (pins 104, 105) are powered down, and the high-level pins will output periodic pulses with the paging cycle. The driving capacity, status indication and data transmission functions of these pins will be invalid. Take this into consideration when designing circuits.
3. Keep all RESERVED pins and unused pins unconnected.

Pin Description

The following table shows the pin descriptions.

Table 5: I/O Parameters Definition

Type	Description
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PI	Power Input
PO	Power Output

DC characteristics include power domain, current rating, etc.

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	42, 43	PI	Power supply for the module	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 2 A. It is recommended to add an external TVS. A test point is recommended to be reserved.
VDD_EXT	24	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	A test point is recommended to be reserved.
GND	1, 10, 27, 34, 36, 37, 40, 41, 45–48, 70–73, 88–95				
Turn On/Off					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	7	DI	Turn on/off the module	V_{IL}max = 0.5 V	Active low. A test point is recommended to be reserved.
RESET_N	15	DI	Reset the module		Active low. A test point is recommended to be reserved if unused.
Indication Signals					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	25	DO	Indicate the module's operation status	V_{OH}min = 1.44 V V_{OL}max = 0.27 V	If unused, keep them open.
NET_STATUS	16	DO	Indicate the module's network activity status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	61	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	A test point must be reserved.
USB_DP	59	AIO	USB differential data (+)		USB 2.0 compliant. Requires differential impedance of 90 Ω. Test points must be reserved.
USB_DM	60	AIO	USB differential data (-)		
USIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_VDD	14	PO	USIM card power supply	$I_O$max = 50 mA **Low voltage:** Vmax = 1.85 V Vmin = 1.75 V **High voltage:** Vmax = 3.05 V Vmin = 2.95 V	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.

USIM_DATA	11	DIO	USIM card data	USIM_VDD	
USIM_CLK	13	DO	USIM card clock		
USIM_RST	12	DO	USIM card reset		
USIM_DET	79	DI	USIM card hot-plug detect	V_{IH}min = 1.33 V V_{IL}max = 0.42 V	If unused, keep it open.
Auxiliary UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
AUX_TXD	29	DO	Auxiliary UART transmit	VDD_EXT	If unused, keep them open.
AUX_RXD	28	DI	Auxiliary UART receive		
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_CTS	22	DO	Clear to send signal from the module	VDD_EXT	Connect to MCU's CTS. If unused, keep it open.
MAIN_RTS	23	DI	Request to send signal to the module		Connect to MCU's RTS. If unused, keep it open.
MAIN_RXD	17	DI	Main UART receive		If unused, keep them open.
MAIN_TXD	18	DO	Main UART transmit		
MAIN_DCD	21	DO	Main UART data carrier detect	V_{OH}min = 1.44 V V_{OL}max = 0.27 V	
MAIN_RI	20	DO	Main UART ring indication		
MAIN_DTR	19	DI	Main UART data terminal ready	V_{IH}min = 1.33 V V_{IL}max = 0.42 V	
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	38	DI	Debug UART receive	VDD_EXT	Test points must be reserved.
DBG_TXD	39	DO	Debug UART transmit		
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

I2C_SCL	67	DO	I2C serial clock	VDD_EXT	External pull-up resistor is required. If unused, keep them open.
I2C_SDA	66	DIO	I2C serial data		
PCM Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	31	DO	PCM data frame sync	VDD_EXT	If unused, keep them open.
PCM_CLK	30	DO	PCM clock		
PCM_DIN	32	DI	PCM data input		
PCM_DOUT	33	DO	PCM data output		
RF Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN [3]	35	AIO	Main antenna interface		50 Ω impedance.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	9	AI	General-purpose ADC interface	Voltage range: 0–1.2 V	If unused, keep them open.
ADC1	96	AI	General-purpose ADC interface		
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	82	DI	Force the module into emergency download mode	VDD_EXT	Active low. A test point must be reserved.
PSM_IND	83	DO	Indicate the module's power saving mode	V_{OH}min = 1.44 V V_{OL}max = 0.27 V	If unused, keep it open.
PSM_INT	87	DI	External interrupt; wake up the module from power saving mode	V_{IH}min = 1.33 V V_{IL}max = 0.42 V	Externally pulling up this pin can make the module exit power saving mode. If unused, keep it open.

[3] ANT_MAIN only supports passive antennas.

GRFC2	104	DO	Generic RF controller	If unused, keep them open.
GRFC1	105	DO	Generic RF controller	
RESERVED	2–6, 8, 26, 44, 49–58, 62–65, 68, 69, 74–78, 80, 81, 84–86, 97–103, 106-109			Keep these pins open.

Some pins of the module are divided into three types: WAKEUP, AGPIO, and AGPIOWU pins. The pin characteristics of these three types are as follows.

Table 7: WAKEUP & AGPIO & AGPIOWU Pin Characteristics

WAKEUP Pins	Characteristics
● PSM_INT ● USB_VBUS ● USIM_DET	● Support wake-up interrupt function. ● High-level voltage: about 1.2 V for PSM_INT and USIM_DET. ● The state of the pins will not be affected even if the module enters the sleep mode.
AGPIO Pins	**Characteristics**
● MAIN_DCD ● PSM_IND ● STATUS ● NET_STATUS ● MAIN_RI	● The state of the pins will not be affected even if the module enters the sleep mode.
AGPIOWU Pin	**Characteristics**
● MAIN_DTR	● Supports wake-up interrupt function. ● High-level voltage: about 1.2 V. ● The state of the pins will not be affected even if the module enters the sleep mode.

Operating Characteristics

Operating Modes

Table 8: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module is registered on the network but has no data interaction with the network.
	Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	● Executing **AT+CFUN =0** sets the module to minimum functionality mode. ● Both RF function and USIM card are invalid.	
Airplane Mode	● Executing **AT+CFUN =4** sets the module to airplane mode. ● RF function is invalid.	
Sleep Mode	Power consumption of the module is reduced to the minimal level, but the module can still receive paging, SMS and TCP/UDP data from the network.	
Power Down Mode	The VBAT power supply for the module remains applied, and software is not executed.	

Sleep Mode

The power consumption of the module is reduced to a minimum level during sleep mode.

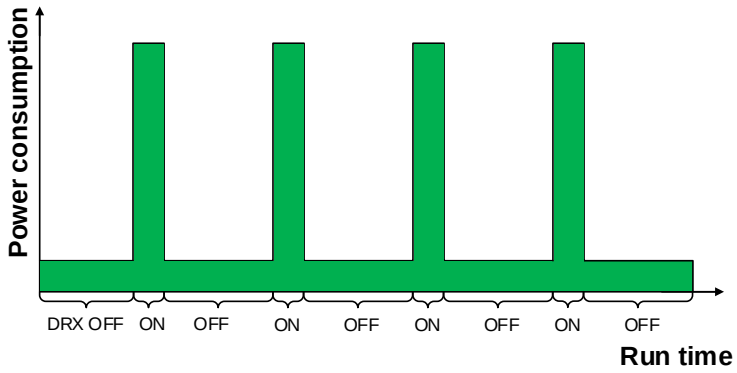


Figure 2: Power Consumption During Sleep Mode

NOTE

1. The DRX period value is sent by the base station over the wireless network.
2. In sleep mode, some pins of the main UART interface (pins 17, 18, 22, 23), auxiliary UART interface (pins 28, 29), debug UART interface (pins 38, 39), USB_BOOT (pin 82), PCM* and I2C interfaces (pins 30–33, 66, 67), GRFC interface (pins 104, 105) are powered down, and the high-level pins will output periodic pulses with the paging cycle. The driving capacity, status indication and data transmission functions of these pins will be invalid. Take this into consideration when designing circuits.

UART Application Scenario

If the MCU communicates with the module via UART interface, the following two preconditions should be met to make the module enter sleep mode.

- Execute **AT+QSCLK=1**.
- Ensure MAIN_DTR is held high or is kept unconnected.

The figure illustrates the connection between the module and the MCU.

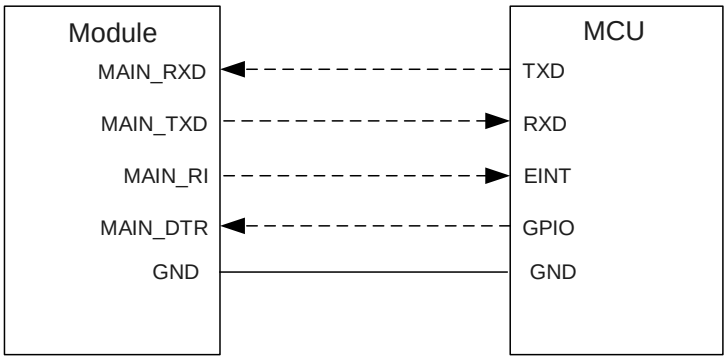


Figure 3: Sleep Mode Application via UART

- Driving the MAIN_DTR low will wake up the module.
- When the module has a URC to report, MAIN_RI signal will wake up the MCU. See ***Chapter 0*** for details about MAIN_RI behavior.

USB Application Scenario

For the two situations below, three preconditions must be met to make the module enter sleep mode.

- Execute **AT+QSCLK=1**.
- Ensure the MAIN_DTR is held high or is kept unconnected.
- Ensure the host's USB bus, which is connected with the module's USB interface, enters suspend state.

USB Application with USB Suspend/Resume & Remote Wakeup Function*

The host supports USB suspend, resume and remote wakeup function. The figure illustrates the connection between the module and the host.

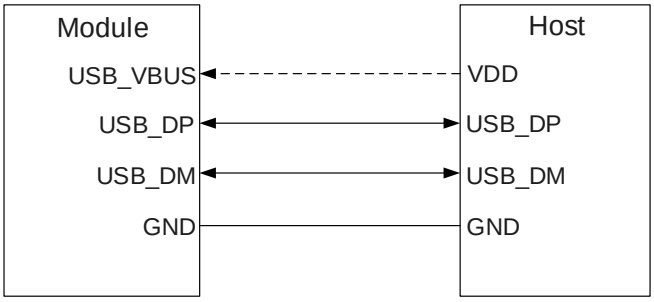


Figure 4: Sleep Mode Application with USB Remote Wakeup

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will send remote wake-up signals through USB bus to wake up the host.

USB Application with USB Suspend/Resume and MAIN_RI Function

If the host supports USB suspend and resume, but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host. The following figure illustrates the connection between the module and the host.

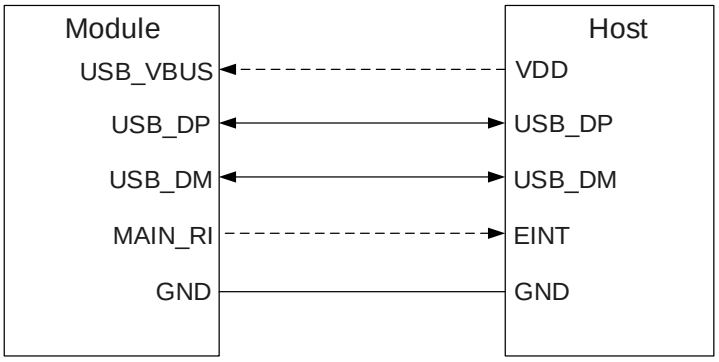


Figure 5: Sleep Mode Application with MAIN_RI

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, MAIN_RI signal will wake up the host. See ***Chapter 0*** for details about MAIN_RI behavior.

USB Application without USB Suspend Function

If the host does not support USB suspend function, the following three preconditions should be met to make the module enter sleep mode.

- Execute **AT+QSCLK=1**.
- Ensure the MAIN_DTR is held high or is kept unconnected.
- Disconnect the USB_VBUS power supply.

If the host does not support USB suspend function, USB_VBUS should be disconnected through an external control circuit to make the module enter sleep mode. The figure illustrates the connection between the module and the host.

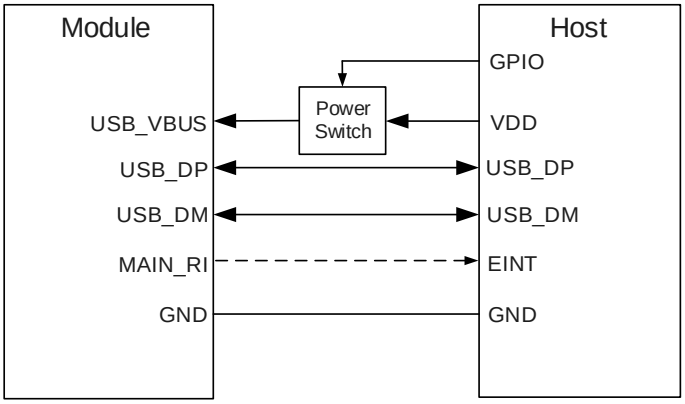


Figure 6: Sleep Mode Application without USB Suspend

Restore the supply power of USB_VBUS will wake up the module.

NOTE

Pay attention to the level match shown in dotted line between the module and the host.

Airplane Mode

When the module enters airplane mode, the RF function is disabled and all related AT commands cannot

be executed. This mode can be set as follows.

Software:

AT+CFUN=<fun> allows you to choose the functionality level through setting **<fun>** as **0**, **1** or **4**.

- **AT+CFUN=0:** Minimum functionality mode. (Both RF and USIM functions are disabled)
- **AT+CFUN=1:** Full functionality mode. (Default).
- **AT+CFUN=4:** Airplane mode. (RF function is disabled)

Power Supply

Power Supply Pins

The module has two VBAT pins for connecting to external power supply.

Table 9: Pin Definition of Power Supply

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT	42, 43	PI	Power supply for the module	3.3	3.8	4.3	V
GND	1, 10, 27, 34, 36, 37, 40, 41, 45–48, 70–73, 88–95						

Power Supply Reference Design

Power supply design is essential for module performance. Module power source should be able to provide at least 2 A current. If the voltage difference between input voltage and the supply voltage is small, it is suggested to use an LDO; if the voltage difference is big, a buck converter is recommended.

A reference design for +5 V input power source is illustrated in the following figure (Please adjust the parameters in accordance with the actual situation).

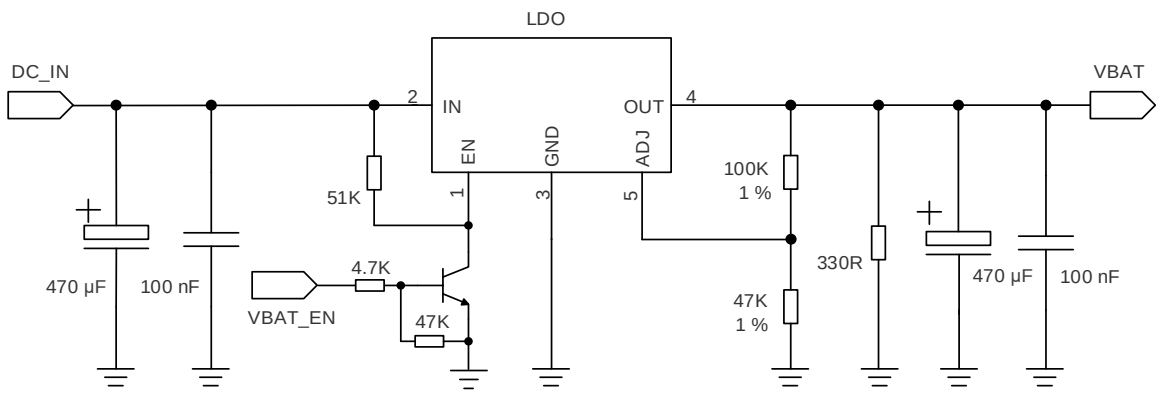


Figure 7: Power Supply Reference Design

Voltage Stability Requirements

The power supply range of the module is 3.3–4.3 V. Make sure the input voltage never drops below 3.3 V.

To decrease the voltage drop, use a bypass capacitor of about 100 μF with low ESR (ESR = 0.7 Ω). A multi-layer ceramic chip (MLCC) capacitor array with ultra-low ESR is recommended. Use three ceramic capacitors (100 nF, 10 pF and 33 pF) to compose the array and place them close to VBAT pins. If the module is powered from a single voltage source, then the power supply distribution path can be traced with a star topology structure when connect to the module. The width of VBAT trace should be at least 2 mm. In principle, the longer the VBAT trace is, the wider it should be.

To avoid power ripples and surges and ensure the stability of the power supply, add a TVS with V_{RWM} = 4.7 V, low clamping voltage and high reverse peak pulse current Ipp at the front end of the power supply. Reference design is shown below.

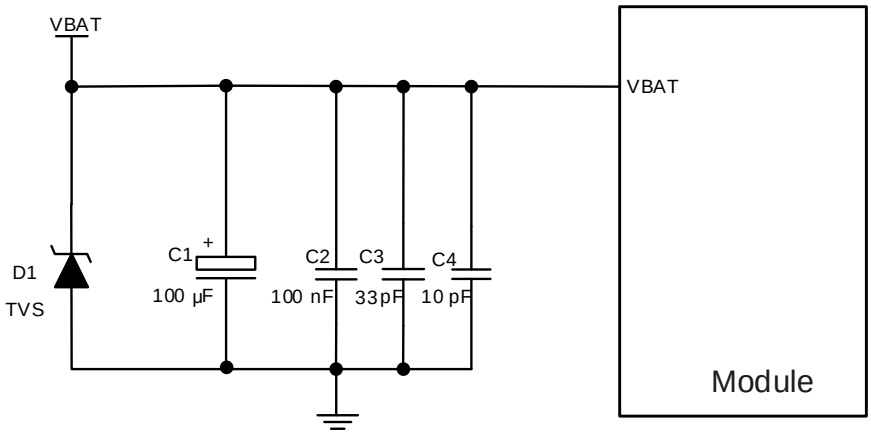


Figure 8: Power Supply Reference Design

Turn On

Turn On with PWRKEY

Table 10: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	7	DI	Turn on/off the module	Active low. A test point is recommended to be reserved.

When the module is in power-down mode, it can be turned on by driving the PWRKEY low for at least 500 ms. It is recommended to use an open collector driver to control the PWRKEY.

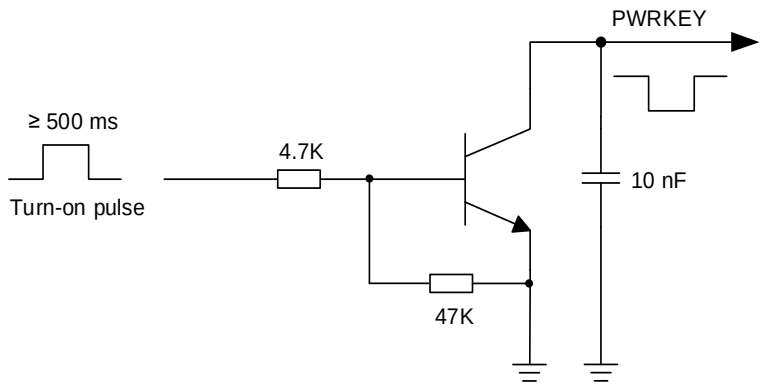


Figure 9: Reference Design of Turning on the Module with Driving Circuit

The module can also be turned on by pressing the PWRKEY button. A TVS diode should be placed near the button for protection against ESD.

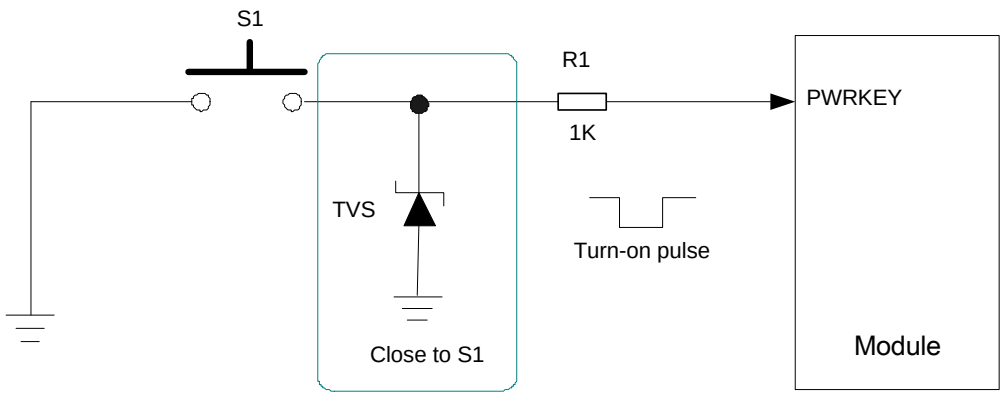


Figure 10: Reference Design of Turning on Module with Keystroke

The power-up timing is illustrated in the following figure.

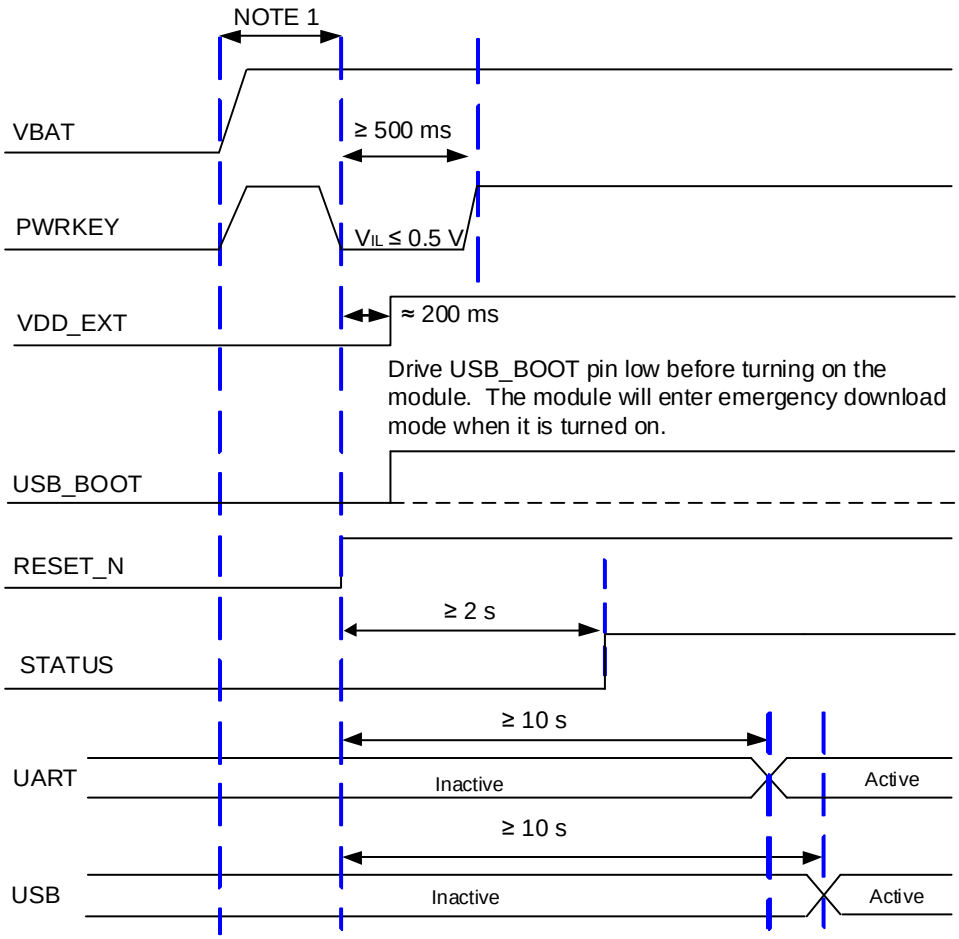


Figure 11: Power-up Timing

NOTE

1. Ensure a stable VBAT for at least 30 ms before driving the PWRKEY low.
2. If the module needs to turn on automatically but does not need turn-off function, you can drive PWRKEY pin low by connecting it directly to the ground with a recommended 4.7 kΩ resistor or by using a GPIO to drive PWRKEY low before the module turns on (PWRKEY needs to remain at low level after the module is turned on).

Turn Off

The following procedures can be used to turn off the module normally.

Turn Off with PWRKEY

The module will execute turn-off procedure if you drive the PWRKEY pin low for at least 650 ms and then

release it.

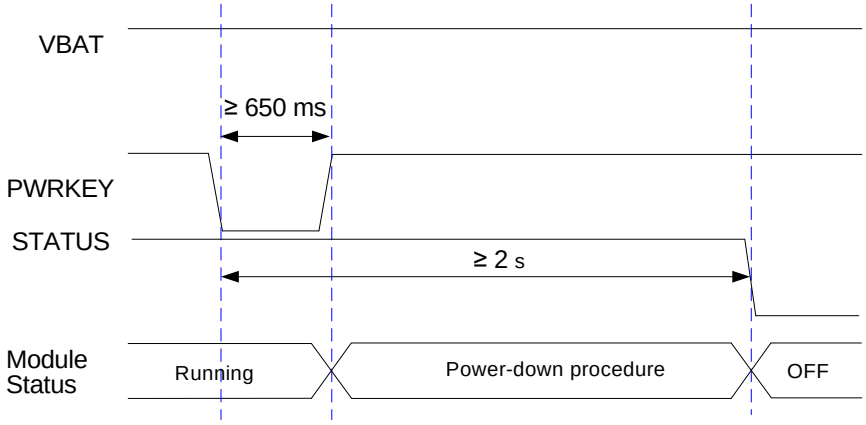


Figure 12: Timing of Turn-off with PWRKEY

Turn Off with AT Command

You can execute **AT+QPOWD**, to turn off the module. The timing and the effect are similar to those when using the PWRKEY pin to turn the module off.

NOTE

1. If the module is turned on by connecting the PWRKEY to ground for a long time, **AT+QPOWD** cannot be used to turn off the module.
2. When turning off the module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on automatically again after successful turn-off.

Reset

Pulling down PWRKEY when RESET_N is at low level can reset the module. The RESET_N signal is sensitive to interference. Therefore, it is recommended to route the trace as short as possible and surround it with ground.

Table 11: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	15	DI	Reset the	Active low.

	module	A test point is recommended to be reserved if unused.

You can use an open collector driver to control RESET_N and PWRKEY pins.

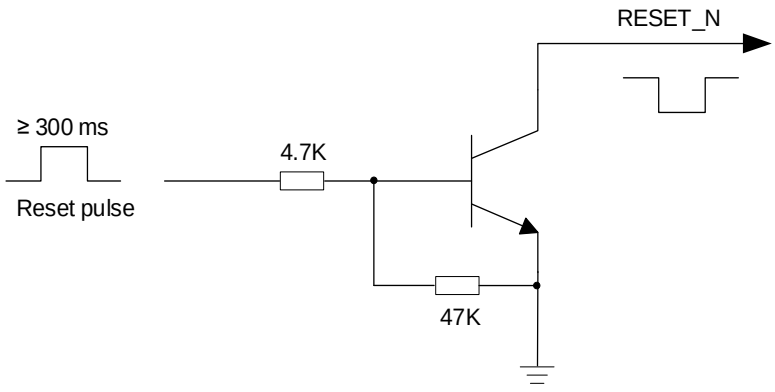


Figure 13: Reference Design of RESET_N with Driving Circuit

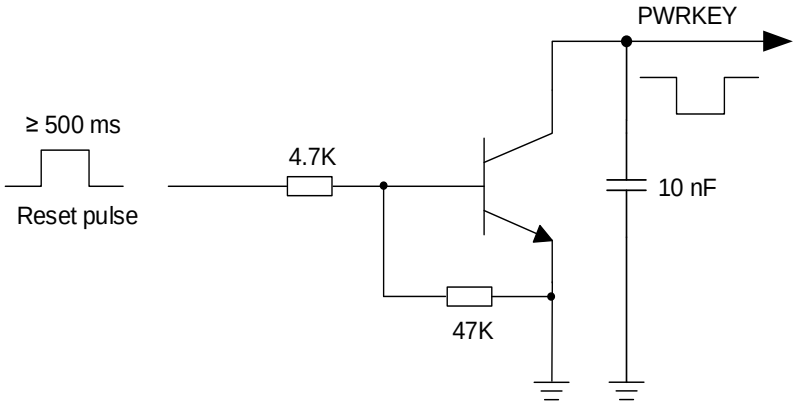


Figure 14: Reference Design of PWRKEY with Driving Circuit

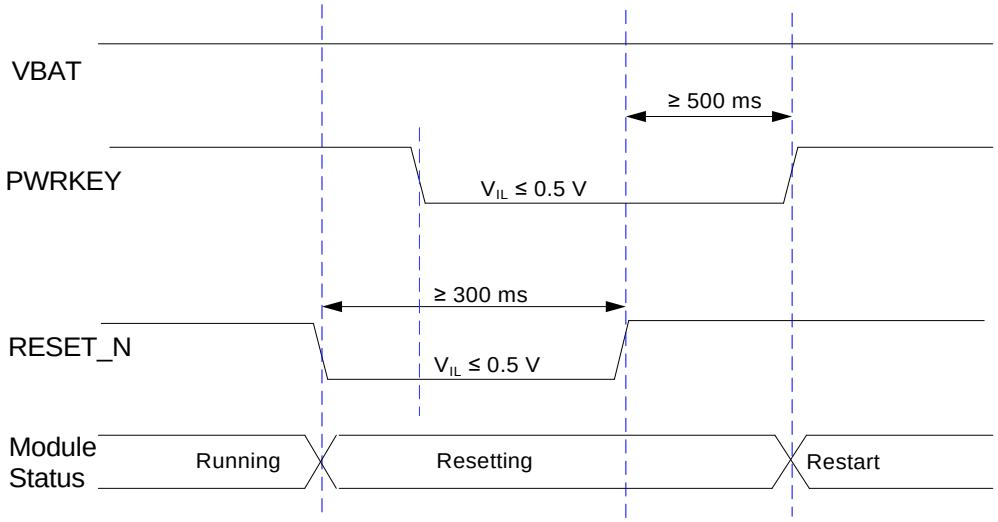


Figure 15: Reset Timing

NOTE

1. Pull down PWRKEY when RESET_N is at low level.
2. Ensure that the capacitances connected to PWRKEY and RESET_N do not exceed 10 nF.
3. When the PWRKEY is normally grounded, the module can be reset by pulling RESET_N to low level.

Application Interfaces

USB Interface

The module has one USB interface, which complies with the USB 2.0 specifications, and supports high speed (480 Mbps) and full speed (12 Mbps) on USB 2.0. The module only supports USB slave mode. The USB interface can be used for AT command communication, data transmission, software debugging, firmware upgrading and outputting logs.

Table 12: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	61	AI	USB connection detect	A test point must be reserved.
USB_DP	59	AIO	USB differential data (+)	USB 2.0 compliant. Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	60	AIO	USB differential data (-)	

It is recommended to use USB interface for firmware upgrading. It is necessary to reserve test points so that logs can be obtained and customers' issues can be found.

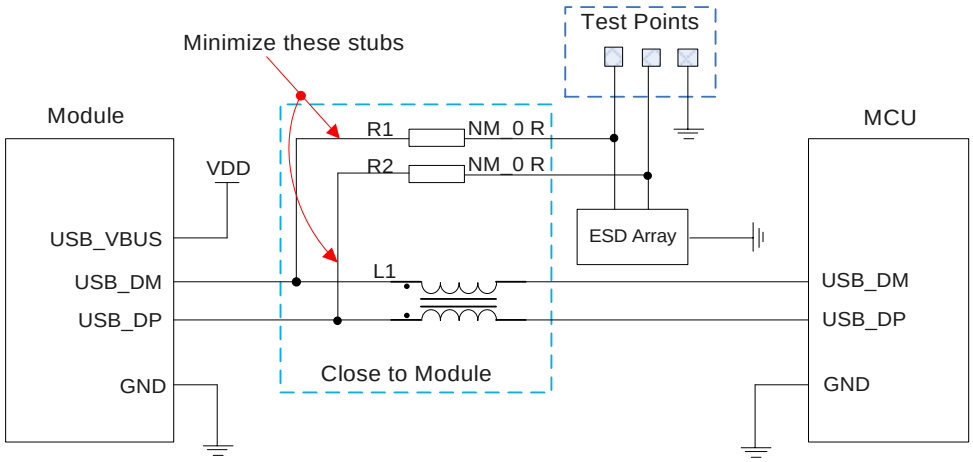


Figure 16: Reference Circuit of USB Interface

It is recommended to add a common-mode choke L1 in series between the module and MCU to

suppress EMI spurious transmission. In addition, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points for debugging. These resistors are not mounted by default. To ensure USB data transmission integrity, L1, R1 and R2 must be placed close to the module, and resistors R1 and R2 should be placed close to each other. Extra trace stubs must be as short as possible.

To ensure performance, you should follow the following principles when designing a USB interface:

- Route the USB signal traces as differential pairs surrounded by ground. The impedance of USB 2.0 differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in an inner layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Pay attention to the impact caused by stray capacitance of the ESD protection component on USB data lines. Typically, the stray capacitance should be less than 2 pF.
- Place ESD protection components as close to the USB interface as possible.

For more details about the USB specifications, visit http://www.usb.org/home.

USB_BOOT

The module has a USB_BOOT pin. If you drive USB_BOOT to the ground before turning on the module, the module will enter emergency download mode when turned on. In this mode, the module supports firmware upgrade over USB 2.0 interface.

Table 13: Pin Definition of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	82	DI	Force the module into emergency download mode	Active low. A test point must be reserved.

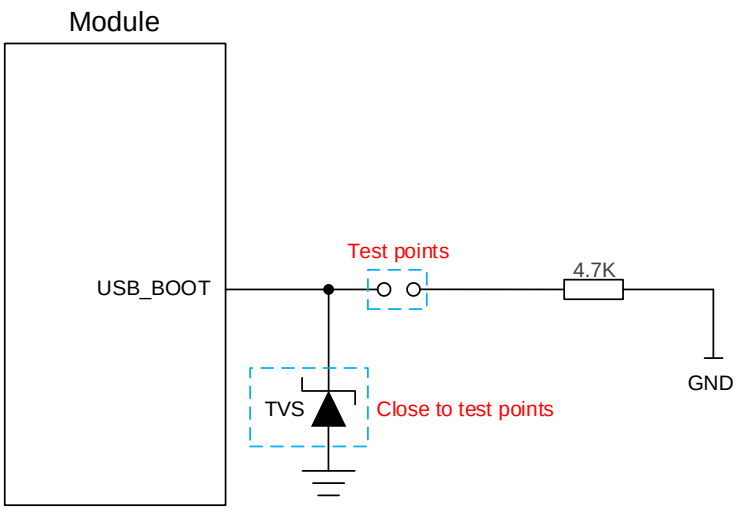


Figure 17: Reference Design of USB_BOOT Interface

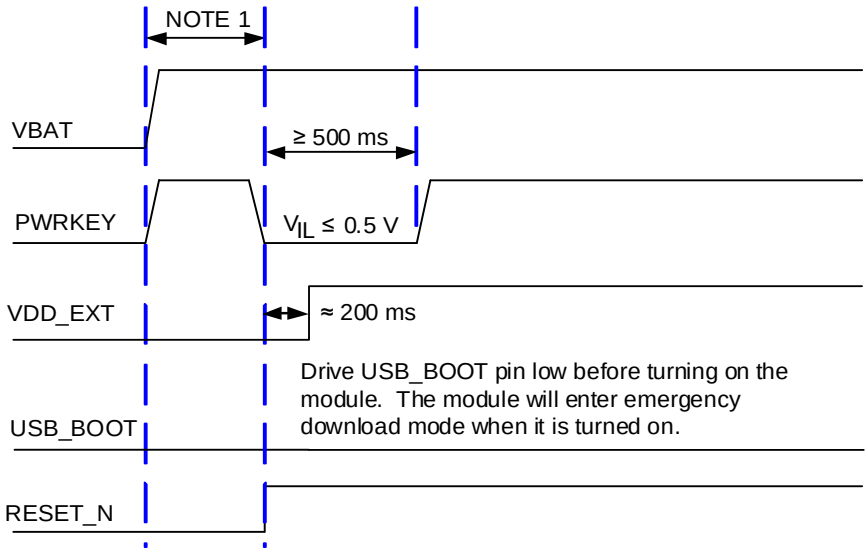


Figure 18: Timing of Entering Emergency Download Mode

NOTE

1. Ensure a stable VBAT for at least 30 ms before driving the PWRKEY low.
2. When using MCU to put the module to emergency download mode, follow the above timing. If you need to manually force the module to enter emergency download mode, connect the test points as shown in ***Figure 17***.

UART Interfaces

The module has 3 UART interfaces.

Table 14: UART Information

UART Types	Supported Baud Rates (bps)	Default Baud Rates (bps)	Functions
Main UART interface	4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600	115200	● AT command communication and data transmission ● RTS and CTS hardware flow control
Debug UART interface	115200, 3000000	115200	● Partial log output
Auxiliary UART interface	115200	115200	● AT command communication and data transmission

Table 15: Pin Definition of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	22	DO	Clear to send signal from the module	Connect to MCU's CTS. If unused, keep it open.
MAIN_RTS	23	DI	Request to send signal to the module	Connect to MCU's RTS. If unused, keep it open.
MAIN_RXD	17	DI	Main UART receive	If unused, keep them open.
MAIN_DCD	21	DO	Main UART data carrier detect	
MAIN_TXD	18	DO	Main UART transmit	
MAIN_RI	20	DO	Main UART ring indication	
MAIN_DTR	19	DI	Main UART data terminal ready	
AUX_TXD	29	DO	Auxiliary UART transmit.	
AUX_RXD	28	DI	Auxiliary UART receive.	
DBG_RXD	38	DI	Debug UART transmit	Test points must be reserved.
DBG_TXD	39	DO	Debug UART receive	

The module has 1.8 V UART interfaces. If the level of the external device is 1.8 V, and the MAIN_TXD of the module is connected to the RXD of the external device, the MAIN_TXD must be connected to a 10 kΩ resistor and pulled up to 1.8 V to prevent the peripheral from receiving error messages when the module is in sleep mode. A voltage-level translator should be used if the application features a 3.3 V UART interface.

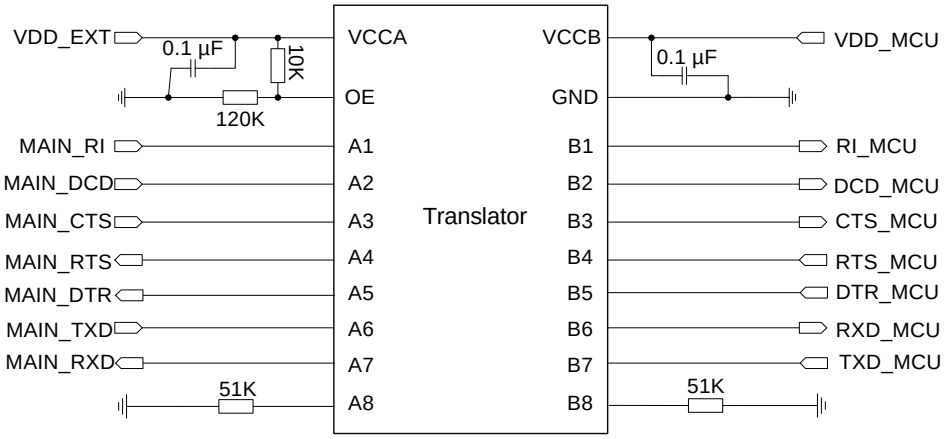


Figure 19: Reference Design of UART with Voltage-Level Translator

Another example of level-shifting circuit is shown below. For the design of input/output circuits in dotted lines, see the ones in solid lines, but pay attention to the direction of the connection.

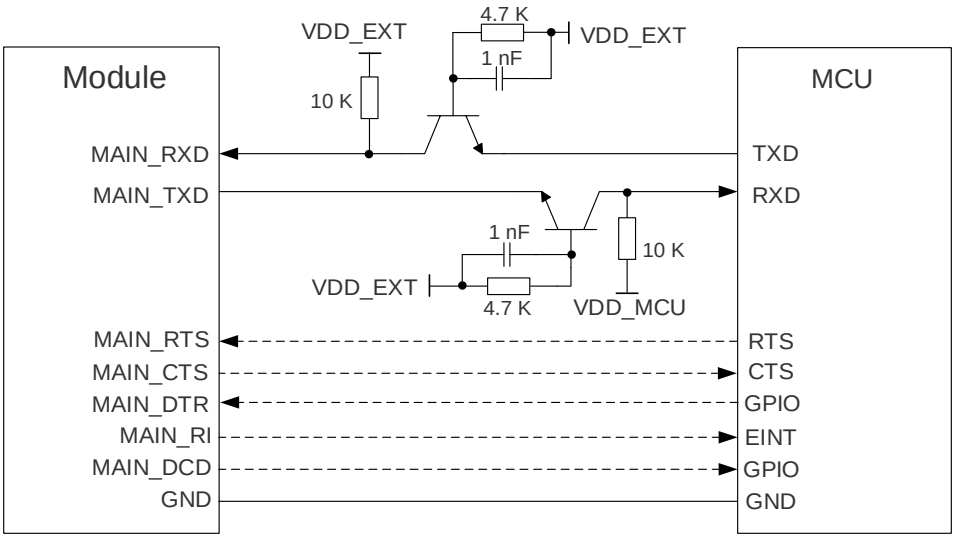


Figure 20: Reference Design of UART with Transistor Level-Shifting Circuit

NOTE

1. Transistor level-shifting circuit above is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to MCU's CTS, and the module's RTS is connected to MCU's RTS.

USIM Interface

The USIM interface meets ETSI and IMT-2000 requirements. Both the 1.8 V and the 3.0 V USIM cards are supported.

Table 16: Pin Definition of USIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	14	PO	USIM card power supply	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM_DATA	11	DIO	USIM card data	
USIM_CLK	13	DO	USIM card clock	
USIM_RST	12	DO	USIM card reset	
USIM_DET	79	DI	USIM card hot-plug detect	If unused, keep it open.

The module supports USIM card hot-plug detection via the USIM_DET pin, and both high and low level detection are supported.

A reference design of USIM card interface with an 8-pin USIM card connector is illustrated in the following figure.

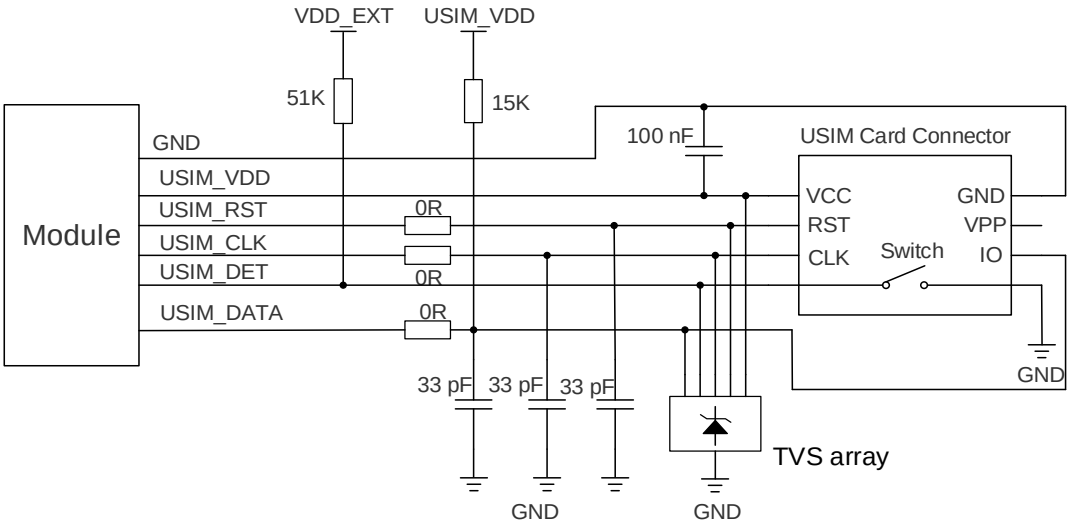


Figure 21: Reference Design of USIM Interface with an 8-Pin USIM Card Connector

If USIM card detection function is not needed, keep USIM_DET disconnected. A reference design of USIM interface with a 6-pin USIM card connector is illustrated in the following figure.

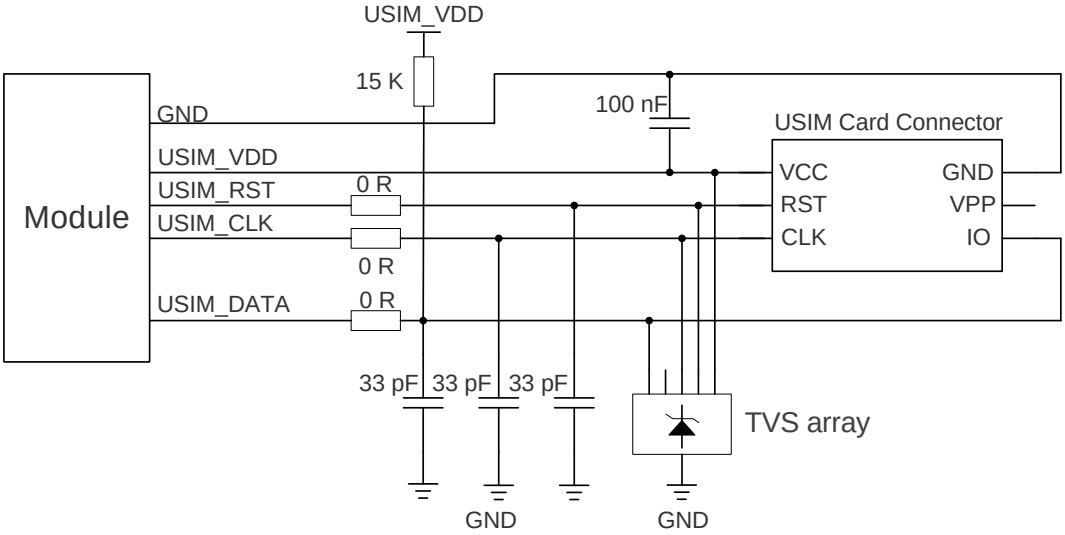


Figure 22: Reference Design of USIM Interface with a 6-Pin USIM Card Connector

To enhance USIM card reliability and availability in applications, follow the principles below in the USIM circuit design:

- Place the USIM card connector close to the module. Keep the trace length as short as possible, at most 200 mm.
- Keep USIM card signal traces away from RF and power supply traces.
- Make sure that the bypass capacitor between USIM_VDD and GND does not exceed 1 μF, and should be placed close to the USIM card connector.

- To avoid cross talk between USIM_DATA and USIM_CLK, keep the traces away from each other and shield them by surrounding them with ground.
- To improve ESD protection, it is recommended to add a TVS array on USIM pins. The parasitic capacitance of the TVS array should not exceed 15 pF. Add 0 Ω resistors in series between the module and the USIM card connector to facilitate debugging. The 33 pF capacitors on USIM_DATA, USIM_CLK and USIM_RST are used for filtering out RF interference. In addition, keep the USIM peripheral circuit close to the USIM card connector.
- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability when long layout trace and sensitive occasions are applied, and should be placed close to the USIM card connector.

PCM* and I2C Interfaces

The module has one Pulse Code Modulation (PCM) digital interface and one I2C interface.

Table 17: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	31	DO	PCM data frame sync	If unused, keep them open.
PCM_CLK	30	DO	PCM clock	
PCM_DIN	32	DI	PCM data input	
PCM_DOUT	33	DO	PCM data output	
I2C_SCL	67	DO	I2C serial clock	External pull-up resistor is required. If unused, keep them open.
I2C_SDA	66	DIO	I2C serial data	

A reference design of PCM and I2C interfaces with external Codec IC is illustrated in the following figure.

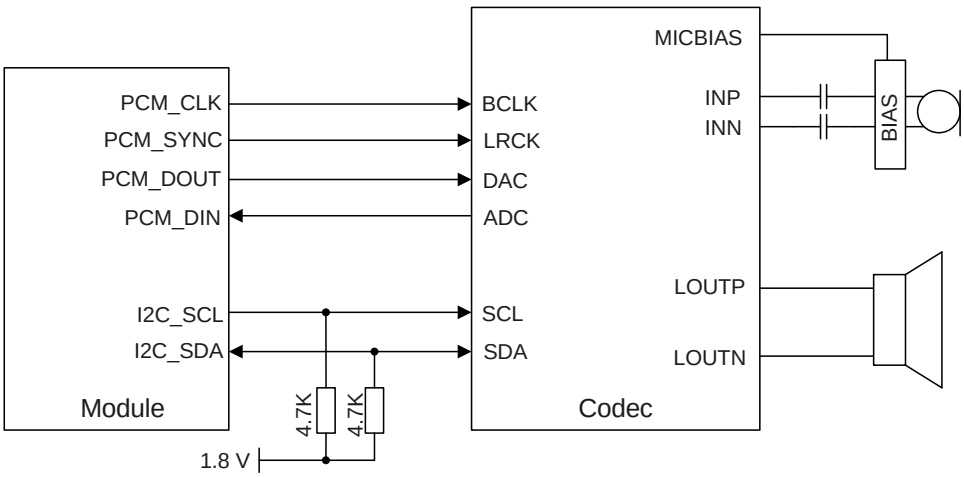


Figure 23: Reference Circuit of PCM and I2C Interfaces

NOTE

1. It is recommended to reserve RC circuits (R = 22 Ω, C = 22 pF) on the PCM signal traces, especially on the PCM_CLK pin.
2. The module can only be used as a master device in applications related to both the PCM interface and the I2C interface.

ADC Interfaces

The module features two Analog-to-Digital Converter (ADC) interfaces. To improve ADC accuracy, the trace of ADC interfaces should be surrounded by ground.

Table 18: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	9	AI	General-purpose ADC interface	If unused, keep them open.
ADC1	96	AI	General-purpose ADC interface	

With **AT+QADC=<port>**, you can:

- **AT+QADC=0**: read the voltage value on ADC0
- **AT+QADC=1**: read the voltage value on ADC1

Table 19: ADC Interface Features

Name	Min.	Typ.	Max.	Unit
ADC voltage range	0	-	1.2	V
ADC input resistance	0.26	-	0.75	MΩ
ADC resolution	-	12	-	bits

NOTE

If the acquisition voltage is greater than or equal to 1.2 V, it is recommended to use resistor divider circuit for ADC interface application. Resistance of the resistor divider should not exceed 100 kΩ, or the measurement accuracy of ADC would be significantly reduced. It is recommended to reserve a 100 nF capacitor for the design.

PSM_IND & PSM_INT

The module supports power saving mode (PSM).

Table 20: Pin Definition of PSM_IND and PSM_INT

Pin Name	Pin No.	I/O	Description	Comment
PSM_IND	83	DO	Indicate the module's power saving mode	If unused, keep it open.
PSM_INT	87	DI	External interrupt; wake up the module from power saving mode	Externally pulling up this pin can make the module exit power saving mode. If unused, keep it open.

Indication Signals

Table 21: Pin Definition of Indication Signals

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	16	DO	Indicate the module's network activity status	If unused, keep them open.
STATUS	25	DO	Indicate the module's operation status	

Network Status Indication

The NET_STATUS pin indicates the module's network activity status, and can be used to drive network status indication LEDs.

Table 22: Network Connection Status/Activity Indicated by NET_STATUS Pin

Pin Name	Status	Description
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Ongoing data transmission

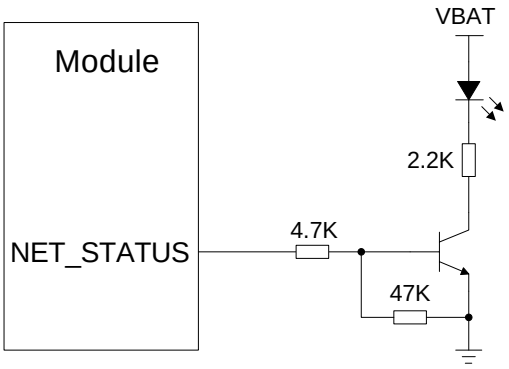


Figure 24: Reference Design of NET_STATUS

STATUS

The STATUS pin is used to indicate the module's operation status. It outputs high level when the module is turned on successfully.

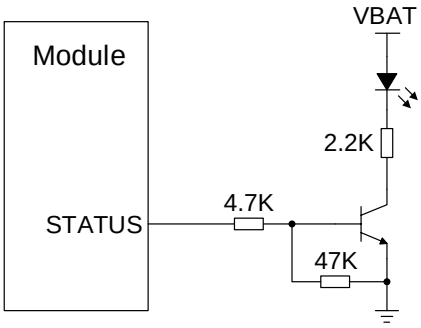


Figure 25: Reference Design of STATUS

MAIN_RI

AT+QCFG= "risignaltype","physical" can be used to configure MAIN_RI as URC indication pin. An URC will trigger MAIN_RI regardless of the URC output port. For more details about **AT+QCFG.**

NOTE

The **AT+QURCCFG** allows you to configure the main UART, USB AT port or USB modem port as the URC output port. The USB AT port is the URC output port by default.

MAIN_RI can be configured flexibly. However, its default behaviors are:

Table 23: Behaviors of MAIN_RI

Module Status	MAIN_RI Level Status
Idle	High
When a new URC information returns	MAIN_RI outputs low level that lasts at least 120 ms. Once the module outputs the data, the level status will become high.

The MAIN_RI can be configured as URC indication pin via **AT+QCFG="urc/ri/ring"**.

RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

Cellular Network

Antenna Interface & Frequency Bands

Table 24: Pin Definition of Cellular Network Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN [4]	35	AIO	Main antenna interface	50 Ω impedance.

Table 25: Operating Frequency

Operating Frequency	Transmit (MHz)	Receive (MHz)
B1	1920–1980	2110–2170
B2	1850–1910	1930–1990
B3	1710–1785	1805–1880
B4	1710–1755	2110–2155
B5	824–849	869–894
B7	2500–2570	2620–2690
B8	880–915	925–960
B12	699–716	729–746

[4] ANT_MAIN supports only passive antenna.

B13	777–787	746–756
B20	832–862	791–821
B28	703–748	758–803
B66	1710–1780	2110–2180

Rx Sensitivity

Table 26: EG800Q-EU Conducted RF Receiver Sensitivity

Frequency Bands	Receiver Sensitivity (Typ.)	3GPP (SIMO)
	Primary	
LTE-FDD B1 (10 MHz)	-99.5 dBm	-96.3 dBm
LTE-FDD B3 (10 MHz)	-99.0 dBm	-93.3 dBm
LTE-FDD B5 (10 MHz)	-99.5 dBm	-94.3 dBm
LTE-FDD B7 (10 MHz)	-97.1 dBm	-94.3 dBm
LTE-FDD B8 (10 MHz)	-99.5 dBm	-93.3 dBm
LTE-FDD B20 (10 MHz)	-99.5 dBm	-93.3 dBm
LTE-FDD B28 (10 MHz)	-98.8 dBm	-94.8 dBm

Table 27:EG800Q-NA Conducted RF Receiver Sensitivity

Frequency Bands	Receiver Sensitivity (Typ.)	3GPP (SIMO)
	Primary	
LTE-FDD B2 (10 MHz)	-98.9 dBm	-94.3 dBm
LTE-FDD B4 (10 MHz)	-98.8 dBm	-96.3 dBm
LTE-FDD B5 (10 MHz)	-99.5 dBm	-94.3 dBm

LTE-FDD B12 (10 MHz)	-99.8 dBm	-93.3 dBm
LTE-FDD B13 (10 MHz)	-98.8 dBm	-93.3 dBm
LTE-FDD B66 (10 MHz)	-99.0 dBm	-95.8 dBm

Reference Design

The module has one RF antenna interface for antenna connection. It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (C1, R1, and C2) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

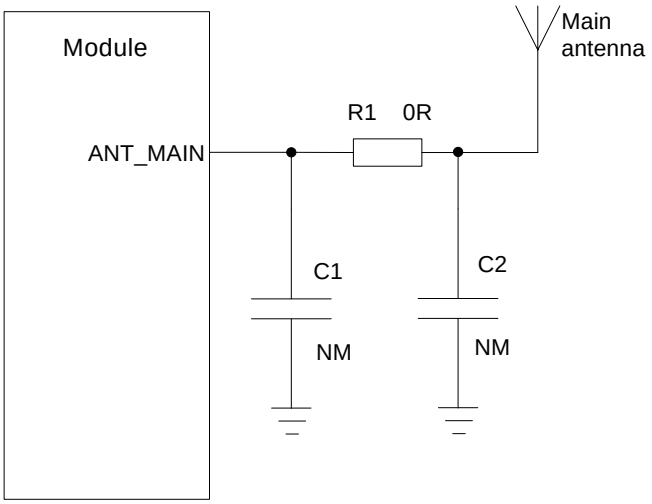


Figure 26: Reference Design of RF Antenna Interfaces

RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

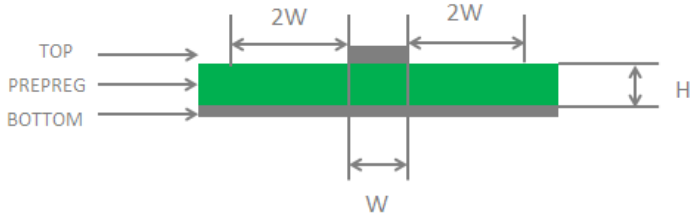


Figure 27: Microstrip Design on a 2-layer PCB

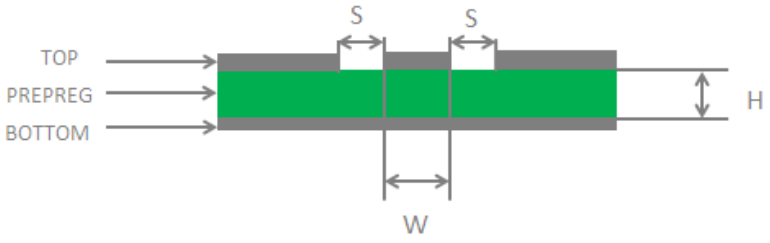


Figure 28: Coplanar Waveguide Design on a 2-layer PCB

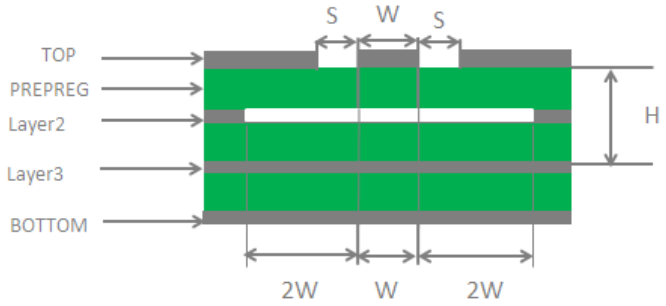


Figure 29: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

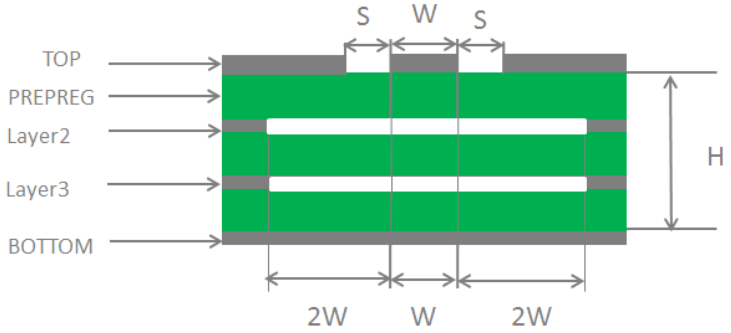


Figure 30: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

Antenna Design Requirements

Table 28: Antenna Design Requirements

Antenna Type	Requirements
LTE	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Gain: 1 dBi ● Max input power: 50 W ● Input impedance: 50 Ω

	● Vertical polarization ● Cable insertion loss: **< 1 dB:** LB (< 1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)

RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

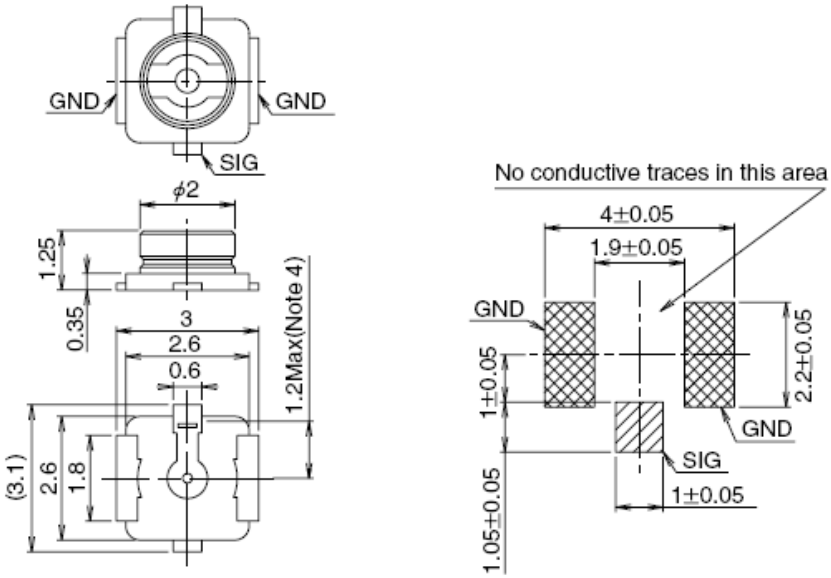


Figure 31: Receptacle Dimensions (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

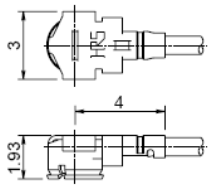
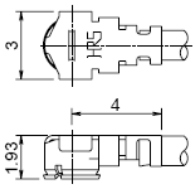
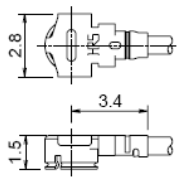
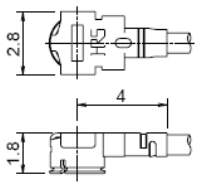
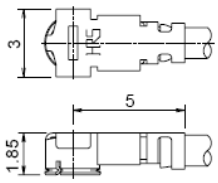
	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Part No.					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 32: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors.

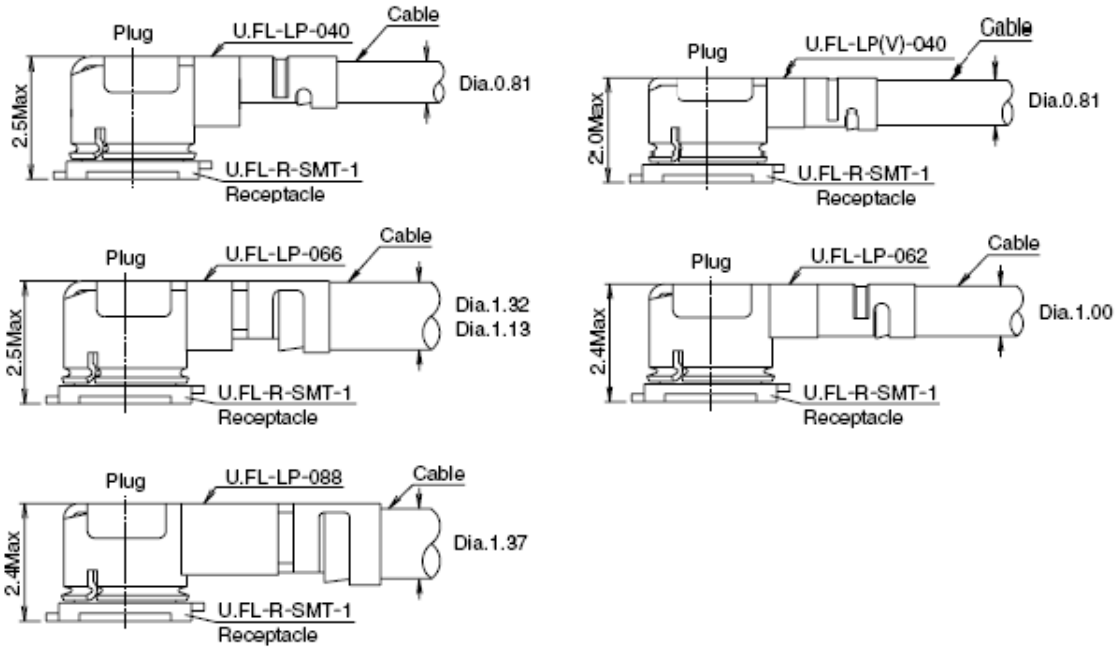


Figure 33: Space Factor of Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

Electrical Characteristics & Reliability

Absolute Maximum Ratings

Table 29: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Voltage at VBAT	-0.3	5	V
Voltage at USB_VBUS	-0.3	5.25	V
Voltage at digital pins	-0.3	2.3	V
Peak Current at VBAT	-	2.0	A

Power Supply Ratings

Table 30: Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	Power supply for the module	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V
I_{VBAT}	Peak power consumption	At maximum power control level	-	1.5	2	A
USB_VBUS	USB connection detect	-	3.0	5.0	5.25	V

Power Consumption

Table 31: EG800Q-EU Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	55	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	0.06	mA
	AT+CFUN=4 (USB disconnected)	0.15	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.23	mA
	LTE-FDD @ PF = 64 (USB disconnected)	0.70	mA
	LTE-FDD @ PF = 128 (USB disconnected)	0.45	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.35	mA
Idle state	LTE-FDD @ PF = 64 (USB disconnected)	4.50	mA
	LTE-FDD @ PF = 64 (USB connected)	25.50	mA
LTE data transfer	LTE-FDD B1	662	mA
	LTE-FDD B3	641	mA
	LTE-FDD B5	545	mA
	LTE-FDD B7	696	mA
	LTE-FDD B8	550	mA
	LTE-FDD B20	577	mA
	LTE-FDD B28	578	mA

Table 32: EG800Q-NA Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	50	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	0.06	mA
	AT+CFUN=4 (USB disconnected)	0.15	mA

	LTE-FDD @ PF = 32 (USB disconnected)	1.20	mA
	LTE-FDD @ PF = 64 (USB disconnected)	0.70	mA
	LTE-FDD @ PF = 128 (USB disconnected)	0.45	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.35	mA
Idle state	LTE-FDD @ PF = 64 (USB disconnected)	4.50	mA
	LTE-FDD @ PF = 64 (USB connected)	25.00	mA
LTE data transfer	LTE-FDD B2	588	mA
	LTE-FDD B4	656	mA
	LTE-FDD B5	499	mA
	LTE-FDD B12	572	mA
	LTE-FDD B13	586	mA
	LTE-FDD B66	631	mA

Digital I/O Characteristics

Table 33: VDD_EXT I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	0.7 x VDD_EXT	VDD_EXT + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.2 x VDD_EXT	V
V_{OH}	High-level output voltage	0.8 x VDD_EXT	-	V
V_{OL}	Low-level output voltage	-	0.15 x VDD_EXT	V

Table 34: USIM Low/High-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	0.7 x USIM_VDD	-	V

V_{IL}	Low-level input voltage	-	0.2 x USIM_VDD	V
V_{OH}	High-level output voltage	0.8 x USIM_VDD	-	V
V_{OL}	Low-level output voltage	-	0.15 x USIM_VDD	V

ESD Protection

Static electricity occurs naturally and may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 35: Electrostatics Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±8	±12	kV
Antenna Interface	±5	±10	kV
Other Interfaces	±0.5	±1	kV

Operating and Storage Temperatures

Table 36: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [5]	-35	+25	+75	°C
Extended Operating Temperature Range [6]	-40	-	+85	°C
Storage temperature range	-40	-	+90	°C

[5] Within the operating temperature range, the module meets 3GPP specifications.
[6] Within the extended temperature range, the module retains the ability to establish and maintain functions such as SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeters (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

Mechanical Dimensions

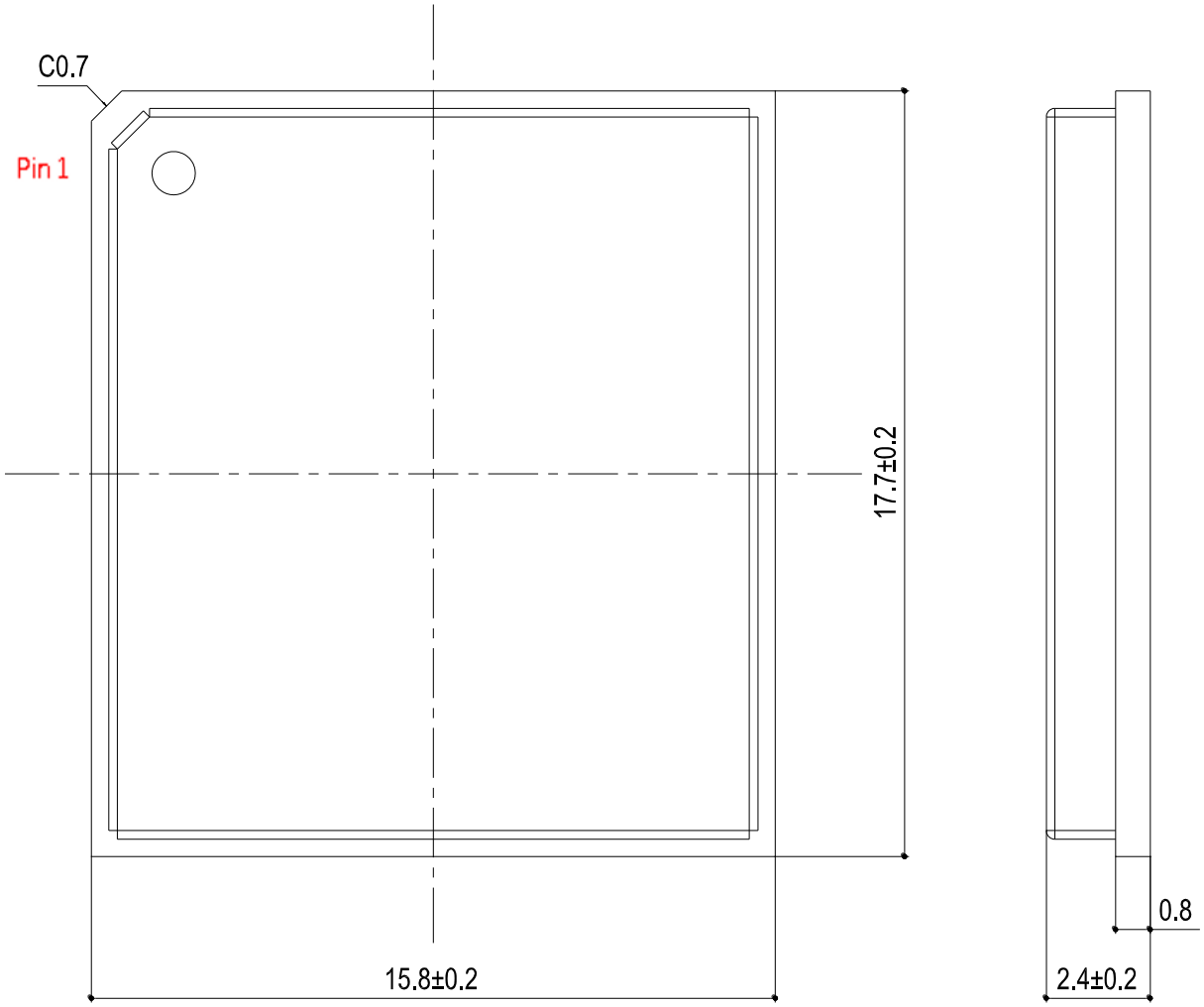


Figure 34: Module Top and Side Dimensions (Unit: mm)

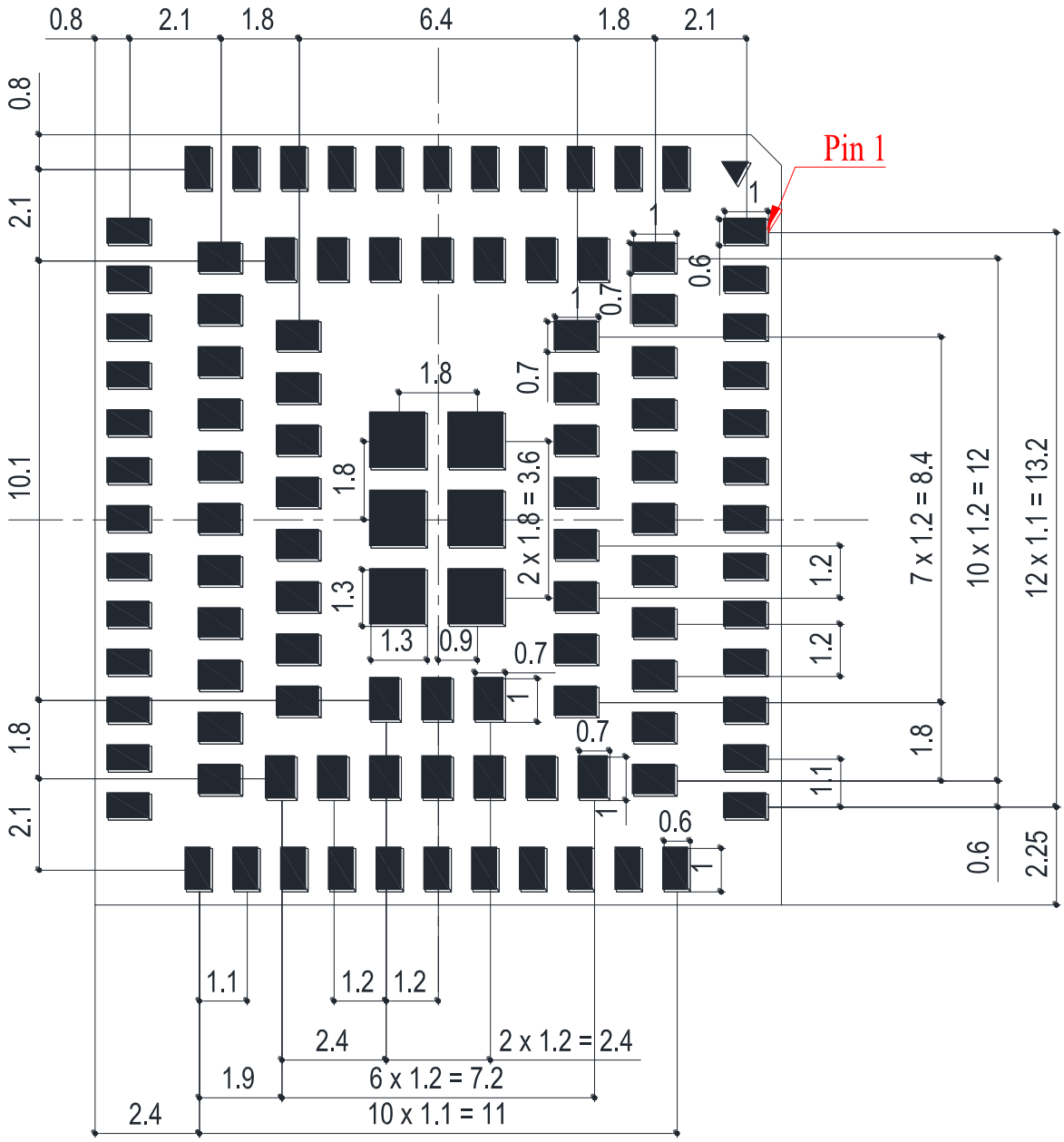


Figure 35: Bottom Dimensions (Bottom View, Unit: mm)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

Recommended Footprint

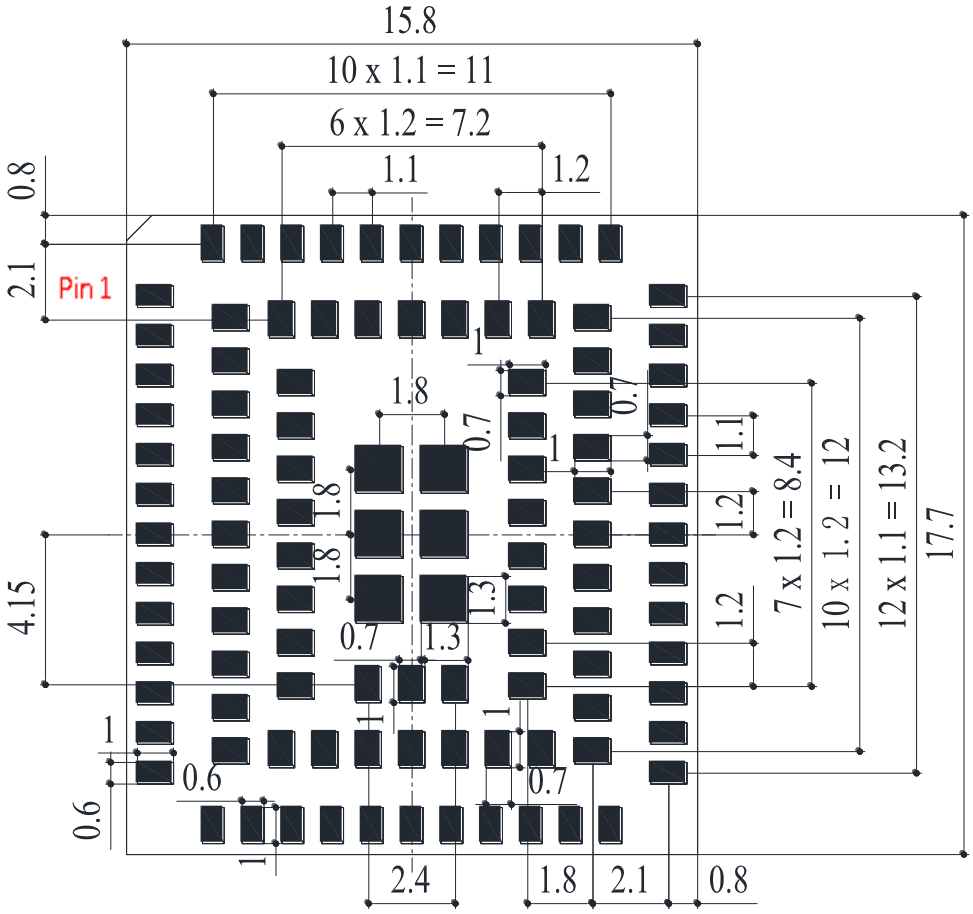


Figure 36: Recommended Footprint (Unit: mm)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

Top and Bottom Views

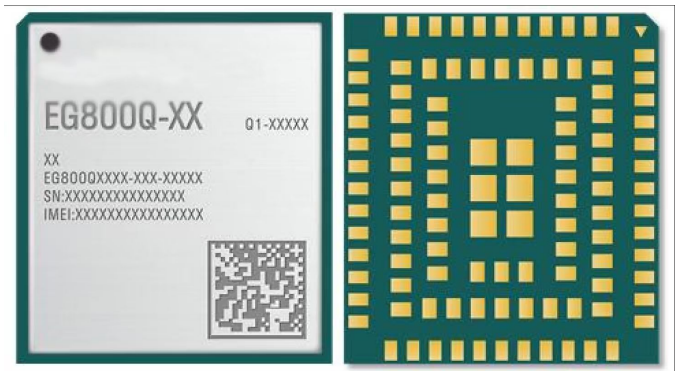


Figure 37: Module Top and Bottom Views

NOTE

Images above are for illustrative purposes only and may differ from the actual module. For authentic appearance and label, please refer to the module received from CTVZN.

Storage, Manufacturing & Packaging

Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [7] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

NOTE

[7] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

Manufacturing and Soldering

Push the squeegee to apply the solder paste on stencil surface, thus making the paste fill the stencil openings and then penetrate the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, 0.13–0.15 mm stencil thickness for the module is recommended.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid module damage caused by repeated heating, it is recommended to mount the module only after reflow soldering the other side of the PCB. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

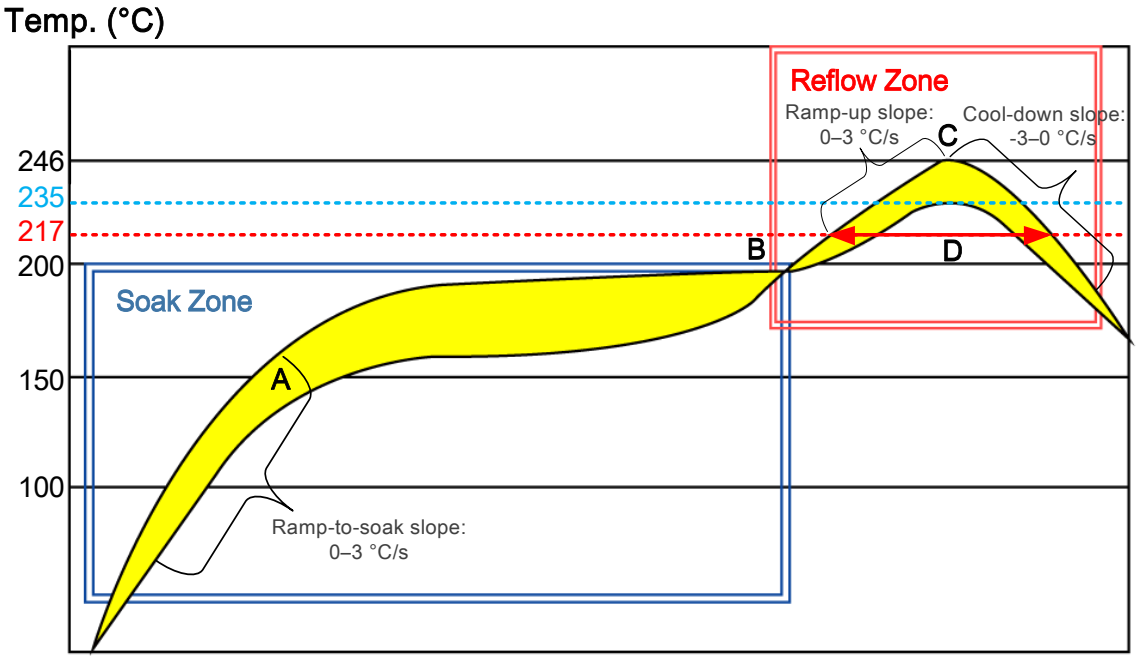


Figure 38: Recommended Reflow Soldering Thermal Profile

Table 37: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may require direct contact with the module, **NEVER** wipe the module shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol and trichloroethylene. Otherwise, the shielding can may become rusty.
3. The module shielding can be made of cupronickel base material. The Neutral Salt Spray Test has shown that after 12 hours the laser-engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, **DO NOT** use any coating material that may react with the PCB or shielding cover. Prevent the coating material from penetrating the module shield.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6.

Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

Carrier Tape

Dimension details are as follow:

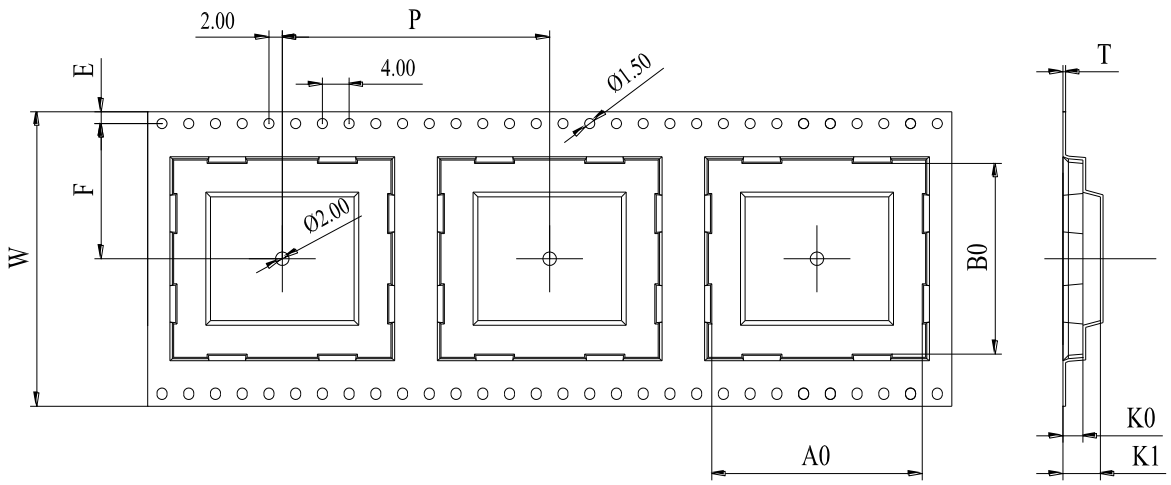


Figure 39: Carrier Tape Dimension Drawing

Table 38: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
32	24	0.4	16.2	18.1	2.8	7.6	14.2	1.75

Plastic Reel

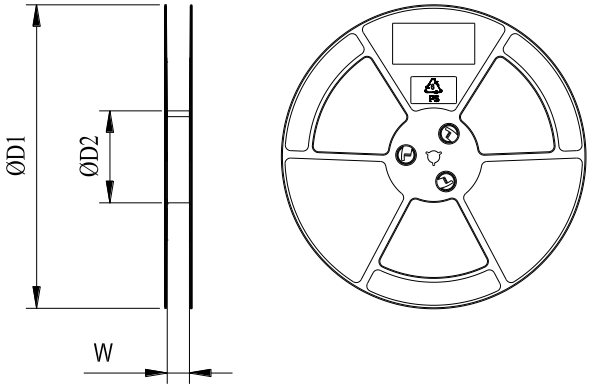


Figure 40: Plastic Reel Dimension Drawing

Table 39: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	32.5

Mounting Direction

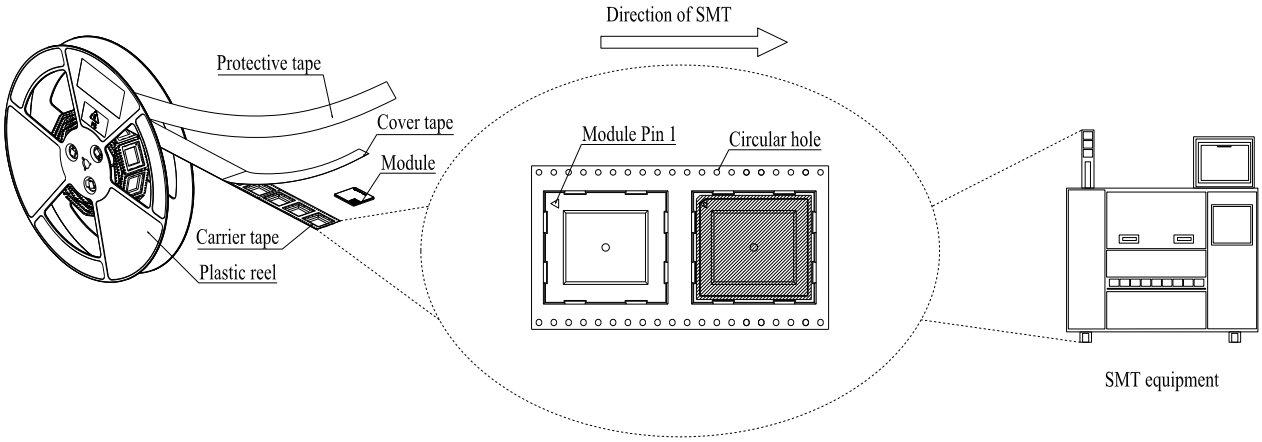
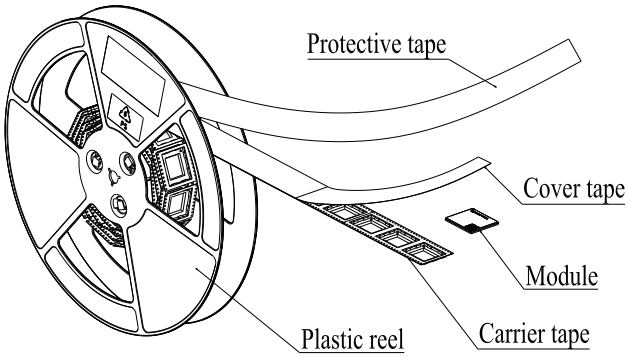


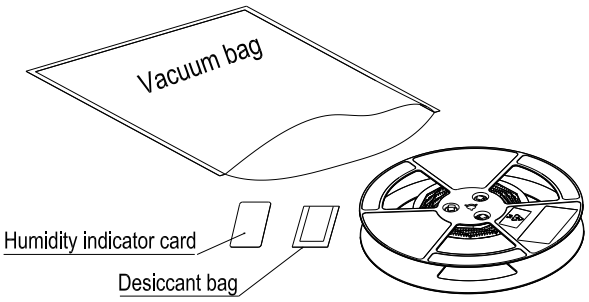
Figure 41: Mounting Direction

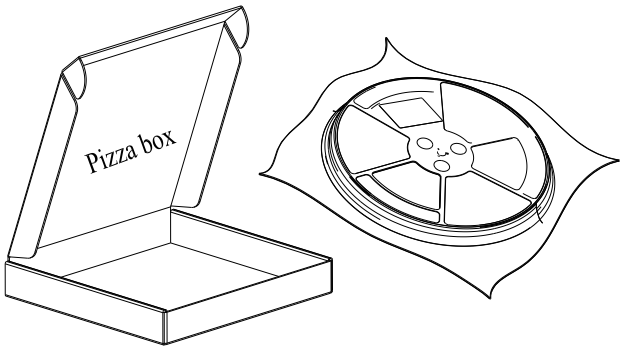
Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 carton box and seal it. 1 carton box can pack 1000 modules.

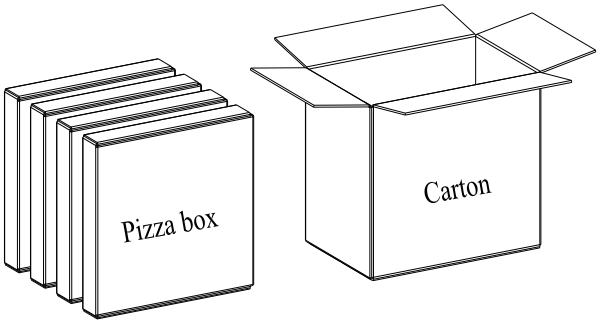


Figure 42: Packaging Process

Appendix References

Table 40: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
bps	Bytes per second
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection MUX
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over-The-Air
DTE	Data Terminal Equipment
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVB	Evaluation Board
FDD	Frequency Division Duplexing
FILE	File Protocol
FTP	File Transfer Protocol
FTPS	FTP over SSL
GND	Ground

HB	High Band
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
IMT-2000	International Mobile Telecommunications 2000
I2C	Inter-Integrated Circuit
$I_O$max	Maximum Output Load Current
LB	Low Band
LCC	Leadless Chip Carrier (package)
LDO	Low-dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
M2M	Machine to machine
MB	Medium Band
MCU	Microcontroller Unit/Microprogrammed Control Unit
ME	Mobile Equipment
MMS	Multimedia Messaging Service
MO	Mobile Origination
MQTT	Message Queuing Telemetry Transport
MT	Mobile Termination
NITZ	Network Identity and Time Zone
NTP	Network Time Protocol
PAP	Password Authentication Protocol
PC	Personal Computer
PCB	Printed Circuit Board

PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PING	Packet Internet Groper
POS	Point of Sale
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTS	Request To Send
SMD	Surface Mount Device
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)

V_{IH}	High-level input voltage
V_{IL}	Low-level input voltage
V_{OH}	High-level output voltage
V_{OL}	Low-level output voltage
Vmax	Maximum Voltage
Vmin	Minimum Voltage
Vnom	Nominal Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{RWM}	Working Peak Reverse Voltage
VSWR	Voltage Standing Wave Ratio

FCC

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part
15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to XXXX that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: 2AZL7-ZY-G2

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.

EG800Q-NA		
Band	Frequency (MHz)	Gain (dBi)
LTE-FDD B2	1850-1910	1.59
LTE-FDD B4	1710–1755	2
LTE-FDD B5	824–849	2.53
LTE-FDD B12	699–716	3.95
LTE-FDD B13	777–787	4.45
LTE-FDD B66	1710-1780	2

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.

- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, 15.247 and 15.407 requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

IC

Industry Canada Statement

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions:

(For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions

suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: XXXXX-XXXXXXXX”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: XXXXX-XXXXXXXX ".

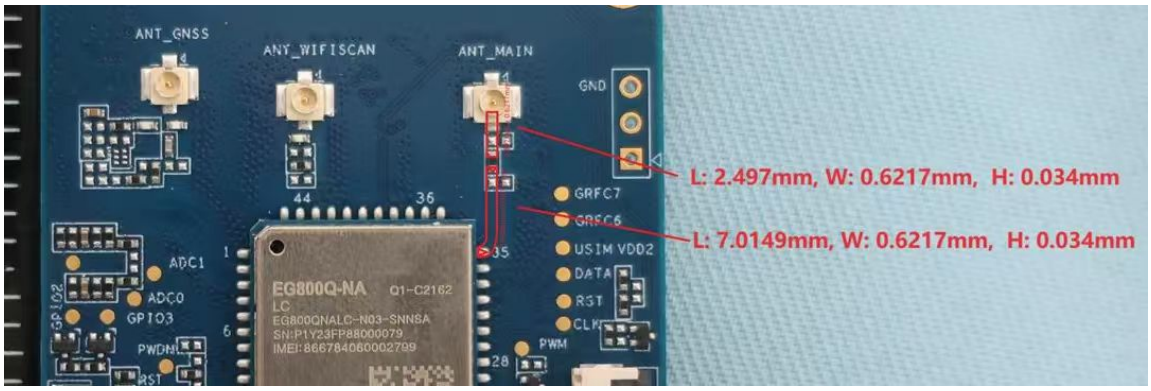
Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

Trace design



Dielectric constant, and Impedance

Layer classification	Simulated thickness (finished product	Stacking diagram					Standard thickness UM	PP，CORE model	Material name	DK value of each layer	DF	Residual copper rate of each layer		TG	TD
												make up	Single PC		
Resistance welding	20		0			~ ~	20								
L1	30	0.33oz	11.55	1.155	0.00	Foil 0.33oz	30+/-5								
PP	47.21		47.2102	10.16	4.90	SY S1150GB 106 RC75%	52+/-7.5	106 75%	PP	3.96	0.016				
L2	23	0.33oz	22.8152	1.155	0.00	Foil 0.33oz	23+/-5					70	80		
PP	126.77		126.768	15.24	4.90	SY S1150GB 2116 RC58%	122+/-10%	2116 57%	PP	4.43	0.013				
L3	16	0.5oz 0.5oz	76	18	4.50	SY S1150G Core 0.076MM H/H_1080*1	16					65	75		
CORE	76						75+/-13	0.075MM No Copper	CORE	4.3	0.014				
L4	16		121.083	15.24	4.90	SY S1150GB 2116 RC58%	16					78	88		
PP	121.08	0.5oz 0.5oz	76	18	4.50	SY S1150G Core 0.076MM H/H_1080*1	122+/-10%	2116 57%	PP	4.43	0.013				
L5	16						16					66	76	≥150	≥325
CORE	76						75+/-13	0.075MM No Copper	CORE	4.3	0.014				
L6	16		127.516	15.24	4.90	SY S1150GB 2116 RC58%	16					78	88		
PP	127.52	0.33oz	22.8152	1.155	0.00	Foil 0.33oz	122+/-10%	2116 57%	PP	4.43	0.013				
L7	23		46.5258	10.16	4.90	SY S1150GB 106 RC75%	23+/-5					63	73		
PP	46.53	0.33oz	11.55	1.155	0.00	Foil 0.33oz	52+/-7.5	106 75%	PP	3.96	0.016				
L8	30						30+/-5								
Resistance welding	20		0			~ ~	20								
		Specification thickness	0.8+/-0.08			Total plate thickness									
Total	SR-SR		Pt-Pt		BVH	831.11									

Impedance-Meter										
Type	Control lay	Reference layer	Customer Line Width	Customer Line Distance	Finished product impedance	Adjusting Line Weights	Adjust line spacing	Impedance control range	Green oil front impedance	Original to copper sheet distance
Single ended	L1	L2	90		50.00	65		+/-5.0	54.8	
Single ended	L2	L3/L1	50		50.00	54		+/-5.0	/	
Single ended	L3	L4/L2	72		50.00	80		+/-5.0	/	
Single ended	L5	L6/L4	74		50.00	78		+/-5.0	/	
Differential	L7	L6/L8	65	150	90.00	63	152	+/-9.0	/	