

Project Name : MPC43

Platform : INTEL COMPUTE MODULE

PAGE CONTENT

- 1. INDEX
- 2. SYSTEM BLOCK
- 3. POWER DIAGRAM & SEQUENCE
- 4. CONN
- 5. EC
- 6. ECFLASH
- 7. Charging
- 8. TYPE-C PD
- 9. Type-C_VBUS_POWER
- 10. TYPE-C CONNECTOR
- 11. HDMI BD
- 12. FAN
- 13. CODEC(ALC269Q)/INT MIC/SPKR
- 14. EXT_MIC
- 15. eDP CONN/CAMERA
- 16. HDMI
- 17. PWR SW
- 18. M.2/NGFF/SENSORS
- 19. TP/LED/Click-pad/USB
- 20. BATT IN
- 21. DC IN/Discharge/HOLE
- 22. 5VA/3.3VA/1.05VA
- 23. VCC SW/1.5V/HIGH-SPEED CAP
- 24. History

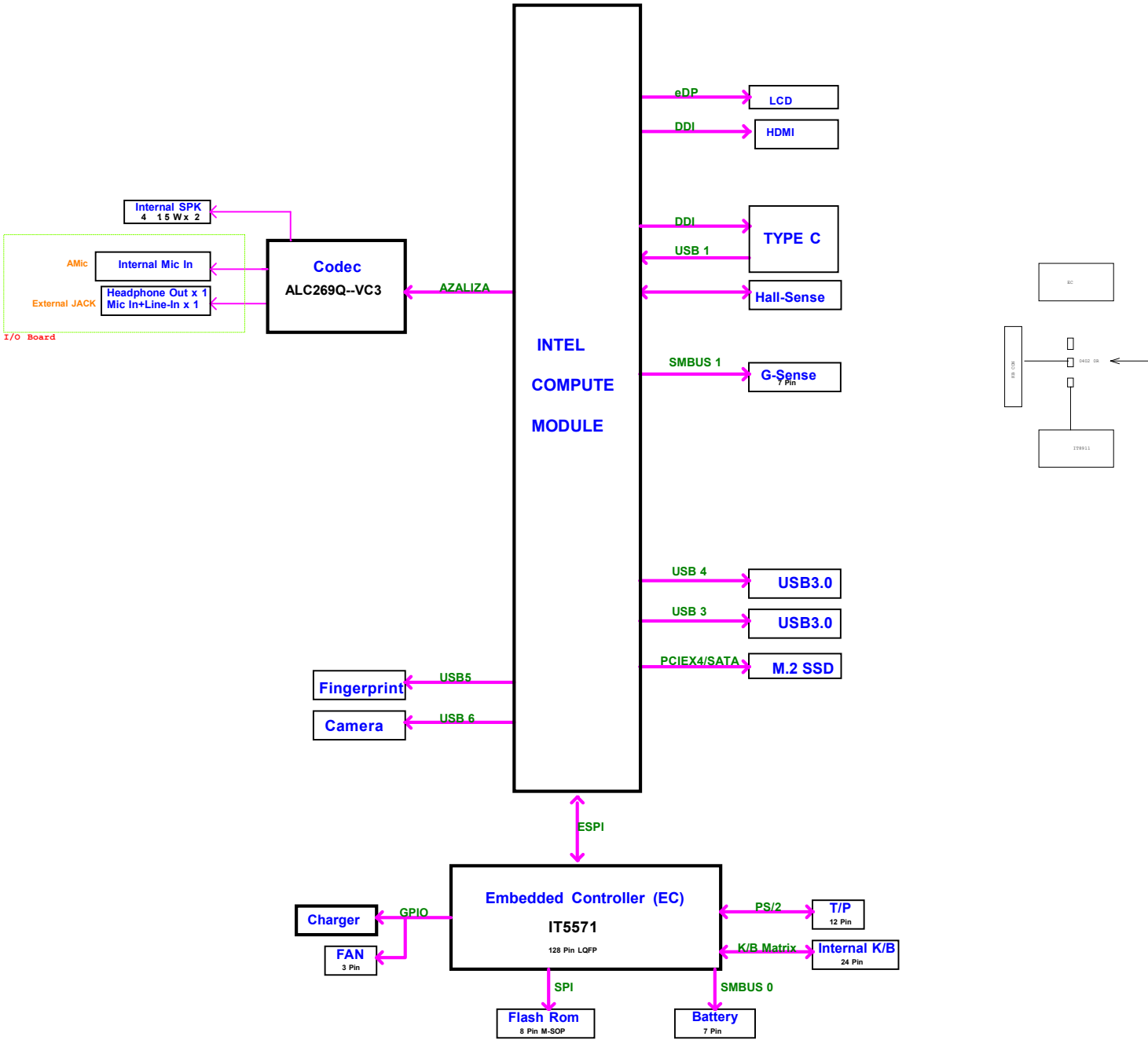
M/B Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

Daughter Board Schematic Version Change List

Release Date	Version	PCB P/N	PCB Description	PCBA P/N	Note

SYSTEM BLOCK DIAGRAM



5

3

3

1

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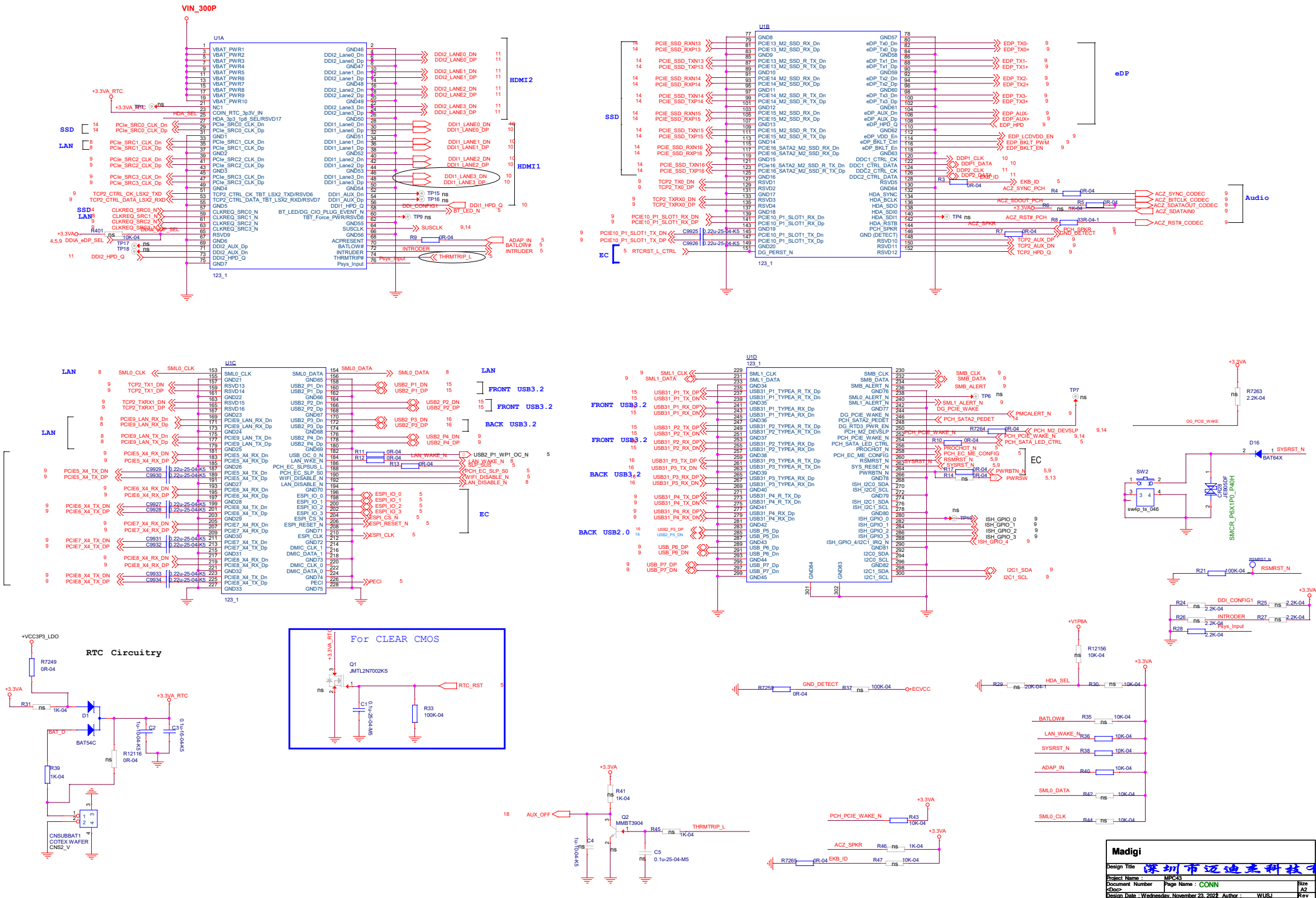
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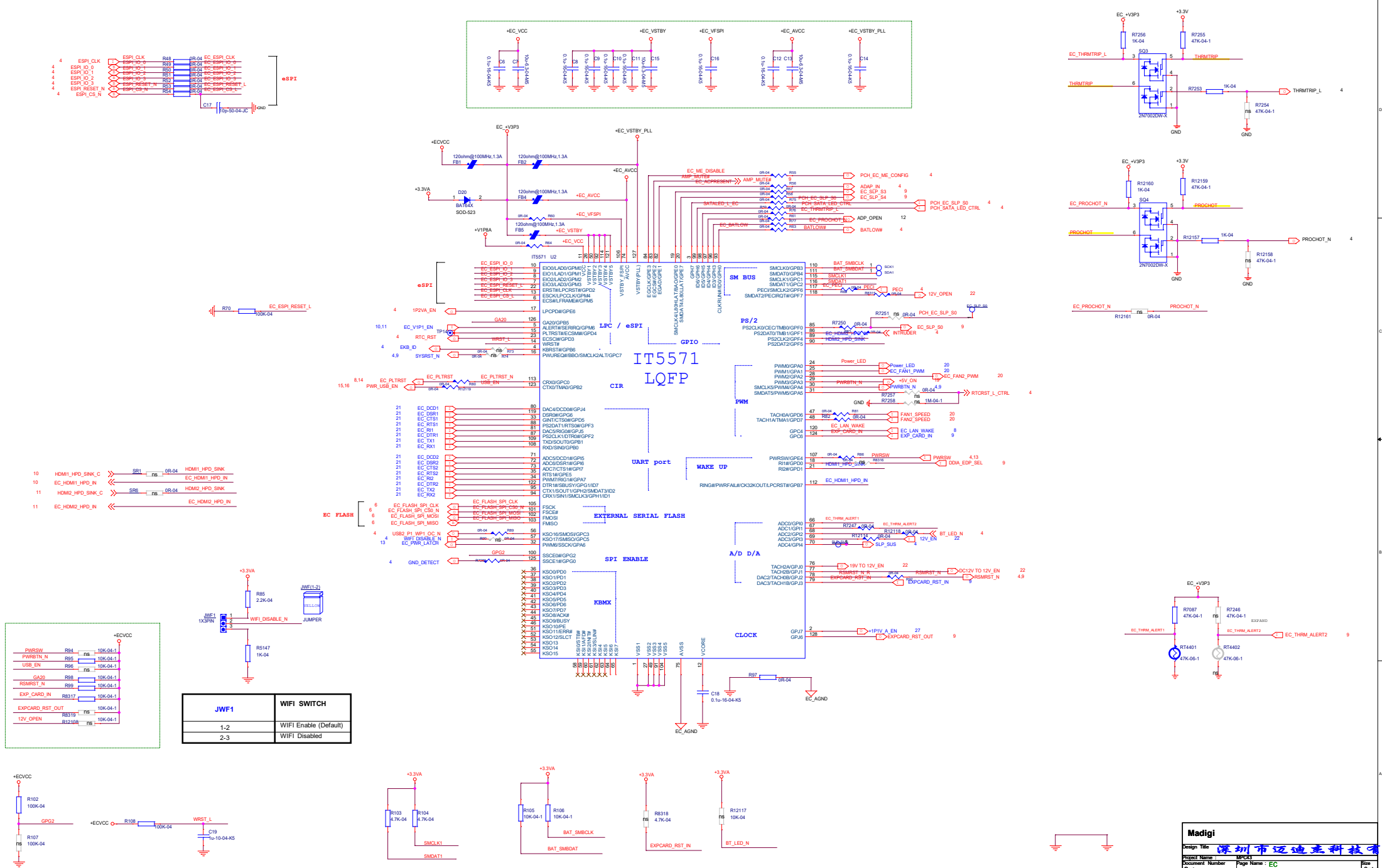
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1

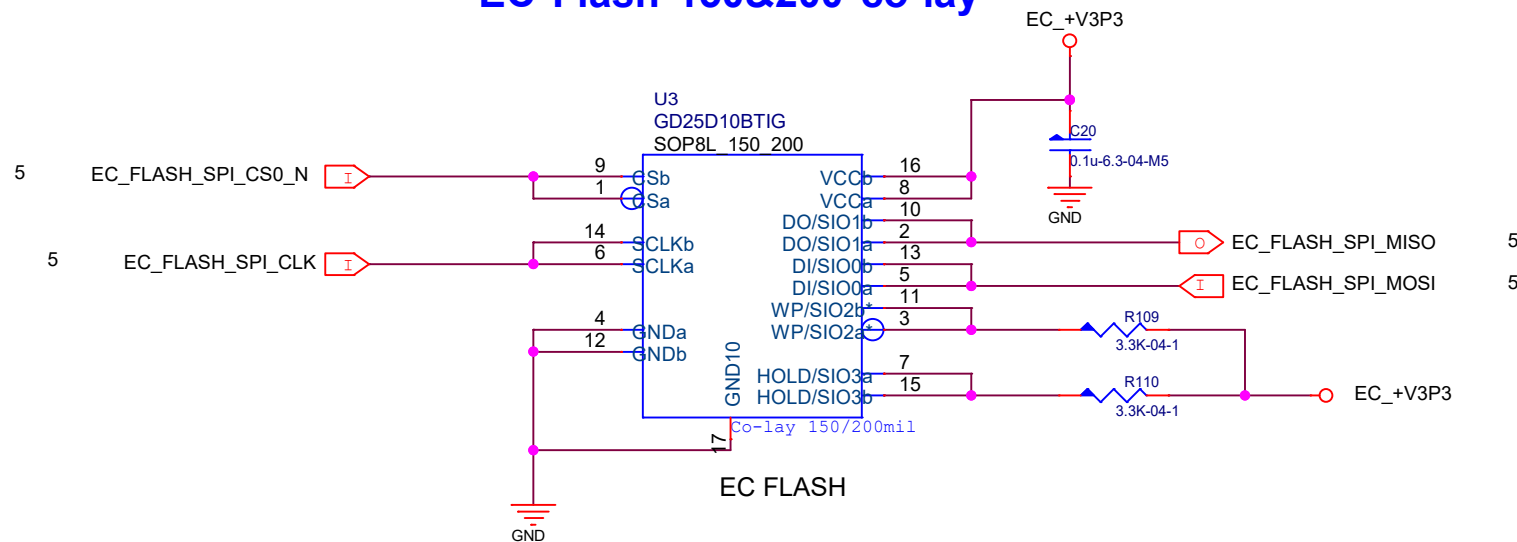




JWF1	WIFI SWITCH
1-2	WIFI Enable (Default)
2-3	WIFI Disabled

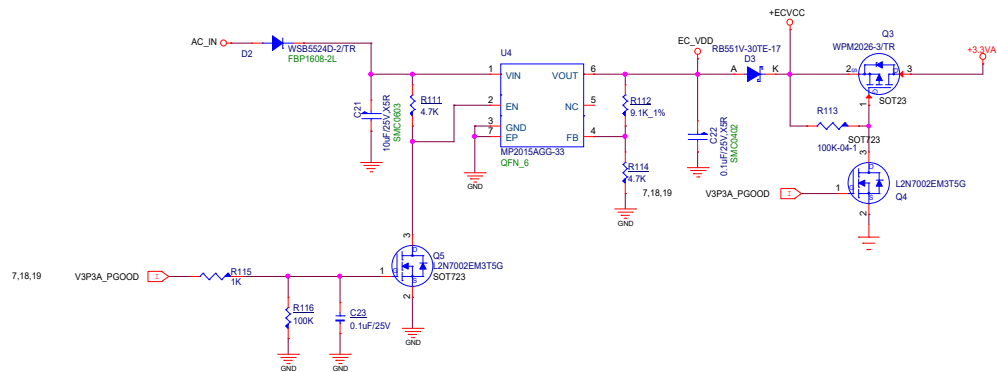
EC -2

EC Flash 150&200 co-lay

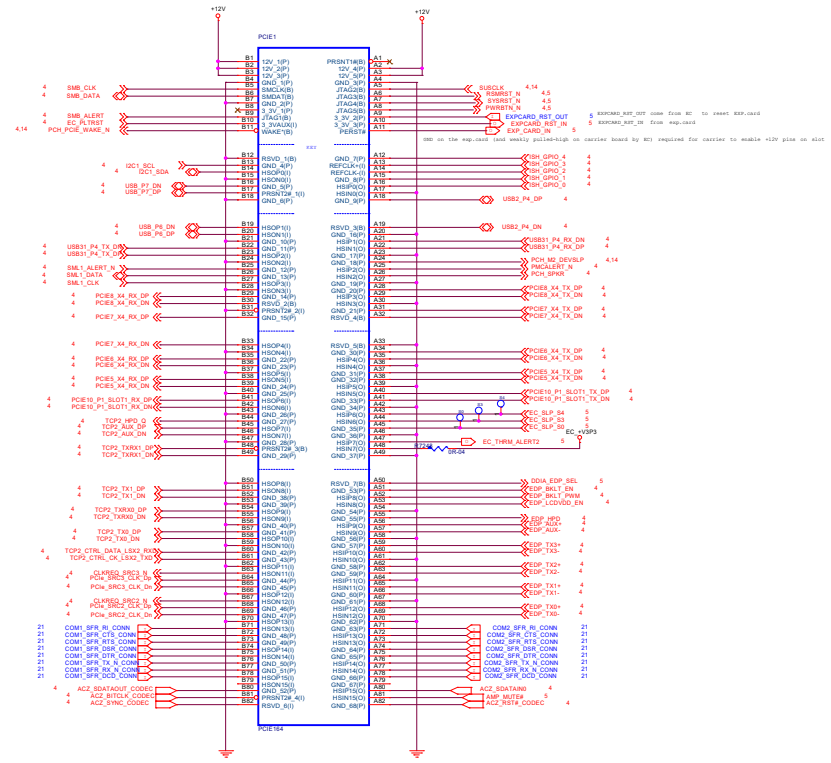


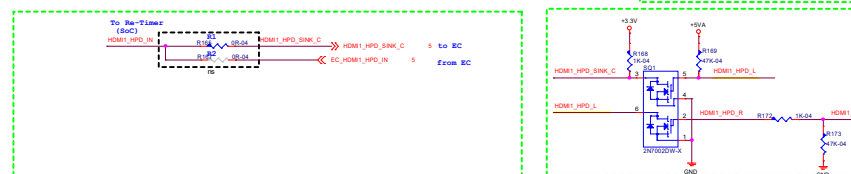
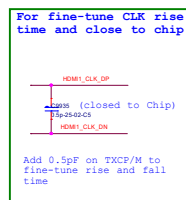
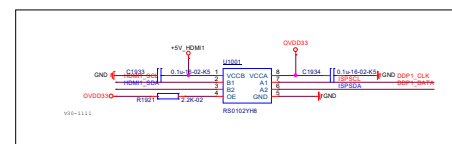
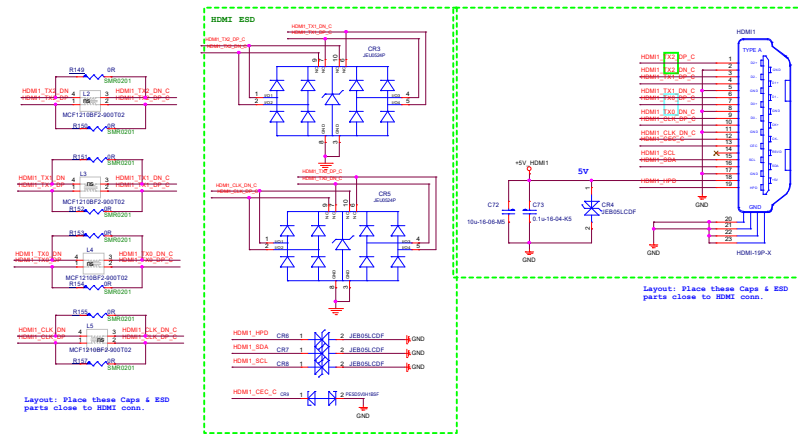
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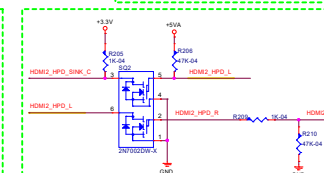
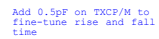
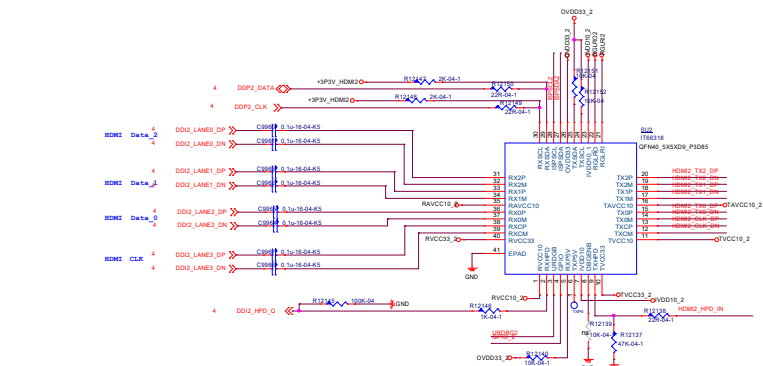
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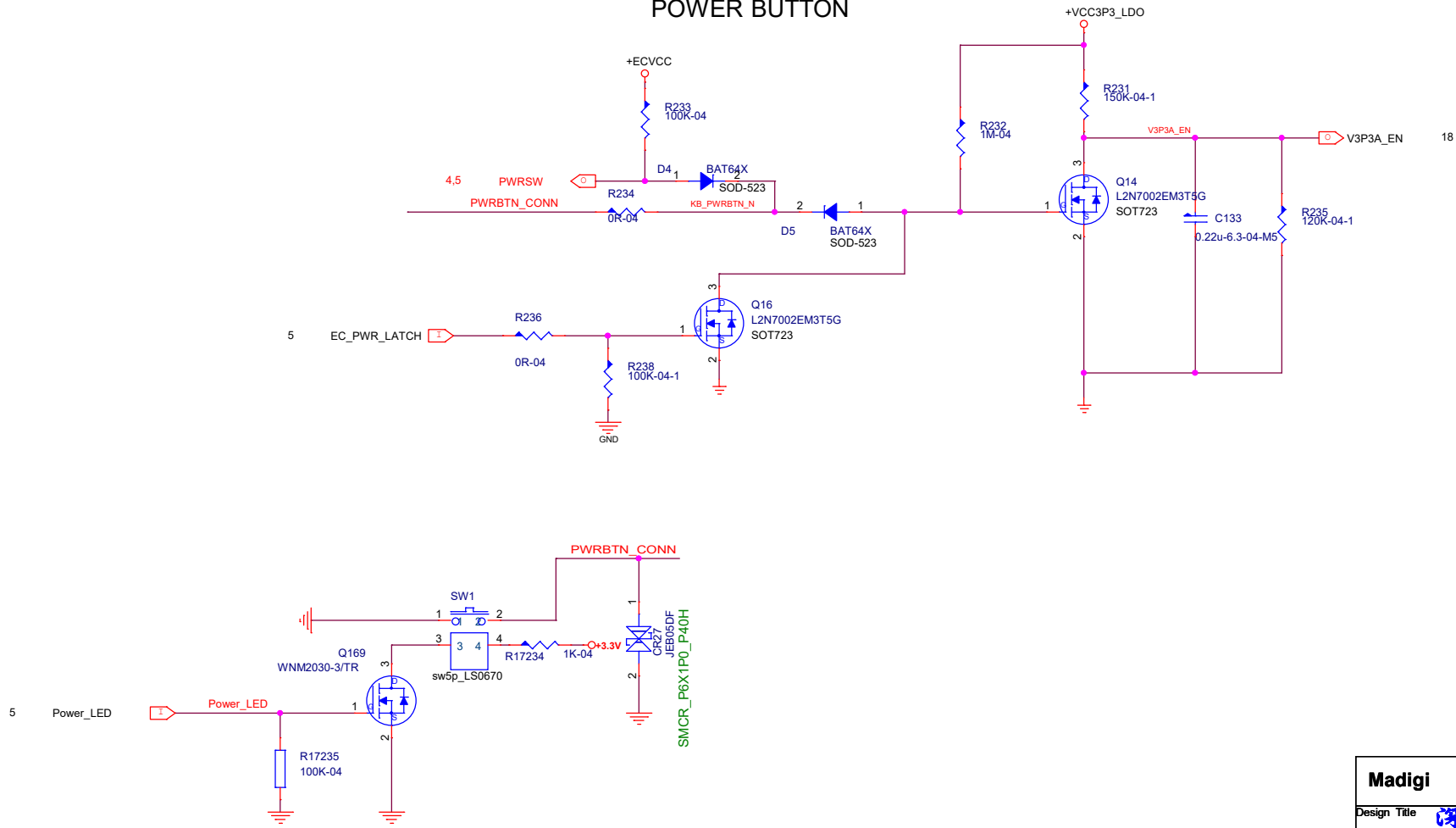






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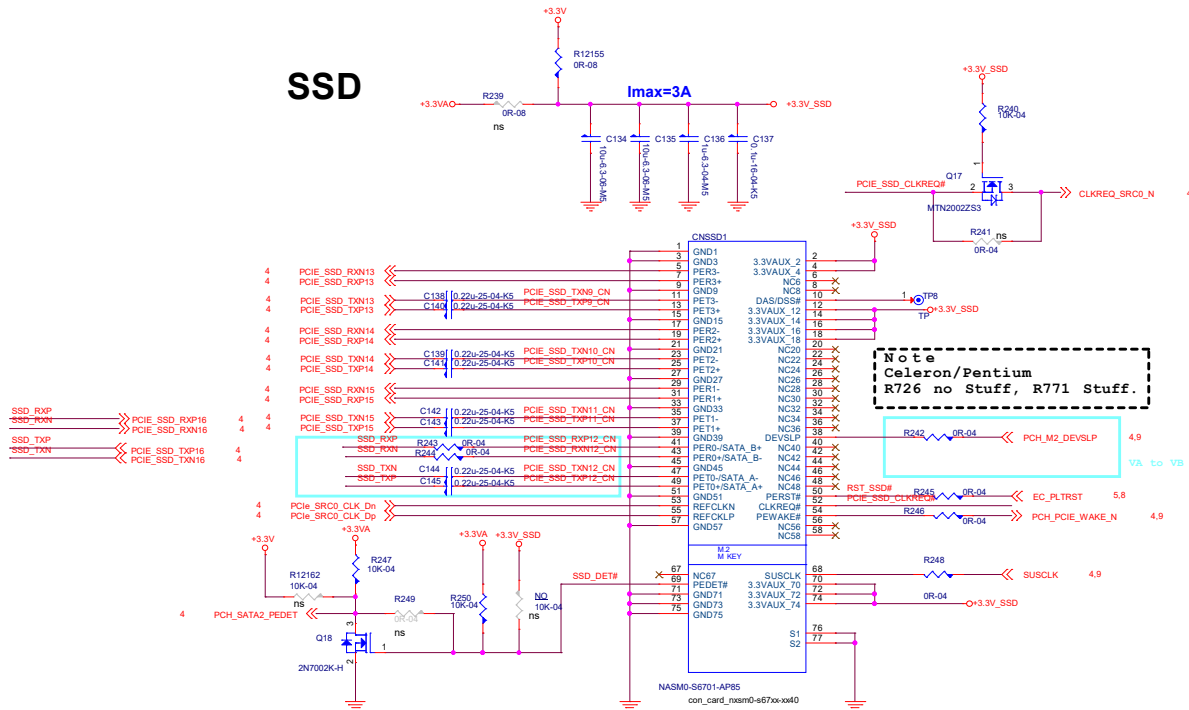
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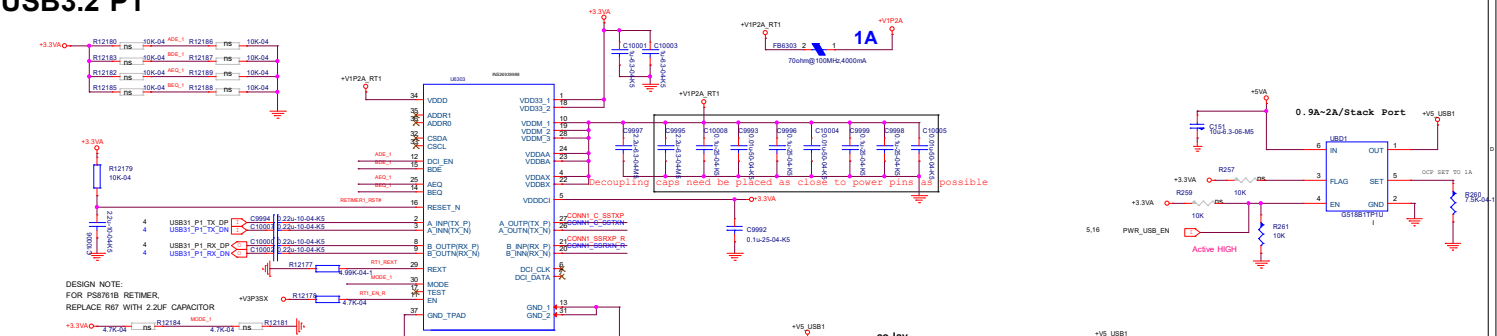
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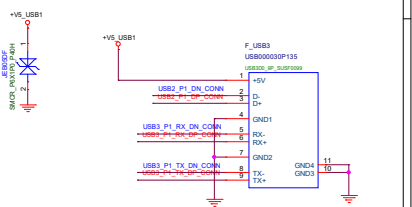
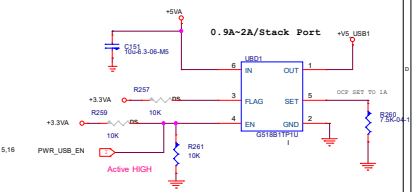
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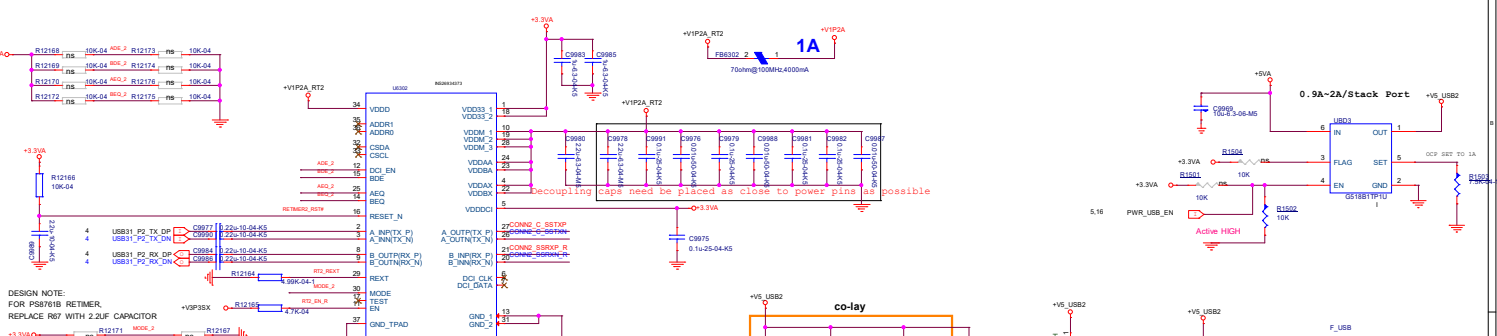
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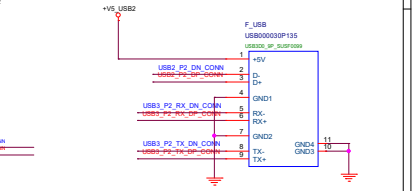
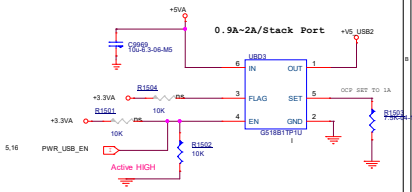
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Default is Middle Level
L: Redriver Mode
M(Default): Redriver Mode for 5Gbps; Retimer Mode for 10Gbps
H: Retimer Mode



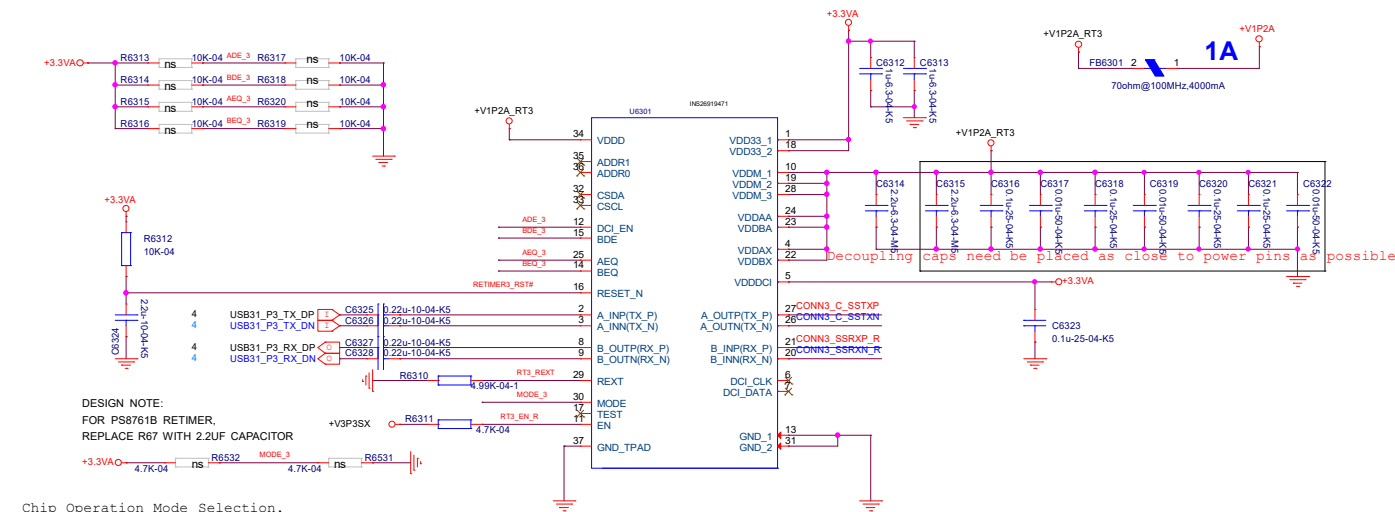
USB3.2 P2



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H: Retimer Mode

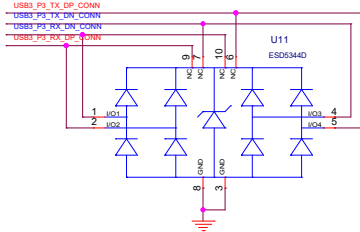
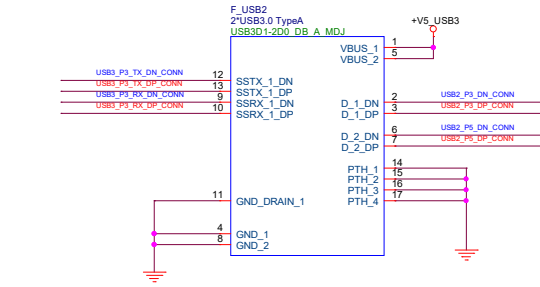
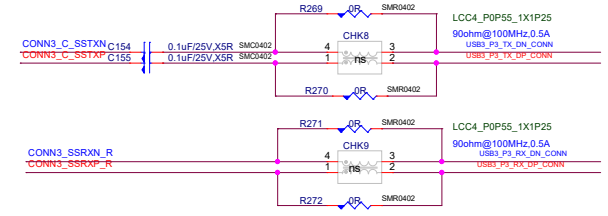
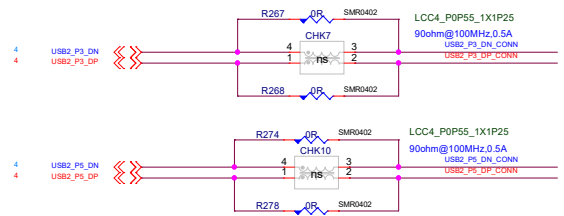
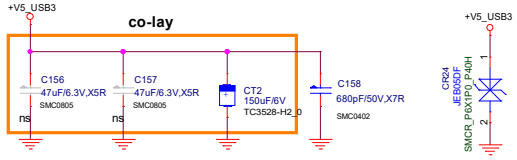
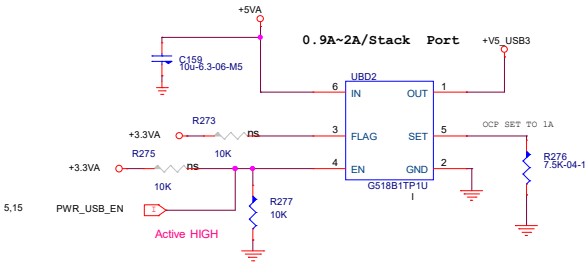


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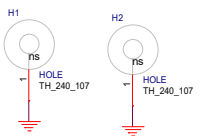
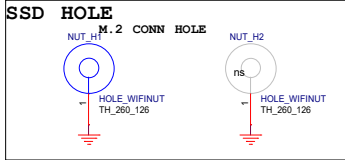
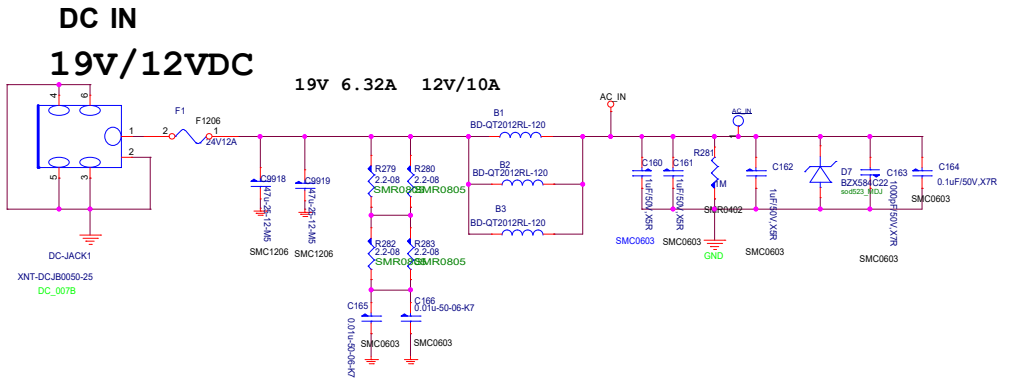


Chip Operation Mode Selection.
Default is Middle Level

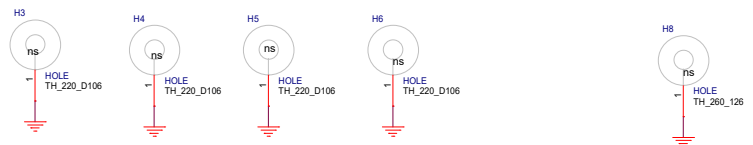
L: Redriver Mode
M(Default): Redriver Mode for 5Gbps; Retimer Mode for 10Gbps
H: Retimer Mode



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Page Date	Wednesday, November 23, 2022	Sheet	16 of 30



SCREW HOLE



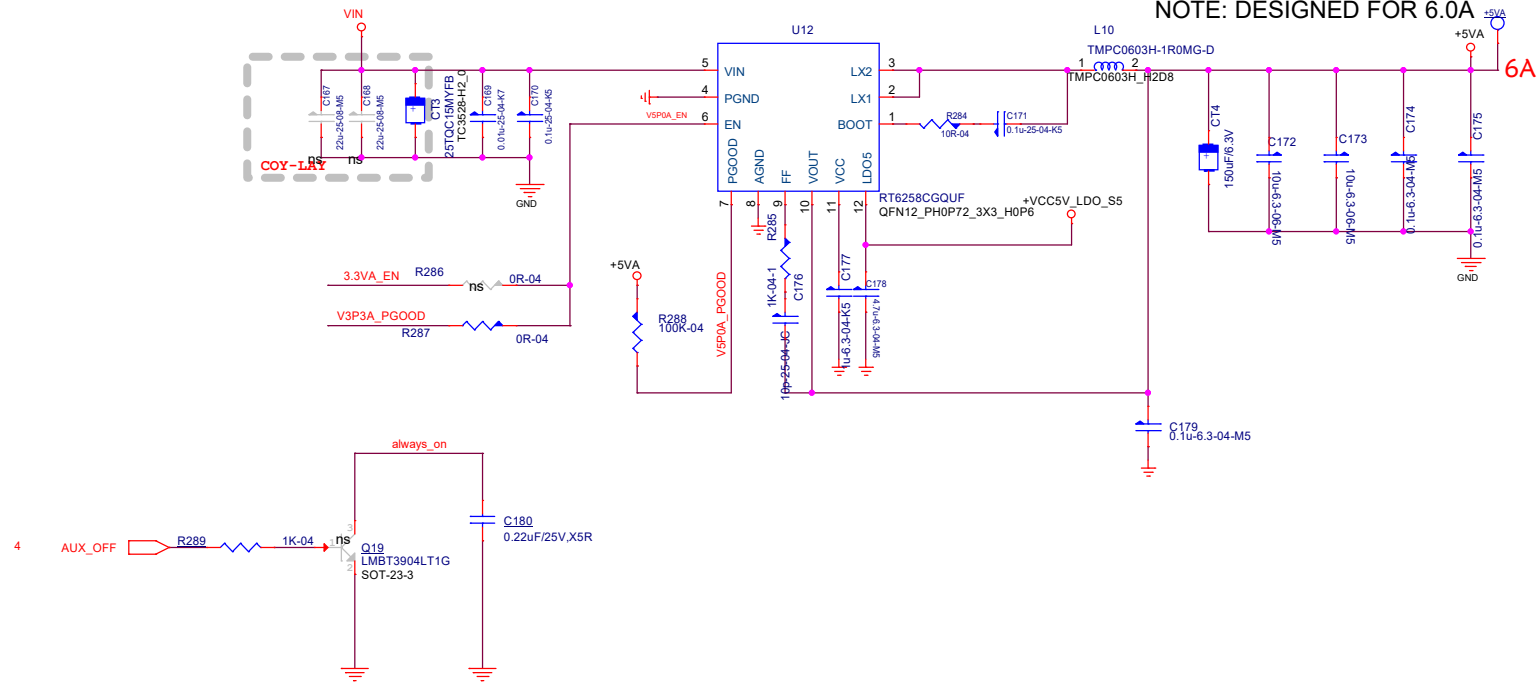
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深圳市迈迪杰科技有限公司

5VA Converter

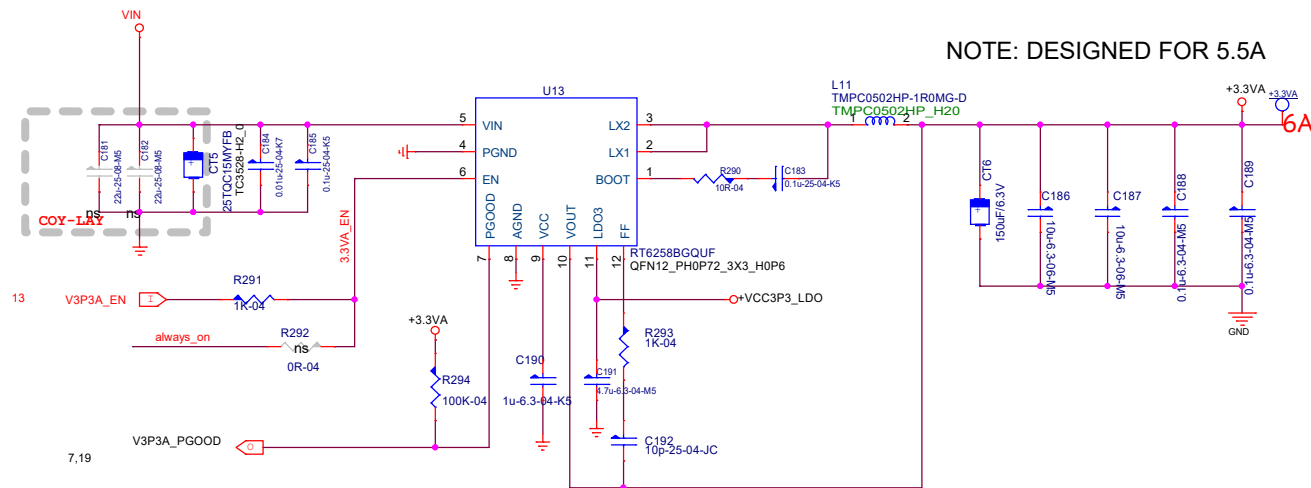
+V5P0A / +V3P3A POWER SUPPLY

NOTE: DESIGNED FOR 6.0A



3.3VA

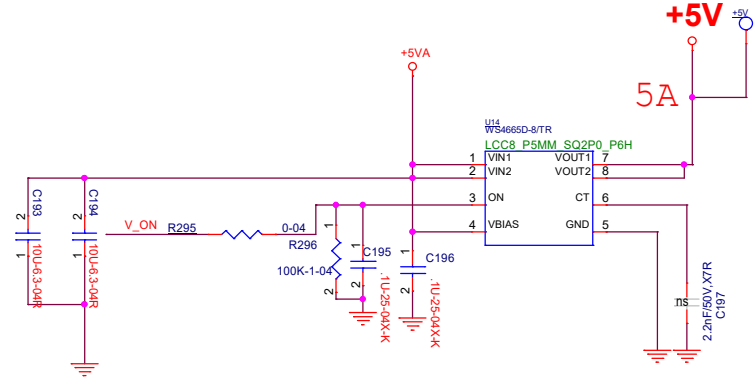
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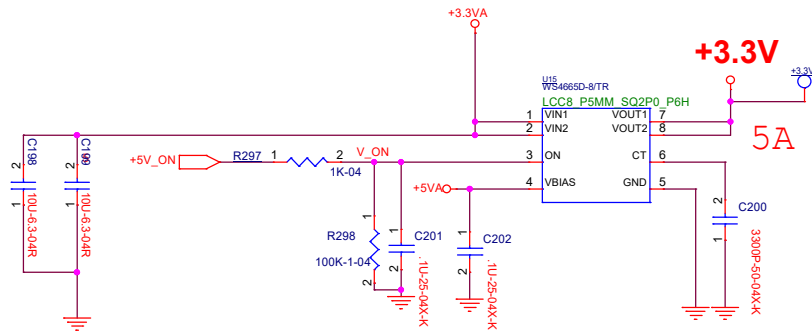
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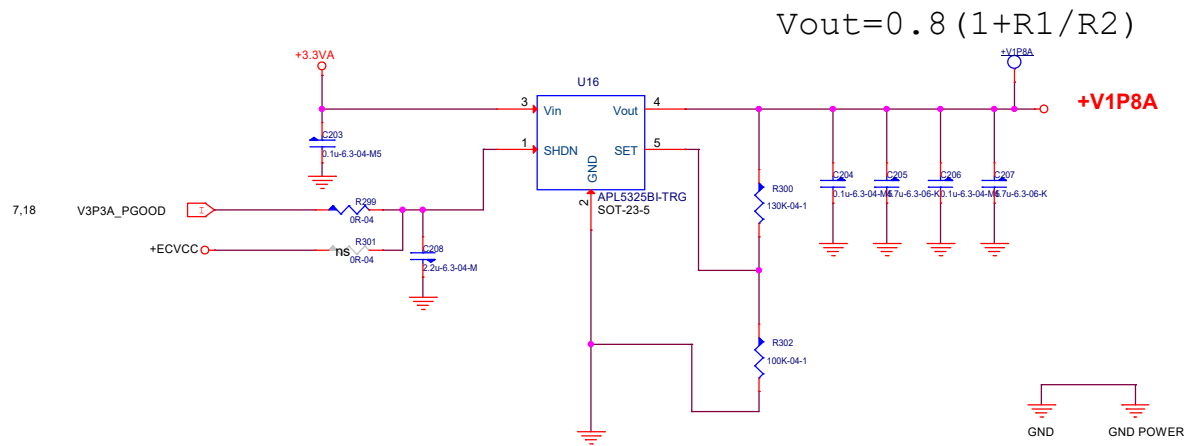
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+3.3V



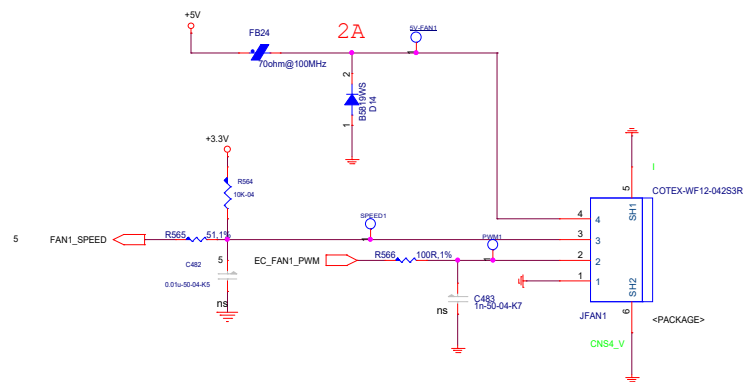
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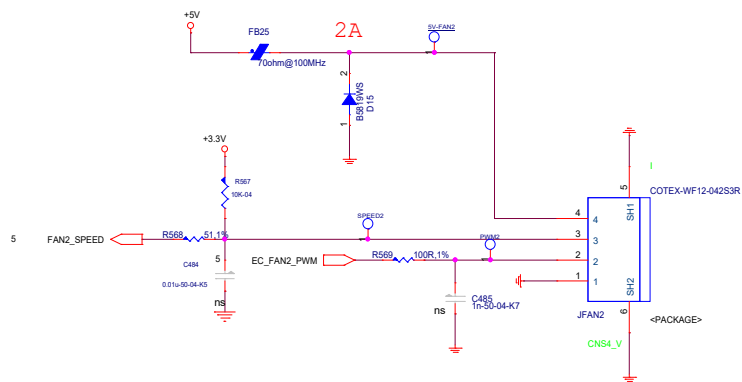
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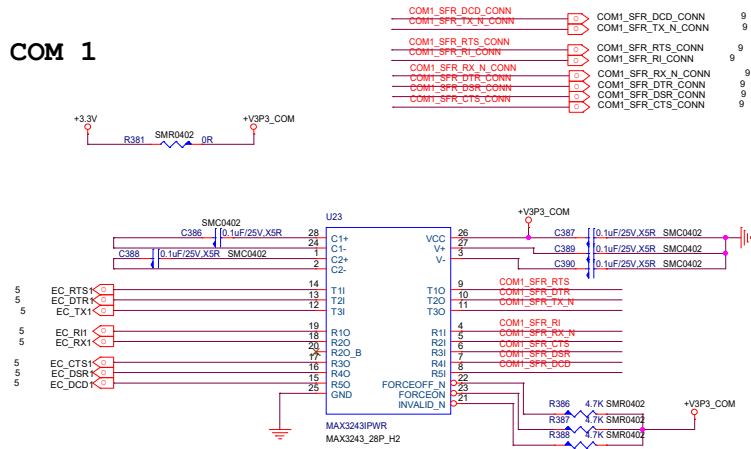
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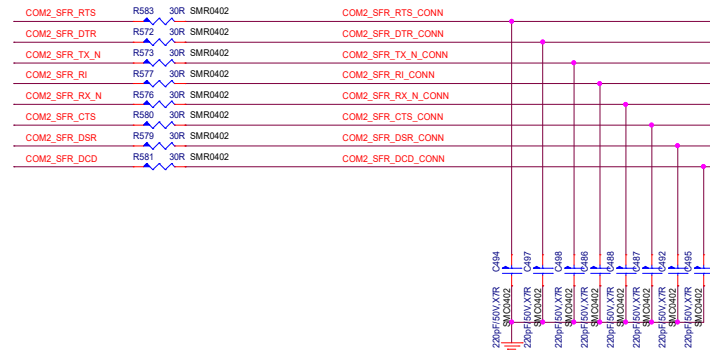
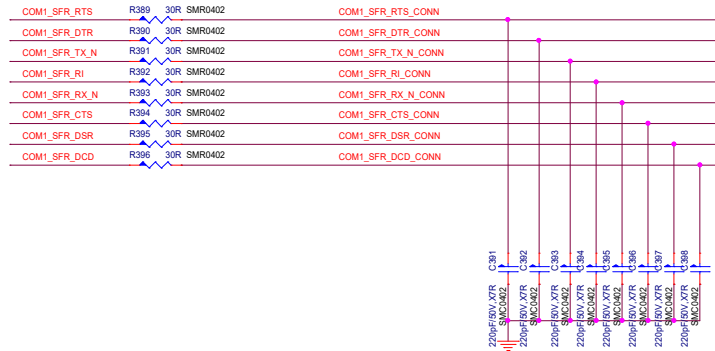
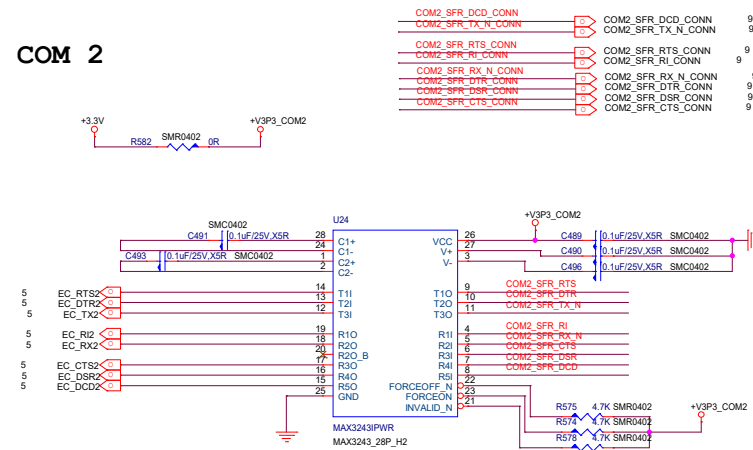
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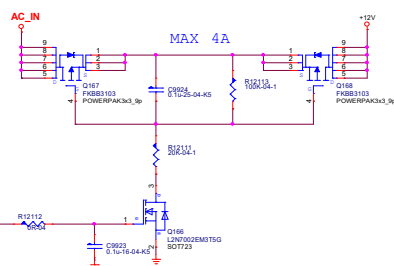
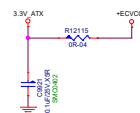
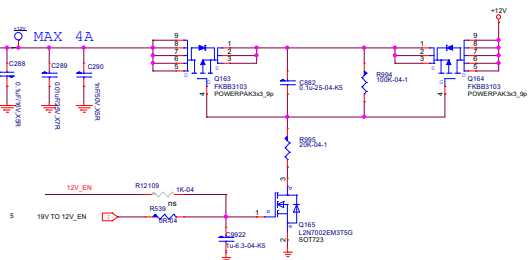


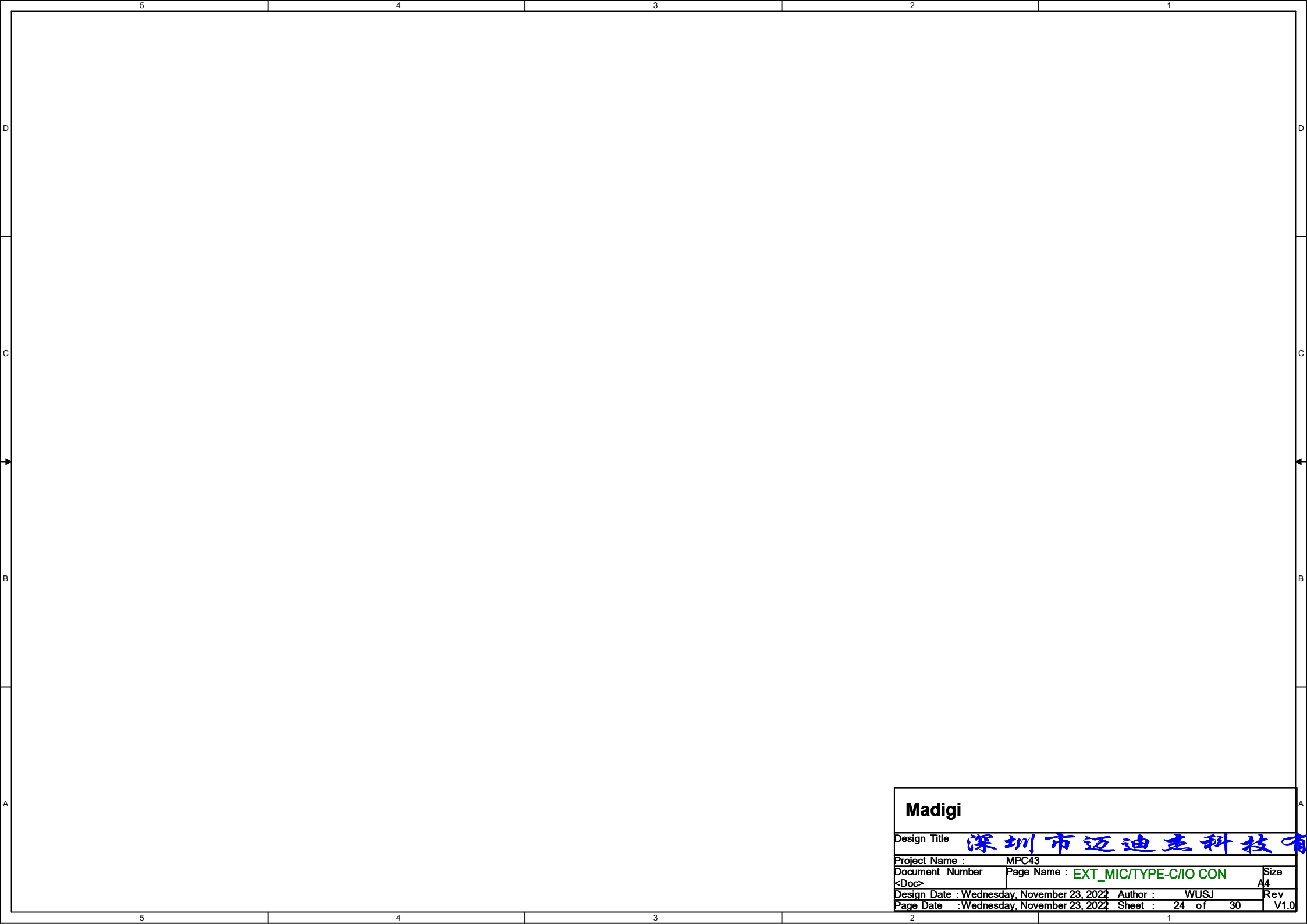
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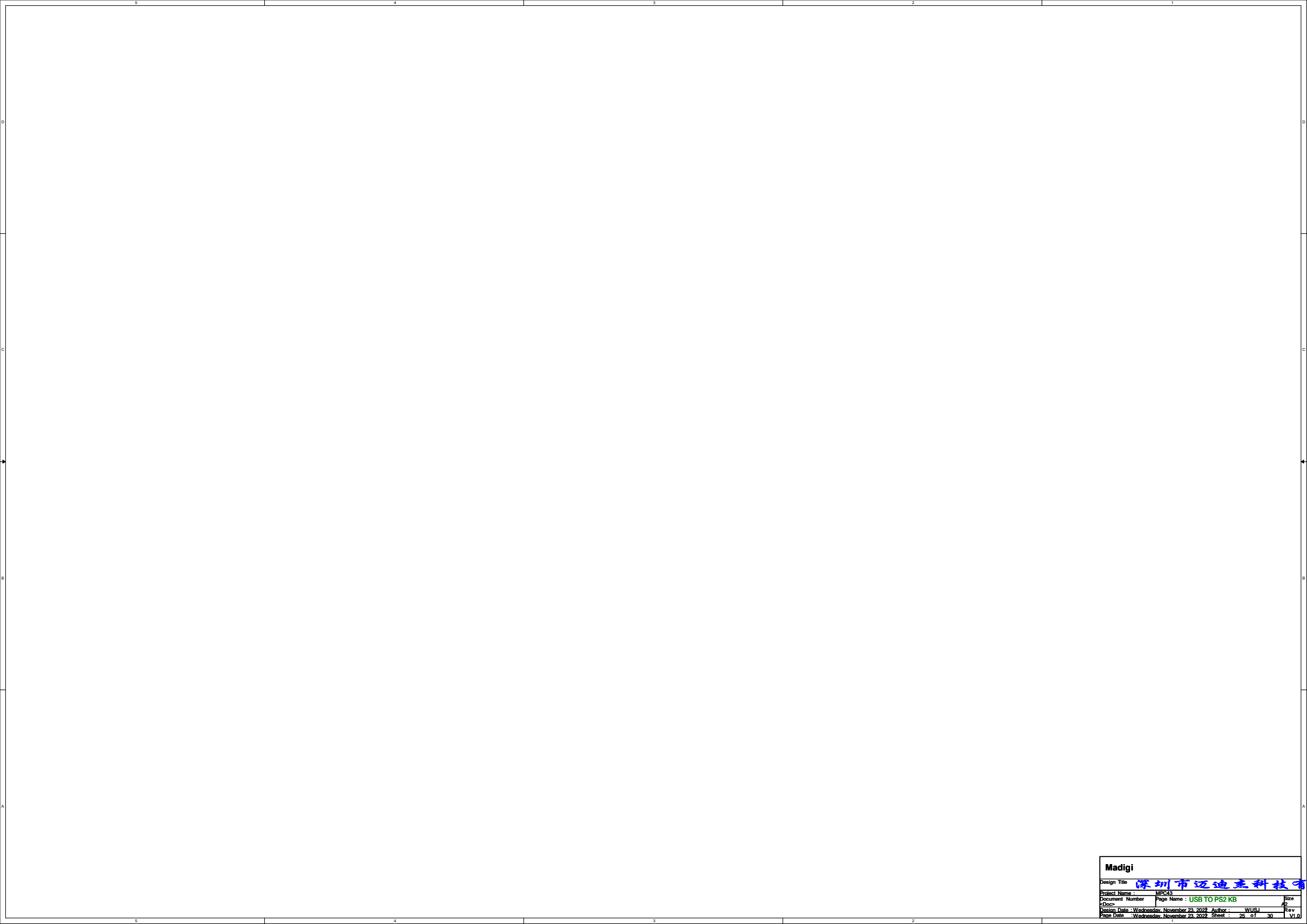
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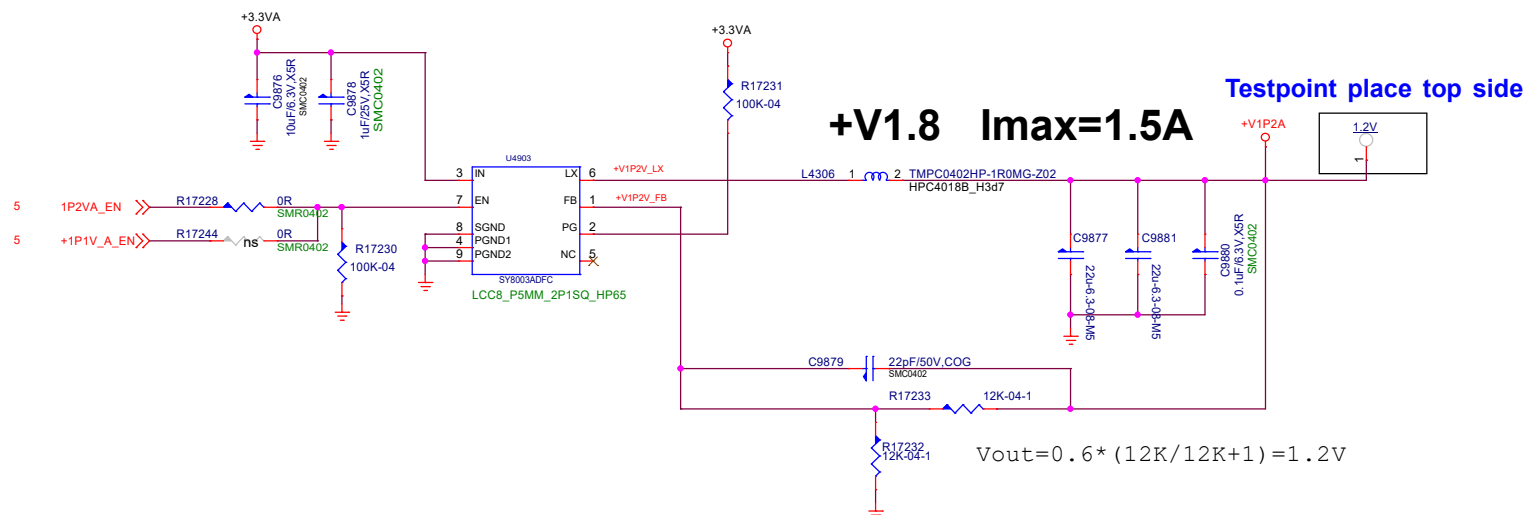


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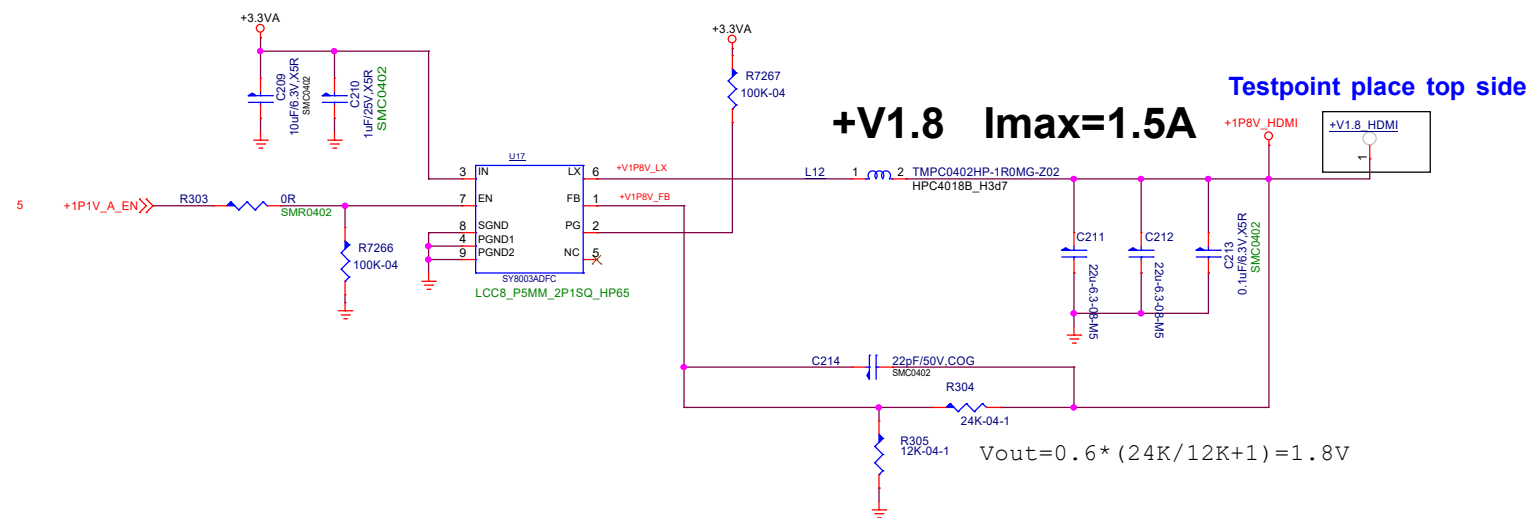


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Print Date : Wednesday, November 23, 2022	Sheet : 26 of 30	V1	



+1P8V_HDMI



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Page Date : Wednesday, November 23, 2022	Sheet : 29 of 30	V1.0	

2022.1.14 V11 版

- 1.P4 HDA_SEL~~端~~预留 8V A 上 拉
- 2.P5 EC_PROCHOT_N和PROCHOT_~~端~~网络，同时c o l ay
- 3.P10 DDP1_CLK~~连~~ISPSC，DDP1_D~~直~~连ISSDA。+1P8VHDMI~~新~~电 间 增 加 0 R 电 阻~~预~~
- 4.P11 DDP2_CLK~~连~~ISPSC~~2~~，DDP2_D~~直~~连ISBDA2。+1P8VHDMI~~和~~电 间 增 加 0 R ~~预~~留
- 5.P14 SSD~~改~~为3.3~~电~~同时 做3.3 V~~o~~~~u~~
- 6.P16 BACK USB2.0~~改~~用USB_P5_DP~~改~~~~端~~修改~~路~~名

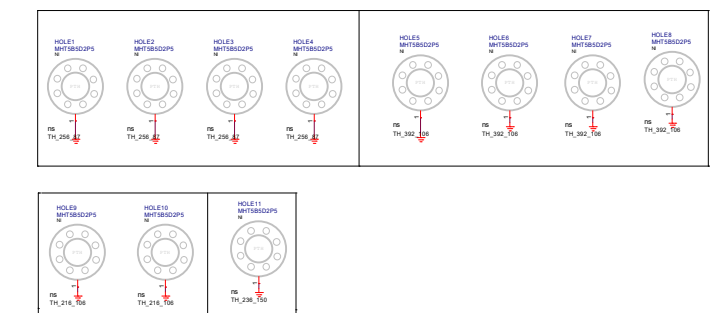
2022.2.24 增修

- 1.P14 PCH_SATA2_PEDET~~微~~电由3V~~改~~为A，同时~~预~~留3~~做~~co~~u~~；SS D电改 回3.3V来供
- 2.P22 卡1~~端~~信号修 改， R12109 no s tuff,R539 stuff;~~u~~DET信号上拉电阻改为1M

2022.3.4 增修改

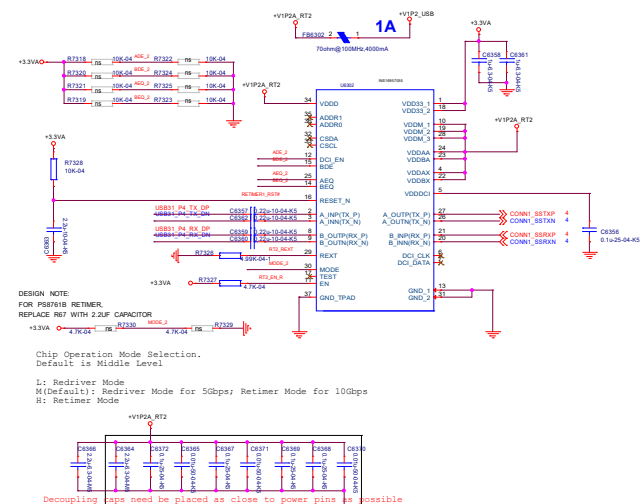
- 1.P14 SSD_DET#~~修~~改+3~~电~~，预留+33V_SD 做~~a~~y

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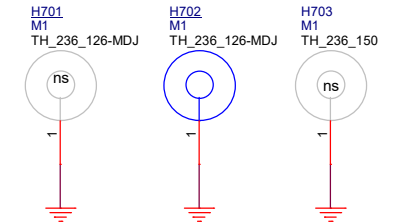
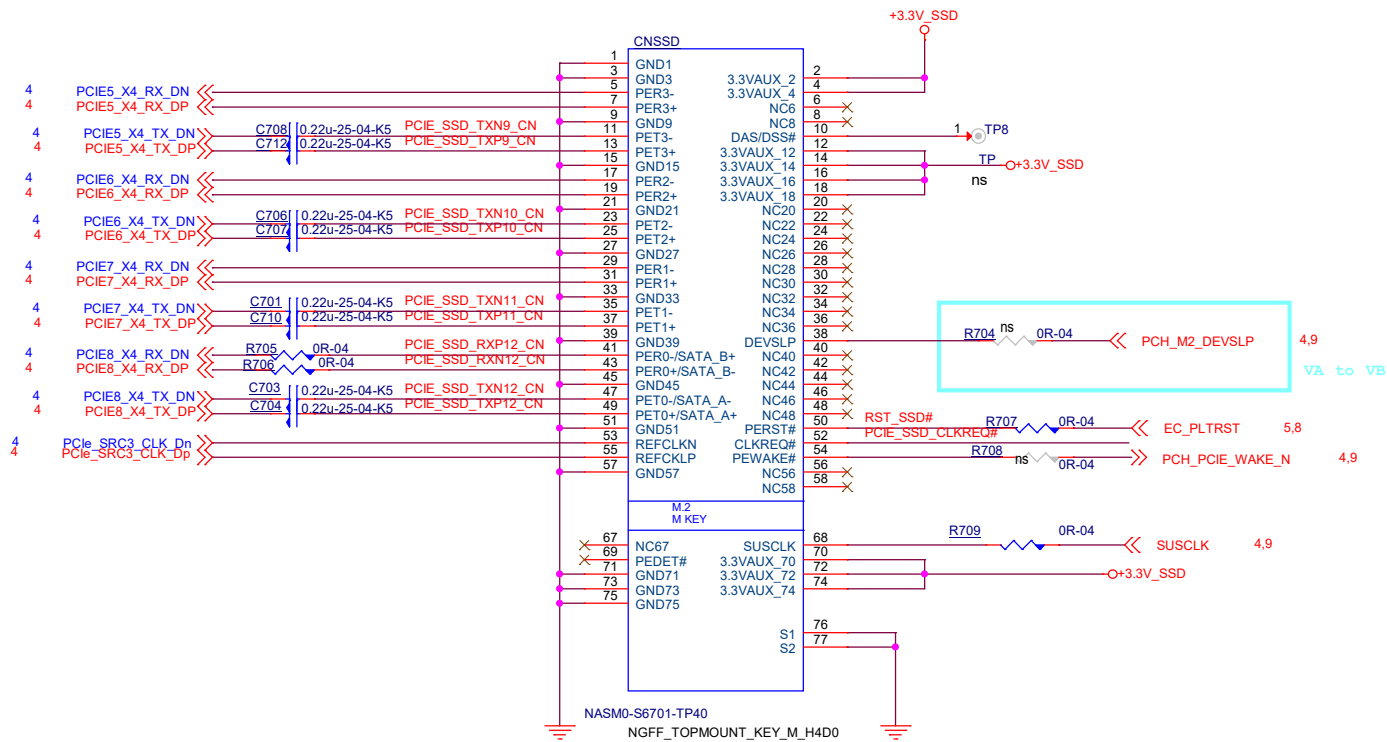
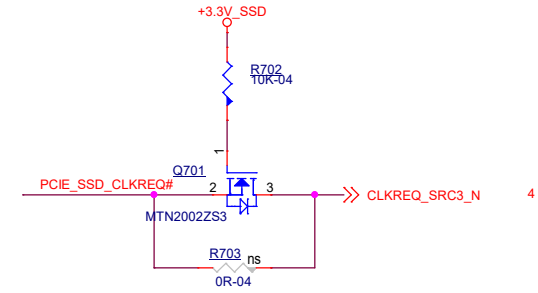
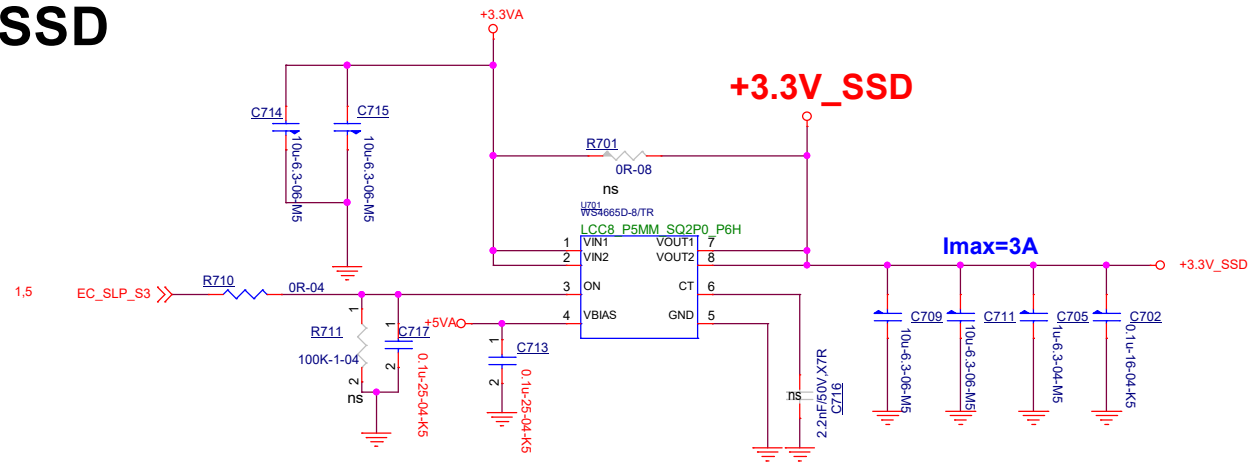


USB3.0

+V3P3A/+V5P0A POWER SUPPLY

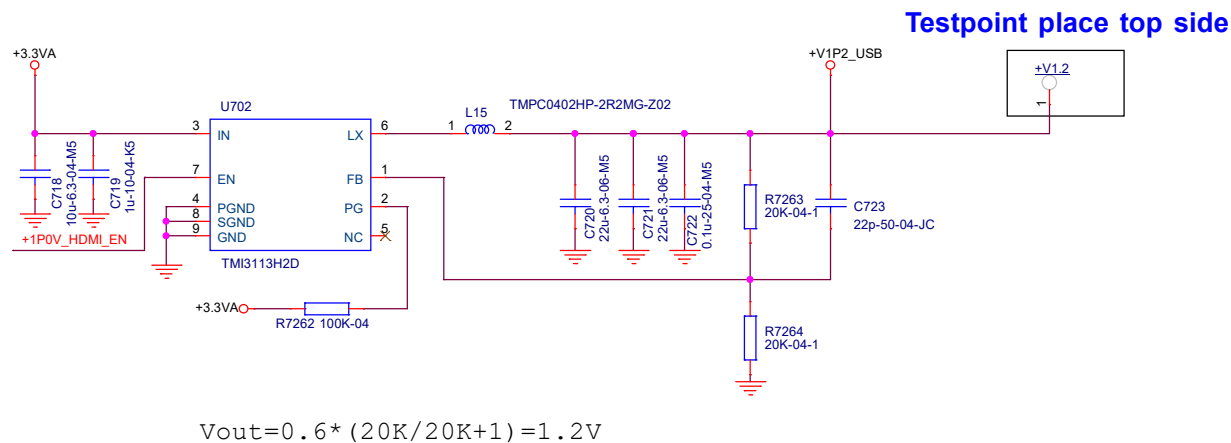
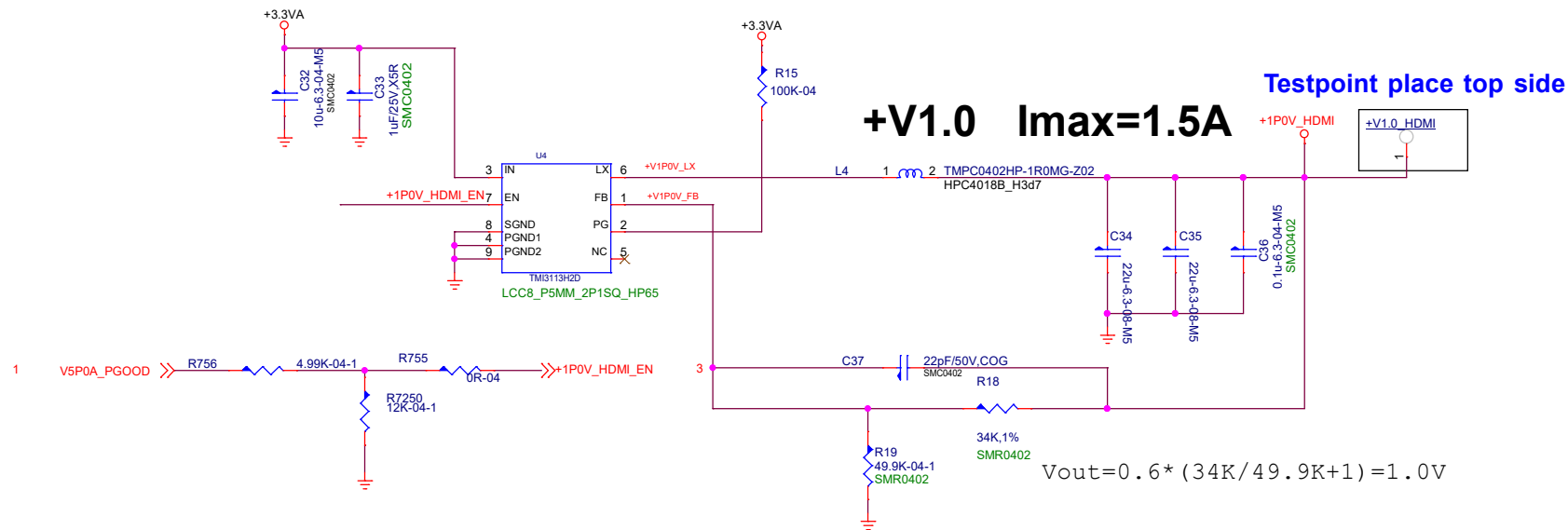


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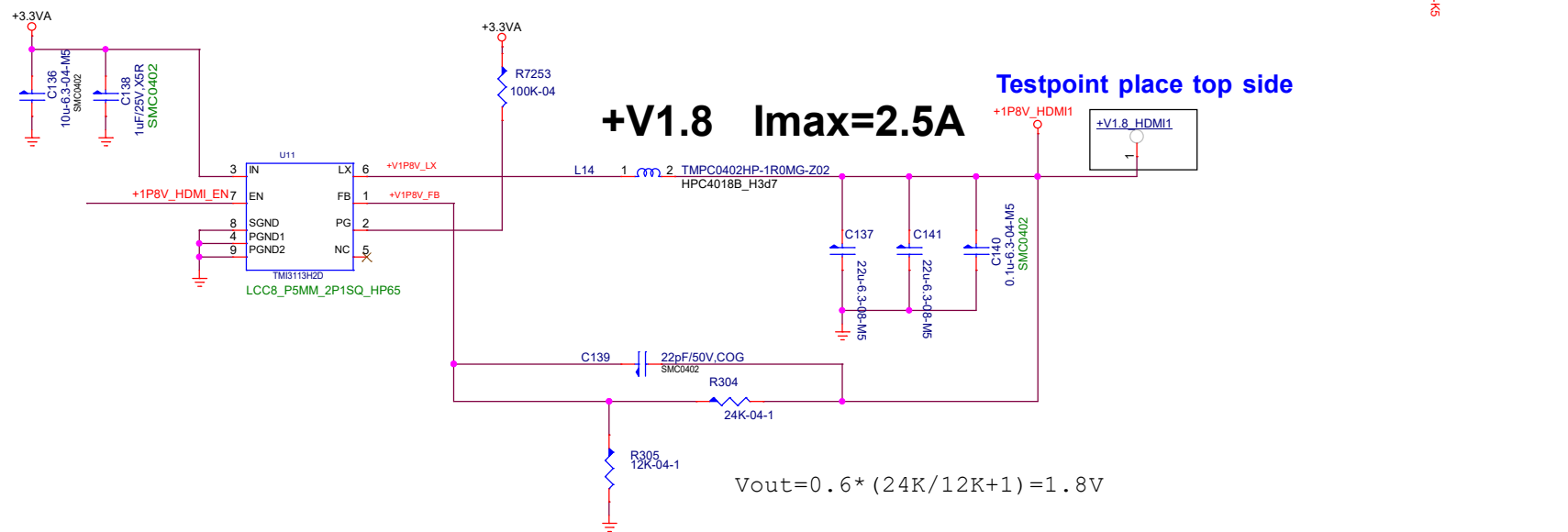
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+1P0V_HDMI



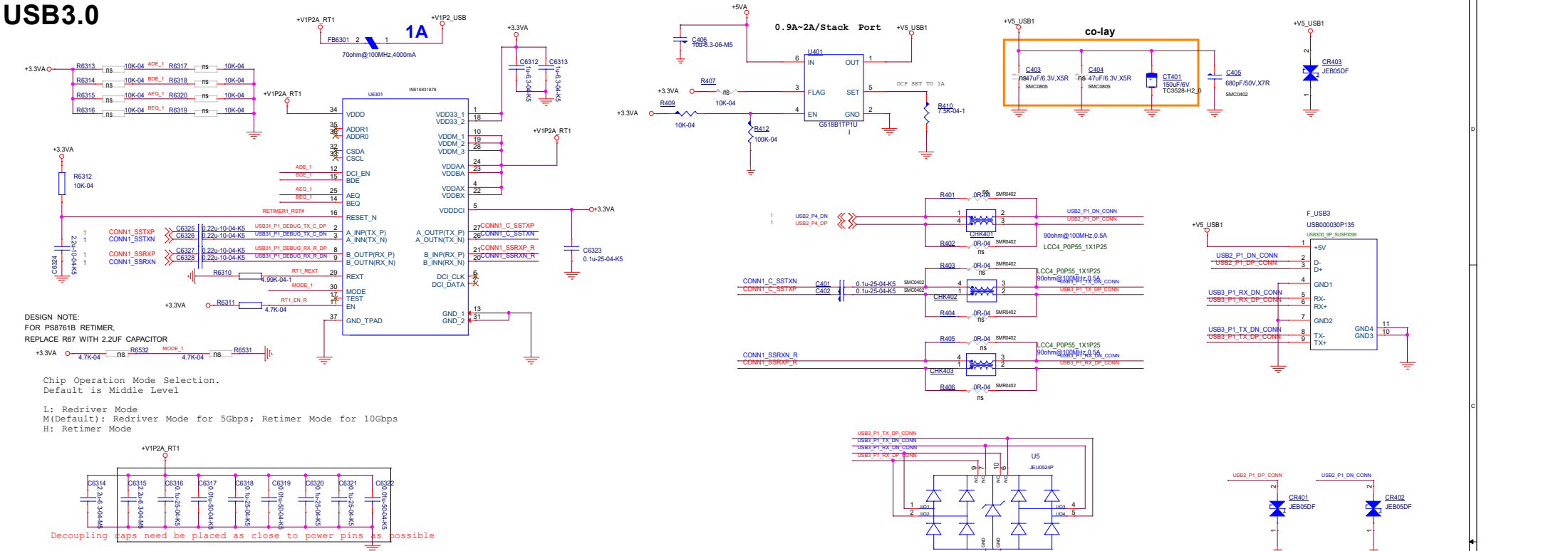
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+1P8V_HDMI

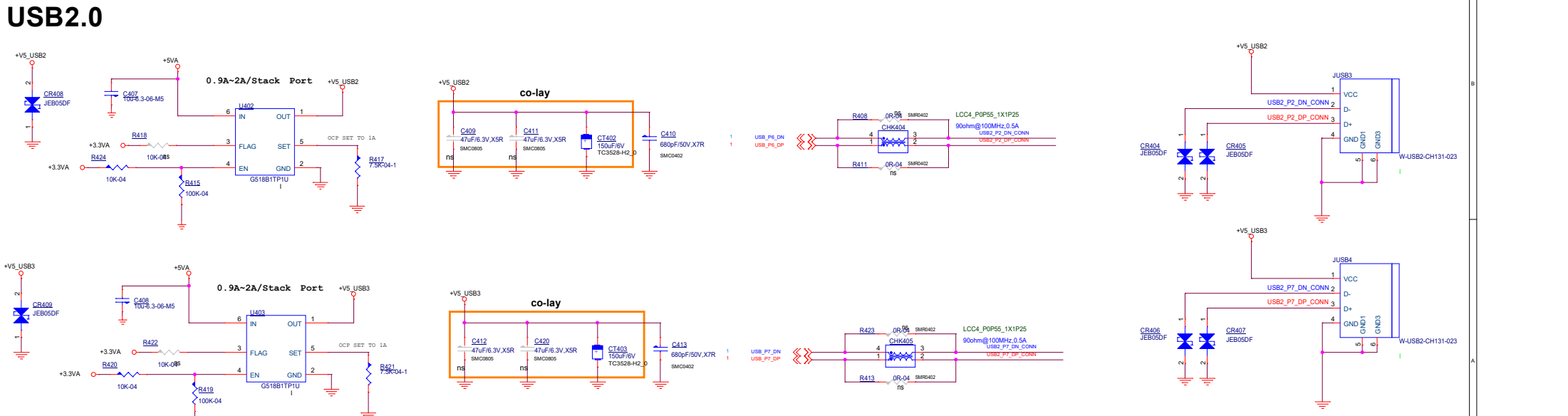


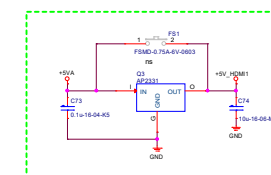
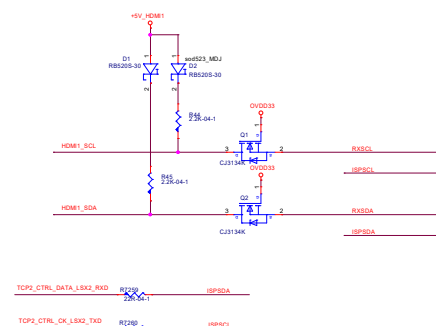
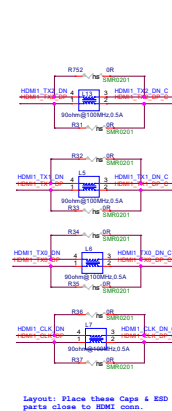
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Date: Thursday, March 16, 2023		Sheet	3 of 6

USB3.0

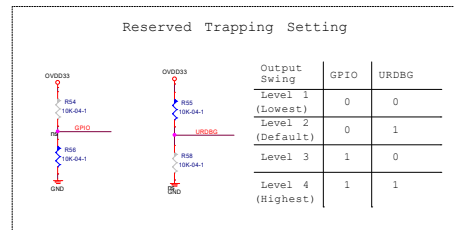


USB2.0





Description	Signal Mapping	
	TCP	HDMI
Main Link (Tx)	TCP_TX0	HDMI Data_2
	TCP_TX1	HDMI Data_0
	TCP_TXRX0	HDMI Data_1
	TCP_TXRX1	HDMI CLK
Note: Apply to TCP ports only.		



For fine-tune CLK rise time and close to chip



0.5p-25-02-C3 (closed to Chip)

Add 0.5pF on TXCP/M to fine-tune rise and fall time

