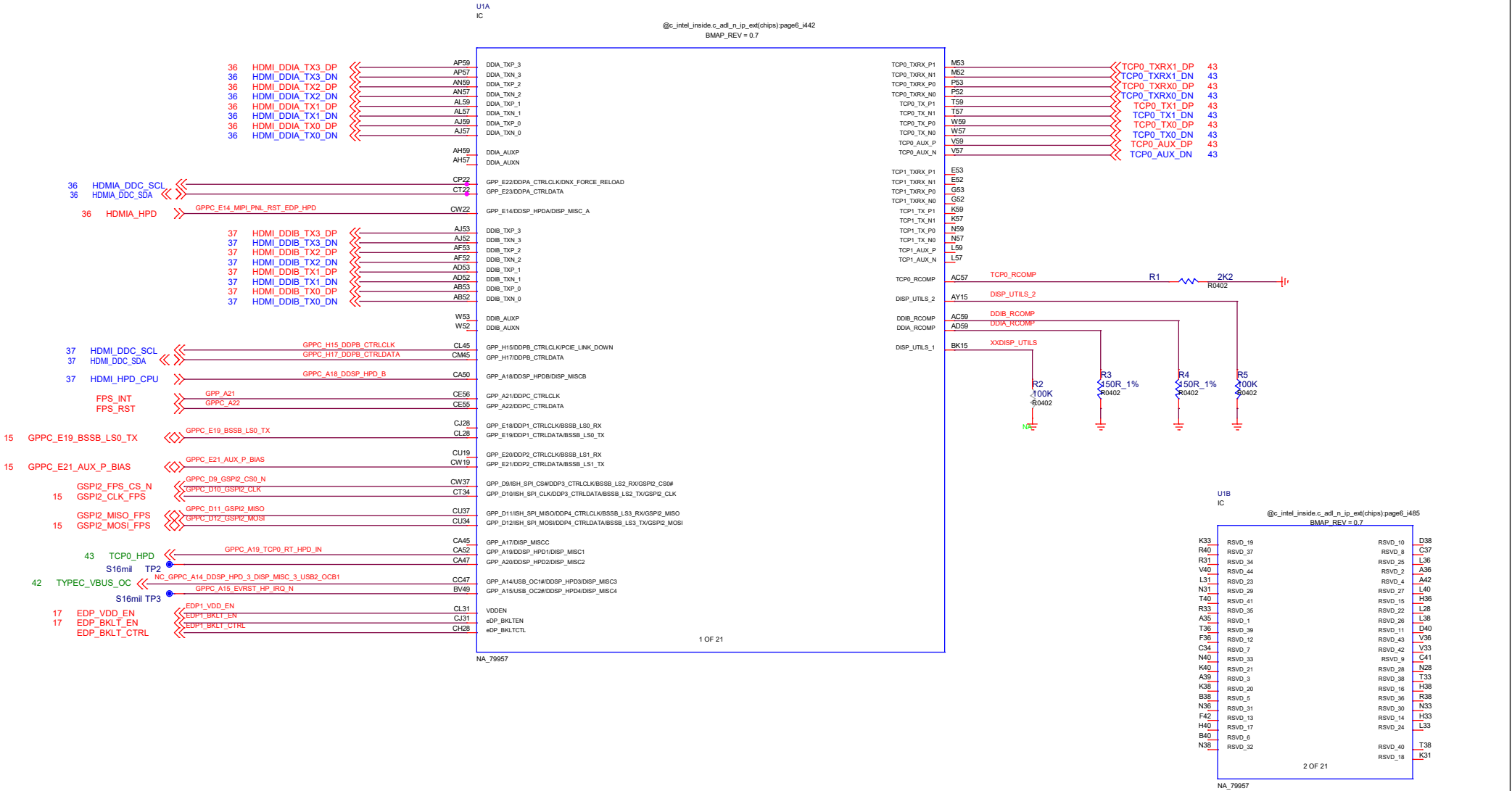
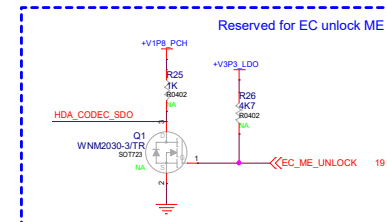
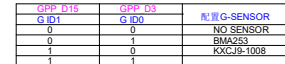
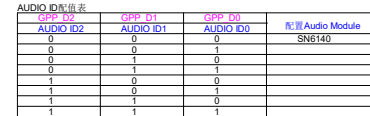


04_ADL-N MCP-DISP

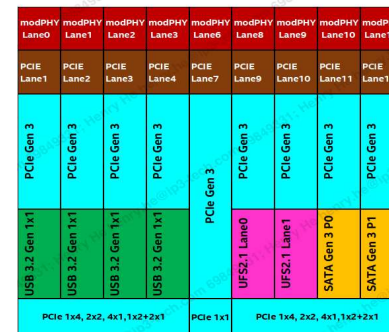


BMAP_REV = 0.7



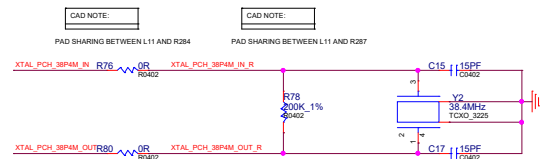
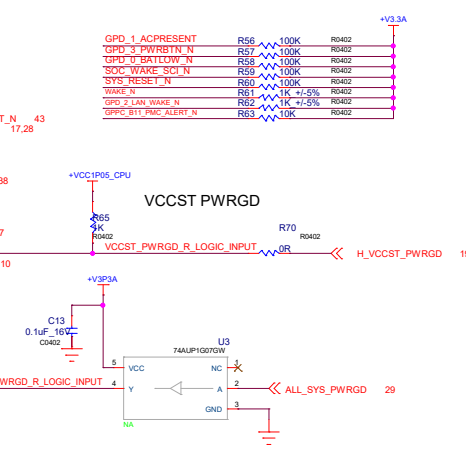
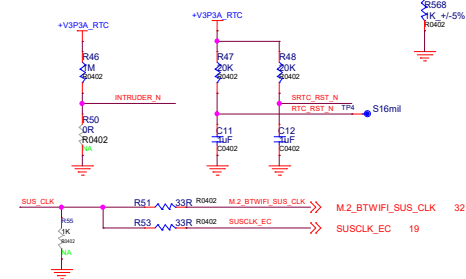
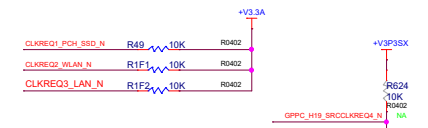
英众科技		Title _____ Drawn By _____	
Size	Document Number	Rev	
B	07_ADL-N MCP - EMMC	1.0	
Date	Monday, March 14, 2022	Sheet	7 of 45

Alder Lake-N HSIO Lane Assignments

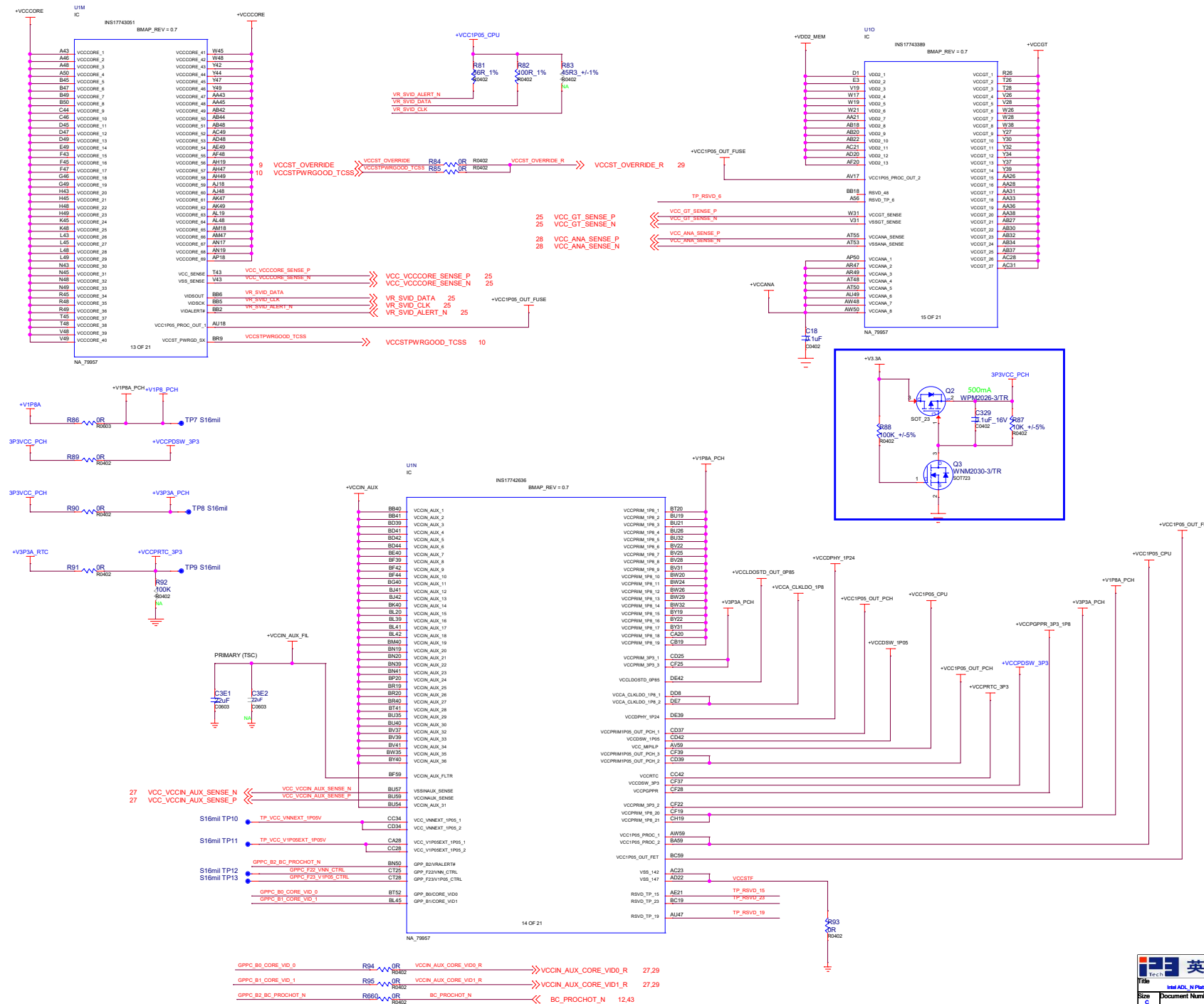


- Total 9 ModPHY Lanes
- Up to 9 PCIe* Gen 3 lanes with 5 PCIe* Clks
- Up to 4 USB3.2 Gen 2x1
- Up to 2 SATA3
- 4 USB3.2 Gen 1x1 + PCIe* muxed lanes
- 1 PCIe* only lanes
- 2 PCIe + UFS2.1 muxed lane
- 2 PCIe + SATA muxed lane

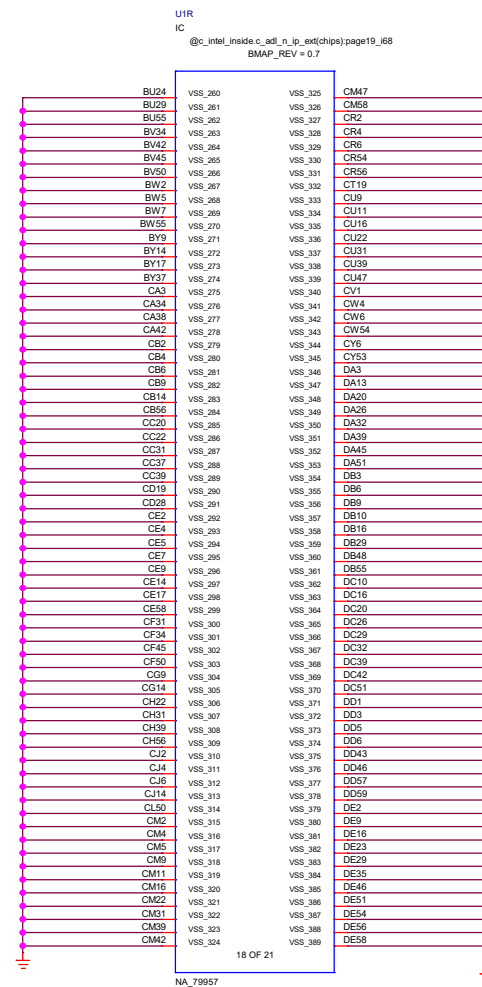
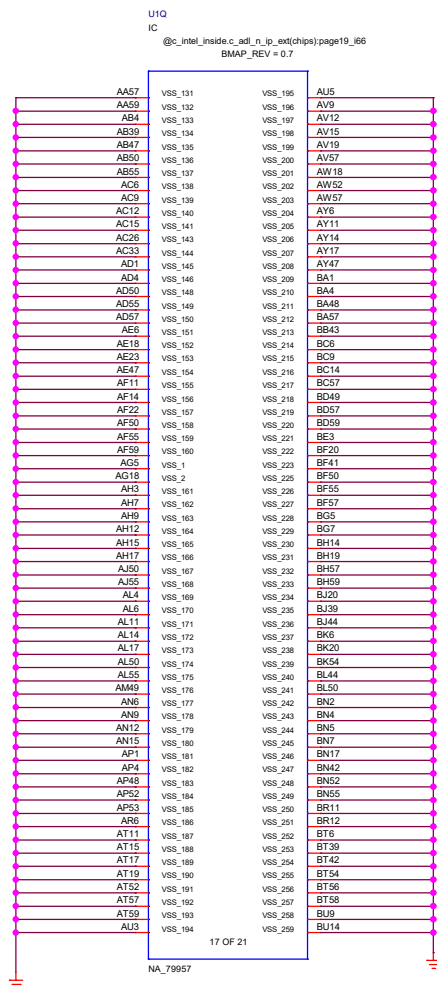
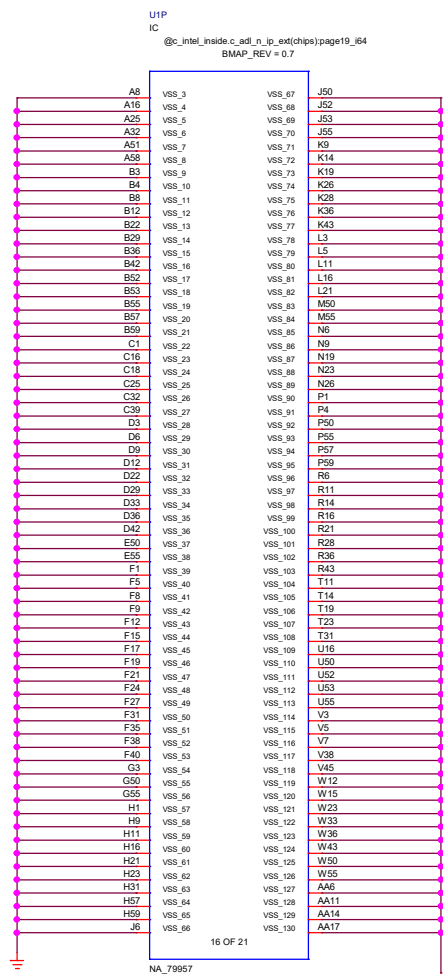
32.768KHZ



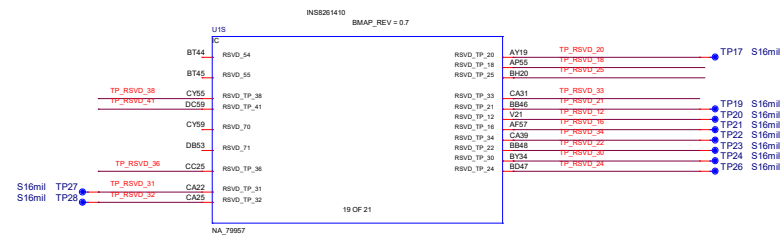
10 ADL-N MCP - CPU-POWER



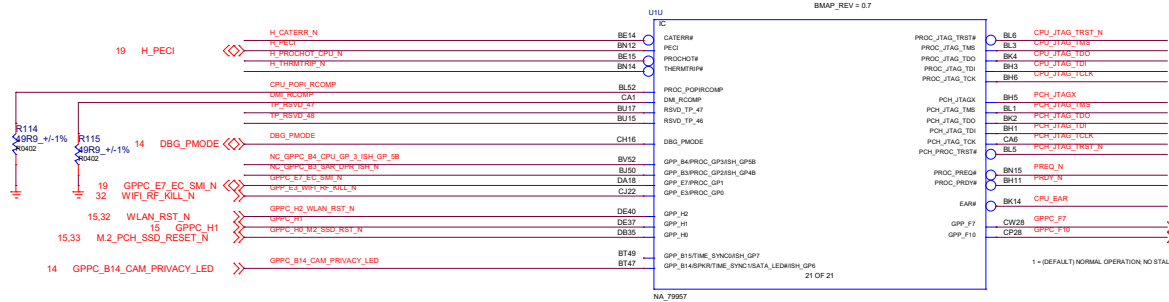
11_ADL-N MCP GND



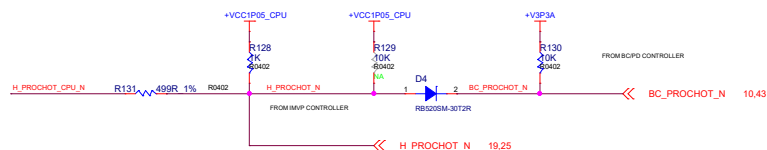
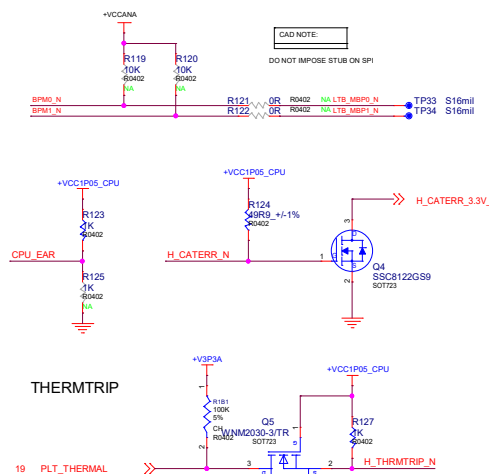
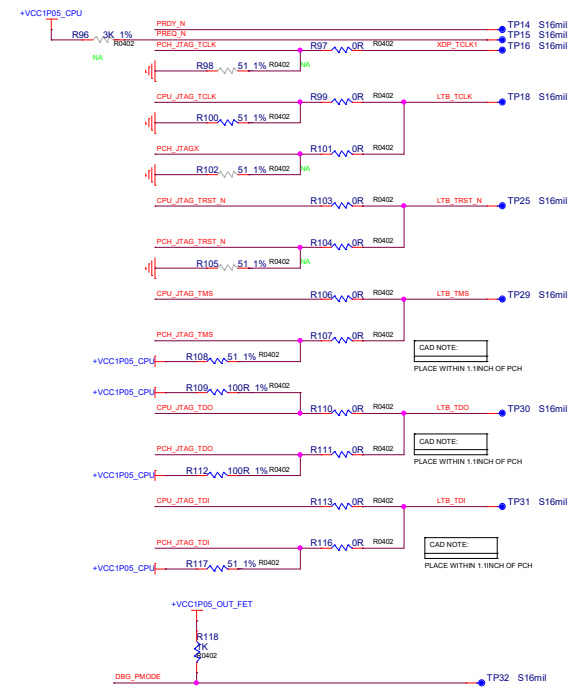
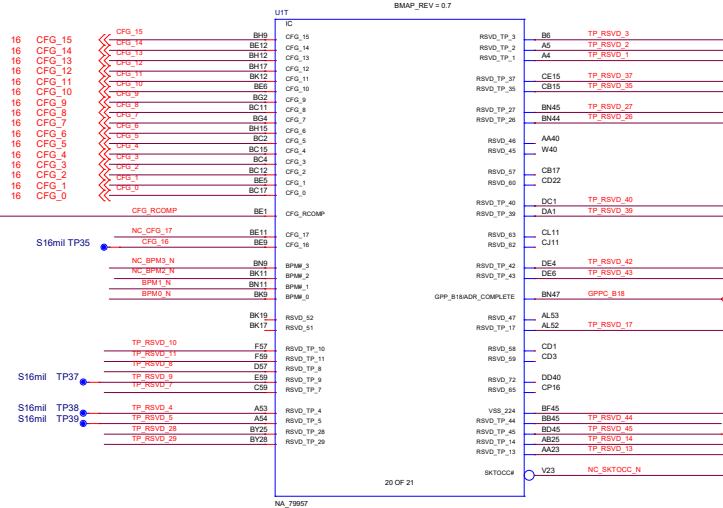
12_ADL-N MCP FIV& CPU&DEB



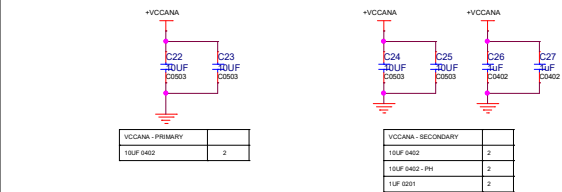
@c:\inf\msh-c_and_p_en\chips\page21_238 BMAP_REV = 0.7



INSB26321 BMAP_REV = 0.7

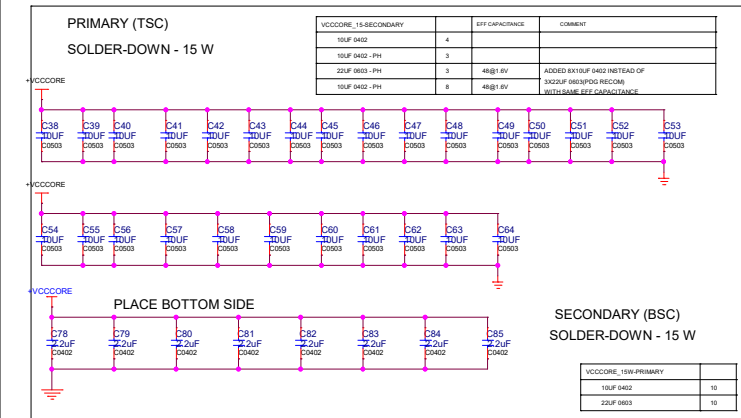


VCCANA PDBOM

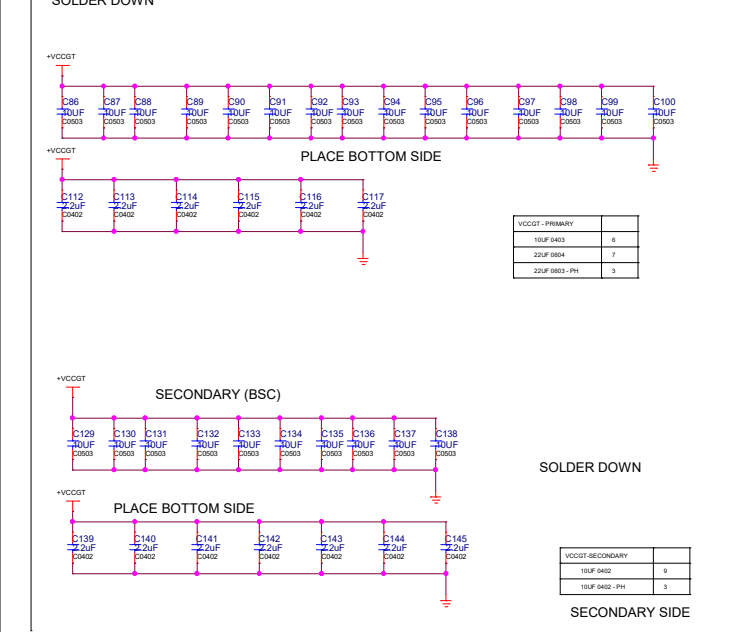


PLACE BOTTOM SIDE

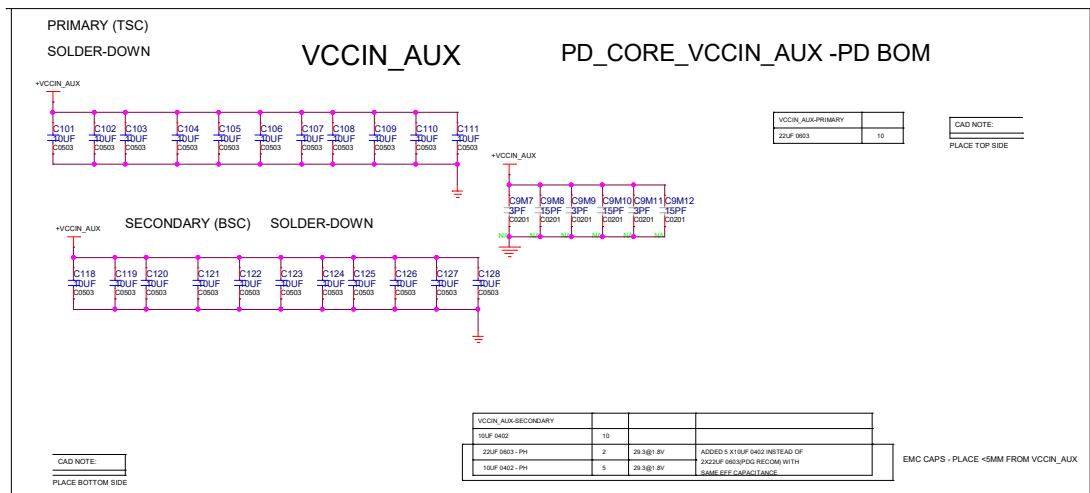
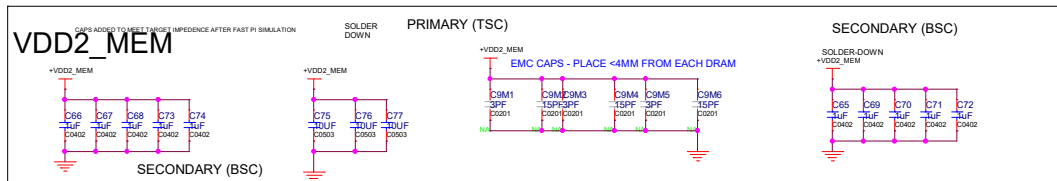
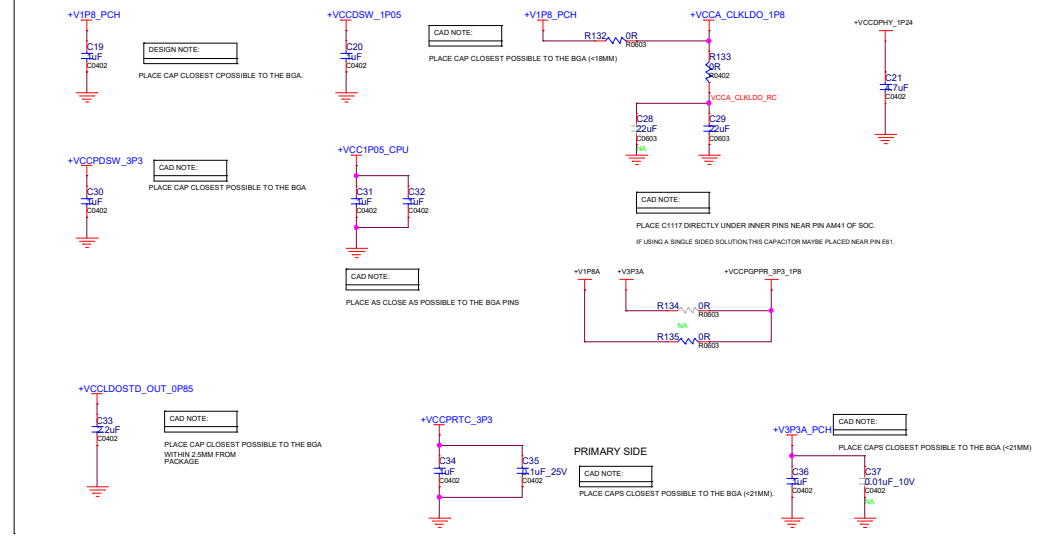
PD_CORE_PD BOM (VCCCORE)



PD_CORE_PD BOM (GT)



PCH_PD BOM

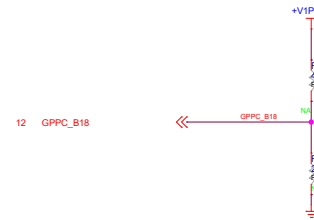


14_PCH STRAPS



TOP SWAP OVERRIDE

HIGH- TOP SWAP ENABLED
LOW-DISABLED
WEAK INTERNAL PD 20K
SAMPLING- PCH_PWROK



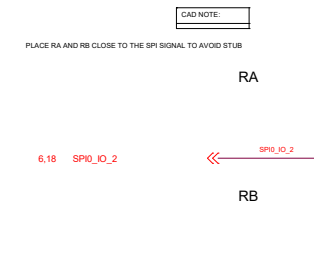
NO REBOOT

HIGH - NO REBOOT
LOW - REBOOT ENABLED
WEAK INTERNAL PD 20K
SAMPLING- PCH_PWROK



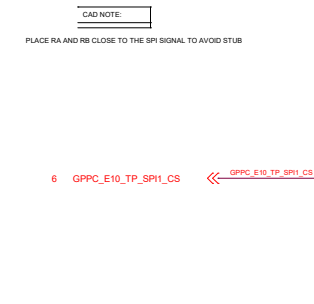
TLS CONFIDENTIALITY

LOW - TLS CONFIDENTIALITY DISABLE
HIGH - TLS CONFIDENTIALITY ENABLE
WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

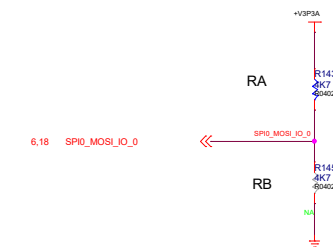


CONSENT STRAP

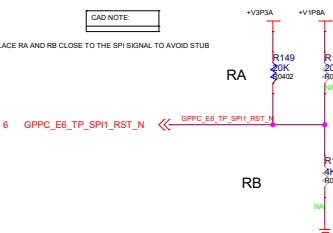
HIGH: DISABLED
LOW: ENABLED
NO INTERNAL PU/PD
SAMPLING - RSMRSTB



ESPI OR EC LESS
HIGH: ESPI IS DISABLED
LOW: ESPI SELECTED
WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

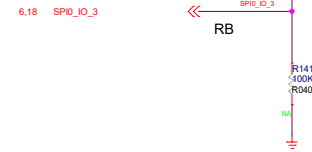


BOOT HALT
HIGH - DISABLED
LOW - ENABLED
NO INTERNAL PU/PD
SAMPLING - RSMRSTB



JTAG ODT DISABLE
LOW: JTAG ODT DISABLED
HIGH: JTAG ODT ENABLED
NO INTERNAL PU/PD
SAMPLING - RSMRSTB

CAD NOTE:
PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB



DESIGN NOTE:
NOTE 2: STUFF RA WHEN WE ARE VALIDATING 100MHZ FLASH

A0 PERSONALITY STRAP

HIGH: DISABLED
LOW: ENABLED
NO INTERNAL PU/PD
SAMPLING - RSMRSTB

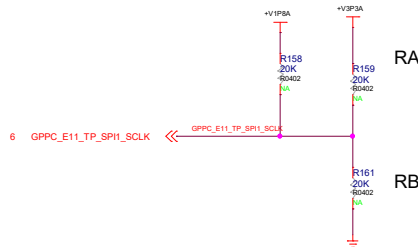


DFXTESTMODE

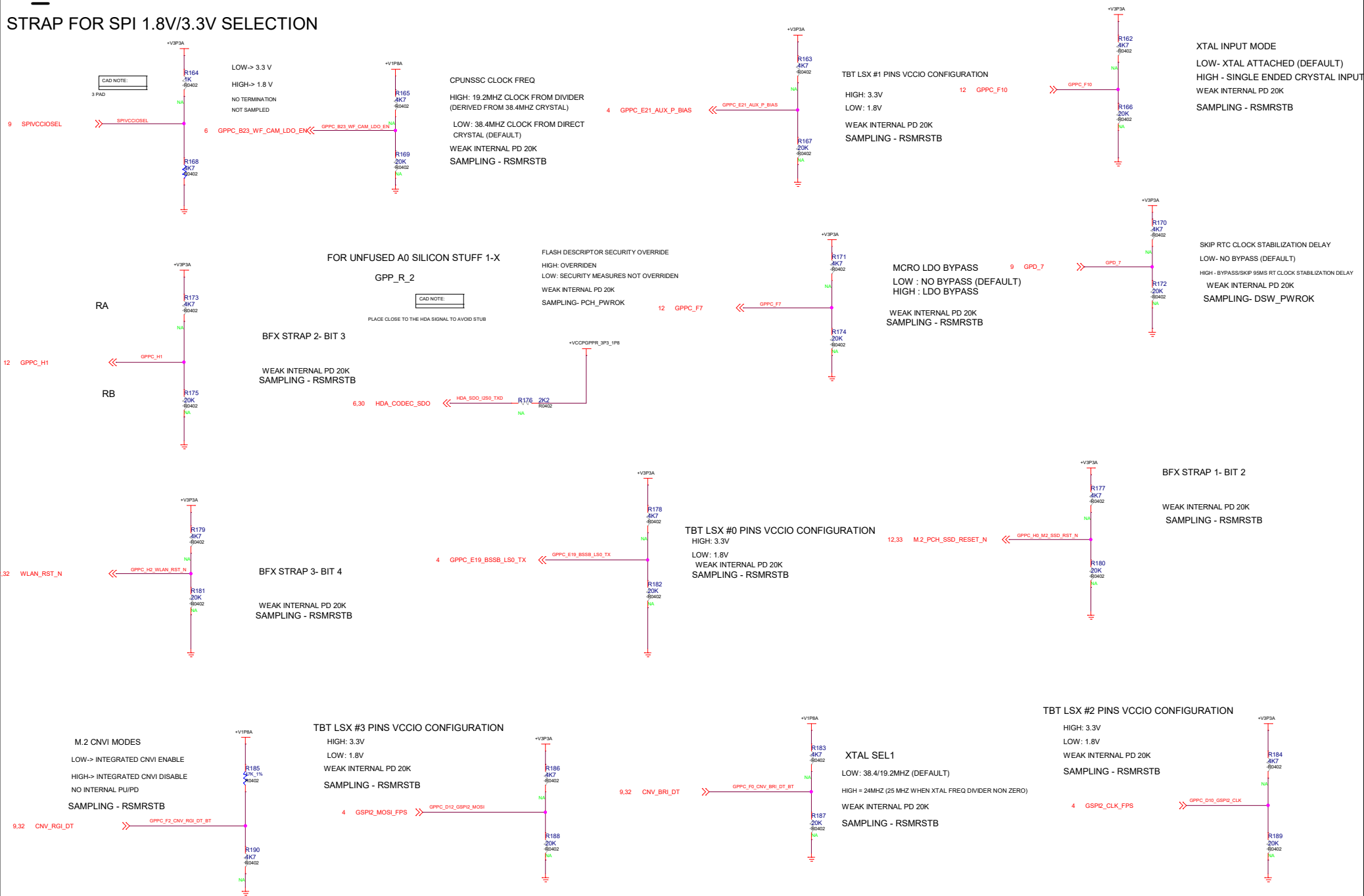
PGDMON
HIGH - DFXTESTMODE DISABLED(DEFAULT)
LOW - DFXTESTMODE ENABLED
WEAK INTERNAL PU 20K
SAMPLING - RSMRSTB



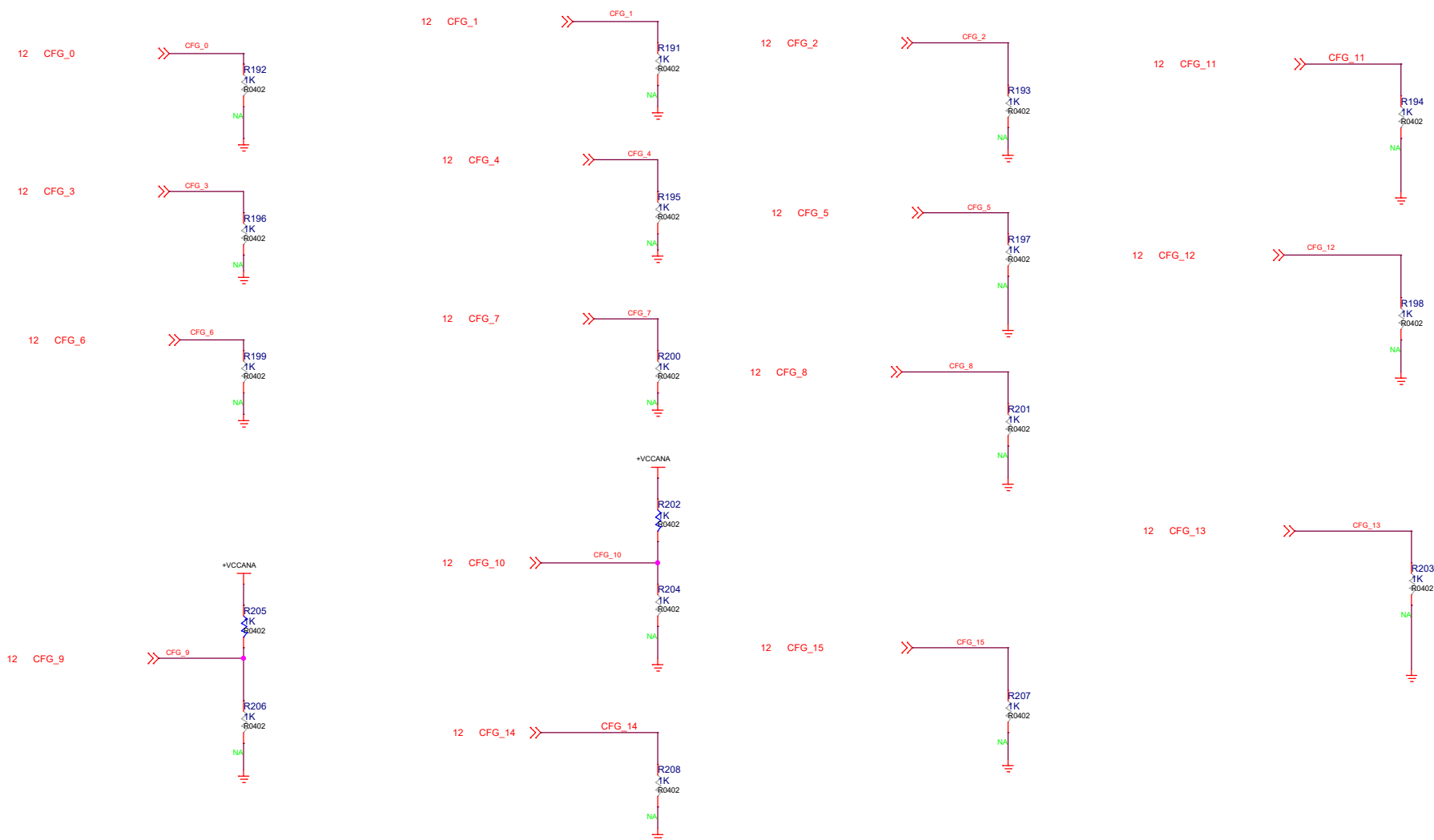
CAD NOTE:
PLACE RA AND RB CLOSE TO THE SPI SIGNAL TO AVOID STUB



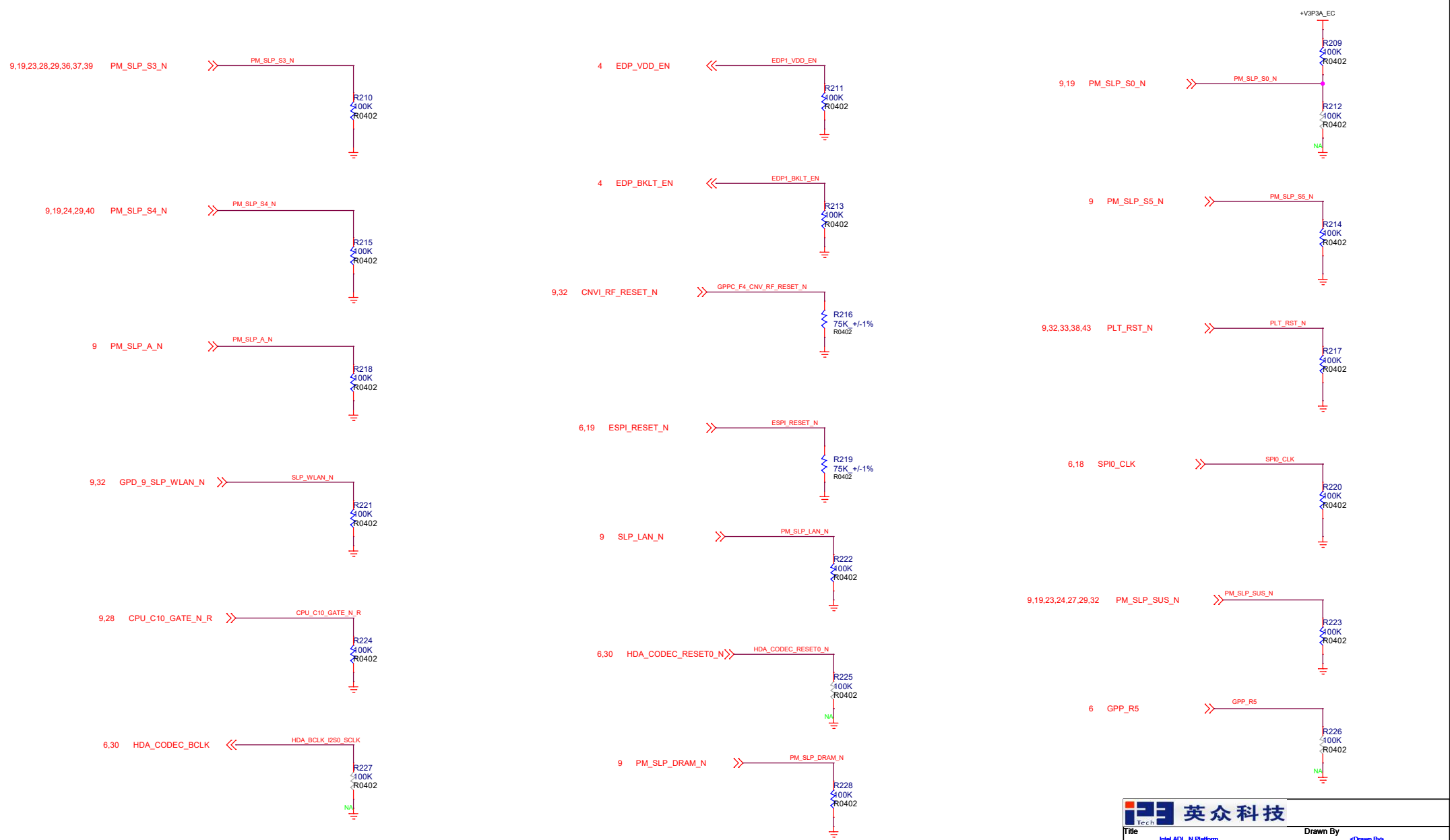
STRAP FOR SPI 1.8V/3.3V SELECTION

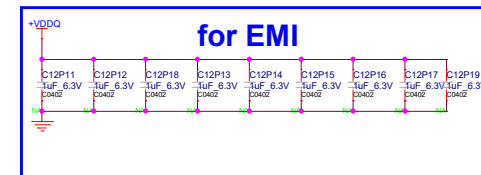
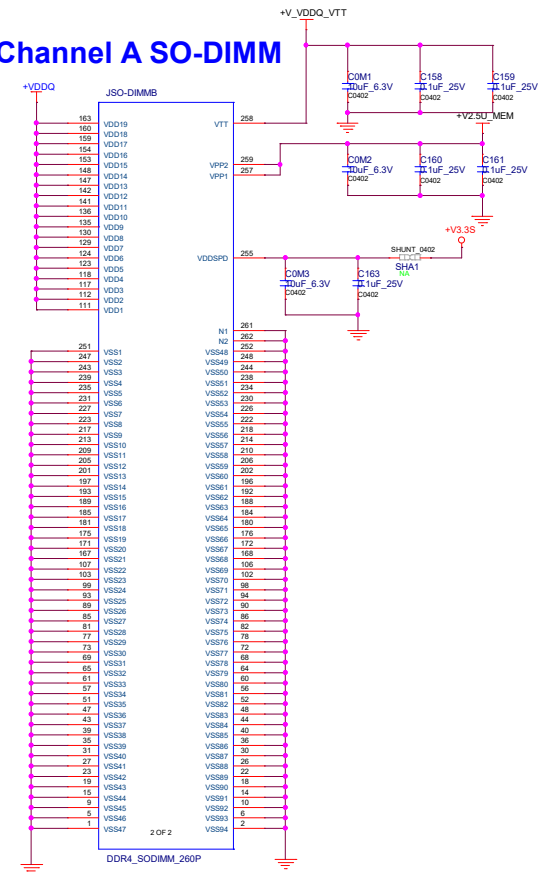
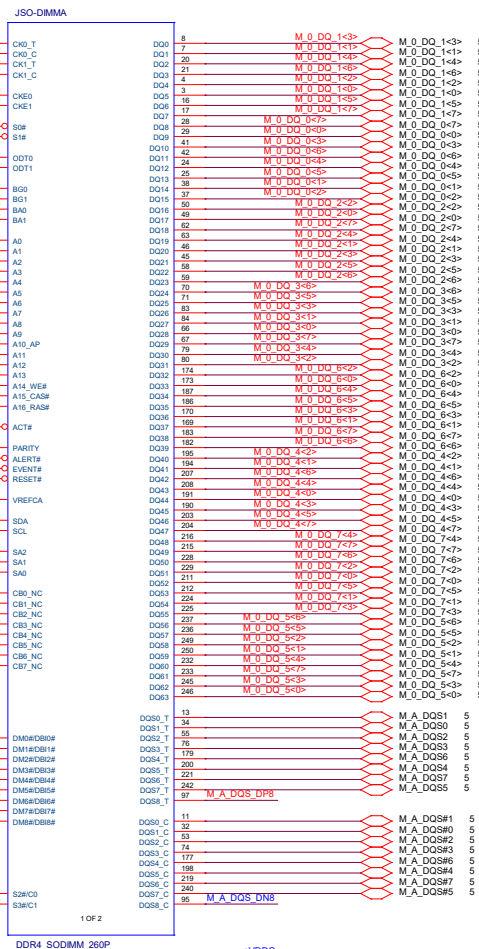
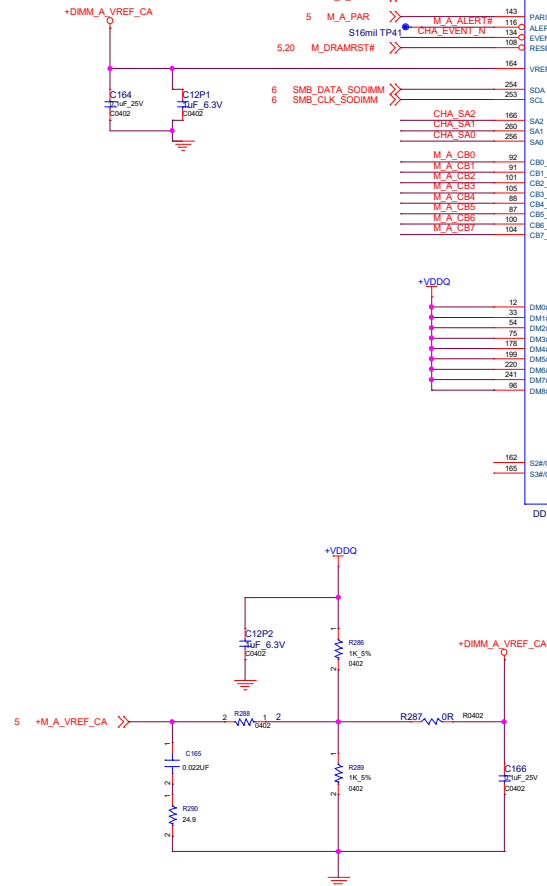


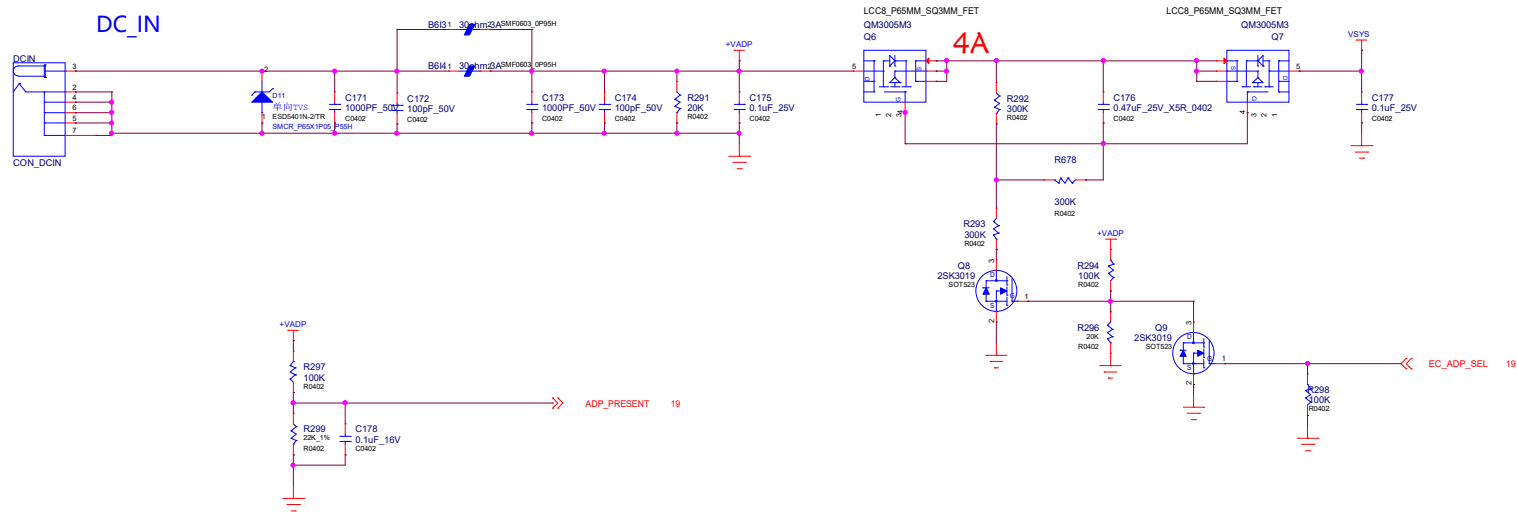
16_CPU_STRAPS



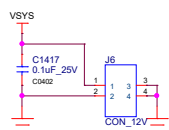
17_GLITCH FREE CIRCUIT



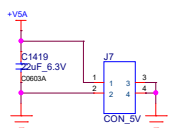




预留外部供电19v

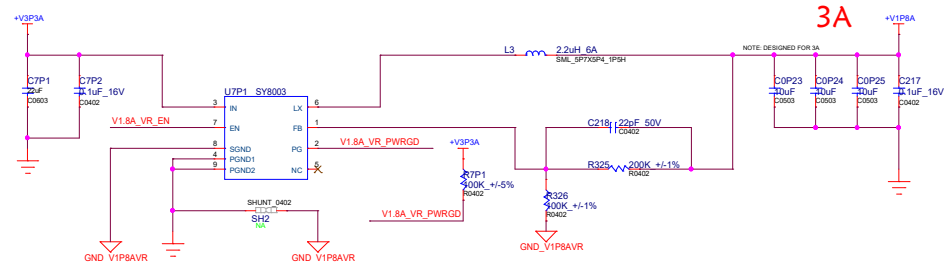
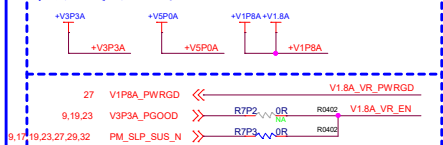


预留5v

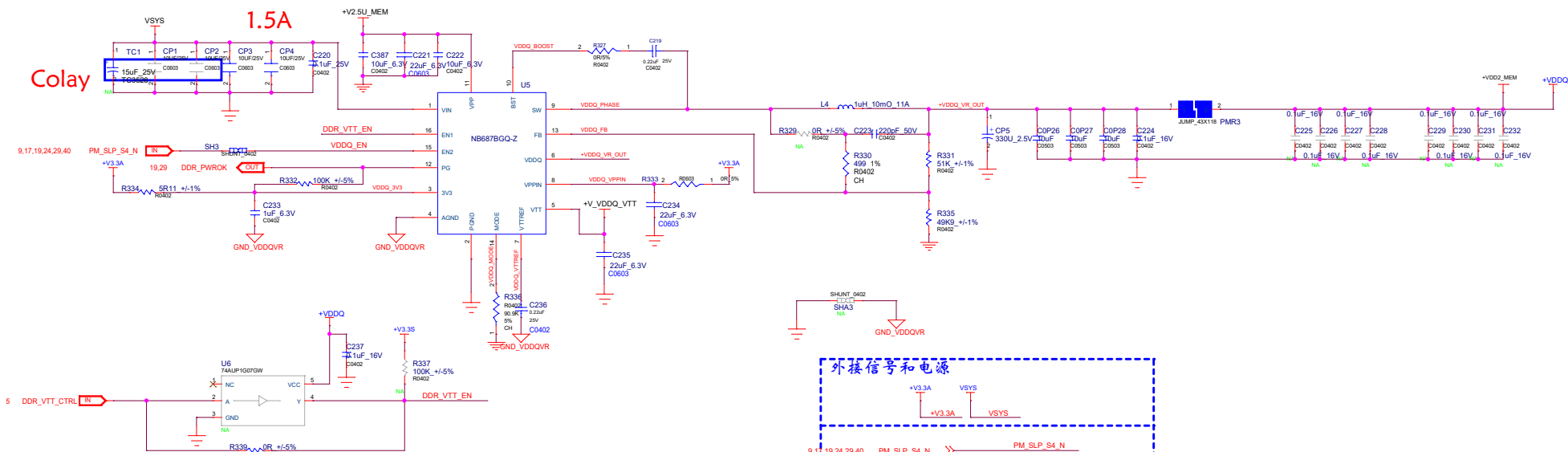


+V1P8A

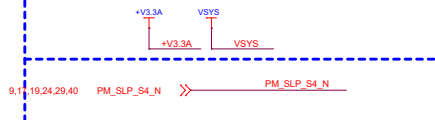
外接信号和电源



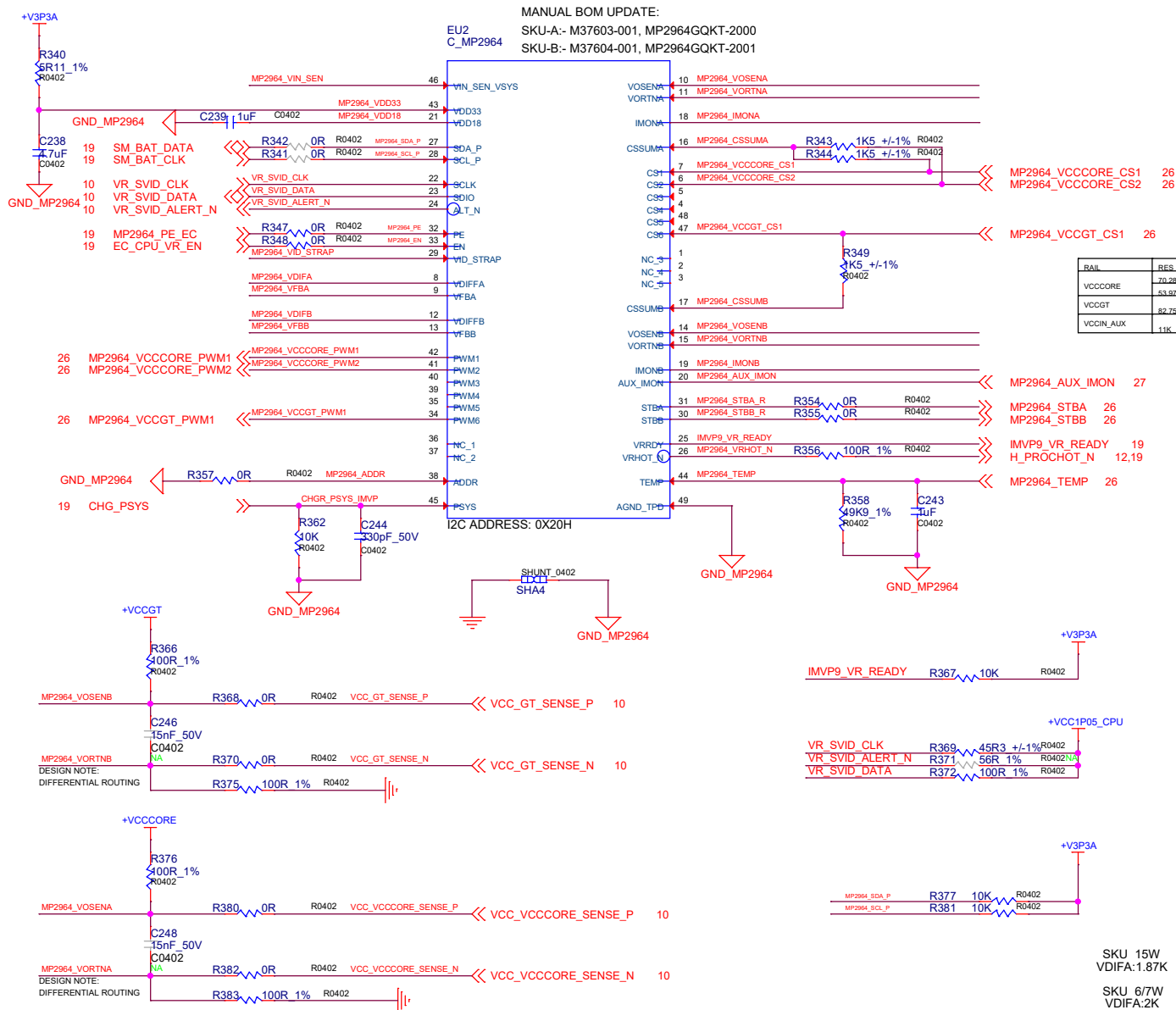
Colay



外接信号和电源



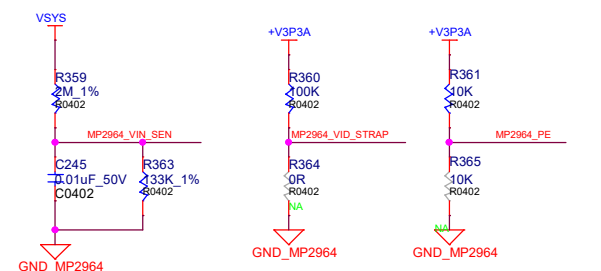
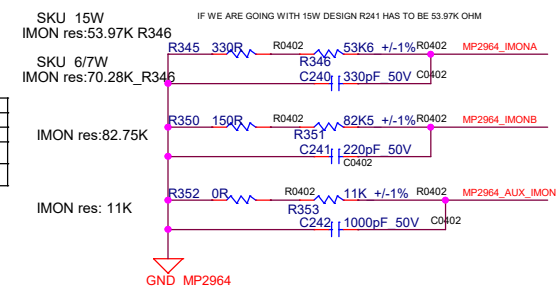
25 PWR IMVP CONTROLLER



VCCIA	(VCCCORE)
VOUT	= SVID
IMAX	= 53 A
FSW	= 800KHZ

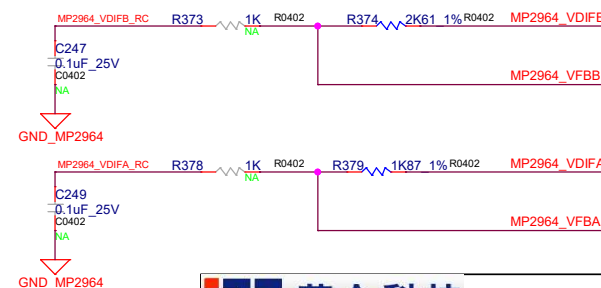
VCCGT	
VOUT	= SVID
IMAX	= 29A
FSW	= 800KHZ

VID_STRAP LEVEL	HIGH	LOW
VID STEP	0.005V	0.010V

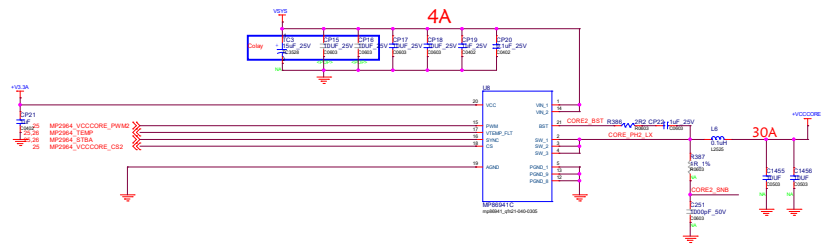
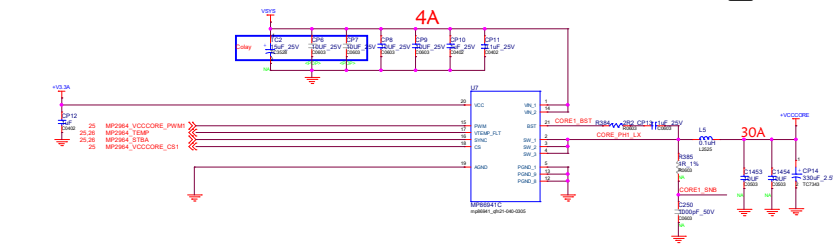


CAD NOTE:

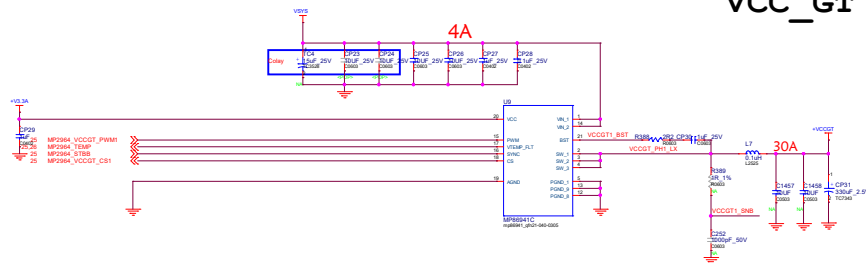
PLACE R121,R123,R126 NEAR EU3



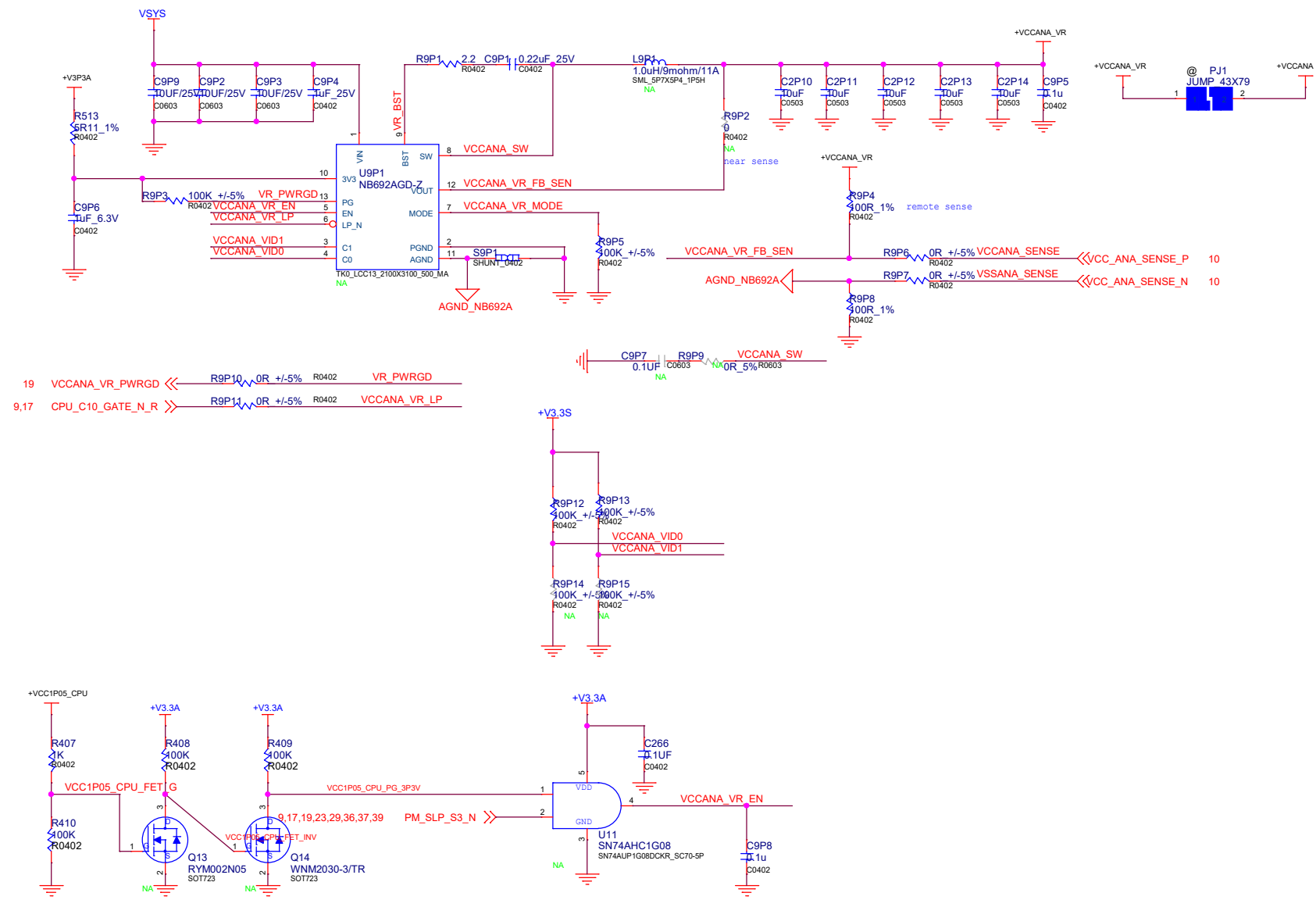
VCC_CORE



VCC_GT

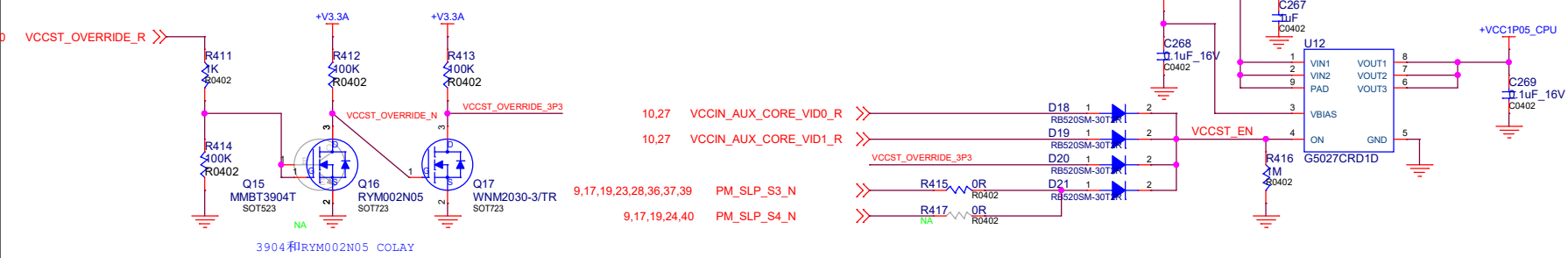


28_VCCANA POWER

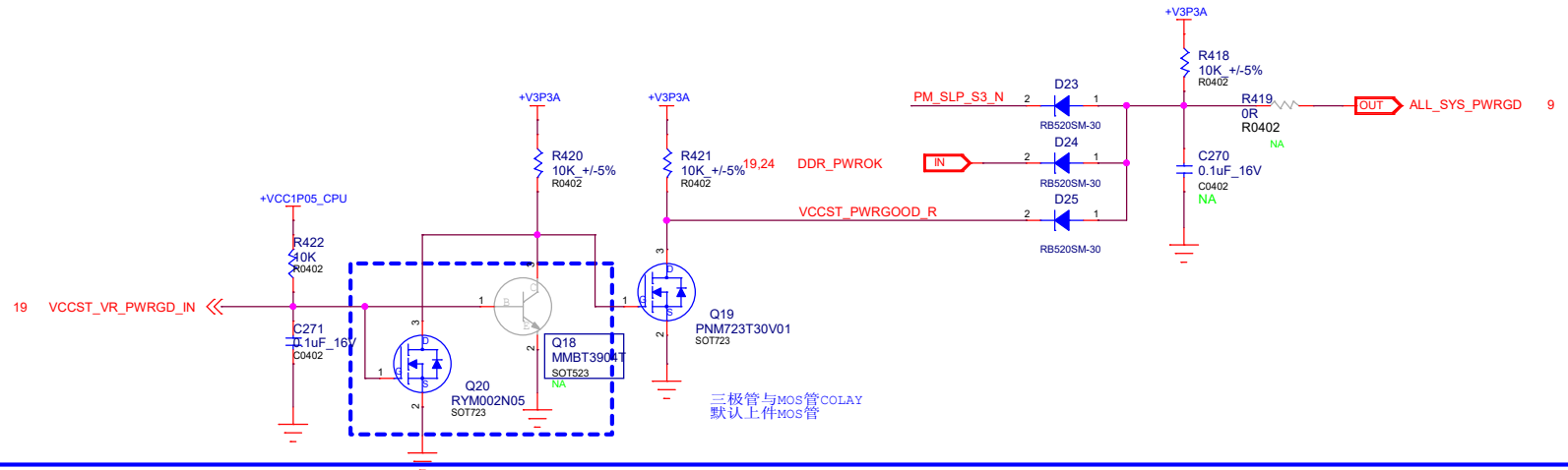


VCCANA	
VOUT	1.05V
SWITCHING FREQUENCY	750 KHz
ICC MAX	3.6A
VR/MOSFET MPN	NB692D
INDUCTOR MPN	TMPC0315H-1R0MG
INDUCTOR IRMS	3.6A
INDUCTOR ISAT	5.8 A
INDUCTOR DCR(TYP)	41 MILLI OHM

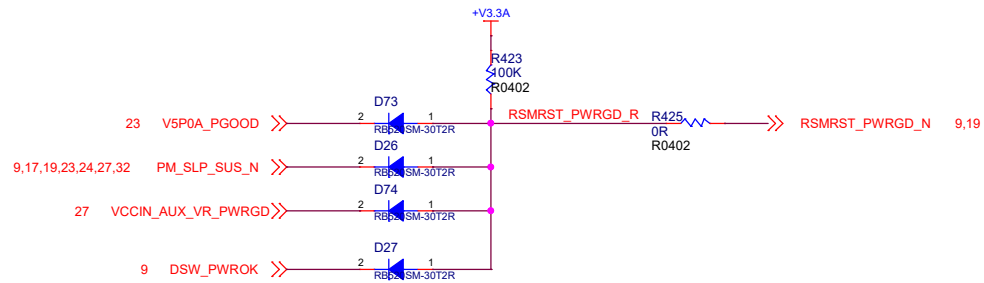
+VCC1P05_CPU

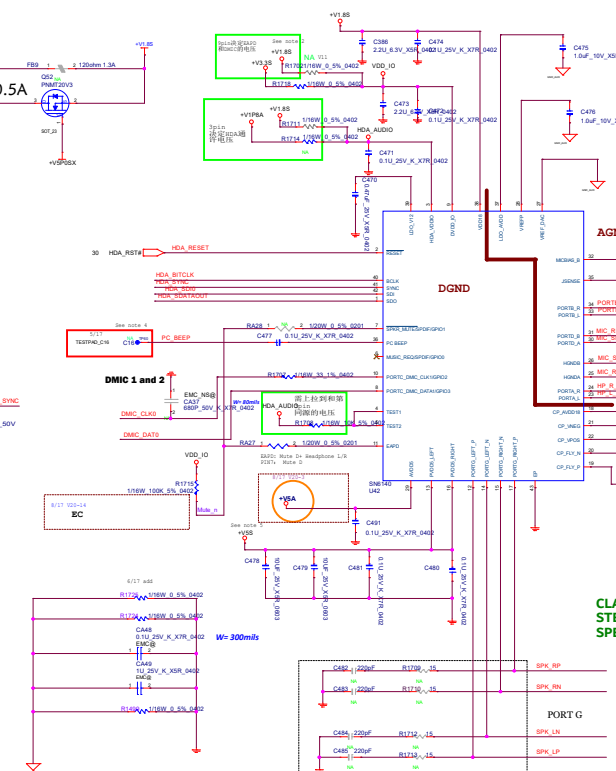
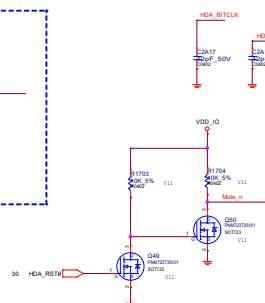
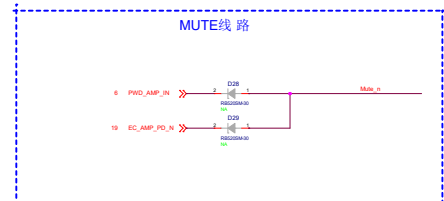
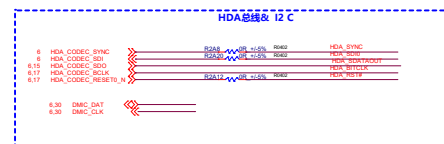


VCCST_VR_PWRGD_IN



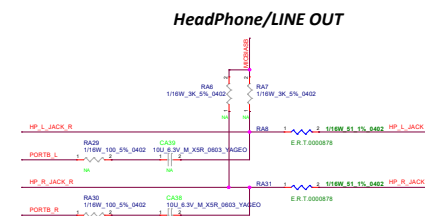
RSMRST PWRGD





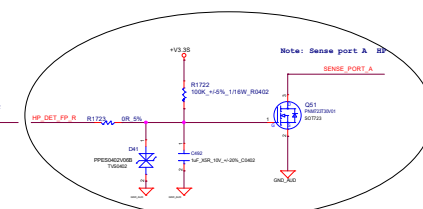
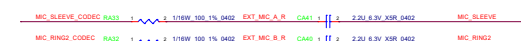
Notes:

- 1.VDD_HDA must be connected to same HDA bus power supply that is used for FCH bus controller(3.3V or 1.8V or 1.5V).
- 2.VDD_IO_3.3V needs the DMIC, SPICL, EPAP and GPIO levels (3.3V or 1.8V).
- 3.Make sure that HDA_BIFSEL, SYNC, SDATA_OUT and RESET# have series terminators at the controller. PC pin 10 has a max level of 1.8V max, need to attenuate signal if 3.3V level.
- 4.Detect-switch headset jack: The CX11880 has integrated high noise attenuation for external powered speakers with high impedance. The headset will be active when the system is off. Some speakers have excessive leakage and the internal solution may not attenuate the noise sufficiently. Optional solution is to detect AVDD5V(pin 39) to an always on supply. Requires15uA while system is off;2mA optional runtime.

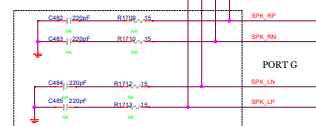


EXT. MIC/LINE IN

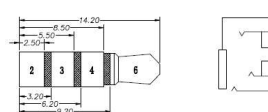
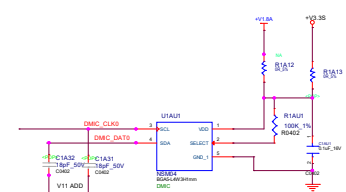
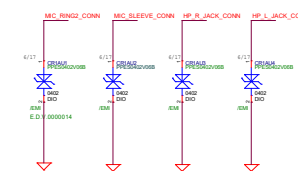
Apple --> EXT_MIC_A, HGND B
Nokia --> EXT_MIC_B, HGND A



Address	Value	Field	Value	Field	Value	Field	Value	Field
630	DMIC_DAT	R513	OR	NA	ROREG	DMIC_DAT		
630	DMIC_CLK	R514	OR	NA	ROREG	DMIC_CLK0		

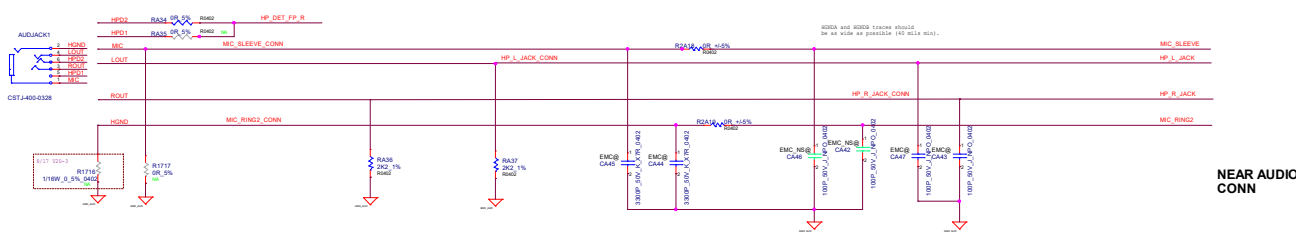


Place sunbber networks (C70-73, R70-73) very close to codec pins.

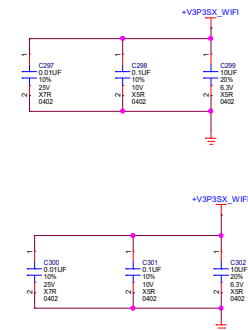


Plug In	PIN4	PIN5	Open
	PIN6	PIN7	Open
Plug Out	PIN4	PIN5	Short
	PIN6	PIN7	Short

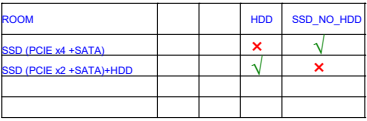
Audio CONN

NEAR AUDIO
CONN

32 WLAN module



SATA/PCIE SSD:1X



EMMC

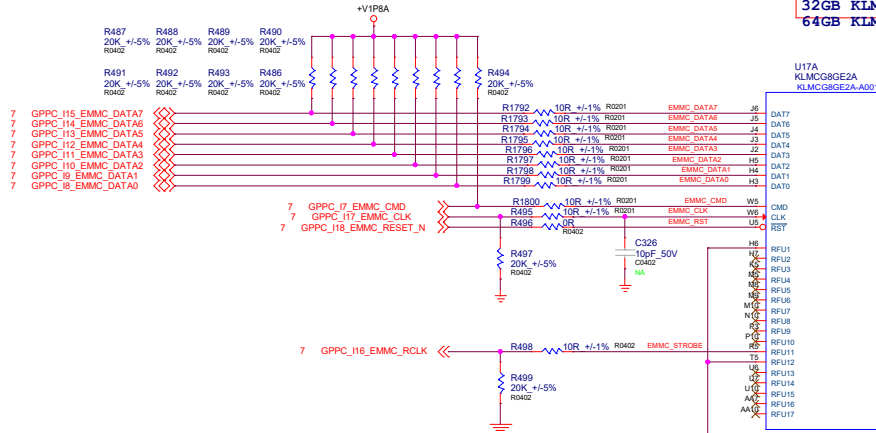
emMC AVL:

Samsung

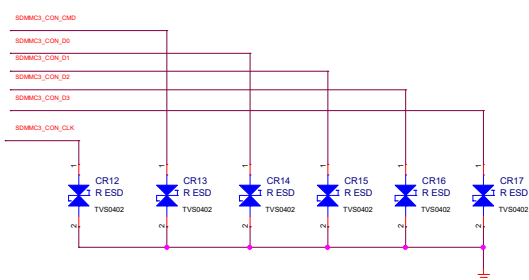
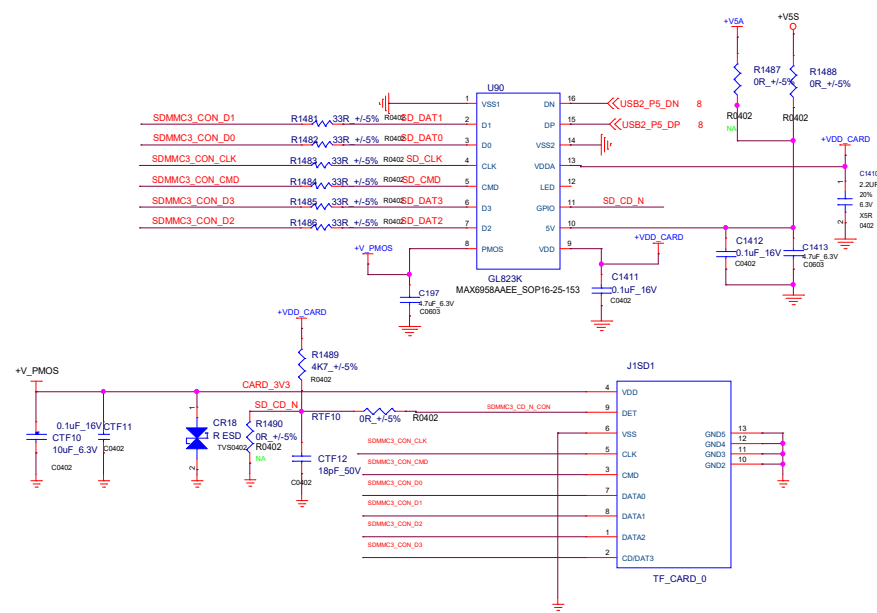
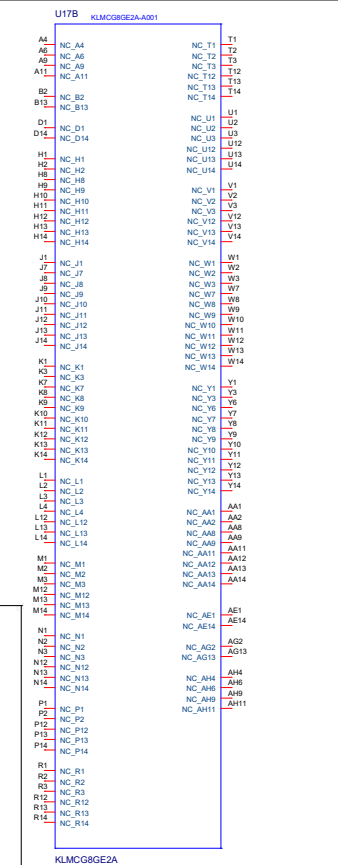
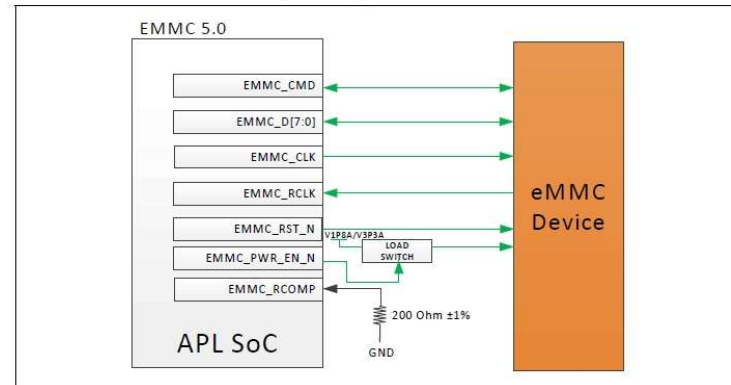
16GB KLMAG2WEMB-B031 / KLMAG2GEAC-B031

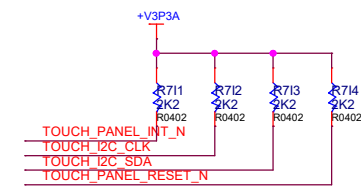
32GB KLMBG4WECB-B031 / KLMBG4GEAC-B031

64GB KLTCG8WECB-B031 / KLTCG8GEAC-B031

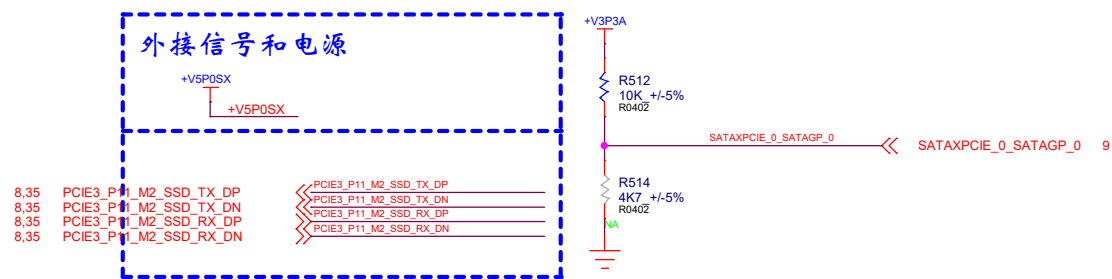
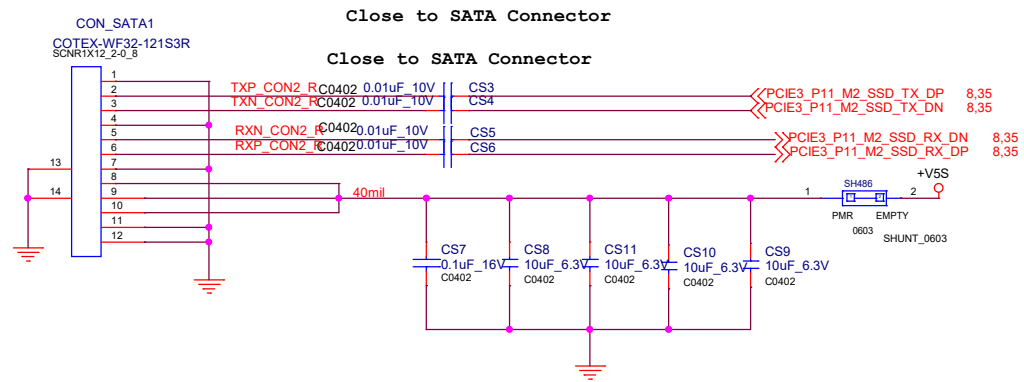


embedded MultiMedia Card (eMMC*) Interface



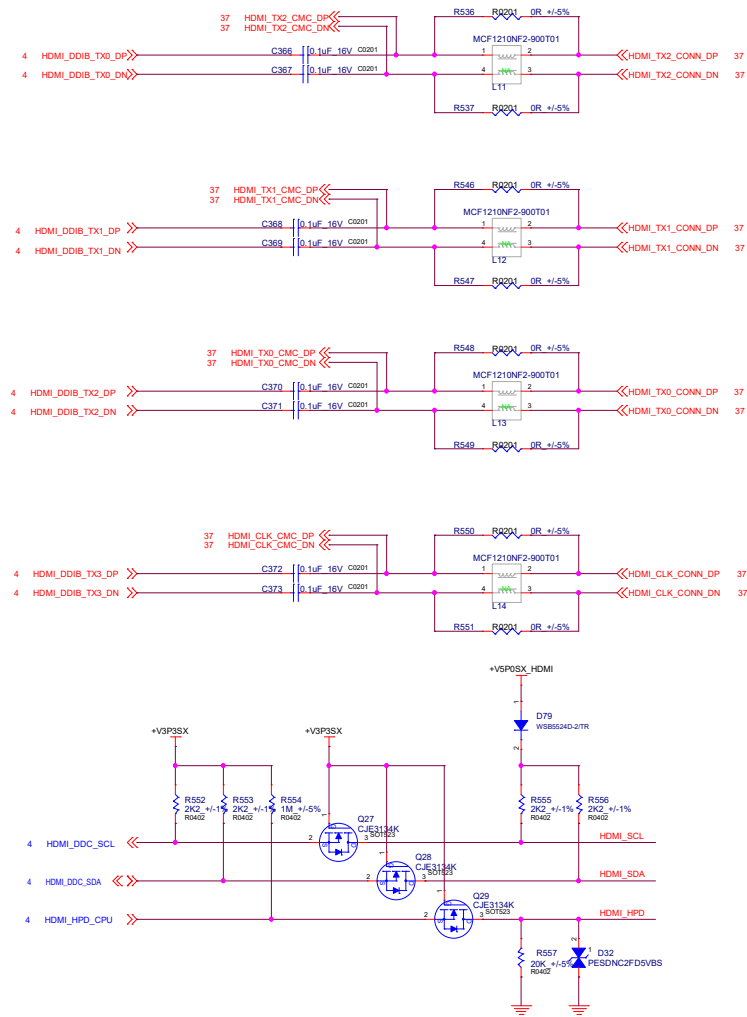


硬盘连接器/CON_HDD

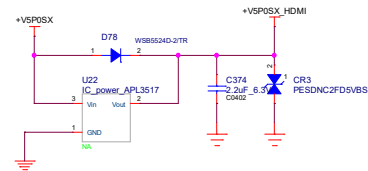
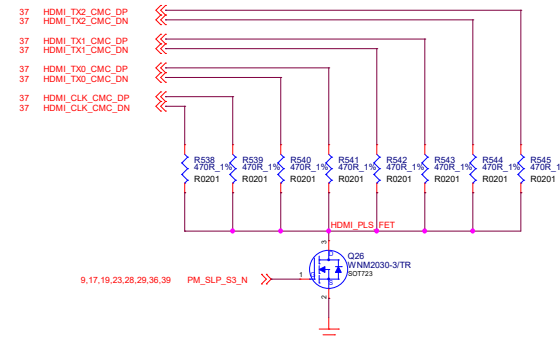


外接信号和电源

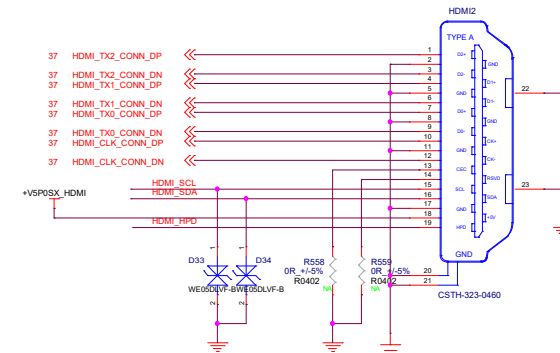




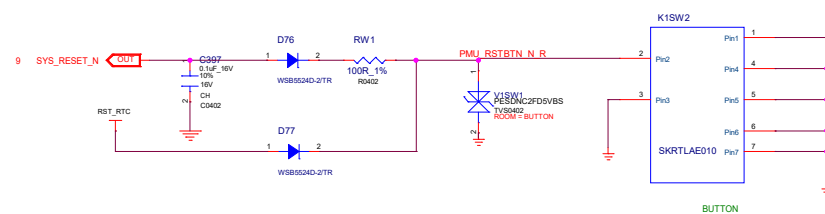
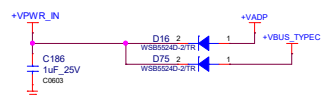
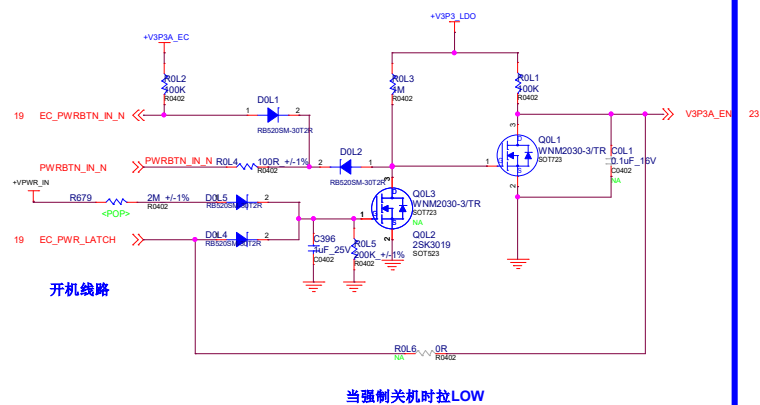
HDMI LEVEL SHIFTERS 1.65Gbps



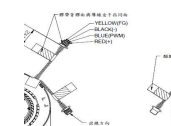
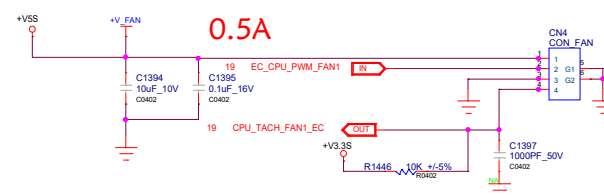
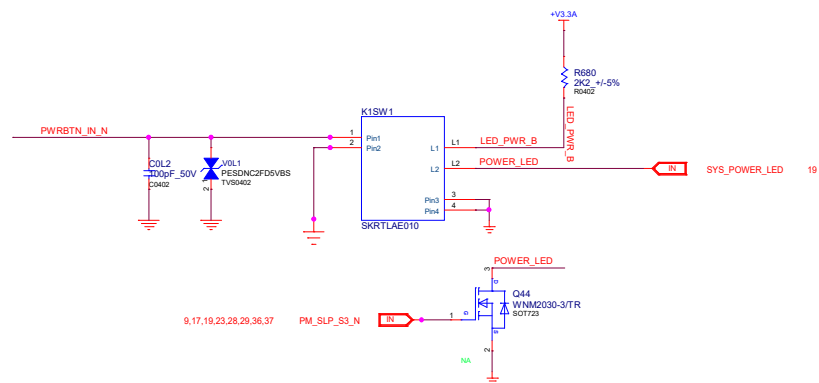
HDMI CONNECTOR

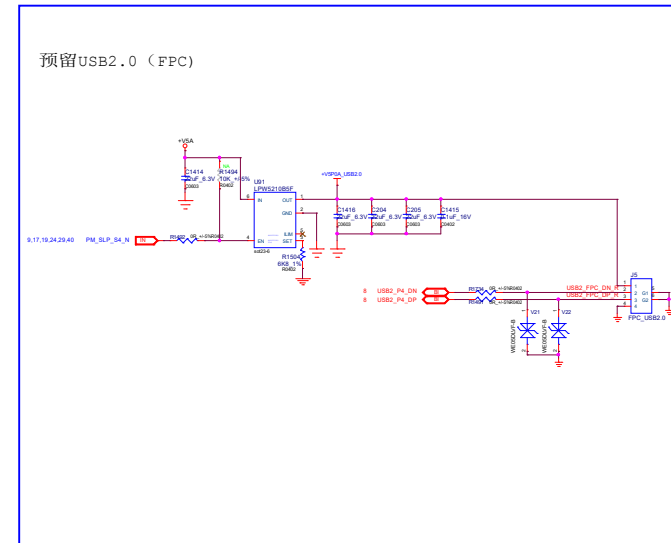
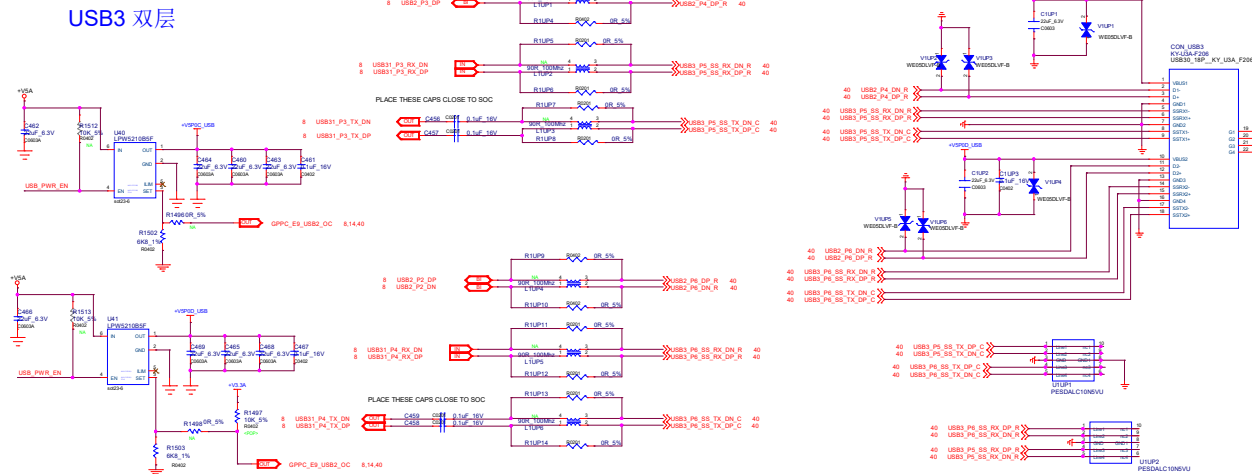


39 CON KB&PWR SW&LED

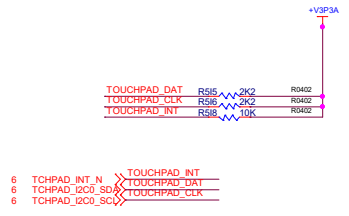


LED控制

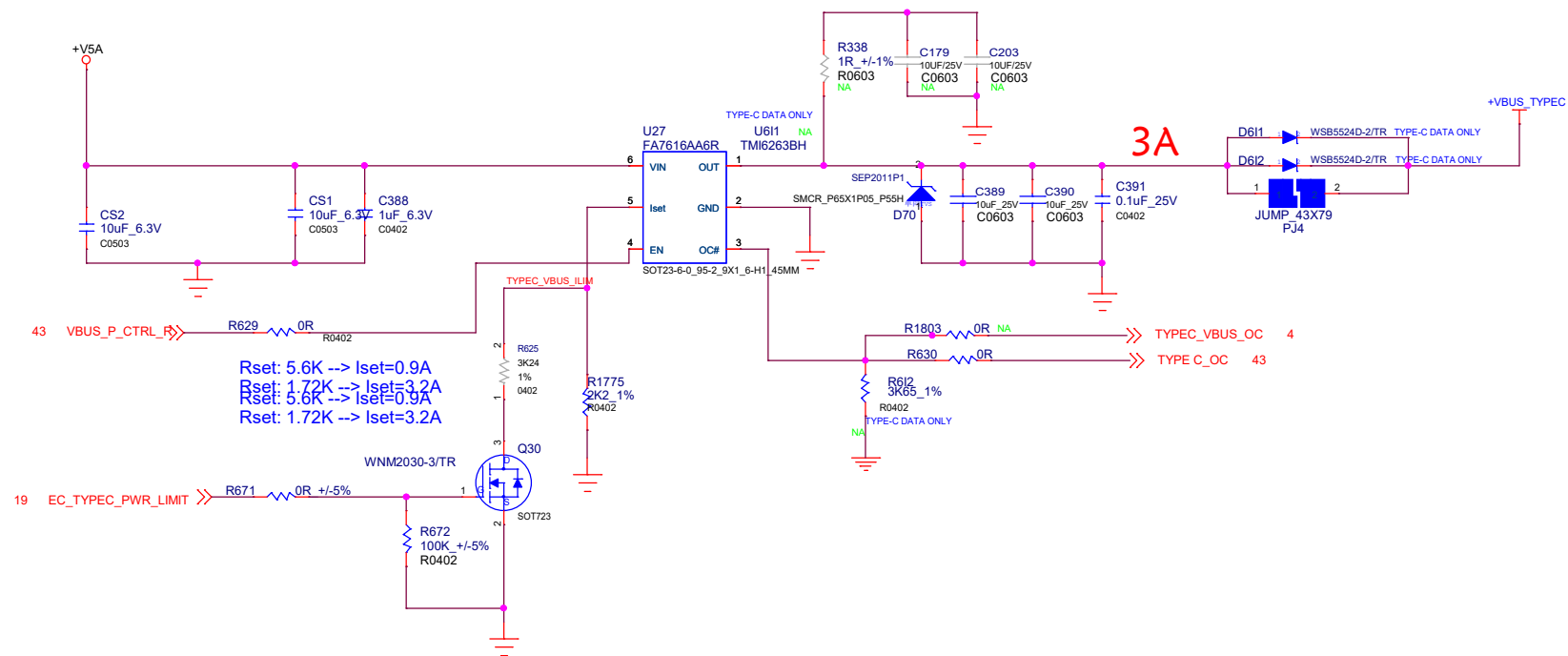


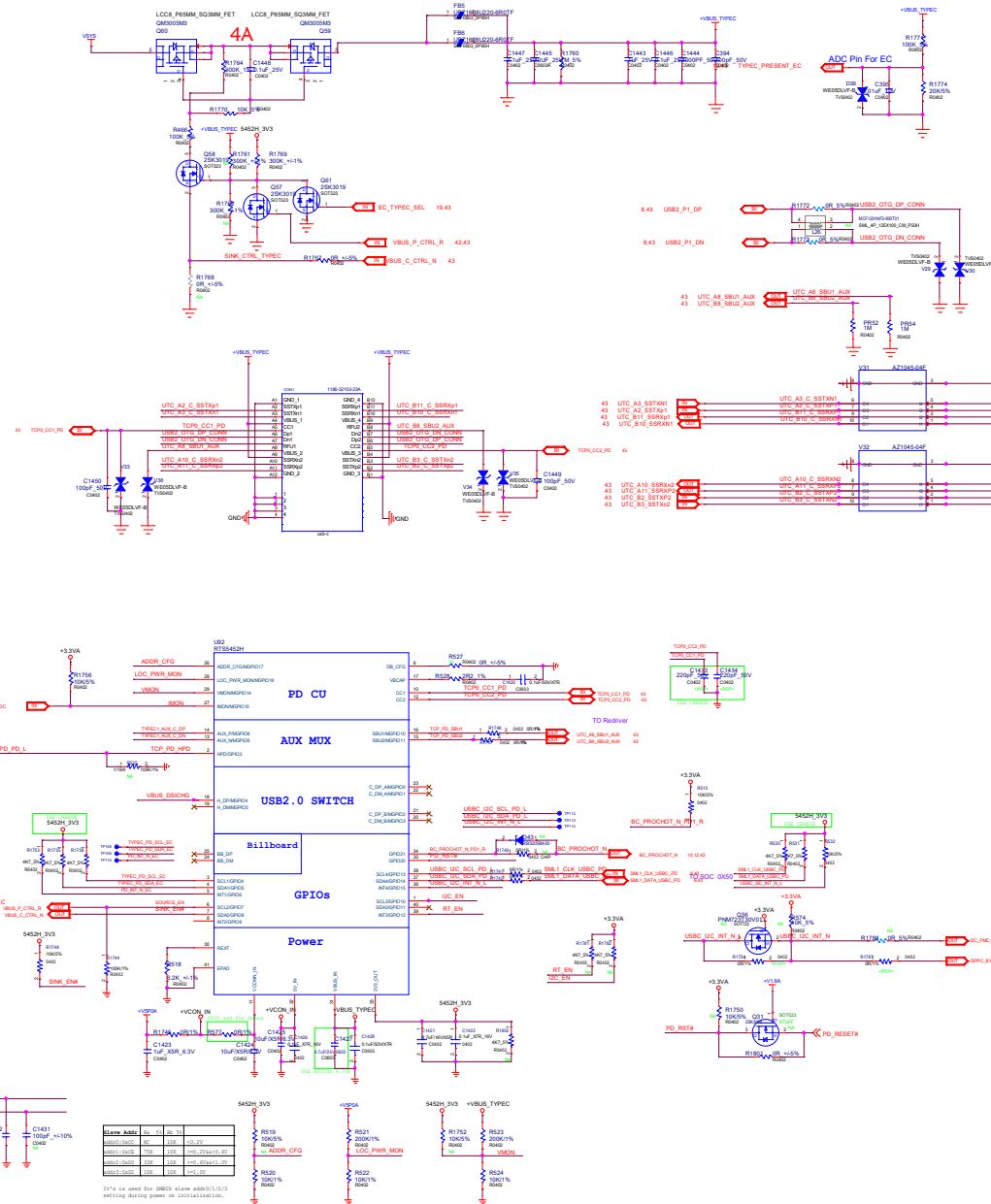


LID/霍尔传感器



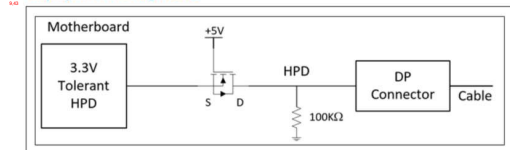
42 USB-C Power





Type C	TCPx_TX_N0	DDIx_DP_LANE0_N
	TCPx_TX_P0	DDIx_DP_LANE0_P
	TCPx_TX_N1	DDIx_DP_LANE2_N
	TCPx_TX_P1	DDIx_DP_LANE2_P
	TCPx_TXRX_N0	DDIx_DP_LANE1_N
	TCPx_TXRX_P0	DDIx_DP_LANE1_P
	TCPx_TXRX_N1	DDIx_DP_LANE3_N
	TCPx_TXRX_P1	DDIx_DP_LANE3_P
	TCPx_AUX_P	DDIx_DP_AUX_P
	TCPx_AUX_N	DDIx_DP_AUX_N
DDSP_HPDx	DPx_HPD	

DisplayPort Hot Plug Detect

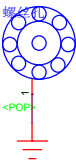


V11 Change list

- Page 43: change to +3.3VA from +3.3VS, change to +V3P3SX from +3.3VS(EQ check issue)
- Page 23: Q12 NA
- Page 42: U6I2 NA
- Page 23: R1P4 NA to ment NB690 operates in normal mode
- Page 38: R705,R706 NA
- Page 26: delete U2, U93,U94 colay,change U7,U8,U9 footprint to mp86941_qfn21-040-0305 from MP86941_QFN21_0D4_3X5_H0D8C
- Page 25: mark R379 15W=1.87K, 6W/7W=2K from MPS advice
- Page 26: reserve C1453~C1458
- Page 39: reserve R0L6 to Q0L1 for EC to control 3P3A
- Page 19: R242 net to BATT_ID_EC, EC PIN94 net to EC_SIN1
- Page 44: R299 Change to 22K
- Page 06: R13,R14 NA
- Page 43: Q36,R1788,R574 NA, R1754,R1787 mount, R532 NA
- Page 26: DEL +VCCANA_VR due to BIOS can enable FIVR to replace MBVR (U9P1,L9P1,U11,Q13,Q14 NA)
- Page 18: U0F1 change to 16M(W25Q128JVS1Q) from 32M
- Page 21:Change C176 to 0.47uF from 0.1uF to delay VSYS to 3ms
- Page 36:Change Q47 PIN3 netname to HDMIA_HPD_C form HDMIA_HPD
- Page 19:Change EC PIN85 PM_RSMRST_N to PIN67, PIN85 renet: HDMIA_CEC , DEL: R244,R246,RT_CHG1,RT_CPU1
- Page 36: ADD CEC Circuit
- Page 37: ADD CEC Circuit
- Page 26: Change R384,R386,R388 to 2.2R from 0R to reduce SW voltage
- Page 32: R1F23 NA duplication
- Page 33: R478 NA duplication
- Page 30: R1711 MOUNT,R1714 NA to ment vender request
- Page 25: R342,R341 MOUNT for EC burn MPS FW

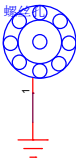
SSD
SCREW

H9
SSD_NUT_MAX



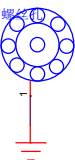
WIFI
NUT

H14
WIFI_NUT
M.T.N.0000046
NUT_C6_0D3_1

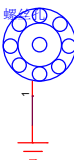


CPU
SCREW

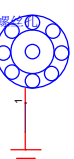
H5
Hole



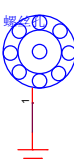
H6
Hole



H7
Hole



H8
Hole



MK1



FMARKS
FIDUCIAL_40_PACKAGE

NA

MK3



FMARKS
FIDUCIAL_40_PACKAGE

NA

MK2



FMARKS
FIDUCIAL_40_PACKAGE

NA

MK4

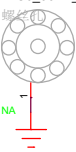


FMARKS
FIDUCIAL_40_PACKAGE

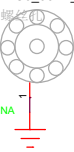
NA

ME Hole

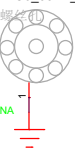
H3
02AP0974
C6_00D2_50



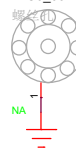
H13
02AP0974
C6_00D2_50



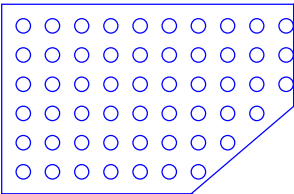
H11
02AP0974
C6_00D2_50



H1
02AP0974
C6_00D2_50



MP1



PingBIZhao

MPCB1



PCB

MPCBA1



PCBA