



Cavli C17QS LTE CAT1.bis Module

Hardware Manual

External Release Version 1.0

Connect to our website and feel free to contact our technical support team for any assistance.

Cavli Inc.,

99 South Almaden Blvd., Suite 600, San Jose, California, 95113

Web: www.cavliwireless.com

IoT Connectivity Platform: www.cavlihubble.io

Support Center

<https://www.cavliwireless.com/support-center.html>

e-Mail: support@cavliwireless.com

For sales enquiries

<https://www.cavliwireless.com/contact-us.html>

e-Mail: sales@cavliwireless.com

More IoT Modules

<https://www.cavliwireless.com/iot-modules/cellular-modules.html>

COPYRIGHT

THE INFORMATION CONTAINED HERE IS PROPRIETARY TECHNICAL INFORMATION OF CAVLI WIRELESS INC. TRANSMITTING, REPRODUCTION, DISSEMINATION AND EDITING OF THIS DOCUMENT AS WELL AS UTILIZATION OF THE CONTENT ARE FORBIDDEN WITHOUT PERMISSION. OFFENDERS WILL BE HELD LIABLE FOR PAYMENT OF DAMAGES. ALL RIGHTS ARE RESERVED IN THE EVENT OF A PATENT GRANT OR REGISTRATION OF A UTILITY MODEL OR DESIGN. EVERY EFFORT HAS BEEN MADE IN PREPARATION OF THIS DOCUMENT TO ENSURE ACCURACY OF THE CONTENTS. BUT ALL STATEMENTS, INFORMATION, AND RECOMMENDATIONS IN THIS DOCUMENT DO NOT CONSTITUTE A WARRANTY OF ANY KIND, EXPRESS OR IMPLIED. THE INFORMATION IN THIS DOCUMENT IS SUBJECT TO CHANGE WITHOUT NOTICE DUE TO PRODUCT VERSION UPDATE OR OTHER REASONS. FOR MOST RECENT DOCUMENTS, ALWAYS REFER THE PRODUCT PORTFOLIO SECTION AT www.cavliwireless.com.

Copyright © Cavli Inc. All rights reserved



Table of Contents

1 Introduction	8
2 Module Overview	9
2.1 Module Introduction.....	9
2.2 Module Characteristics	10
2.3 Module Function	11
2.4 Module Working Mode.....	12
3 Interface Application Description	13
3.1 Chapter Overview	13
3.2 Module Interface	14
3.2.1 C17QS Pin Layout.....	14
3.2.2 C17QS Pin Interface.....	15
3.2.3 Absolute maximum ratings.....	16
3.2.4 Operating Conditions.....	16
3.2.4.1 Digital I/O characteristics.....	17
3.2.5 C17QS PIN Assignment.....	19
3.3 Power interface	25
3.3.1 Power Supply Design.....	26
3.3.2 Power Reference Circuit.....	28
3.3.3 VDD_EXT 1.8 Voltage Output.....	28
3.4 Switching Machine Reset Mode.....	29
3.4.1 Turn ON Module	29
3.4.2 Reset Control.....	30
3.5 USB Interface	30



3.6 UART Interface.....	32
3.6.1 UART2 Serial Port.....	32
3.6.2 UART1 Serial Port.....	32
3.6.3 UART0 Serial Port.....	33
3.6.4 Serial Port Application Circuit	34
3.7 USIM Interface.....	35
3.7.1 USIM Card Reference Circuit.....	36
3.8 General Purpose GPIO Interface.....	37
3.9 Network Status Indication Interface	38
3.9.1 Network Status.....	38
3.9.2 Module Status Indication	40
3.10 I2S Interface.....	41
3.11 I2C Bus	41
3.12 SWD Interface.....	42
3.13 ADC Interface.....	42
3.14 Antenna	43
3.14.1 RF Trace Reference	46
3.15 Control Interface	48
3.16 GNSS Interface	48
3.17 SPI Interface.....	50
4 Overall Technical Indicators.....	52
4.1 Chapter Overview	52
4.2 Working Frequency	52
4.3 GNSS Performances	53
4.4 Antenna Requirements.....	54



5 Interface Electrical Characteristics.....	56
5.1 Chapter Overview	56
5.2 Working Storage Temperature	56
5.3 Electrostatic Property	56
5.4 Module IO Level	57
5.5 Power Supply.....	58
5.6 Power Consumption Characteristics.....	58
6 Structural and Mechanical Properties.....	60
6.1 Chapter Overview	60
6.2 C17QS Module Mechanical Size.....	61
7 Appendix.....	64
7.1 Chapter Overview	64
7.2 Abbreviations	64
7.3 Safety and Precautions.....	66

Table of Figures

Figure 1 C17QS Functional Block Diagram	12
Figure 2 C17QS module Interface definition (top view).....	14
Figure 3 VBAT power supply	27
Figure 4 Buck converter reference circuit	28
Figure 5 Power-on reference circuit.....	29
Figure 6 Reset reference circuit	30
Figure 7 USB connection design circuit diagram	31
Figure 8 UART sequence diagram.....	32
Figure 9 Full-featured serial port design	34
Figure 10 UART serial port design	35
Figure 11 Level conversion chip circuit	35
Figure 12 USIM design circuit diagram.....	36
Figure 13 Net light reference circuit diagram.....	39
Figure 14 STATUS Pin Reference Circuit.....	40
Figure 15 I2C interface reference circuit diagram	42
Figure 16 Main antenna matching circuit.....	44
Figure 17 GNSS active antenna matching circuit	45
Figure 18 GNSS passive antenna matching circuit.....	45
Figure 19 Coplanar antenna	46
Figure 20 The complete structure of the two-layer PCB microstrip line.....	47
Figure 21 The complete structure of the multilayer PCB strip line.....	47
Figure 22 GNSS BAT Input.....	49
Figure 23 SPI master sequence diagram CPHA = 0.....	50
Figure 24 SPI master sequence diagram CPHA = 1.....	51
Figure 25 Top view and bottom view of the module	60
Figure 26 Front view and side view of the module (unit: mm)	61
Figure 27 Bottom view of the module (unit: mm)	62
Figure 28 Recommended Footprint (Top View) (unit: mm).....	63

VERSION HISTORY

Version	Edit	Date (DD/MM/YYYY)
Pre-Release Version		
1.0	Initial Version	03-05-2024
1.1	Updated Supply Voltage and Temperature values	28-05-2024
1.2	Updated GNSS performance parameters, configurable pin functions, UART, SPI Timing diagrams	19-08-2024
External Release Version		
1.0	- Updated Variant Lists and Band lists - Updated Power Consumption details	13-01-2025

1 Introduction

This document is the **Hardware Manual** of the Cavli Wireless solution product **C17QS Smart Module**, which describes:

- ✓ The hardware composition and functional features of the module
- ✓ The definition and usage of the application interface
- ✓ The electrical performance and mechanical properties of the module

This document and the other application documents combined will enable users to develop end devices with Cavli Modules.



2 Module Overview

2.1 Module Introduction

C17QS integrates an application processing subsystem, a communication subsystem, multimedia and connectivity peripherals to enable a single chip 4G LTE feature phone solution.

The C17QS communication subsystem integrates **LTE CAT.1bis** technology and a RF transceiver to cover 1/2/3/4/5/7/8/12/13/14/18/19/20/25/26/28/34/38/39/40/41/66/71(optional) **(W.W)** bands, 1/3/5/7/8/18/19/20/26/28/38/40/41 **(EAJ)** bands, 1/3/7/8/20/28 **(EU)**, 1/3/5/8/18/19/26/28 **(AN)** bands, 1/2/3/4/5/7/8 **(LA)** bands, 1/3/5/8/40/41 **(IN)** bands and 2/4/5/12/13/14/25/34/66/B71(optional) **(NA)**.
Band 40 will be disable by SW for North America market.

The application subsystem runson a single ARM Cortex M3 processor at 306 MHz with integrated peripherals for connectivity and multimedia.



NOTE

- **W.W** - WorldWide
- **EAJ** - Europe, APAC & Japan
- **EU** - Europe
- **AN** - Australia, New Zealand
- **LA** - LatinAmerica
- **IN** - India
- **NA** - North America



2.2 Module Characteristics

Table 2.1 Key Features

Characteristics		Description
Physical Characteristics		26.5mmx 22.5mmx 2.3mm
Package		LGA package
Memory		8 MB Flash + 2 MB RAM
Operating Voltage		3.6V - 4.5V Typical: 3.8V
Application Processor		ARM Cortex M3 with a clock frequency of 306MHz.
Application Interface	USIM card	Supports 3.0V/1.8V Supports hot swap function
	USB	✓ USB2.0 (High-Speed) (only supports Slave mode) ✓ Data transfer rate up to 480Mbps
	UART	✓ UART3(4 lines), UART1(7 lines) and UART2(4 lines) ✓ AT commands and data transfer - UART1 ✓ DM data - UART2 ✓ The baud rate is up to 3000000bps. Default is 115200bps.
	ADC	✓ 2 x Analogue to Digital converter
	I2S	✓ Compliant with I2S bus protocol
	I2C	✓ Compliant with I2C bus protocol ✓ High speed mode supports 3.3Mbps rate
	Network Indication	✓ WWAN_STATE network status indication ✓ STATUS Module status
	GPIO	✓ 11 x GPIO Interfaces
	GNSS	✓ GPS/QZSS: L1, L5 ✓ BDS: B1C, B2a, B2b, B3I ✓ GLONASS ✓ Galileo

		✓ NavIC: L5 ✓ SBAS
	SPI	✓ 2 x Standard SPI interface
	SWD	✓ StandardSWD interface (2 Lines)
Frequency Band	LTE BANDS: WW: 1/2/3/4/5/7/8/12/13/14/18/19/20/25/26/28/34/38/39/40/41/66/71 (optional) Band 40 will be disabled by SW for North America market. EAJ: 1/3/5/7/8/18/19/20/26/28/38/40/41 EU: 1/3/7/8/20/28 AN: 1/3/5/8/18/19/26/28 LA: 1/2/3/4/5/7/8 IN: 1/3/5/8/40/41 NA: 2/4/5/12/13/14/25/34/66/B71 (optional)	
Data Network	✓ FDD/TDD LTE CAT 1.bis ✓ Peak DL 10Mbps/ UL 5Mbps (CAT 1. bis)	
AT Command	✓ Support for standard AT instruction sets (Hayes 3GPP TS 27.007 and 27.005) ✓ Specific AT Query C17QSAT command set	
Network Protocol	TCP(S)/HTTP(S)/MQTT(S)/FTP(S)/PPP TLS versions supported as well	
Antenna Interface	✓ MAIN x 1 ✓ GNSS x 1 ✓ Characteristic impedance 50 Ω	
Temperature Range	Operating Temperature: -40°C - +85°C Storage Temperature: -55°C - 150°C	

2.3 Module Function

C17QS Module mainly consists of the following circuit units:

- ✓ RF Band SAW Duplex array
- ✓ Multi-Band PA
- ✓ Interfaces



The functional block diagram of the C17QS module is shown below :

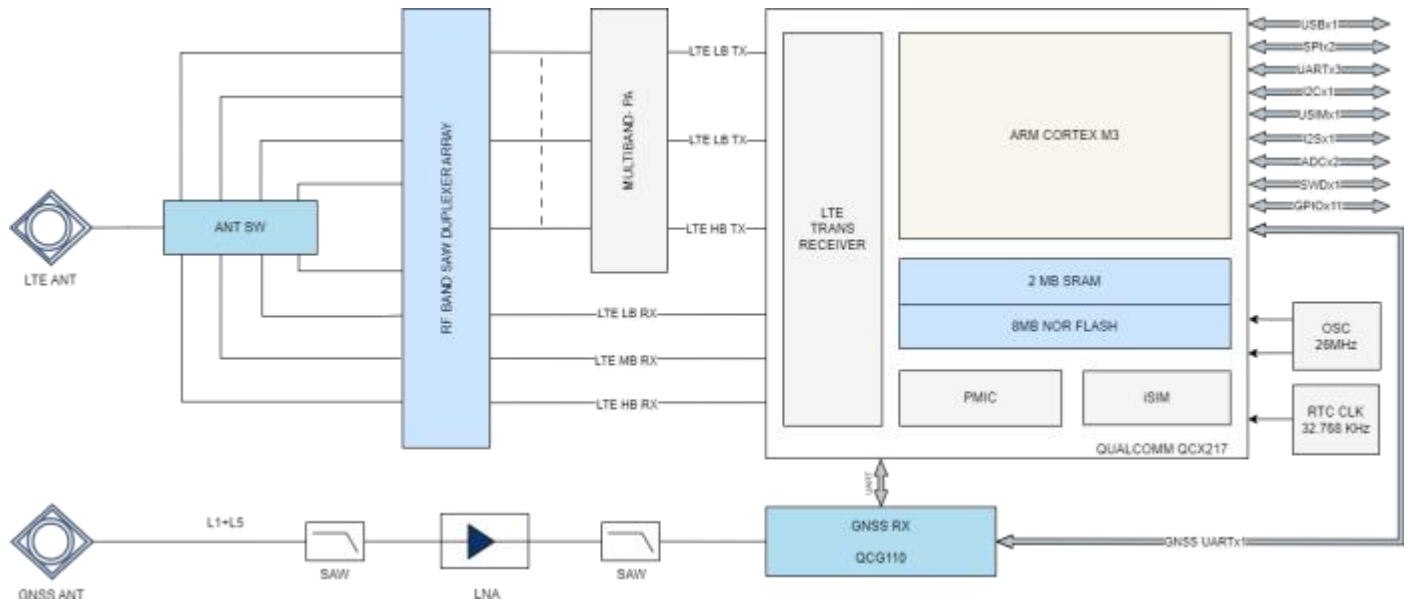


Figure 1 C17QS Functional Block Diagram

2.4 Module Working Mode

Table 1.2 work mode

Working mode	Description
Turnoff Mode	In the case of shutdown, the module is fully powered off.
Flight Mode	The module closes the module RF circuit, unable to interact with the network.
Idle Mode	Turn on the machine and register the network successfully, in the idle state
Data transmission Mode	The module is in working state and has data interaction with the network.



3 Interface Application Description

3.1 Chapter Overview

This chapter mainly describes the interface definition and application of this module. It contains the following sections:

- Module Interface
- Power Interface
- Switching Machine Reset Mode
- USB Interface
- UART Interface
- USIM Interface
- GPIO Interface
- Network Status Indicator Interface
- I2S Interface
- I2C Bus
- SWD Interface
- Antenna
- ADC Interface
- GNSS Interface
- SPI Interface



3.2 Module Interface

3.2.1 C17QS Pin Layout

C17QS pins are assigned as follows :

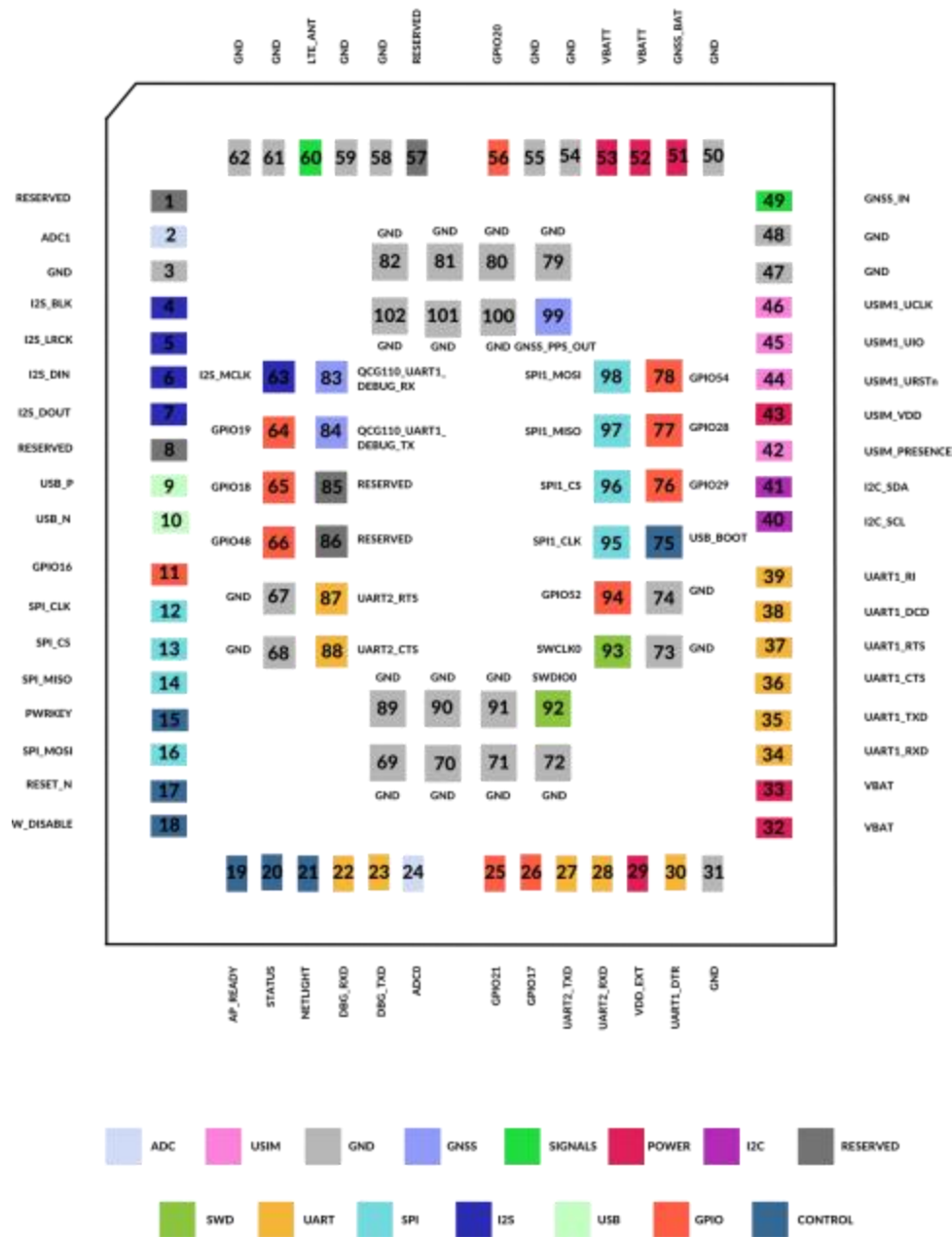


Figure 2 C17QS module Interface definition (top view)

3.2.2 C17QS Pin Interface

The C17QS module has the LGA interface. The module interface definition is shown in the following table:

Symbol	Description
PAD ATTRIBUTE	
AI	Analog Input
AO	Analog Output
AIO	Analog input output
B	Bidirectional digital with CMOS input
DI	Digital Input (CMOS)
DO	Digital Output (CMOS)
DIO	Digital Input/Output
H	High voltage tolerant
PI	Power Input
PO	Power Output
RF_I	Radio Frequency Input
RF_IO	Bidirectional Radio Frequency Input/Output
GND	Common ground
Pad pull details	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpu = default no-pull with programmable options following the colon (:) PD: nppu = default pull-down with programmable options following the colon (:) PU: nppd = default pull-up with programmable options following the colon (:)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device

3.2.3 Absolute maximum ratings

The absolute maximum ratings table reflects the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in Operating conditions.

Table 3.2 Absolute Maximum ratings

Pin Type	V_min	V_max
VB	-0.3	5
P2	-0.3	2
P3	-0.3	3.6
P4	-0.3	4.2

3.2.4 Operating Conditions

The operating voltages are listed below.

Table 3.3 Operating Condition

Pin Type	V_min (if applicable)	V_typical	V_max (if applicable)
VB	3.1	3.8	4.8
P2	1.7	1.8	1.89
P3	-	-	3.4
P4	1.7/2.95	1.8/3	1.89/3.05

3.2.4.1 Digital I/O characteristics

The Digital I/O characteristics of RESETN, AGPIO, AGPIOWU are follows;

Table 3.4 Digital I/O characteristics OF Reset

Parameter	Description	Min	Typical	Max	Unit
VIH	High-level input voltage	$0.7 \times VDD$	-	-	V
VOL	Low-level output voltage	-	-	$0.2 \times VDD$	V
V-Sleep	Sleep voltage	1.05	1.2	1.25	V
V-Hib	Hib. Voltage	1.05	1.2	1.25	V
RPULL-UP	Pull-up resistance	70	120	170	kΩ

Table 3.4 Digital I/O characteristics of AGPIO (LDO_AONIO = 1.8 V)

Parameter	Description	Min	Typical	Max	Unit
VIH	High-level input voltage	$0.7 \times VDD$	-	-	V
VIL	Low-level input voltage	-	-	$0.2 \times VDD$	V
VOH	High-level output voltage	$0.8 \times VDD$	-	-	V
VOL	Low-level output voltage	-	-	$0.15 \times VDD$	V
V-Sleep	Sleep voltage	1.7	1.8	1.9	V
V-Hib	Hib. Voltage	1.7	1.8	1.9	V
IOH	Digital high, output current	3	5	7	mA
IOL	Digital low, output current	6	8	10	mA
RPULL-UP	Pull-up resistance	110	160	210	kΩ
RPULL-DOWN	Pull-down resistance	160	210	260	kΩ

Table 3.4 Digital I/O characteristics of AGPIOWU - AGPIO function (LDO_AONIO = 1.8 V)

Parameter	Description	Min	Typical	Max	Unit
VIH	High-level input voltage	$0.7 \times VDD$	-	-	V
VIL	Low-level input voltage	-	-	$0.2 \times VDD$	V
VOH	High-level output voltage	$0.8 \times VDD$	-	-	V
VOL	Low-level output voltage	-	-	$0.15 \times VDD$	V
V-Sleep	Sleep voltage	1.7	1.8	1.9	V
V-Hib	Hib. Voltage	1.7	1.8	1.9	V
IOH	Digital high, output current	1.05	1.2	1.25	mA
IOL	Digital low, output current	1.05	1.3	1.25	mA
RPULL-UP	Pull-up resistance	110	160	210	kΩ
RPULL-DOWN	Pull-down resistance	160	210	260	kΩ

Table 3.4 Digital I/O characteristics of WAKEUP, AGPIO (WAKEUP function)

Parameter	Description	Min	Typical	Max	Unit
VDD	I/O supply voltage	-	1.8	-	V
VIH	High-level input voltage	$0.7 \times VDD$	-	-	V
VOL	Low-level output voltage	-	-	$0.2 \times VDD$	V
V-Sleep	Sleep voltage	1.05	1.2	1.25	V
V-Hib	Hib. Voltage	1.05	1.2	1.25	V
RPULL-UP	Pull-up resistance	70	120	170	kΩ
RPULL-DOW	Pull-down resistance	60	110	160	Kω

3.2.5 C17QS PIN Assignment

The C17QS pin names are mentioned as follows.

Pin No.	Pin name	Voltage definition	IO Type	Configurable function	Pin Description	Comments
1	RESERVED					-
2	ADC1	P3	AI		ADC channel	-
3	GND					-
4	I2S_BLK	P2	DIO DIO DI DIO DO DO	GPIO11 I2S 0 Bit Clock UART 2 RxD I2C 1 SCL PWM0 PWM1n	Configurable I/O I2S 0 -bit clock UART2 receive data I2C 1 serial clock Pulse-width modulation 0 Pulse-width modulation 1n	-
5	I2S_LRCK	P2	DIO DIO DO DIO DO DO	GPIO12 I2S 0 strobe Clock UART 2 TXD I2C 1 serial data PWM1 PWM0n	Configurable I/O I2S 0 strobe clock UART2 transmit data I2C 1 serial data Pulse-width modulation 1 Pulse-width modulation 0n	-
6	I2S_DIN	P2	DIO DIO DO DO DO DO DO	GPIO13 I2S 0 DIN UART0 RTSn UART2_RTSn SPI1_SS1 (slave select) PWM2 PWM3n	Configurable I/O I2S 0 data in UART0 request to send UART2 request to send SPI 1 slave select 1 Pulse-width modulation 2 Pulse-width modulation 3n	-
7	I2S_DOUT	P2	DIO DIO DI DIO DO DO	GPIO14 I2S 0 DOUT UART2 CTS I2C 0 SCL PWM3 PWM2n	Configurable I/O I2S 0 data out UART2 clear to send I2C 0 serial clock Pulse-width modulation 3 Pulse-width modulation 2n	-
8	RESERVED					-
9	USB_P		AIO			90 Ohm impedance
10	USB_N		AIO			90 Ohm impedance
11	GPIO16	P2	DIO DIO	GPIO16 TESiCi_TCK (iSIM JTAG)	Configurable I/O iSIM JTAG	-

			DO DO	PWM1 PWM0n	Pulse-width modulation 0 Pulse-width modulation 1n	
12	SPI_CLK	P2	DIO DO DIO	GPIO25 SPI0_SCLK TESICo_GPO3	Configurable I/O SPI 0 serial clock iSIM GPO3	-
13	SPI_CS	P2	DIO DO DIO	GPIO22 SPI0_SS0 TESICo_GPO0	Configurable I/O SPI 0 slave select 0 iSIM GPO0	-
14	SPI_MISO	P2	DIO DI DIO	GPIO24 SPI0_MISO TESICo_GPO2	Configurable I/O SPI 0 master in slave out iSIM GPO2	-
15	PWRKEY_N		AI		Power key	
16	SPI_MOSI	P2	DIO DO DIO	GPIO23 SPI0_MOSI TESICo_GPO1	Configurable I/O SPI 0 master out slave in iSIM GPO1	-
17	RSTN		AI	System Reset active-low, assertion of RESETn causes the modem to enter power up sequence and the whole chip will go to reset state.		-
18	W_DISABLE	P2	DIO DIO DO DO DO	AGPIOWU0 (WAKEUP3) GPIO47 FEM7 PWM0 PWM1n	Configurable function General purpose I/O Front end module control 7 Pulse-width modulation 0 Pulse-width modulation 1n	-
19	AP_READY	P2	AI	AP_READY		-
20	STATUS		DIO DO DO DO	GPIO50 FEM4 PWM3 PWM2n	Configurable I/O Front end module control 4 Pulse-width modulation 3 Pulse-width modulation 2n	-
21	NETLIGHT	P2	DIO DO DO DO	GPIO53 FEM1 PWM0 PWM1n	Configurable I/O Front end module control 1 Pulse-width modulation 0 Pulse-width modulation 1n	-
22	DBG_RXD	P2	DIO DI	GPIO1 UART0_RXD	Configurable I/O UART0 receive dat	-
23	DBG_TXD	P2	DIO	GPIO2	Configurable I/O	

			DO	UART0_TXD	UART0 transmit data	
24	ADC0	P3	AI	AIO4 (ADC Channel)	ADC channel	-
25	GPIO21	P2	DIO DIO DO DO	GPIO21 TESiCi_PWRON PWM5 PWM4n	Configurable I/O iSIM PWRON Pulse-width modulation 5 Pulse-width modulation 4n	-
26	GPIO17	P2	DIO DIO DO DO	GPIO17 TESiCi_TCK PWM1 PWM0n	Configurable I/O iSIM JTAG Pulse-width modulation 1 Pulse-width modulation 0n	-
27	UART2_TXD	P2	DIO DO DIO	GPIO31 UART2_TXD TESiCi_GPI1	Configurable I/O UART2 transmit data iSIM GPI1	-
28	UART2_RXD	P2	DIO DI DIO	GPIO30 UART2_RXD TESiCi_GPI0	Configurable I/O UART2 receive data iSIM GPI0	-
29	VO_LDO1833I O (VDD_EXT)		AO	1.8 V I/O Power		-
30	UART1_DTR	P2	DIO DI DIO DO DO	GPIO36 UART0_CTSn TESiCi_BOOTCFG1 UART1_DTRn PWM2	Configurable I/O UART 0 clear to send iSIM BOOTCFG1 UART 1 data terminal ready Pulse-width modulation 2	-
31	GND					-
32	VBATT	VB	PI		VBATT power supply	-
33	VBATT	VB	PI		VBATT power supply	-
34	UART1_RXD	P2	DIO DI	GPIO3 UART1_RXD	Configurable I/O UART1 receive data	-
35	UART1_TXD	P2	DIO DO	GPIO4 UART1_TXD	Configurable I/O UART1 transmit data	-
36	UART1_CTS	P2	DI DIO DI	UART1_CTS GPIO6 UART0_CTSn	Configurable I/O UART1 clear to send UART0 clear to send	-
37	UART1_RTS	P2	DO DO DIO	UART1_RTSn UART0_RTSn GPIO5	Configurable I/O UART1 request to send UART0 request to send	-
38	UART1_DCD	P2	DIO DI DO DIO	GPIO35 UART1_DCD UART0_RTSn TESiCi_BOOTCFG0	Configurable I/O UART0 request to send iSIM BOOTCFG0 UART 1 data carrier detect	-



			DO	PWM1	Pulse-width modulation 1	
39	UART1_RI	P2	DIO DO DO DO	GPIO51 FEM3 PWM4 PWM5n	Configurable I/O Front end module control 3 Pulse-width modulation 4 Pulse-width modulation 5n	-
40	I2C_SCL	P2	DIO DIO DIO DO	GPIO26 I2C0_SCL TESICo_GPO4 UART0_RTSn	Configurable I/O I2C 0 serial clock iSIM GPO4 UART0 request to send Configurable I/O	-
41	I2C_SDA	P2	DIO DIO DIO DI	GPIO27 I2C0_SDA TESICo_GPO5 UART0_CTSn	Configurable I/O I2C 0 serial data iSIM GPO5 UART0 clear to send	-
42	USIM_PRESEN CE	P4	AI	WAKEUP0 (AGPIO)		-
43	USIM_VCC	P4	PO		LDO output for SIM card, 1.8 V/3.0 V	-
44	USIM1_URSTn	P4	DIO		SIM Card Reset	-
45	USIM1_UIO	P4	DIO		SIM card I/O	-
46	USIM1_UCLK	P4	DIO		SIM card clock	-
47	GND					-
48	GND					-
49	GNSS_IN		I		RF Input	50 Ohm impedance
50	GND					-
51	GNSS_BAT	AVD33B AK			Power input for the backup power domain	-
52	VBATT	VB			VBATT power supply	-
53	VBATT	VB			VBATT power supply	-
54	GND					-
55	GND					-
56	GPIO20	P2	DIO DIO DO DO	GPIO20 TESICo_TDO PWM4 PWM5n	Configurable I/O iSIM JTAG Pulse-width modulation 4 Pulse-width modulation 5n	-

57	RESERVED					-
58	GND					-
59	GND					-
60	LTE_ANT	IO			RFTx / Rx	50 Ohm impedance
61	GND					-
62	GND					-
63	I2S_MCLK	P2	DIO DIO DIO DI DO DO DO	GPIO15 USP0_MCLK ONEW UART0_CTSn I2C0_SDA PWM4 PWM5n	Configurable I/O I2S 0 master clock 1-wire interface UART0 clear to send I2C 0 serial data Pulse-width modulation 4 Pulse-width modulation 5n	-
64	GPIO19	P2	DIO DIO DO DO	GPIO19 TESICi_TDI PWM3 PWM2n	Configurable I/O iSIM JTAG Pulse-width modulation 3 Pulse-width modulation 2n	-
65	GPIO18	P2	DIO DIO DO DO	GPIO18 TESICi_TMS PWM2 PWM3n	Configurable I/O iSIM JTAG Pulse-width modulation 2 Pulse-width modulation 3n	-
66	GPIO48	P2	DIO DIO DO DO DO	AGPIOWU1 (WAKEUP4) GPIO48 FEM6 PWM1 PWM0n	Configurable function General purpose I/O Front end module control 0 Pulse-width modulation 1 Pulse-width modulation 0n	-
67	GND					-
68	GND					-
69	GND					-
70	GND					-
71	GND					-
72	GND					-
73	GND					-
74	GND					-

75	USB_BOOT	P2	DIO	GPIO0 (USB boot)	Configurable I/O	-
76	GPIO29 I2C1_SCL	P2	DIO DIO DIO DO	GPIO29 I2C1_SDA TESICo_GPO7 UART1_DTRn	Configurable I/O I2C 1 serial data iSIM GPO7 UART 2 data terminal ready	-
77	GPIO28 I2C1_SDA	P2	DIO DIO DIO DI DO	GPIO28 I2C1_SCL TESICo_GPO6 UART1_DCDn SPI0_SS1n	Configurable I/O I2C 1 serial clock iSIM GPO6 UART 1 data carrier detect SPI 0 slave select 1	-
78	GPIO54	P2	DIO DO DO DO	GPIO54 FEM0 PWM1 PWM0n	Configurable I/O Front end module control 0 Pulse-width modulation 1 Pulse-width modulation 0n	-
79	GND					-
80	GND					-
81	GND					-
82	GND					-
83	QCG110_UART1_DEBUG_RX		DI		GNSS Debug UART RX	Should be left floating
84	QCG110_UART1_DEBUG_TX		DO		GNSS Debug UART TX	-
85	RESERVED					-
86	RESERVED					-
87	UART2_RTS	P2	DIO DO DIO	GPIO32 UART2_RTSn TESICi_GPI2	Configurable I/O UART2 request to send iSIM GPI2	-
88	UART2_CTS	P2	DIO DO DIO	GPIO33 UART2_CTSn TESICi_GPI3	Configurable I/O UART2 clear to send iSIM GPI3	-
89	GND					-
90	GND					-
91	GND					-
92	SWDIO0	P2	DIO DIO	SWDIO0 GPIO3	Configurable function Serial wire debug data General purpose I/O	-

93	SWCLK0	P2	DIO DIO	SWCLK0 GPIO4	Configurable function Serial wire debug clock General purpose I/O	-
94	GPIO52	P2	DIO DO DO DO	GPIO52 FEM2 PWM5 PWM4n	Configurable I/O Front end module control 2 Pulse-width modulation 5 Pulse-width modulation 4n	-
95	SPI1_CLK	P2	DIO DO DIO	GPIO10 SPI1_SCLK ONEW	Configurable I/O SPI 1 serial clock 1-wire interface	-
96	SPI1_CS	P2	DIO DO DIO	GPIO7 SPI1_SS0 USIM1_URSTn	Configurable I/O SPI 1 slave select 0 SIM card 1 reset	-
97	SPI1_MISO	P2	DIO DI DIO	GPIO9 SPI1_MISO USIM1_UIO	Configurable I/O SPI 1 master in slave out SIM card 1 I/O	-
98	SPI1_MOSI	P2	DIO DO DIO	GPIO8 SPI1_MOSI USIM1_UCLK	Configurable I/O SPI 1 master out slave in SIM card 1 clock	-
99	GNSS_PPS_OUT	P2	DIO DO DO DO	GPIO46 GNSS_PPS_OUT PWM5 PWM4n	Configurable I/O GNSS_PPS_OUT Pulse-width modulation 5 Pulse-width modulation 4n	-
100	GND					-
101	GND					-
102	GND					-

NOTE

- ✓ The module typically has an IO port level of 1.8V (in addition to the SIM, the SIM card port level supports 1.8V and 3.0V).
- ✓ All **RESERVED** and unused pin feet need to be left floating

3.3 Power interface

The C17QS module power interface consists of three parts:

- ✓ **VBAT** is the module working power supply.
- ✓ **VBAT** is the module RF power supply
- ✓ **GNSS_IN** is the RTC power
- ✓ **USIM_VCC** is the working power supply for SIM card

3.3.1 Power Supply Design

The power interface of the C17QS module is as follows:

Table 3.5 Power pin definitions

Power supply							
Pin No.	Definition	IO	Description	Remarks	V_Min	V_Typ	V_Max
32, 33	VBAT	PI	Module input voltage	-	3.1V	3.8V	4.5V
52, 53	VBAT	PI	Module input voltage	-	3.1V	3.8V	4.5V
43	USIM_VCC	PO	External SIM card power supply	Output voltage 1.8/3	1.75/2.95	1.8/3	1.85/3.05
51	GNSS_BAT		GNSS Backup Battery				
29	VDD_EXT	PO	1.8V output LDO / Reference Voltage	Output voltage 1.8V	1.75	1.8	1.85
3, 31, 47, 48, 50, 54, 55, 58, 59, 61, 62, 67-74, 79-82, 89-91, 100-102	GND	-	Ground	-	-	0	-

The C17QS module can be powered by a single power supply mode.

- The module has 4 channels of power supply.
- The module power supply range is between 3.6V - 4.5V
- It is recommended to use 1mm trace width for 1 oz of copper for **VBAT** (Top layer)
- It is recommended to use 3.8 V/830 mA power supply.
- If the module's operating voltage drop causes the VCC supply voltage to be too low or the supply current is insufficient, the module may shutdown or restart. Therefore, to reduce the power fluctuation of the module when working, it is necessary to use a low-ESR value of the voltage regulator capacitor, the power pin and the ground pin should be connected and can provide sufficient power supply capability.
- The external power supply is connected to the module from a single voltage source and can be expanded to two sub paths with star structure.
- The GNSS_VDD voltage is for powering ON GNSS IC and GNSS_EN is to start the NMEA streaming in the independent operation mode of GNSS and LTE. In normal working mode, both pins can be left floating.
- For more information, refer *C17QS GNSS Application Note*.

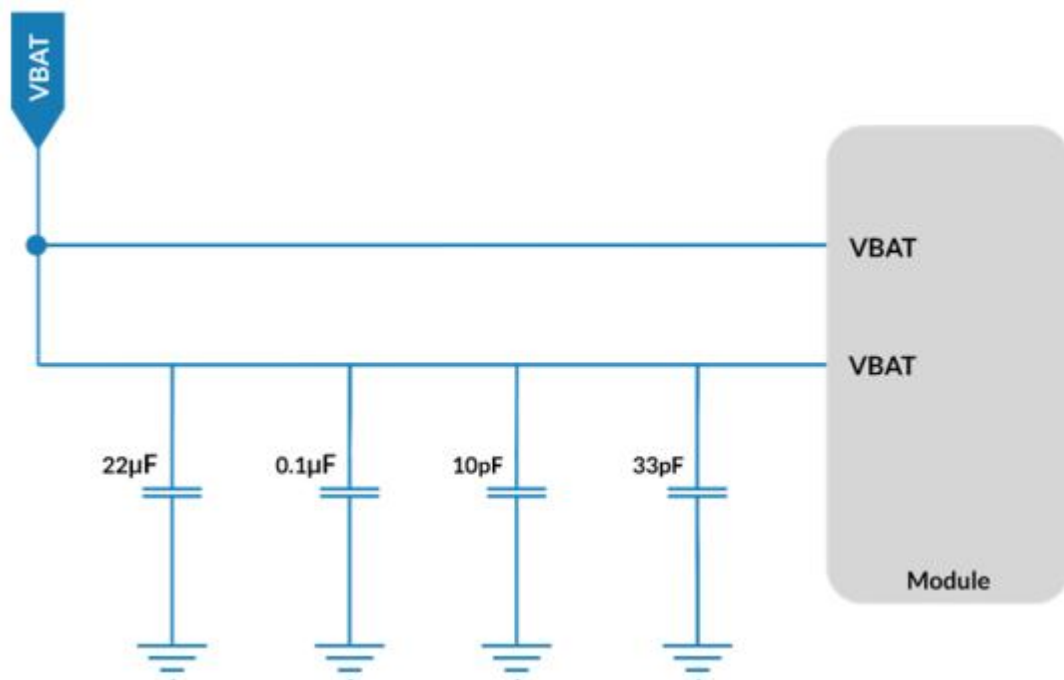


Figure 3 VBAT power supply

 NOTE

- ✓ To ensure that the power supply is sufficient, a 10pF, 33pF, 0.1μF, 22μF ceramic capacitors can be added to the VBAT line and placed near the VBAT pin to improve the performance and stability of the system.

3.3.2 Power Reference Circuit

A Buck converter can be used to design the VBAT power supply. For better understanding, refer the circuit given below.

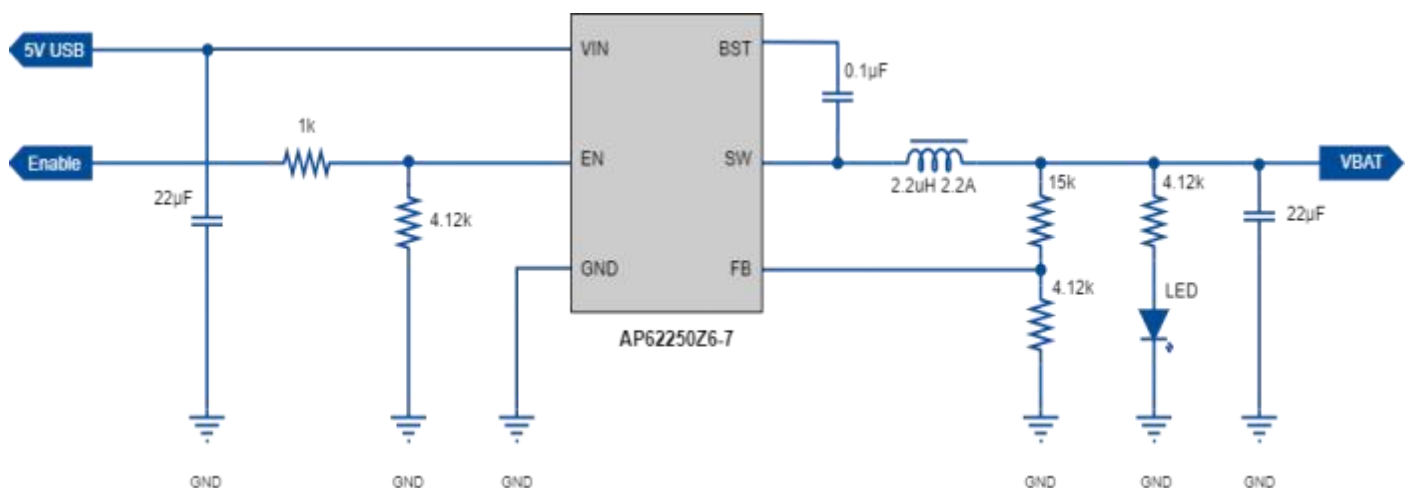


Figure 4 Buck converter reference circuit

3.3.3 VDD_EXT 1.8 Voltage Output

The C17QS module outputs 1.8V through VDD_EXT for internal digital circuitry. This voltage is the logic level voltage of the module. After normal power-on, the 29th pin will output 1.8V and the current load will be 50mA.

The external master can read the voltage of VDD_EXT to determine if the module is powered on. VDD_EXT can also be used as an external power supply, such as a level shifting chip, but maximum load should be within 50mA

Pin No.	Signal name	I/O	Description	Voltage		
				V_min	V_Typical	V_max
29	VDD_EXT	PO	1.8V output LDO / Reference Voltage	1.75	1.8	1.85

3.4 Switching Machine Reset Mode

3.4.1 Turn ON Module

The 15th pin of the C17QS module is Power on pin. The module can be powered on by pulling down the POWER_KEY Low for at least 500ms. The user can check whether the module is powered on by querying the high and low levels of the VDD_EXT pin.

Table 3.7 Switch pin definition

Pin No.	Signal name	I/O	Description
15	PWRKEY_N	DI	Power key

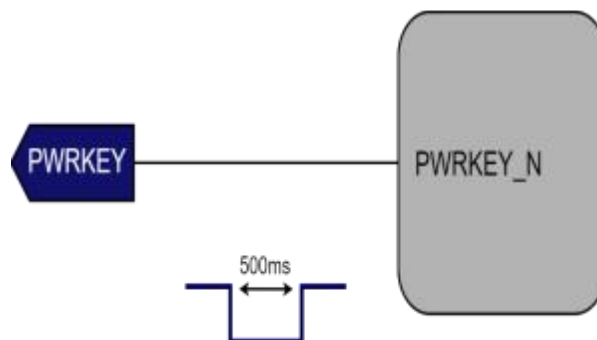


Figure 5 Power-on reference circuit

NOTE

- ✓ If you want to enable automatic boot up for the C17QS, connect the PWRKY_N via pull-up with a 4.7K resistor to the module's VDD_EXT. (Not from external 1.8V source)

3.4.2 Reset Control

The C17QS module Pin 17th is a reset pin. The application detects that the module is abnormal. When the software does not respond, the module can be reset. Pull the pin low for 100-500ms to reset the module. The RESET pin is sensitive to interference. A 10nF to 0.1uF capacitor can be installed near the signal for signal filtering. Keep away from RF interference signals when routing.

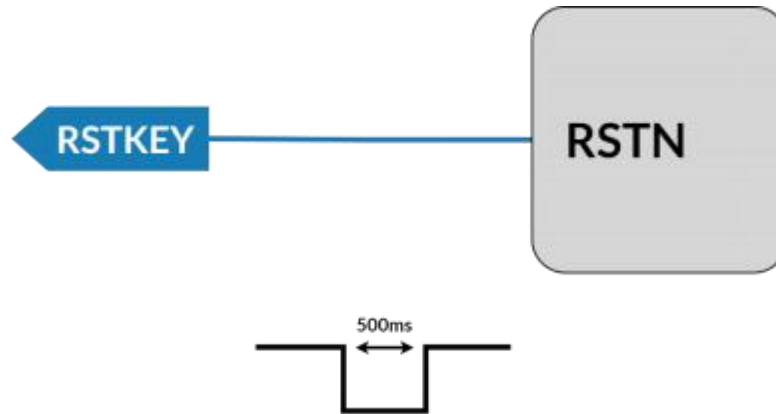


Figure 6 Reset reference circuit

Table 3.8 RESET pin parameters

Pin No.	Signal name	I/O	Description	Voltage		
				V_min	V_Typical	V_max
17	RSTN	DI	Module Reset Control	1.9	-	2.1

NOTE

- ✓ The C17QS module supports AT command reset, and the AT command is **AT+TRB** to restart the module. Detailed instructions can be found in the C17QSAT Command Set Manual.

3.5 USB Interface

The C17QS module USB interface supports **USB2.0** high-speed protocol, only in slave mode, and does not support USB charging mode. USB input and output traces must comply with the **USB2.0** feature. The input



power supply of USB_VBUS is 3.3V - 5V. AT interfacing and Ethernet via USB is possible in Cavli C17QS module.

The USB interface is defined as follows:

Table 3.9 USB interface pin definition

Pin No.	Signal name	I/O	Description	Voltage		
				V_min	V_Typical	V_max
9	USB_P	AIO	Differential input/output signal of USB +	3.25	3.3	3.35
10	USB_N	AIO	Differential input/output signal -	3.25	3.3	3.35

The module only acts as a USB slave device and supports *USB Sleep* and *Wake-Up* mechanisms. USB interface application reference circuit is as follows :

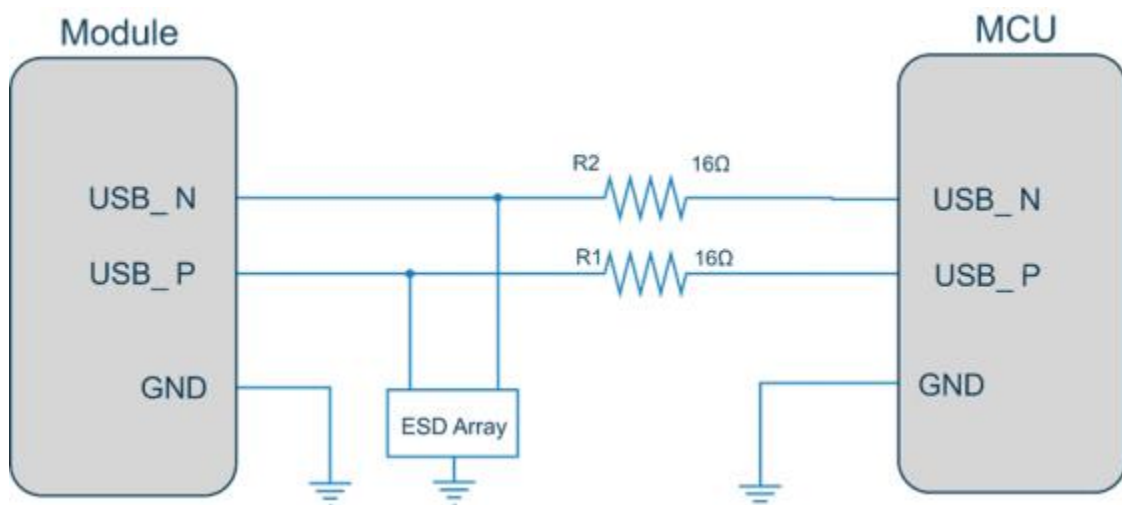


Figure 7 USB connection design circuit diagram

 NOTE

- ✓ Required a resistance of 16Rfor R1/R2.
- ✓ The USB interface supports high-speed (480Mbps) and full-speed (12Mbps) modes, so the trace design needs to strictly follow the USB2.0 protocol requirements, pay attention to the protection of the data line, differential trace, control impedance is 90Ω.
- ✓ In order to improve the antistatic performance of the USB interface, it is recommended to add an

ESD protection device on the data line. The equivalent capacitance of the protection device is less than 2pF.

- ✓ The USB interface bus supply voltage is provided internally by the module and does not need to be externally supplied. At the same time, since the USB interface of the module does not provide USB bus power, the module can only be used as a slave device of the USB bus device.

3.6 UART Interface

The C17QS module provides three sets of UART interfaces. Main serial port and Auxiliary serial ports, serial port level is 1.8V.

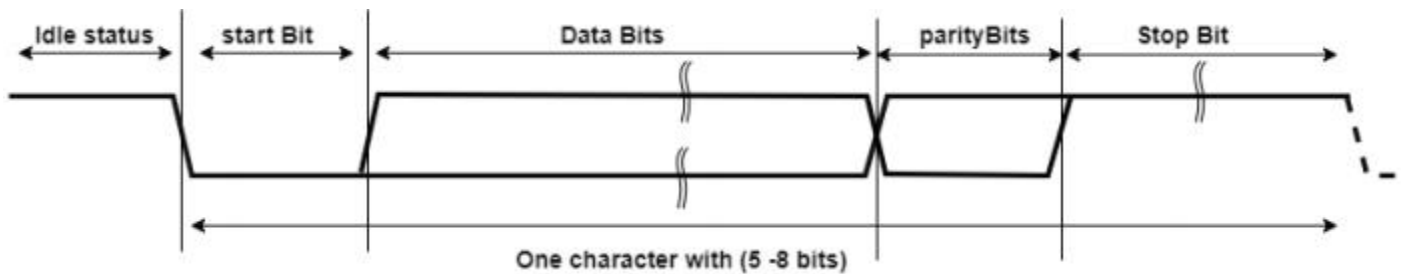


Figure 8 UART sequence diagram

3.6.1 UART2 Serial Port

The pins 27 and 28 of the module are UART2 serial port pins. This can be used for the serial data communication.

Table 3.10 UART3 serial port pin definition

Pin No.	Signal name	I/O	Description	Voltage		
				V_min	V_typical	V_max
27	UART2_TXD	DO	UART 2 Data transmission	1.75	1.8	1.85
28	UART2_RXD	DI	UART 2 Data reception	1.75	1.8	1.85

3.6.2 UART1 Serial Port

The serial port can realize AT interactive instructions, print program log information, and interact with peripheral data and firmware update.

The module's serial port baud rate can be set to 600,1200,2400,4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800,921600,1152000, 3000000 bps.

The default baud rate is 115200 bps and maximum baud rate is 3000000 bps

The UART interface is defined as follows :

Table 3.11 UART1 serial port signal definition

No.	Name	I/O	Description	Voltage		
				V_min	V_Typical	V_max
38	UART1_DCD	DI	UART 1 Data carrier detect	1.75	1.8	1.85
36	UART1_CTS	DO	UART 1 Clear to send	1.75	1.8	1.85
37	UART1_RTS	DI	UART 1 request to send	1.75	1.8	1.85
30	UART1_DTR	DO	UART 1 Data terminal ready	1.75	1.8	1.85
35	UART1_TXD	DO	UART 1 Transmit data	1.75	1.8	1.85
34	UART1_RXD	DI	UART 1 Receive data	1.75	1.8	1.85

3.6.3 UART0 Serial Port

The pins 22 and 23 of the module are UART2 serial port pins. This UART is used for debugging data. The pins are defined as follows:

Table 3.12 UART2 serial port pin definition

Pin No.	Signal name	I/O	Description	Voltage		
				V_min	V_Typical	V_max
22	DBG_RXD	DI	UART2 Data transmission	1.75	1.8	1.85

23	DBG_TXD	DO	UART2 Data reception	1.75	1.8	1.85
----	---------	----	----------------------	------	-----	------

3.6.4 Serial Port Application Circuit

- The serial level is 1.8V.
- The module's serial port baud rate can be set to 600 to 3000000bps baud rate and the default is 115200bps.
- The UART1 serial port can realize
 - ✓ AT interactive instructions
 - ✓ Print program log information
 - ✓ Interact with peripheral data

When users want to use the full-featured serial port, they can refer to the following connection methods

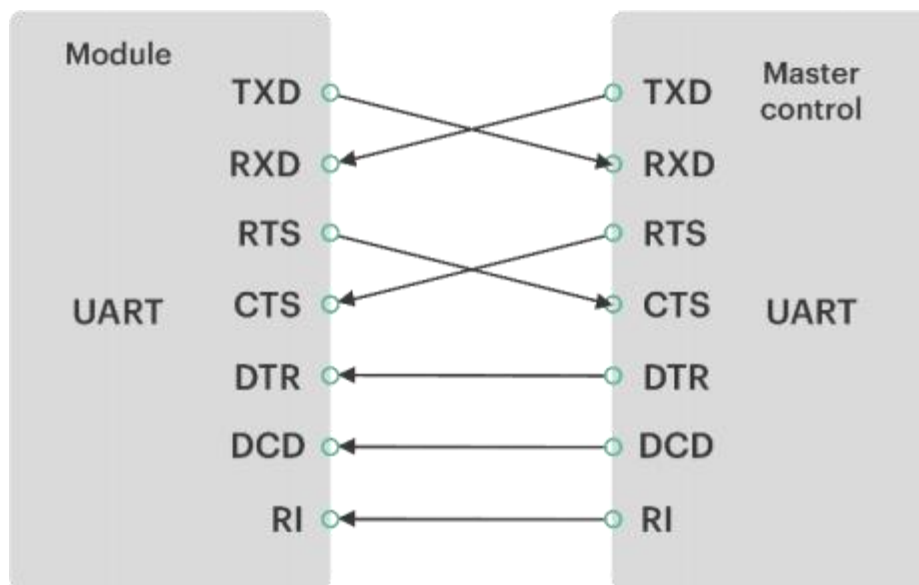


Figure 9 Full-featured serial port design

If you need to use a 2-wire serial port, you can refer to the following serial port design:

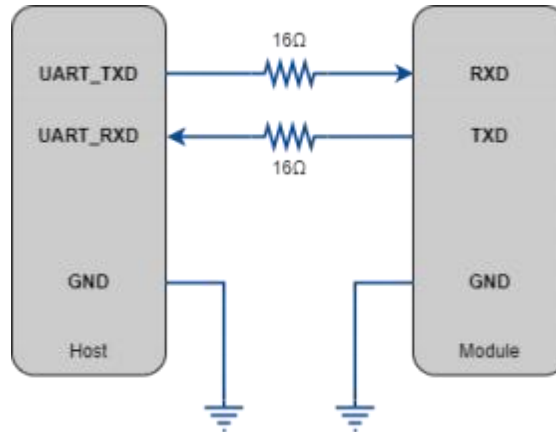


Figure 10 UART serial port design

The serial port of the module is TTL 1.8V level. If the serial port needs to be connected to the MCU of 3.3V level, it is necessary to add a level conversion chip externally to achieve level matching. Use an external 1.8V power source for VCCA. For the chip connection method, refer to the following circuit:

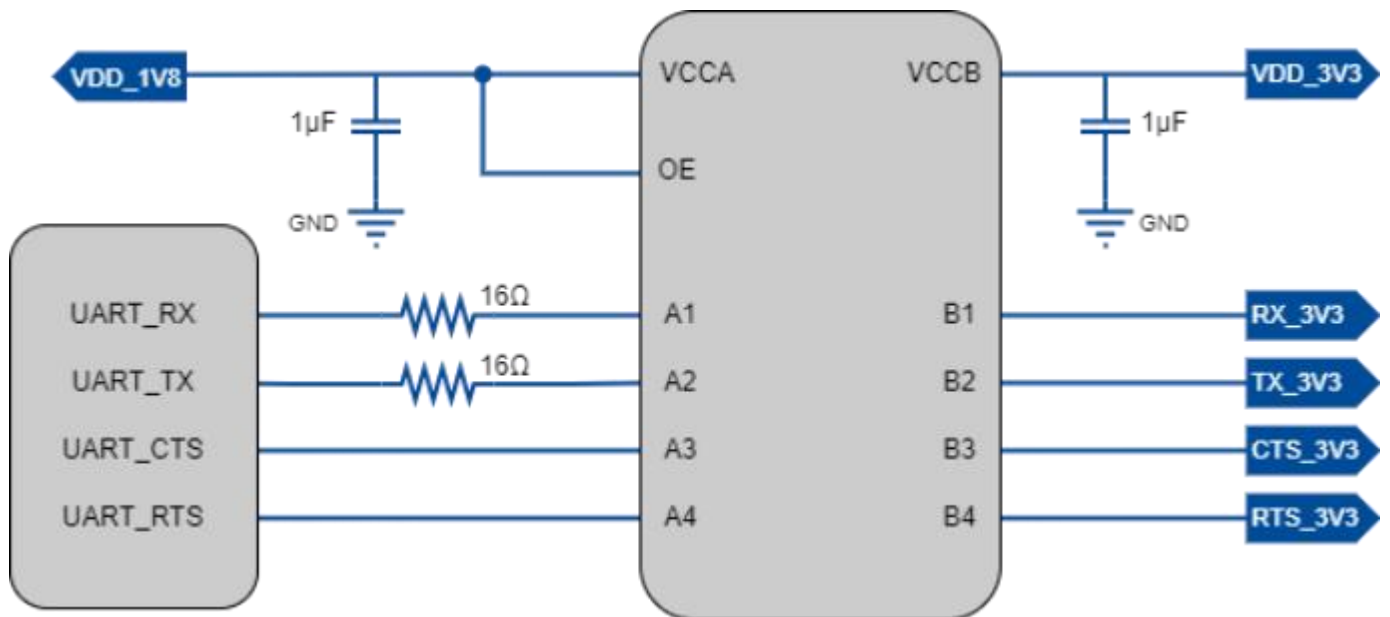


Figure 11 Level conversion chip circuit

3.7 USIM Interface

The C17QS module provides a USIM card interface compatible with the ISO 7816-3 standard. The USIM card power supply is provided by the module's internal power manager and supports 1.8V/3.0V

Table 3.13 SIM card signal definition

No	Signal name	I/O	Description	Voltage		
				V_min	V_typical	V_max
42	USIM_PRESENCE	DI	SIM detect Pin	1.75/2.95	1.8/3	1.85/3.05
43	USIM_VCC	PO	External SIM power	1.75/2.95	1.8/3	1.85/3.05
45	USIM1_UIO	DIO	External SIM card IO	1.75/2.95	1.8/3	1.85/3.05
46	USIM1_UCLK	DIO	External SIM clock	1.75/2.95	1.8/3	1.85/3.05
44	USIM1_URSTn	DIO	External SIM card reset	1.75/2.95	1.8/3	1.85/3.05

3.7.1 USIM Card Reference Circuit

The C17QS module does not come with a USIM card slot. Users need to design a USIM card slot on their own interface board. The module supports USIM of voltages 1.8V and 2.85V.

The USIM card interface reference circuit is as follows:

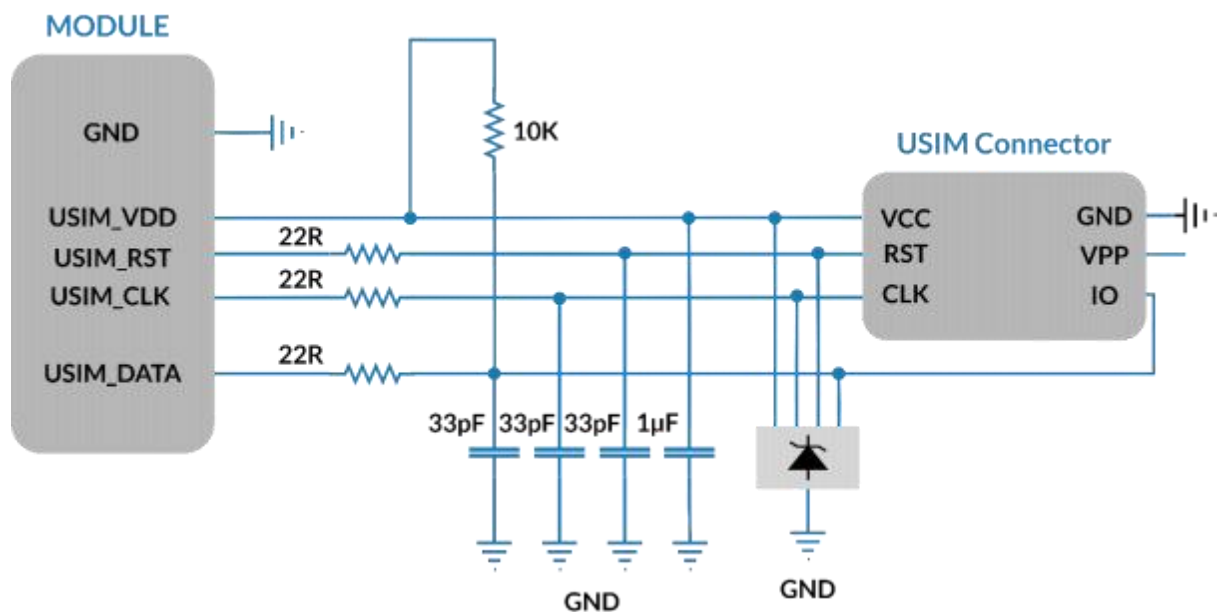


Figure 12 USIM design circuit diagram

NOTE

- ✓ The USIM interface cable is recommended to use ONSEMI's SMF15C device for ESD protection. The peripheral circuit components should be placed close to the card holder. The SIM card holder is close to the module layout.

- ✓ The USIM card circuit is susceptible to radio frequency interference and does not recognize or drop the card. Therefore, the card slot should be placed as far as possible from the RF radiation of the antenna. The card trace should be as far away as possible from the RF, power supply and high-speed signal lines.
- ✓ USIM_PRESENCE is high by default. The SIM card status can be detected by this PIN during hot plug application. It is recommended to provide provision for pull-up.
- ✓ To avoid transient voltage overload, the USIM interface requires a 22R resistor in series with each other on the signal line path.
- ✓ The ground of the USIM deck and the ground of the module should maintain good connectivity.

3.8 General Purpose GPIO Interface

The C17QS module contains eleven general purpose control signals. The interface is defined as follows:

Table 3.14 General GPIO Pin Definitions

Pin No.	Definition	I/O	Functional description	Voltage		
				V_min	V_typical	V_max
11	GPIO16	DIO	Configurable IO	1.75	1.8	1.85
25	GPIO21	DIO	Configurable IO	1.75	1.8	1.85
26	GPIO17	DIO	Configurable IO	1.75	1.8	1.85
56	GPIO20	DIO	Configurable IO	1.75	1.8	1.85
64	GPIO19	DIO	Configurable IO	1.75	1.8	1.85
65	GPIO18	DIO	Configurable IO	1.75	1.8	1.85
66	GPIO48	DIO	Configurable IO	1.75	1.8	1.85
76	GPIO29	DIO	Configurable IO	1.75	1.8	1.85

77	GPIO28	DIO	Configurable IO	1.75	1.8	1.85
78	GPIO54	DIO	Configurable IO	1.75	1.8	1.85
94	GPIO52	DIO	Configurable IO	1.75	1.8	1.85

3.9 Network Status Indication Interface

The C17QS module provides an open-drain GPIO signal to indicate the status of the RF communication.

3.9.1 Network Status

C17QS provides two network status indication pins: **USB_BOOT** & **NET_STATUS** (Pins **21** & **75**). These pins are used to drive a network status indication LED. Since both the pins have the same functionality, use only one and keep the other floating.

The following tables describe the pin definition and logic level changes of NETLIGHT in different network activity status.

Table 3.15 Network Indicator Pin Definition

Pin	Signal name	I/O	Description	Voltage		
				V_min	V_typical	V_max
21	NETLIGHT	DO	NET_STATUS function	1.75	1.8	1.85
75	USB_BOOT	DO	Network status indication	1.75	1.8	1.85

Table 3.16 Network Indication Status

Status	LED display status
No service	OFF
Searching for Network	Flashing

The module registers 4G network or module to register non-4G network for voice SMS and other services (Latched onto Network)

Constantly Bright

The LED network indicator reference design is as follows:

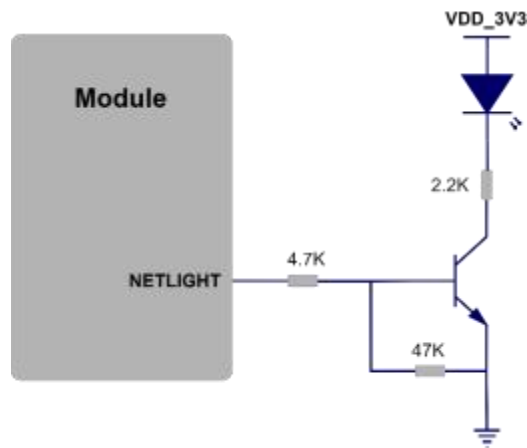


Figure 13 Net light reference circuit diagram

When the module enters flight mode, the RF function does not work and all AT commands related to RF functions will be inaccessible. This mode can be set by

- ✓ Software: **AT+CFUN=4**

Table 3.17 Network Indicator Pin Definition

Pin	Signal name	I/O	Description
19	AP_READY	DI	Wake up Interrupt
18	W_DISABLE	DI	Put into Flight Mode

 NOTE

- The brightness of the network indicator can be adjusted by adjusting the current limiting resistor, which can be adjusted to a maximum of 40 mA.
- Remember to use only one among the pins **21** and **75**. While using one, keep the other floating.

3.9.2 Module Status Indication

- ✓ The C17QS module provides a pin as a working status indicator for the module
- ✓ This pin can be used to connect to a GPIO or LED with pull-up
- ✓ It is used to indicate the power-on status of the module
- ✓ The drive current should be less than 0.8mA
- ✓ The STATUS pin will output a high level.

Table 3.18 Module Status Indicator Pin Definition

Pin	Signal name	I/O	Description
20	STATUS	DO	Module power on status indication

The following figure shows the STATUS reference circuit design:

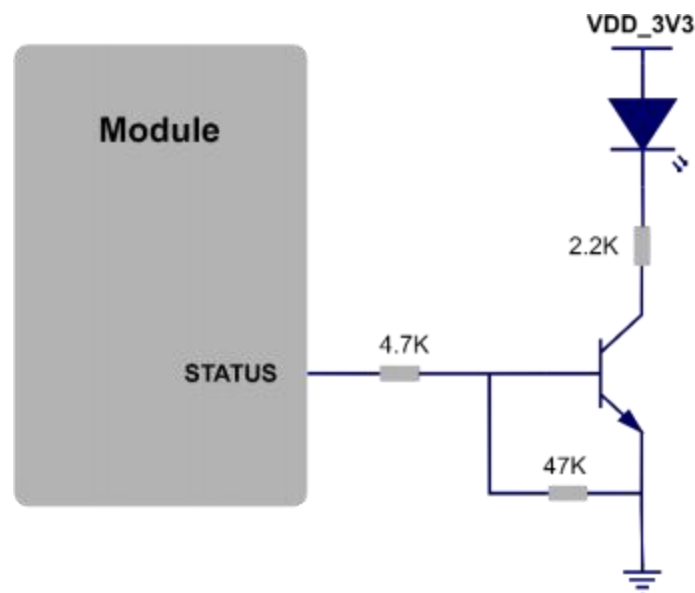


Figure 14 STATUS Pin Reference Circuit

3.10 I2S Interface

C17QS module provides a set of I2S bus interface which is used for connecting digital audio devices.

Table 3.19 I2S pin definition

No	Signal name	I/O	Description	Voltage		
				V_min	V_typical	V_min
7	I2S_DOUT	DIO	I2S Data out	1.75	1.8	1.85
6	I2S_DIN	DIO	I2S Data in	1.75	1.8	1.85
5	I2S_LRCK	DIO	I2S Strobe Clock	1.75	1.8	1.85
4	I2S_BLK	DIO	I2S Master Clock	1.75	1.8	1.85
63	I2S_MCLK	DIO	I2S Bit Clock	1.75	1.8	1.85

3.11 I2C Bus

The C17QS module provides a set of hardware bidirectional serial buses with an I2C interface of 1.8V level, a *5.0 Protocol* interface, and a clock rate of 400 KHz.

Table 3.20 I2C pin definition

Pin No.	Signal name	I/O	Description	Voltage		
				V_min	V_Typical	V_max
40	I2C_SCL	DO	I2C Serial Clock	1.75	1.8	1.85
41	I2C_SDA	DIO	I2C Serial data	1.75	1.8	1.85

The I2C reference circuit is connected as follows:

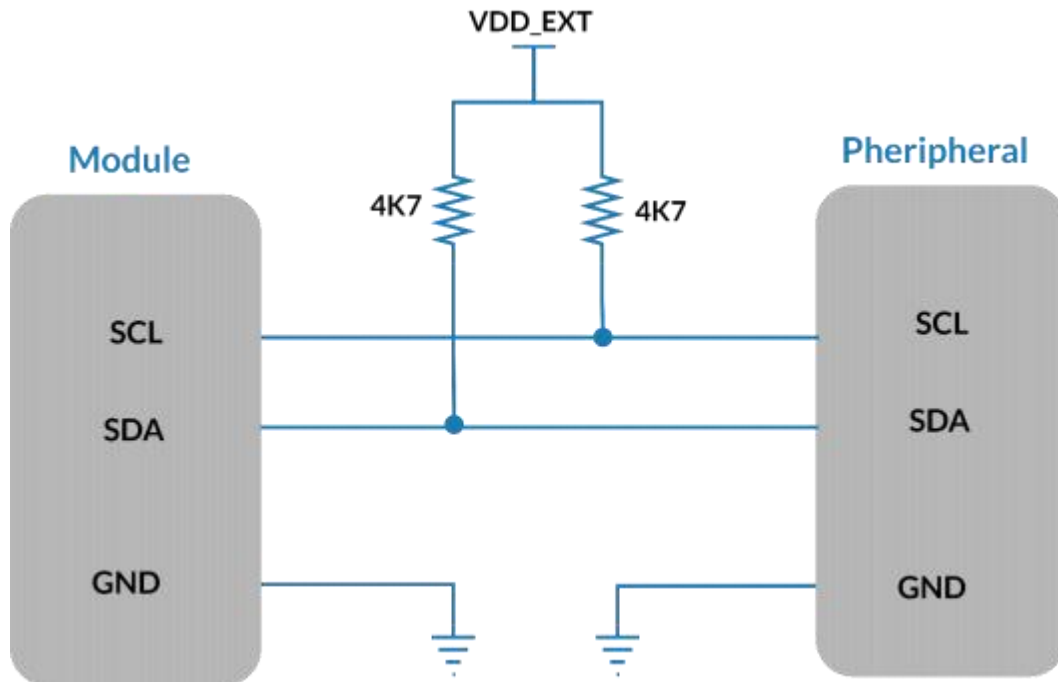


Figure 15 I2C interface reference circuit diagram

3.12 SWD Interface

C17QS module provides a 2-pin serial wire debug (SWD) interface which is an alternative to JTAG.

Table 3.21 SWDIO Pin Definitions

Pin No.	Pin name	IO	Definition	Voltage		
				V_min	V_Typical	V_max
92	SWDIO0	DIO	Serial wire debug data	1.75	1.8	1.85
93	SWCLK0	DIO	Serial wire debug clock	1.75	1.8	1.85

3.13 ADC Interface

The C17QS provides two analog-to-digital converter interfaces to read the voltage value.

- ✓ The ADC interface input voltage cannot exceed VBAT
- ✓ It is recommended that the ADC pin be input with a voltage divider circuit

Table 3.22 ADC Pin Definitions

Pin No.	Signal name	IO	Description	Voltage		
				V_min	V_Typical	V_max
2	ADC1	AIO	Analog to digital converter interface 1	0	-	3.4
24	ADC0	AIO	Analog to digital converter interface 0	0	-	3.4

3.14 Antenna

The C17QS module provides two antenna interfaces, one main set antenna interface, which is responsible for the CAT .1bis signals of the transceiver module, and another GNSS antenna interface.

The GNSS antenna interface is **L1+L5**.

The impedance of the antenna interfaces are 50 ohms.

Table 3.23 Antenna interface pin definition

Pin No.	Signal Name	Description	Remarks
60	LTE_ANT	Main antenna interface	50Ω characteristic impedance
49	GNSS_IN	GNSS L1 antenna interface	50Ω characteristic impedance

The pin 60 of the C17QS is the main set antenna interface.

To facilitate the debugging of the antenna, a π -type matching circuit needs to be added to the main board, and a 50-ohm impedance line is taken.

Recommended circuit is shown below :

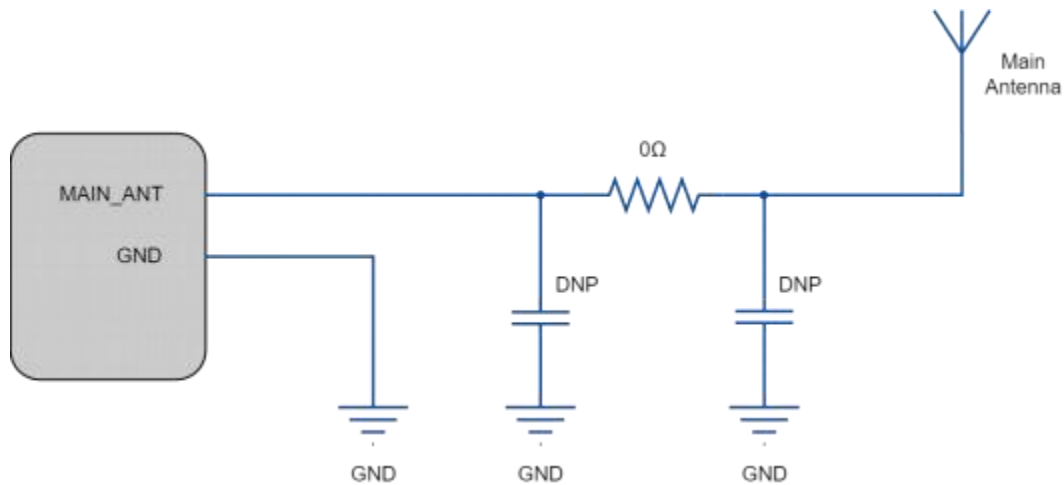


Figure 16 Main antenna matching circuit

The pin 49 of C17QS is the GNSS antenna interface.

The C17QS has a dedicated antenna **L1+L5**, it supports GPS/QZSS: L1, L5 /BDS: B1C, B2a, B2b, B3I/GLONASS/Galileo / NavIC: L5

SBAS.

In order to facilitate antenna debugging, a π -type matching circuit needs to be added to the motherboard and a 50-ohm impedance line is used.

NOTE

- ✓ The GNSS antenna needs to maintain a certain distance from the main antenna.
- ✓ The GNSS antenna has two antenna connection modes:
Passive antenna mode and Active antenna mode.
- ✓ An external power supply is required while using an Active antenna, as the module cannot provide power to GNSS Active antenna.

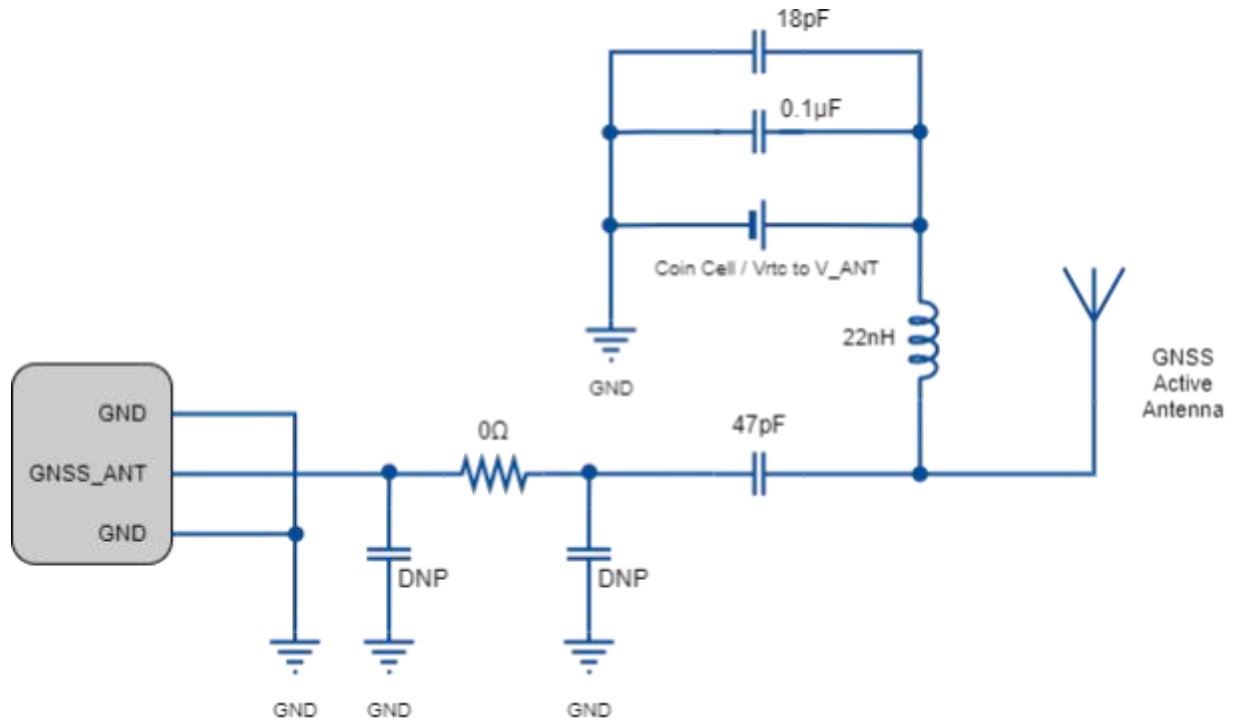


Figure 17 GNSS active antenna matching circuit

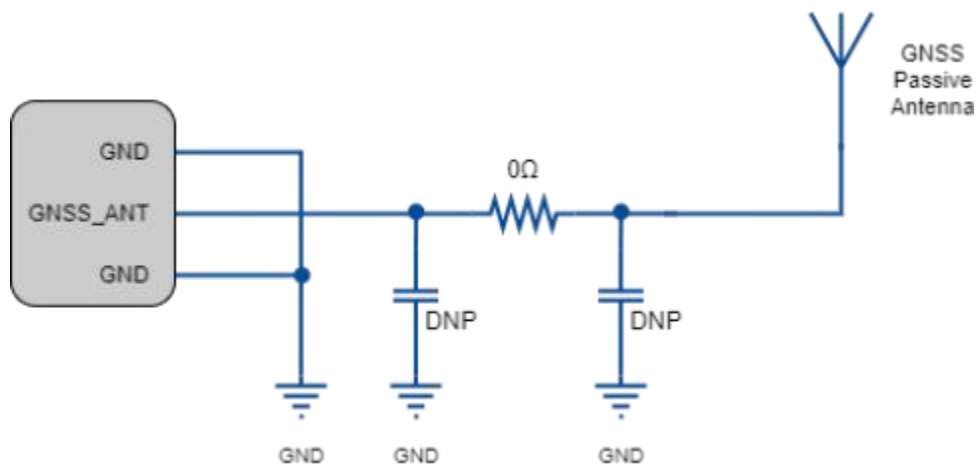


Figure 18 GNSS passive antenna matching circuit

 NOTE

- ✓ An external LDO can be selected to supply power according to the active antenna requirement.
- ✓ If the module is designed with a passive antenna, then the VDD circuit is not needed.
- ✓ The LTE_MAIN antenna is distributed reasonably to improve the receiving sensitivity.

- ✓ In actual use, the antenna board can be debugged and optimized according to the user's circuit board.
- ✓ Antenna impedance traces need to be away from digital signal lines, power supplies and other interference signals.
- ✓ The antenna impedance traces need to be three-dimensionally packaged, and the ground holes are added on both sides of the trace to isolate.

3.14.1 RF Trace Reference

The mainset of the C17QS module are extracted by pad. The antenna pad to the antenna feed point must use microstrip lines or other types of RF traces. The characteristic impedance of the signal line should be controlled at 50Ω .

The impedance of the RF signal line is determined by the material's dielectric constant, trace width (W), ground clearance (S), and reference ground plane height (H). Therefore, the RF trace requires an impedance simulation tool to calculate the impedance of the RF trace.

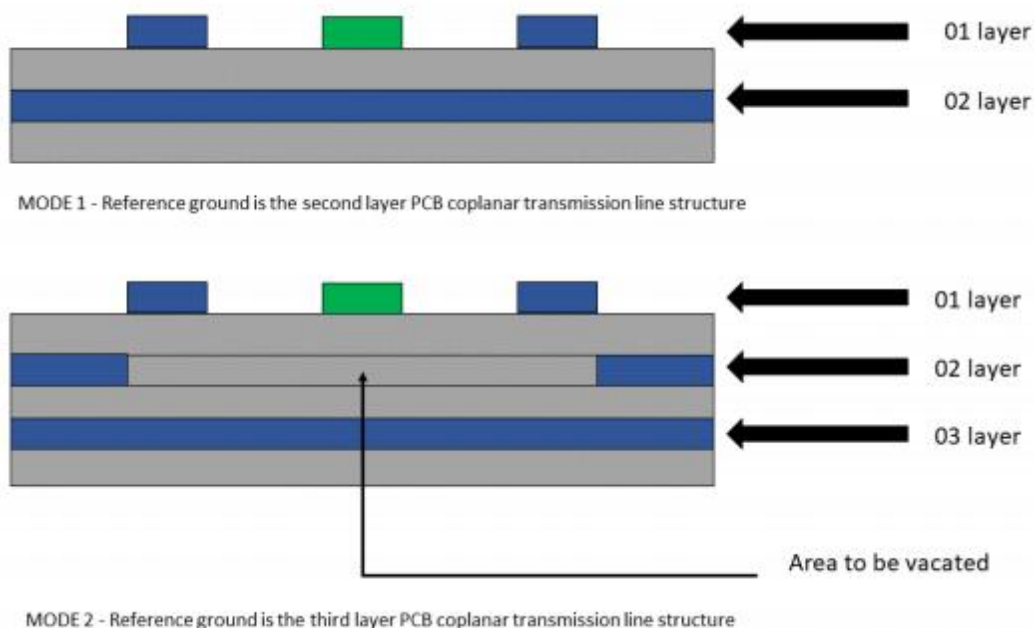


Figure 19 Coplanar antenna

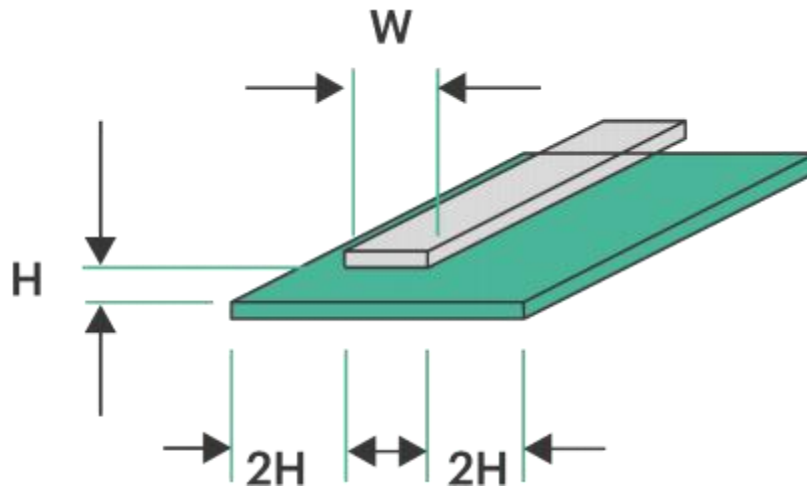


Figure 20 The complete structure of the two-layer PCB microstrip line

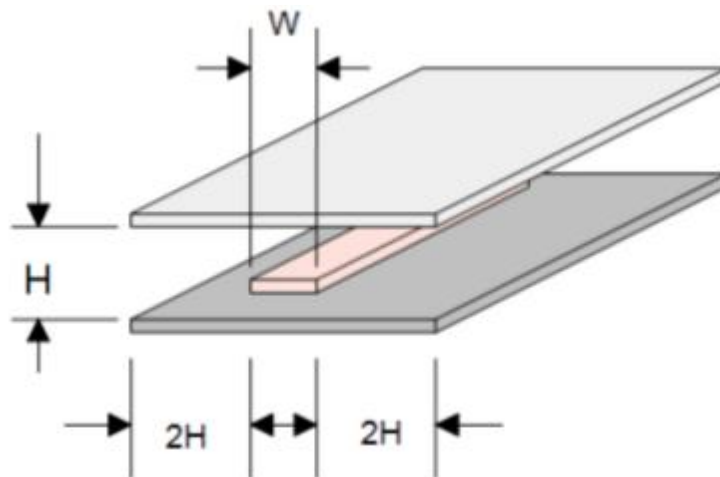


Figure 21 The complete structure of the multilayer PCB strip line

 NOTE

- Since Coplanar antennas are having maximum noise immunity, it is preferred.

3.15 Control Interface

Table 3.25 Control interface pin definition

Pin No.	Signal name	I/O	Description
20	STATUS	DO	Module power on status indication
18	W_DISABLE	DI	Put into Flight Mode

STATUS:

This pin is used to get the status of the module.

FLIGHT_MODE:

This pin is used to put the module into Flight mode and disable the RF transmission.

3.16 GNSS Interface

Multi - GNSS receiver:

- ✓ **L1+L5** multi-band GNSS receiver
- ✓ GPS/QZSS: **L1, L5**
- ✓ BDS: B1C, B2a, B2b, B3I
- ✓ GLONASS
- ✓ Galileo
- ✓ NavIC: L5
- ✓ SBAS

Table 3.26 GNSS interface pin definition

Pin No.	Signal name	I/O	Description	Voltage		
				V_min	V_Typical	V_max
49	GNSS_IN	-	GNSS Antenna interface	-	-	-
99	GNSS_PPS_OUT	DO	1PPS indicator	1.75	1.8	1.85
84	QCG110_UART1_DEBUG_TX	DO	GNSS UART Transmission	1.75	1.8	1.85
83	QCG110_UART1_DEBUG_RX	DI	GNSS UART Reception	1.75	1.8	1.85
51	GNSS_BAT		Power input for the backup power domain			

1PPS:

Synchronized at rising edge, and the pulse width is 500ms. This pin must be low at start-up for normal operation. It has been pulled down internally with a 47KΩ resistor. If unused, keep this pin open.

GNSS interface

NMEA logs are fetched through the AT port after setting the needed AT commands.



Figure 22 GNSS BAT Input

NOTE

- The recommended voltage rating of GNSS_VDD is 3.3 V.
- UART2 and GNSS UART are internally connected so while using GNSS ensure that UART 2 is kept as floating and viceversa.
- When GNSS is operating in independent mode, only GNSS_VDD needs to be supplied; VBAT is not required.

As VBAT_ powers the entire RF of LTE and GNSS. GNSS_VDD can power entire GNSS section

- Please refer the *C17QS GNSS Application note* for further information.

3.17 SPI Interface

Table 3.27 SPI interface pin definition

Pin No.	Signal name	I/O	Description	Voltage		
				V_min	V_Typical	V_max
12	SPI_CLK	DO	Serial Clock	1.75	1.8	1.85
13	SPI_CS	DO	Slave select	1.75	1.8	1.85
14	SPI_MISO	DI	Master input slave output	1.75	1.8	1.85
16	SPI_MOSI	DO	Master output slave input	1.75	1.8	1.85
95	SPI1_CLK	DO	Serial Clock 1	1.75	1.8	1.85
96	SPI1_CS	DO	Slave select 1	1.75	1.8	1.85
97	SPI1_MISO	DI	Master input slave output 1	1.75	1.8	1.85
98	SPI1_MOSI	DO	Master output slave input 1	1.75	1.8	1.85

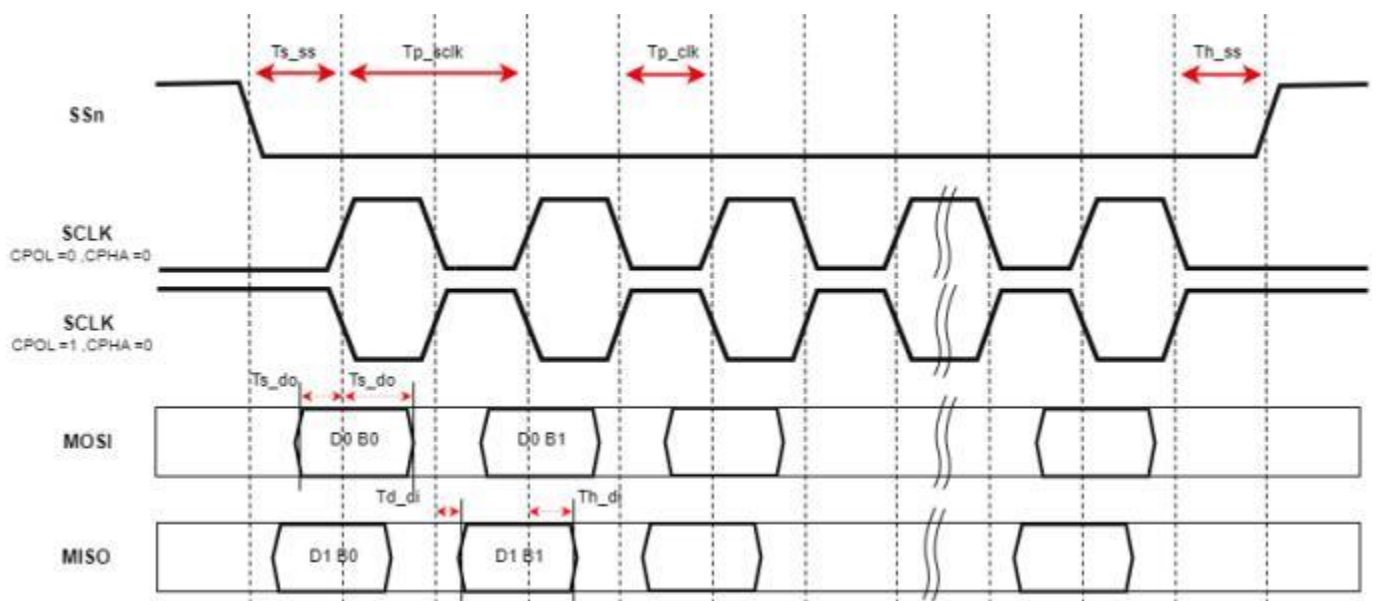


Figure 23 SPI master sequence diagram CPHA = 0

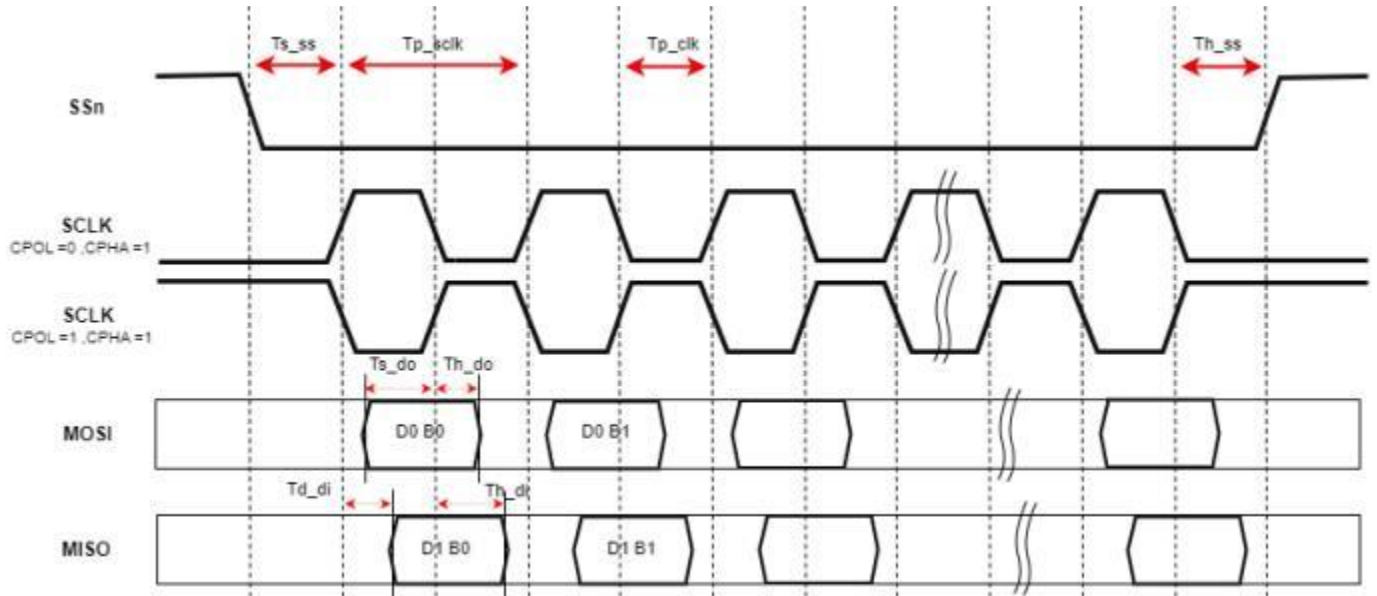


Figure 24 SPI master sequence diagram CPHA = 1

4 Overall Technical Indicators

4.1 Chapter Overview

The C17QS module RF overall specifications include the following sections:

- ✓ Working frequency
- ✓ GNSS Performances
- ✓ Antenna requirements

4.2 Working Frequency

Table 4.1 RF frequency table

Frequency band	Uplink frequency	Downstream frequency	Mode
LTE B1	1920 MHz-1980 MHz	2110 MHz-2170 MHz	FDD
LTE B2	1850 MHz-1910 MHz	1930 MHz-1990 MHz	FDD
LTE B3	1710 MHz-1785 MHz	1805 MHz-1880 MHz	FDD
LTE B4	1710 MHz-1755 MHz	2110 MHz-2155 MHz	FDD
LTE B5	824 MHz-849 MHz	869 MHz-894 MHz	FDD
LTE B7	2500 MHz - 2570 MHz	2620 MHz - 2690 MHz	FDD
LTE B8	880 MHz-915 MHz	925 MHz-960 MHz	FDD
LTE B12	699 MHz - 716 MHz	729 MHz - 746 MHz	FDD
LTE B13	777 MHz - 787 MHz	746 MHz - 756 MHz	FDD
LTE B14	788 MHz - 798 MHz	758 MHz - 768 MHz	FDD
LTE B18	815 MHz - 830 MHz	860 MHz - 875 MHz	FDD
LTE B19	830 MHz - 845 MHz	875 MHz - 890 MHz	FDD

LTE B20	832 MHz- 862 MHz	791 MHz- 821 MHz	FDD
LTE B25	1850 MHz - 1915 MHz	1930 MHz - 1995 MHz	FDD
LTE B26	814 MHz - 849 MHz	859 MHz - 894 MHz	FDD
LTE B28	703 MHz - 748 MHz	758 MHz - 803 MHz	FDD
LTE B34	2010 MHz - 2025 MHz	2010 MHz - 2025 MHz	TDD
LTE B38	2570 MHz- 2620 MHz	2570 MHz- 2620 MHz	TDD
LTE B39	1880 MHz - 1920 MHz	1880 MHz - 1920 MHz	TDD
LTE B40	2300 MHz - 2400 MHz	2300 MHz - 2400 MHz	TDD
LTE B41	2496 MHz - 2690 MHz	2500 MHz - 2690 MHz	TDD
LTE B66	1710 MHz - 1780 MHz	2110 MHz - 2200 MHz	FDD
LTE B71	663 MHz - 698 MHz	617 MHz - 652 MHz	FDD

4.3 GNSS Performances

C17QS Module GNSS performance parameters:

Table 4.2 GNSS performance parameters

Features	Description
Receiving Bands	✓ GPS L1: 1575.42 Mhz ✓ BD2 B1 C/A: 1561.098 MHz ✓ GLONASS ✓ GALILEO ✓ NavIC L5 ✓ SBAS
Positioning Accuracy:	< 1.0 mCEP50
Velocity Accuracy:	< 0.05 m/s CEP
TTFF	✓ Cold Start < 27s ✓ Hot Start ≤ 1s

Sensitivity:	✓ Cold Start: -148 dBm ✓ Tracking: -165 dBm ✓ Hot Start: -155 dBm ✓ Reacquisition: -158 dBm
GNSS Operating limit	✓ Velocity -515 m/s ✓ Altitude -18,000 m

4.4 Antenna Requirements

C17QS Module Antenna Design Requirements:

Table 4.3 Antenna indicator requirements

Frequency band	Standing wave ratio	Antenna gain	Effectiveness	TRP	TIS
B1 FDD	<2:1	> -2.5dbi	> 40%	>16.5	<-88
B2 FDD	<2:1	> -2.5dbi	> 40%	>16.5	<-88
B3 FDD	<2:1	> -2.5dbi	> 40%	>16.5	<-88
B4 FDD	<2:1	> -2.5dbi	> 40%	>16.5	<-88
B5 FDD	<2:1	> -2.5dbi	> 40%	>16.5	<-88
B7 FDD	<2:1	> -2.5dbi	> 40%	>16.5	<-88
B8 FDD	<2:1	> -2.5dbi	> 40%	>16.5	<-88
B12 FDD	<2:1	> -2.5dbi	> 40%	>16.5	<-88
B13 FDD	<2:1	> -2.5dbi	> 40%	>16.5	<-88
B18 FDD	<2:1	> -2.5dbi	> 40%	>16.5	<-88
B19 FDD	<2:1	> -2.5dbi	> 40%	>16.5	<-88
B20 FDD	<2:1	> -2.5dbi	> 40%	>16.5	<-88

B25 FDD	<2:1	> -2.5dbi	> 40%	>16.5	<-88
B26 FDD	<2:1	> -2.5dbi	> 40%	>16.5	<-88
B28 FDD	<2:1	> -2.5dbi	> 40%	>16.5	<-88
B40TDD	<2:1	> -2.5dbi	> 40%	>16.5	<-88
B41 TDD	<2:1	> -2.5dbi	> 40%	>16.5	<-88
B66 FDD	<2:1	> -2.5dbi	> 40%	>16.5	<-88

5 Interface Electrical Characteristics

5.1 Chapter Overview

- Working storage temperature
- Electrostatic property
- Reliability index
- Module IO level
- Power supply
- Power consumption characteristics

5.2 Working Storage Temperature

Table 5.1 C17QS module working storage temperature

Parameter	Minimum	Maximum
Normal operating temperature	-40. C	85. C
Storage temperature	-55. C	150. C

5.3 Electrostatic Property

There is no overvoltage protection inside the C17QS module.

The ESD protection is required when the module is used to ensure product quality.

ESD design recommendations:

- ✓ The USB port needs to add TVS on VDD, D+, D- for protection, and the TVS parasitic capacitance on D+/D- is <2pF
- ✓ The module's USIM card external pin needs to be protected by TVS, and the parasitic capacitance requirement is <10pF
- ✓ The PCB layout of the protective device should be as close as possible to the "V" line to avoid the "T"

line

- ✓ The ground plane around the module guarantees integrity and should not be split
- ✓ ESD control of the surrounding environment and operators is required during module production, assembly and laboratory testing

Table 5.2 C17QS ESD Features

Test port	Contact discharge	Air discharge	Unit
USB interface	±4	±8	KV
USIM interface	±4	±8	KV
VBAT power supply	±4	±8	KV

5.4 Module IO Level

The C17QS module IO levels are as follows:

Table 5.3 Electrical Characteristics of C17QS module

Parameter	Description	Minimum	Maximum
VIH	High level input voltage	$0.65 * VDD_EXT$	$VDD_EXT + 0.3V$
VIL	Low level input voltage	-	$0.35 * VDD_EXT$
VOH	High level output voltage	$VDD_EXT - 0.45V$	VDD_EXT
VOL	Low level output voltage	0	0.45V

5.5 Power Supply

The C17QS module input power requirements are as follows:

Table 5.4 C17QS module Operating Voltage

Parameter	Minimum value	Typical value	Maximum value
Input Voltage	3.6V	3.8V	4.5V

The power-on time of any interface of the module must not be earlier than the boot time of the module, otherwise the module may be abnormal or damaged.

5.6 Power Consumption Characteristics

Table 5.5: LTE Power consumption

Mode	Band	Sensitivity (dBm)	Current consumption @ 23dBm and @ 3.7V		
			Tx Idle USB-Disconnected	Tx Idle USB-Connected	Peak Tx @ Centre frequency
			Average	Average	Average
CAT 1.bis	Band 1	-95.2	290 uA	26.8 mA	590 mA
	Band 2	-99.5	360 uA	27 mA	510 mA
	Band 3	-97.2	300 uA	27 mA	540 mA
	Band 4	-99.1	290 uA	26.8 mA	400 mA
	Band 5	-98.7	270 uA	27 mA	452 mA
	Band 7	-96.1	350 uA	26.9 mA	700 mA
	Band 8	-96.3	292 uA	26.5 mA	494.7 mA
	Band 12	-96.4	325 uA	26.7 mA	460 mA
	Band 13	-99	320 uA	26.6 mA	420 mA
	Band 14	-99	310 uA	26.7 mA	400 mA

	Band 18	-98.5	320 uA	25 mA	475 mA
	Band 19	-99	388 uA	23.3 mA	468 mA
	Band 20	-96.8	386 uA	22.6 mA	467 mA
	Band 25	-99.5	387 uA	23 mA	510 mA
	Band 26	-98.7	388 uA	23.5 mA	421 mA
	Band 28	-96.5	320 uA	24.5 mA	392 mA
	Band 34	-101.5	300 uA	24.3 mA	333 mA
	Band 38	-98.3	305 uA	24 mA	264 mA
	Band 39	-101.3	311 uA	24.5 mA	260 mA
	Band 40	-98.5	285 uA	24.3 mA	356 mA
	Band 41	-98.4	290 uA	23.7 mA	264 mA
	Band 66	-98.5	350 uA	23.1 mA	570 mA
	Band 71	-98.2	320 uA	22.4 mA	336.5 mA
GNSS	Powering ON (Transient peak)		340 mA	340 mA	
	Tracking		10.2 mA	12 mA	
	Fix		7.1 mA	10 mA	
CFUN=0				109 uA	
CFUN=4				105 uA	
SLEEP1			250 uA	4.48 mA	
SLEEP2			350 uA	4.44 mA	
HIBERNATE 2			50 uA	4.28 mA	
HIBERNATE 1			47.1 uA	4.45 mA	
SHUTDOWN				8.47 uA	
MODULE PEAK				TBD	

6 Structural and Mechanical Properties

6.1 Chapter Overview

- ✓ Module structural image
- ✓ Module mechanical size

6.2 Module Structural Image

The figure below shows the top and bottom view of the module.

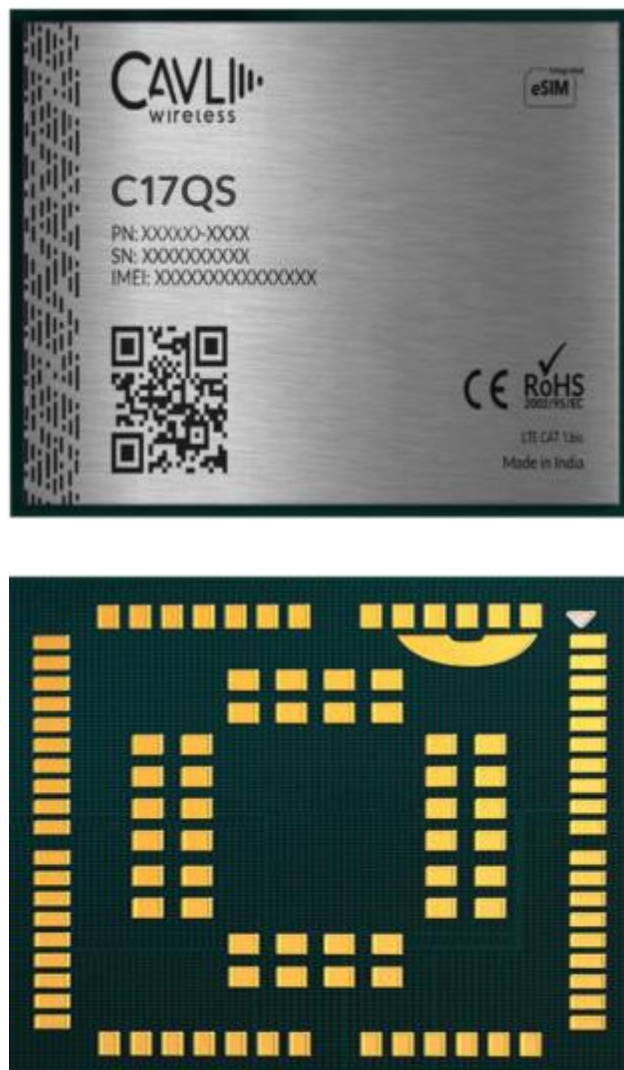


Figure 25 Top view and bottom view of the module

6.2 C17QS Module Mechanical Size

The figure below shows the bottom view size of the module:

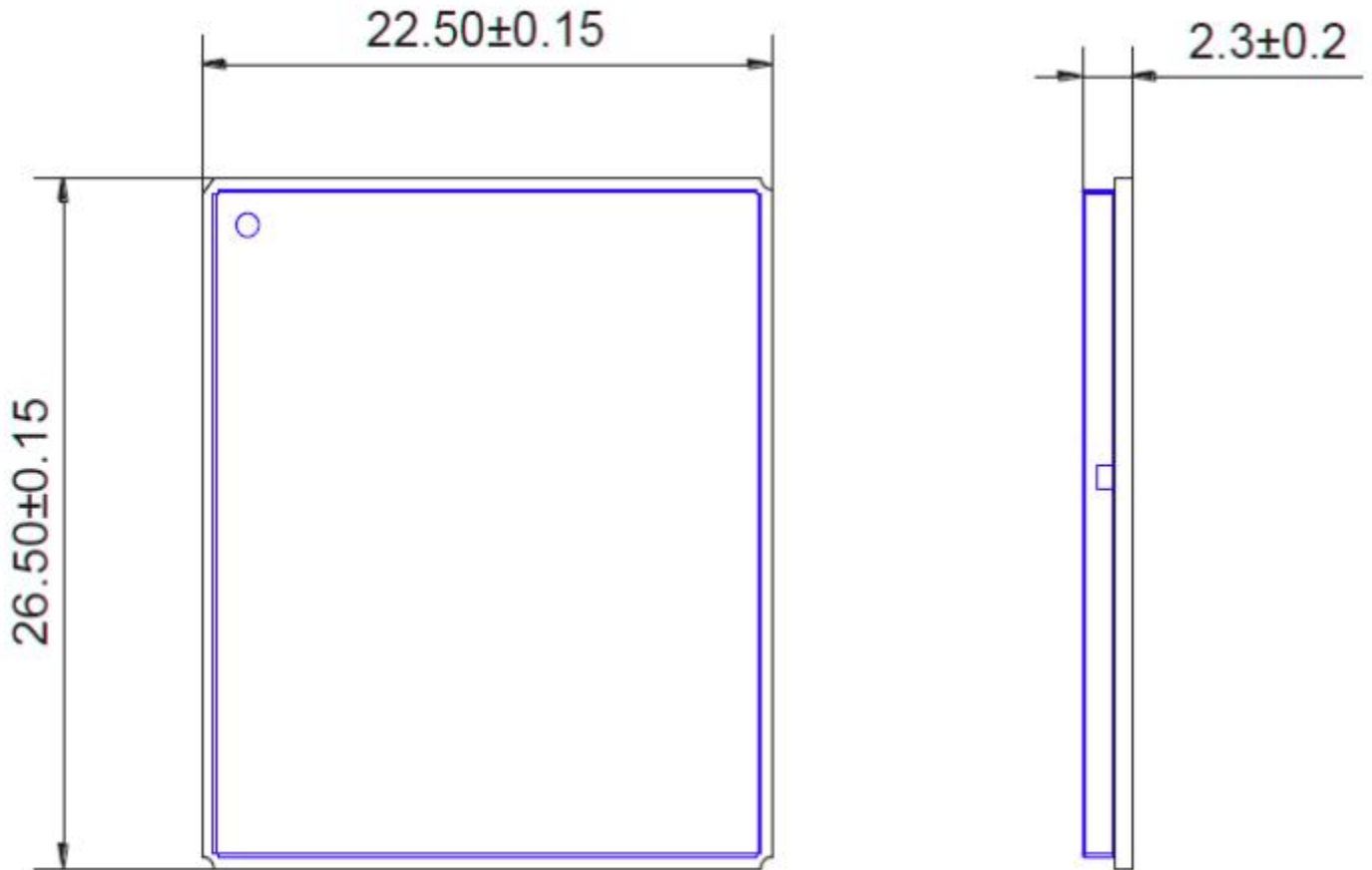


Figure 26 Front view and side view of the module (unit: mm)

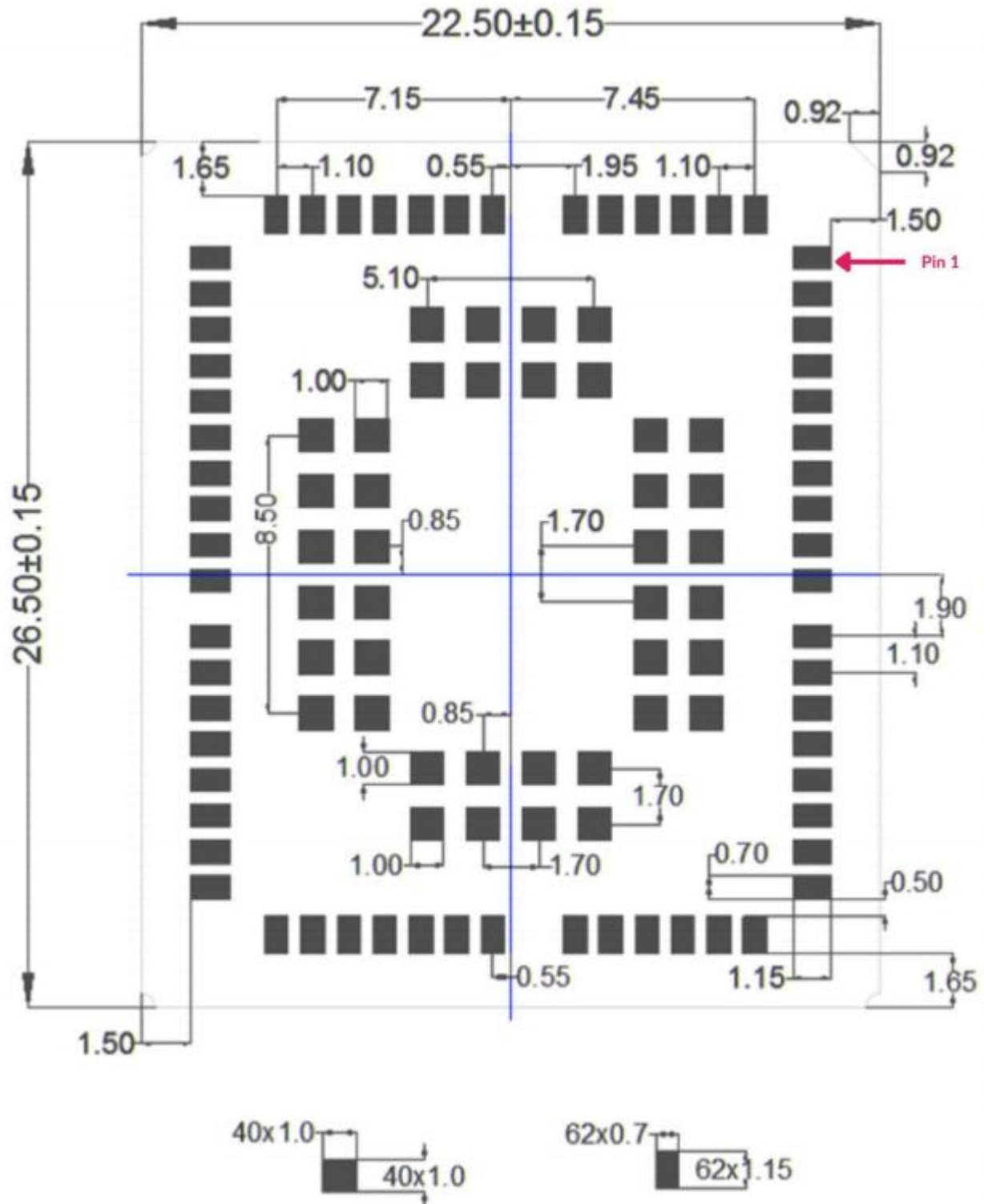


Figure 27 Bottom view of the module (unit: mm)

Module recommended footprint:

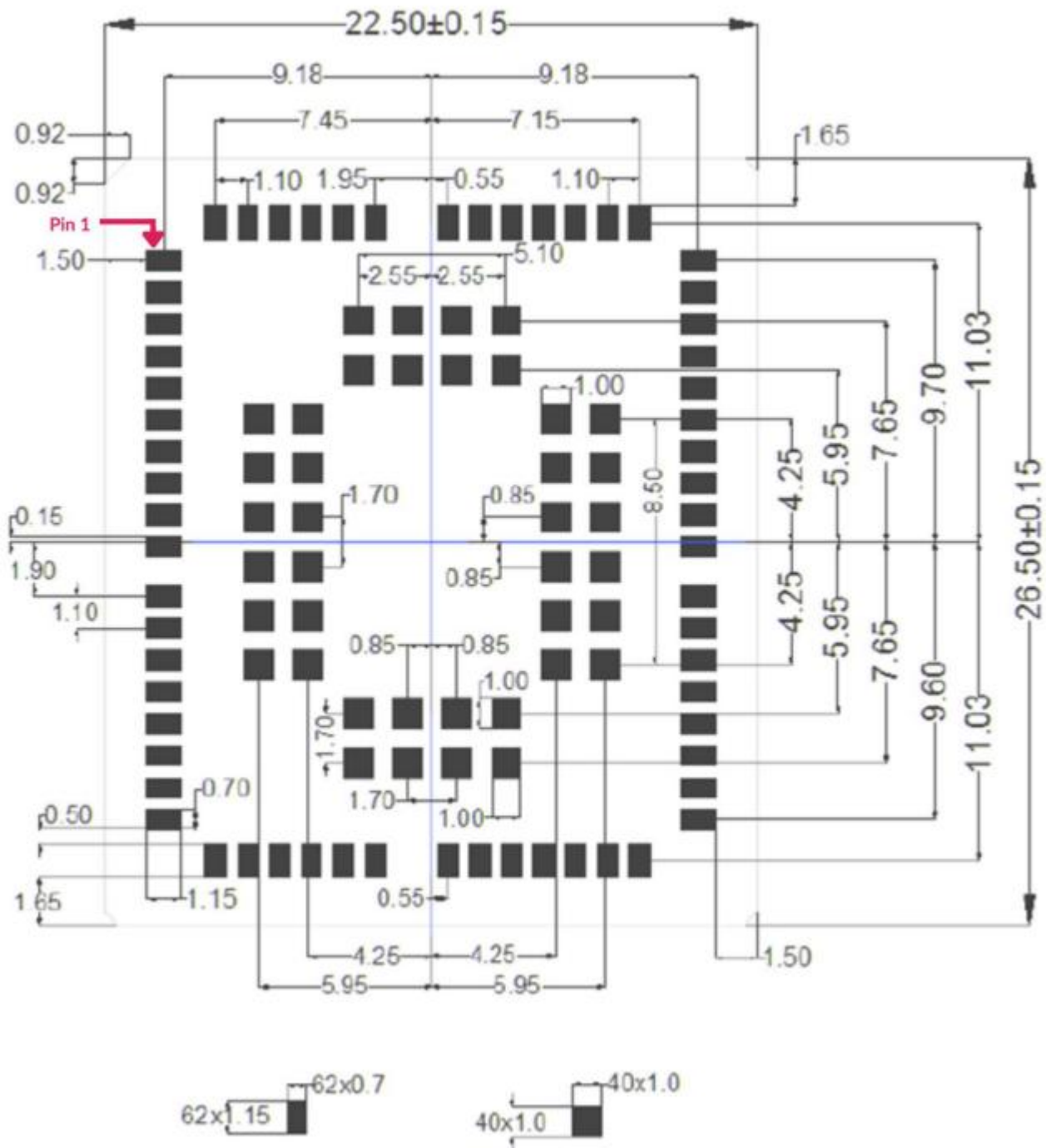


Figure 28 Recommended Footprint (Top View) (unit: mm)

7 Appendix

7.1 Chapter Overview

- ✓ Abbreviations
- ✓ Safety and precautions

7.2 Abbreviations

Table 10.1 Abbreviations

Abbreviations	Full name
3GPP	Third Generation Partnership Project
AP	Access Point
AMR	Adaptive multi-rate
BER	Bit Error Rate
CCC	China Compulsory Certification
CDMA	Code Division Multiple Access
CE	European Conformity
CSD	Circuit Switched Data
CTS	Clear to Send
DC	Direct Current
DTR	Data Terminal Ready
DL	Down Link
DTE	Data Terminal Equipment



DRX	Discontinuous Reception
EDGE	Enhanced Data Rate for GSM Evolution
EU	European Union
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FCC	Federal Communications Commission
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communication
HSDPA	High-Speed Downlink Packet Access
HSPA	Enhanced High Speed Packet Access
HSUPA	High Speed Up-link Packet Access
IMEI	International Mobile Equipment Identity
LED	Light-Emitting Diode
LTE	Long Term Evolution
NC	Not Connected
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PMU	Power Management Unit
PPP	Point-to-point protocol
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RoHS	Restriction of the Use of Certain Hazardous Substances
SMS	Short Message Service
TIS	Total Isotropic Sensitivity

TVS	Transient Voltage Suppressor
TX	Transmitting Direction
UART	Universal Asynchronous Receiver-Transmitter
UMTS	Universal Mobile Telecommunications System
USIM	Universal Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WWAN	Wireless Wide Area Network

7.3 Safety and Precautions

In order to use the wireless device safely, the terminal device informs the user of the relevant safety information:

- ✓ **Interference:** When the use of wireless devices is prohibited or the use of the device may cause interference and security of the electronic device, turn off the wireless device. Because the terminal will send and receive RF signals when it is powered on. It can interfere with TV, radio, computer or other electrical equipment.
- ✓ **Medical equipment:** In medical and health care facilities where the use of wireless devices is prohibited in the express text, please follow the regulations of the site and turn off the device. Some wireless devices may interfere with the medical device, causing the medical device to malfunction or cause errors. If interference occurs, turn off the wireless device and consult a physician.
- ✓ **Flammable and explosive areas:** Inflammable and explosive areas, please turn off your wireless device and follow the relevant label instructions to avoid an explosion or fire. ☒ For example; gas stations, fuel zones, chemical products areas, chemical transportation and storage facilities, areas with explosion hazard signs, areas with “turn off radio equipment” signs, etc.
- ✓ **Traffic Safety:** Please comply with local laws or regulations in your country or region regarding the use of wireless devices when driving a vehicle.
- ✓ **Aviation Safety:** When flying, please follow the airline's regulations and regulations regarding the use of wireless devices. Before taking off, turn off the wireless device to prevent wireless signals from interfering with aircraft control signals.
- ✓ **Environmental Protection:** Please comply with local laws regarding the handling of equipment packaging materials, equipment or accessories, and support recycling operations.
- ✓ **Emergency call:** This device uses wireless signals for propagation. Therefore, there is no guarantee that the network can be connected in all situations, so in an emergency this wireless device cannot be used as the only contact method.



8 Warnings

8.1 CE EU Conformity Statement

HEREBY, CAVLI INC DECLARES THAT THE EQUIPMENT TYPE LTE MODEM, MODEL C17QS is IN COMPLIANCE WITH DIRECTIVE 2014/53/EU

MANUFACTURER ADDRESS: 99 SOUTH ALMADEN BLVD., SUITE 600, SAN JOSE, CA 95113 UNITED STATES.

THE FULL TEXT OF THE EU DECLARATION OF CONFORMITY IS AVAILABLE AT THE FOLLOWING INTERNET ADDRESS:

<https://www.cavliwireless.com/c-series/c17qs.html>

8.2 NCC Caution

減少電磁波影響，請妥適使用

8.3 FCC Warnings

8.3.1 FCC Modular Approval Information

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference.
- (2) This device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.



- This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules.
- These limits are designed to provide reasonable protection against harmful interference in a residential installation.
- This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.
- If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
 - Reorient or relocate the receiving antenna.
 - Increase the separation between the equipment and receiver.
 - Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
 - Consult the dealer or an experienced radio/TV technician for help.

8.3.2 FCC Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

8.3.3 OEM Integration Instructions

This device is intended only for OEM integrators under the following conditions:

The module must be installed in the host equipment such that 20 cm is maintained between the antenna and users, and the transmitter module may not be co-located with any other transmitter or antenna. The module shall be only used with the internal on-board antenna that has been originally tested and certified with this module. External antennas are not supported. As long as these 3 conditions above are met, further transmitter test will not be required.

However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.). The end-product may need Verification testing, Declaration of Conformity testing, a Permissive Class II Change or new Certification. Please involve a FCC certification specialist in order to determine what will be exactly applicable for the end-product.

8.3.4 Validity of using the module certification

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with



another transmitter), then the FCC authorization for this module in combination with the host equipment is no longer considered valid and the FCC ID of the module cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization. In such cases, please involve a FCC certification specialist in order to determine if a Permissive Class II Change or new Certification is required.

8.3.5 Upgrade Firmware

The software provided for firmware upgrade will not be capable to affect any RF parameters as certified for the FCC for this module, in order to prevent compliance issues.

8.3.6 End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains FCC ID : 2BB64C17QSWW".

