

# GLMM24A01

## Hardware Design

**LTE Standard Module Series**

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# About the Document

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# 1 Introduction

This document defines the GLMM24A01 module and describes its air interfaces and hardware interfaces which relate to your applications.

It can help you quickly understand interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, you can use this module to design and to set up mobile applications easily.

## 1.1. Special Marks

**Table 1: Special Marks**

| Mark | Definition                                                                                                                                                                                                                                                                                                                                                               |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| *    | Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable. |

## 2 Product Overview

The module is an SMD module with compact packaging, which is engineered to meet most of the demands of M2M applications, for instance:

- OTT
- CPE
- PoC
- POS
- Tracker
- Data card
- Security system
- Industrial PDA
- Metering

**Table 2: Brief Introduction**

| EG912N-EN      |                                                 |
|----------------|-------------------------------------------------|
| Packaging type | LGA                                             |
| Pin counts     | 126 pins                                        |
| Dimensions     | (29.0 ±0.2) mm × (25.0 ±0.2) mm × (2.4 ±0.2) mm |
| Weight         | Approx. 3.5 g                                   |

### 2.1. Frequency Bands and Functions

**Table 3: Frequency Bands and Functions**

| GLMM24A01 |                                                      |
|-----------|------------------------------------------------------|
| LTE-FDD   | B1/B2/B3/B4/B5/B7/B8/B12/B13/B17/B18/B19/B20/B28/B66 |
| LTE-TDD   | B38/B41                                              |

## 2.2. Key Features

Table 4: Key Features

| Features           | Details                                                                                                                                                                                                                                                                                                                                                                   |
|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Supply Voltage     | <ul style="list-style-type: none"> <li>● Supply voltage range: 3.4–4.3 V</li> <li>● Typical supply voltage: 3.8 V</li> </ul>                                                                                                                                                                                                                                              |
| SMS                | <ul style="list-style-type: none"> <li>● Text and PDU mode</li> <li>● Point-to-point MO and MT</li> <li>● SMS cell broadcast</li> <li>● SMS storage: (U)SIM card and ME; ME by default</li> </ul>                                                                                                                                                                         |
| USB Interface      | <ul style="list-style-type: none"> <li>● Compliant with USB 2.0 specification (slave mode only), with transmission rates up to 480 Mbps</li> <li>● Used for data transmission, AT command communication, software debugging and firmware upgrade</li> <li>● Supports USB serial driver for Windows 7/8/8.1/10/11, Linux 2.6–5.18 and Android 4.x–12.x systems</li> </ul>  |
| USB_BOOT Interface | Supports an emergency download control interface                                                                                                                                                                                                                                                                                                                          |
| (U)SIM Interface   | Supports 1.8 V and 3.0 V                                                                                                                                                                                                                                                                                                                                                  |
| UART Interfaces    | <p><b>Main UART:</b></p> <ul style="list-style-type: none"> <li>● Used for data transmission and AT command communication</li> <li>● Baud rate: 115200 bps by default</li> <li>● Supports RTS and CTS hardware flow control</li> </ul> <p><b>Debug UART:</b></p> <ul style="list-style-type: none"> <li>● Used for log output</li> <li>● Baud rate: 115200 bps</li> </ul> |
| Audio Features     | <ul style="list-style-type: none"> <li>● Supports one digital audio interface: PCM interface</li> <li>● Supports one analog input and one analog output.</li> <li>● LTE: AMR/AMR-WB</li> <li>● Supports echo cancellation and noise suppression</li> </ul>                                                                                                                |
| PCM Interface      | <ul style="list-style-type: none"> <li>● Used for audio function with external codec</li> <li>● Supports 16-bit linear data format</li> <li>● Supports short frame synchronization</li> <li>● Supports master mode</li> </ul>                                                                                                                                             |
| I2C Interface      | <ul style="list-style-type: none"> <li>● One I2C interface</li> <li>● Complies with I2C bus specification version</li> </ul>                                                                                                                                                                                                                                              |
| ADC Interface      | Supports two Analog-to-Digital Converter (ADC) interfaces                                                                                                                                                                                                                                                                                                                 |
| Network Indication | NET_STATUS to indicate network connectivity status                                                                                                                                                                                                                                                                                                                        |

|                            |                                                                                                                                                                                                                                            |
|----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| AT Commands                | Compliant with 3GPP TS 27.007, 3GPP TS 27.005 and Ucloudlink enhancedAT commands                                                                                                                                                           |
| Rx-diversity               | LTE                                                                                                                                                                                                                                        |
| Antenna Interface          | <ul style="list-style-type: none"> <li>● Main antenna interface: ANT_MAIN</li> <li>● 50 <math>\Omega</math> impedance</li> <li>● Wlan antenna interface: AP_WCN_ANT</li> <li>● 50 <math>\Omega</math> impedance</li> </ul>                 |
| Transmitting Power         | <ul style="list-style-type: none"> <li>● LTE-FDD/TDD: Class 3 (23 dBm <math>\pm</math>2 dB)</li> <li>● WIFI: (15dBm <math>\pm</math>3dB)</li> </ul>                                                                                        |
| LTE Features               | <ul style="list-style-type: none"> <li>● Supports up to 3GPP Rel-9 non-CA Cat 1</li> <li>● Supports 1.4/3/5/10/15/20 MHz RF bandwidth</li> <li>● Max. 10 Mbps (DL)/5 Mbps (UL)</li> </ul>                                                  |
| Internet Protocol Features | <ul style="list-style-type: none"> <li>● Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS/FTPS/SSL/FILE/MQTT/MMS/SMTP/SMTPS protocols</li> <li>● Supports PAP and CHAP protocols</li> </ul>                                          |
| Temperature Range          | <ul style="list-style-type: none"> <li>● Operating temperature range <sup>1</sup>: -35 °C to +75 °C</li> <li>● Extended temperature range <sup>2</sup>: -40 °C to +85 °C</li> <li>● Storage temperature range: -40 °C to +90 °C</li> </ul> |
| Firmware Upgrade           | Use USB interface or DFOTA to upgrade                                                                                                                                                                                                      |
| RoHS                       | All hardware components are fully compliant with EU RoHS directive                                                                                                                                                                         |

<sup>1</sup> Within the operating temperature range, the module meets 3GPP specifications.

<sup>2</sup> Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, emergency call, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P<sub>out</sub>, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

## 2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- RAM & Flash
- Radio frequency
- Peripheral interfaces

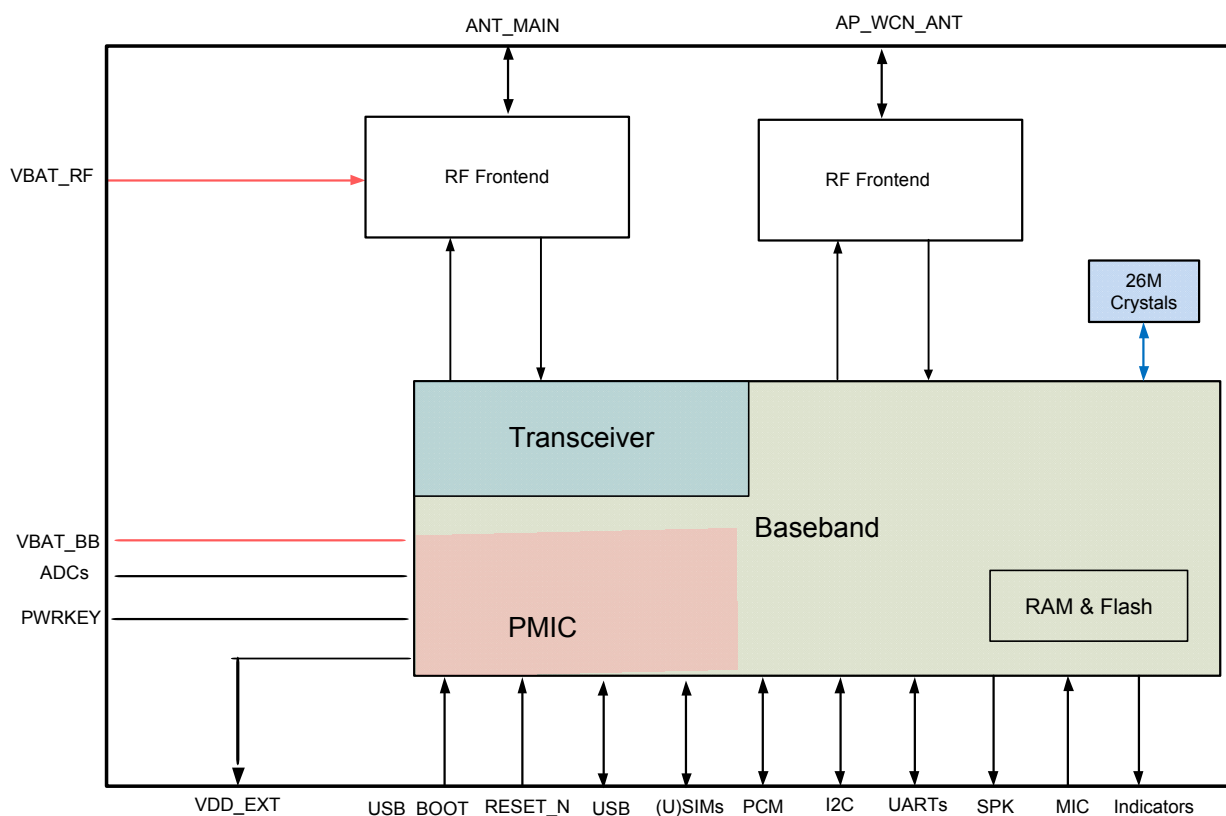
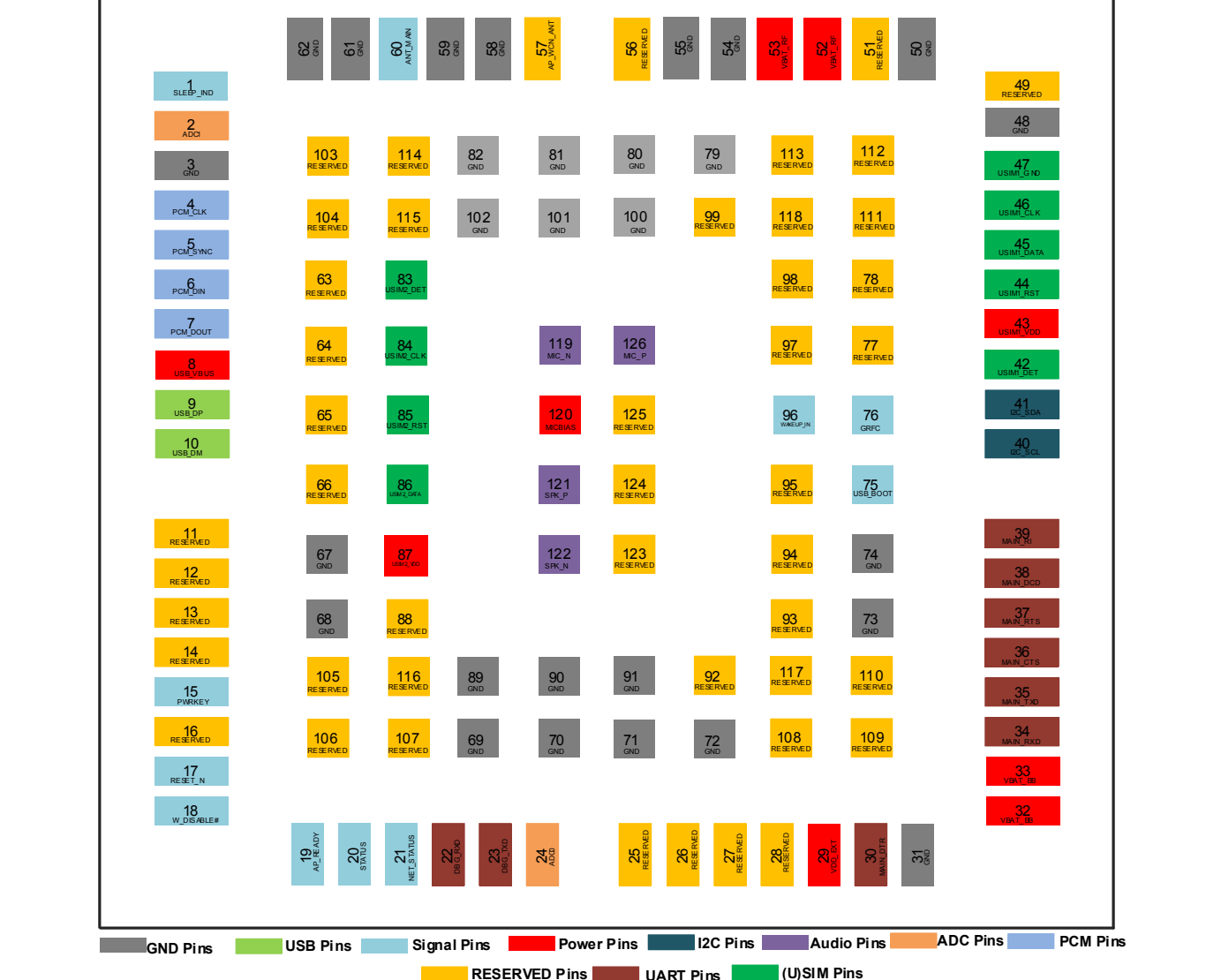


**Figure 1: Functional Diagram**

---



1. All GND pins should be connected to ground, and keep unused and RESERVED pins open

1. All GND pins should be connected to ground, and keep unused and RESERVED pins open.
2. USB\_BOOT cannot be pulled up to high level before the module starts up successfully .
3. Ensure that there is a complete reference ground plane under the module, and the plane shall be placed as close to the module layer as possible. Ensure that there is no other traces on the first layer under the module. And at least a 4-layer board design is recommended.

## 2.5. Pin Description

The following table shows the DC characteristics and pin descriptions.

**Table 5: I/O Parameters Definition**

| Type | Description          |
|------|----------------------|
| AI   | Analog Input         |
| AIO  | Analog Input/Output  |
| AO   | Analog Output        |
| DI   | Digital Input        |
| DIO  | Digital Input/Output |
| DO   | Digital Output       |
| OD   | Open Drain           |
| PI   | Power Input          |
| PO   | Power Output         |

DC characteristics include power domain and rated current, etc.

**Table 6: Pin Description**

| Power Supply |         |     |                                             |                                              |                                                                                                                                       |
|--------------|---------|-----|---------------------------------------------|----------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| Pin Name     | Pin No. | I/O | Description                                 | DC Characteristics                           | Comment                                                                                                                               |
| VBAT_BB      | 32, 33  | PI  | Power supply for the module's baseband part | Vmax = 4.3 V<br>Vmin = 3.4 V<br>Vnom = 3.8 V | External power supply must be provided with sufficient current of at least 0.8 A.<br>It is recommended to add a TVS diode externally. |
| VBAT_RF      | 52, 53  | PI  | Power supply for the module's RF part       |                                              | External power supply must be provided with sufficient current of at least 2.2 A.                                                     |

|         |                                                                     |    |                                    |                               |                                                                                                  |
|---------|---------------------------------------------------------------------|----|------------------------------------|-------------------------------|--------------------------------------------------------------------------------------------------|
|         |                                                                     |    |                                    |                               | It is recommended to add a TVS diode externally.                                                 |
| VDD_EXT | 29                                                                  | PO | Provide 1.8 V for external circuit | Vnom = 1.8 V<br>Iomax = 50 mA | Power supply for external GPIO's pull-up circuits.<br>It is recommended to reserve a test point. |
| GND     | 3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102 |    |                                    |                               |                                                                                                  |

**Turn On/Off/Reset**

| Pin Name | Pin No. | I/O | Description            | DC Characteristics          | Comment                                                                                     |
|----------|---------|-----|------------------------|-----------------------------|---------------------------------------------------------------------------------------------|
| PWRKEY   | 15      | DI  | Turn on/off the module | V <sub>IL</sub> max = 0.5 V | VBAT power domain.                                                                          |
| RESET_N  | 17      | DI  | Reset the module       |                             | Active low.<br>1.8 V power domain.<br>A test point is recommended to be reserved if unused. |

**Indication Interfaces**

| Pin Name   | Pin No. | I/O | Description                                   | DC Characteristics | Comment                    |
|------------|---------|-----|-----------------------------------------------|--------------------|----------------------------|
| STATUS     | 20      | DO  | Indicate the module's operation status        | 1.8 V              | If unused, keep them open. |
| NET_STATUS | 21      | DO  | Indicate the module's network activity status |                    |                            |
| SLEEP_IND  | 1       | DO  | Indicate the module's sleep mode              |                    |                            |

**USB Interface**

| Pin Name | Pin No. | I/O | Description               | DC Characteristics                            | Comment                                   |
|----------|---------|-----|---------------------------|-----------------------------------------------|-------------------------------------------|
| USB_VBUS | 8       | AI  | USB connection detect     | Vmax = 5.25 V<br>Vmin = 3.0 V<br>Vnom = 5.0 V | Test point must be reserved.              |
| USB_DP   | 9       | AIO | USB differential data (+) |                                               | Requires differential impedance of 90 Ω.  |
| USB_DM   | 10      | AIO | USB differential data (-) |                                               | USB 2.0 compliant.<br>Test points must be |

reserved.

**(U)SIM Interfaces**

| Pin Name   | Pin No. | I/O | Description                  | DC Characteristics | Comment                                                                                           |
|------------|---------|-----|------------------------------|--------------------|---------------------------------------------------------------------------------------------------|
| USIM1_DET  | 42      | DI  | (U)SIM1 card hot-plug detect | 1.8 V              | If unused, keep it open.                                                                          |
| USIM1_VDD  | 43      | PO  | (U)SIM1 card power supply    | 1.8/3.0 V          | Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module. |
| USIM1_RST  | 44      | DO  | (U)SIM1 card reset           |                    |                                                                                                   |
| USIM1_DATA | 45      | DIO | (U)SIM1 card data            |                    |                                                                                                   |
| USIM1_CLK  | 46      | DO  | (U)SIM1 card clock           |                    |                                                                                                   |
| USIM1_GND  | 47      | -   | Specified ground for (U)SIM1 |                    |                                                                                                   |
| USIM2_DET  | 83      | DI  | (U)SIM2 card hot-plug detect | 1.8 V              | If unused, keep it open.                                                                          |
| USIM2_CLK  | 84      | DO  | (U)SIM2 card clock           | 1.8/3.0 V          |                                                                                                   |
| USIM2_RST  | 85      | DO  | (U)SIM2 card reset           |                    |                                                                                                   |
| USIM2_DATA | 86      | DIO | (U)SIM2 card data            |                    |                                                                                                   |
| USIM2_VDD  | 87      | PO  | (U)SIM2 card power supply    |                    | Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module. |

**Main UART**

| Pin Name | Pin No. | I/O | Description                   | DC Characteristics | Comment                    |
|----------|---------|-----|-------------------------------|--------------------|----------------------------|
| MAIN_DTR | 30      | DI  | Main UART data terminal ready | 1.8 V              | If unused, keep them open. |
| MAIN_RXD | 34      | DI  | Main UART receive             |                    |                            |
| MAIN_TXD | 35      | DO  | Main UART transmit            |                    |                            |

|          |    |    |                                   |  |                                                |
|----------|----|----|-----------------------------------|--|------------------------------------------------|
| MAIN_CTS | 36 | DO | DTE clear to send signal from DCE |  | Connect to DTE's CTS. If unused, keep it open. |
| MAIN_RTS | 37 | DI | DTE request to send signal to DCE |  | Connect to DTE's RTS. If unused, keep it open. |
| MAIN_DCD | 38 | DO | Main UART data carrier detect     |  | If unused, keep them open.                     |
| MAIN_RI  | 39 | DO | Main UART ring indication         |  |                                                |

**Debug UART**

| Pin Name | Pin No. | I/O | Description         | DC Characteristics | Comment                       |
|----------|---------|-----|---------------------|--------------------|-------------------------------|
| DBG_RXD  | 22      | DI  | Debug UART receive  | 1.8 V              | Test points must be reserved. |
| DBG_TXD  | 23      | DO  | Debug UART transmit |                    |                               |

**I2C Interfaces**

| Pin Name | Pin No. | I/O | Description      | DC Characteristics | Comment                                                                    |
|----------|---------|-----|------------------|--------------------|----------------------------------------------------------------------------|
| I2C_SCL  | 40      | OD  | I2C serial clock |                    | An external 1.8 V pull-up resistor is required. If unused, keep them open. |
| I2C_SDA  | 41      | OD  | I2C serial data  |                    |                                                                            |

**PCM Interfaces**

| Pin Name | Pin No. | I/O | Description         | DC Characteristics | Comment                    |
|----------|---------|-----|---------------------|--------------------|----------------------------|
| PCM_CLK  | 4       | DO  | PCM clock           | 1.8 V              | If unused, keep them open. |
| PCM_SYNC | 5       | DO  | PCM data frame sync |                    |                            |
| PCM_DIN  | 6       | DI  | PCM data input      |                    |                            |
| PCM_DOUT | 7       | DO  | PCM data output     |                    |                            |

**Antenna Interface**

| Pin Name | Pin No. | I/O | Description            | DC Characteristics | Comment                |
|----------|---------|-----|------------------------|--------------------|------------------------|
| ANT_MAIN | 60      | AIO | Main antenna interface |                    | 50 $\Omega$ impedance. |
| ANT_MAIN | 57      | AIO | WIFI antenna interface |                    | 50 $\Omega$ impedance. |

**ADC Interfaces**

| Pin Name         | Pin No. | I/O | Description                                   | DC Characteristics            | Comment                                                                          |
|------------------|---------|-----|-----------------------------------------------|-------------------------------|----------------------------------------------------------------------------------|
| ADC0             | 24      | AI  | General-purpose ADC interface                 | Voltage range:<br>0 V–VBAT_BB | If unused, keep them open.                                                       |
| ADC1             | 2       | AI  | General-purpose ADC interface                 |                               |                                                                                  |
| Other Interfaces |         |     |                                               |                               |                                                                                  |
| Pin Name         | Pin No. | I/O | Description                                   | DC Characteristics            | Comment                                                                          |
| USB_BOOT         | 75      | DI  | Force the module into emergency download mode | 1.8 V                         | Active high.<br>It is recommended to reserve a test point.                       |
| W_DISABLE#       | 18      | DI  | Airplane mode control                         |                               | Pull-up by default.<br>In low voltage level, the module can enter airplane mode. |
| WAKEUP_IN*       | 96      | DI  | Wake up the module                            |                               | If unused, keep them open.                                                       |
| AP_READY*        | 19      | DI  | Application processor ready                   |                               |                                                                                  |
| GRFC             | 76      | DO  | Generic RF control                            |                               | If unused, keep it open.                                                         |
|                  |         |     |                                               |                               |                                                                                  |

---

open.

**Reserved Pins**

| Pin Name | Pin No.                                                                         | Comment         |
|----------|---------------------------------------------------------------------------------|-----------------|
| RESERVED | 11–14, 16, 25–28, 49, 51, 56, 63–66, 77, 78, 88, 92–95, 97–99, 103–118, 123–125 | Keep them open. |

## 2.6. EVB Kit

To help you develop applications with the module, Ucloudlink supplies an evaluation board (UMTS&LTEEVB) with accessories to control or test the module. For more details, see **document [1]**.

## 3 Operating Characteristics

### 3.1. Operating Modes

Table 7: Overview of Operating Modes

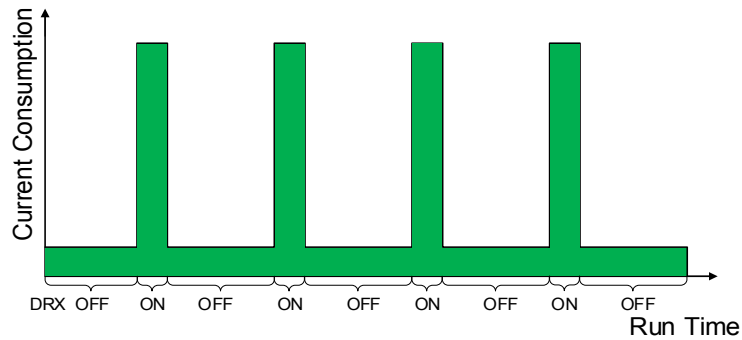
| Mode                       | Details                                                                                                                                                   |                                                                                                                |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|
| Full Functionality Mode    | Idle                                                                                                                                                      | Software is active. The module is registered on the network and ready to send and receive data.                |
|                            | Voice/Data                                                                                                                                                | Network connection is ongoing. Power consumption is decided by the network setting and data transmission rate. |
| Minimum Functionality Mode | <b>AT+CFUN=0</b> can set the module to a minimum functionality mode when the power is on. In this case, both RF function and (U)SIM card will be invalid. |                                                                                                                |
| Airplane Mode              | <b>AT+CFUN=4</b> or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.                                        |                                                                                                                |
| Sleep Mode                 | Power consumption of the module will be reduced to the minimal level. The module can still receive paging, SMS, voice call and TCP/UDP data from network. |                                                                                                                |
| Power Down Mode            | PMIC shuts down the power supply. Software is not active. However, operating voltage connected to VBAT_BB/RF remains applied.                             |                                                                                                                |

#### NOTE

For more details about AT command, see **document [2]**.

### 3.2. \*Sleep Mode

\*With DRX technology, power consumption of the module will be reduced to a minimal level.



\*Figure 3: DRX Run Time and Current Consumption in Sleep Mode

#### NOTE

\*DRX cycle values are transmitted over the wireless network.

The following section describes ways to let the module enter sleep mode.

### 3.2.1. UART Application Scenario

If the module communicates with the host via UART interface, both the following two preconditions should be met to set the module into sleep mode:

- Execute **AT+QSClk=1**.
- Ensure the MAIN\_DTR is held high or is kept disconnected.

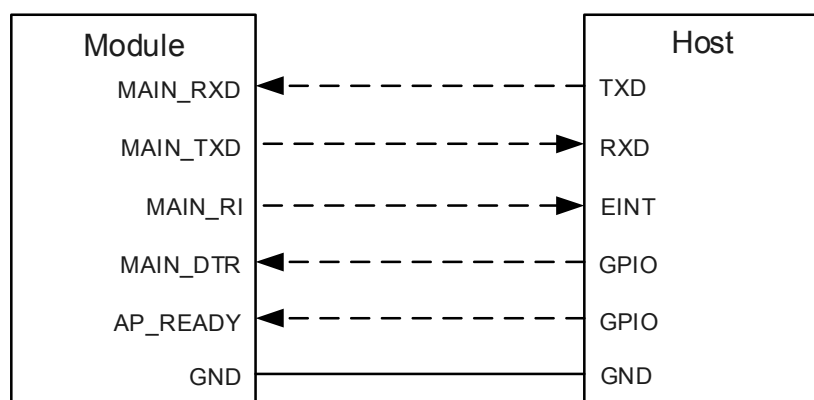


Figure 4: Sleep Mode Application via UART

- Driving the MAIN\_DTR low with the host will wake up the module.
- When the module has a URC to report, MAIN\_RI signal will wake up the host. See **Chapter 4.8.3** for details about MAIN\_RI.

### 3.2.2. USB Application Scenario

For the two situations (USB application with USB suspend/resume and USB remote wakeup function and USB application with USB suspend/resume and RI function) below, three preconditions must be met to set the module into sleep mode:

- Execute **AT+QSCLK=1**.
- Ensure the MAIN\_DTR is held high or is kept disconnected.
- Ensure the host's USB bus, which is connected to the module's USB interface, enters suspend state.

#### 3.2.2.1. USB Application with USB Suspend/Resume and USB Remote Wakeup Function

The host supports USB suspend/resume and remote wakeup function.

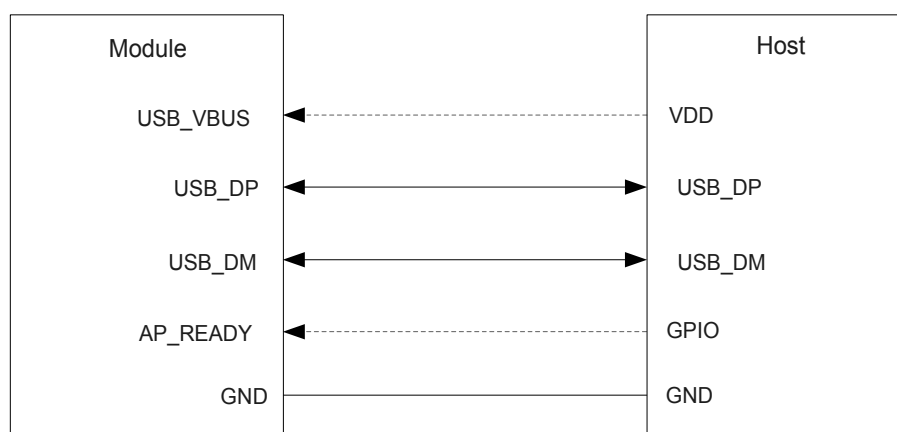


**Figure 5: Sleep Mode Application with USB Remote Wakeup**

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will send remote wake-up signals to USB bus to wake up the host.

#### 3.2.2.2. USB Application with USB Suspend/Resume and RI Function

If the host supports USB suspend/resume, but does not support remote wakeup function, the MAIN\_RI signal is needed to wake up the host.

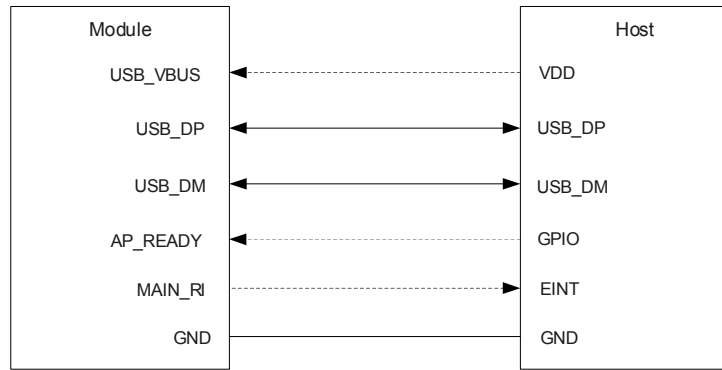


Figure 6: Sleep Mode Application with MAIN\_RI

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will wake up the host through MAIN\_RI signal. See **Chapter 4.8.3** for details about MAIN\_RI.

### 3.2.2.3. USB Application without USB Suspend Function

If the host does not support USB suspend function, disconnect USB\_VBUS with an external control circuit to set the module enter sleep mode. The following three preconditions must be met to set the module into sleep mode:

- Execute **AT+QSCLK=1**.
- Ensure the MAIN\_DTR is held high or kept disconnected.
- Disconnected the USB\_VBUS power supply.

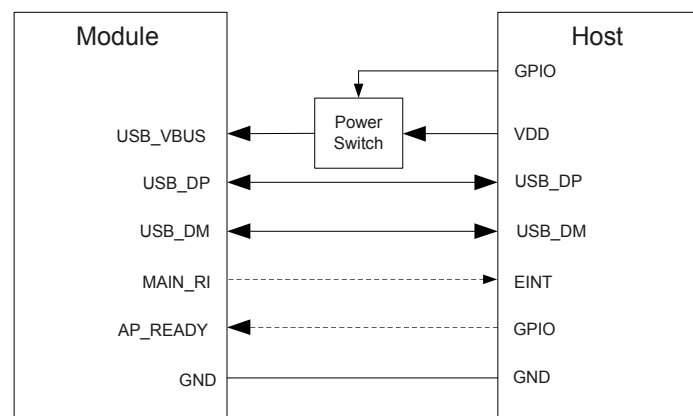


Figure 7: Sleep Mode Application without Suspend Function

Turn on the power switch and supply power to USB\_VBUS will wake up the module.

**NOTE**

1. Pay attention to the level match shown in dotted line between the module and the host in the circuit diagrams of **Chapter 3.2**.
2. For more information about the AT command, see **document [2]** for details.

### 3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

**Hardware:**

The W\_DISABLE# pin is pulled up by default. Its control function for airplane mode is disabled by default and **AT+QCFG="airplanecontrol",1** can be used to enable the function. Driving it low will set the module enter airplane mode.

**Software:**

**AT+CFUN=<fun>** provides choices of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0**: Minimum functionality (disable RF function and (U)SIM function).
- **AT+CFUN=1**: Full functionality (default).
- **AT+CFUN=4**: Airplane mode (disable RF function).

**NOTE**

For more information about the AT command, see **document [2]** for details.

### 3.4. Power Supply

#### 3.4.1. Power Supply Pins

The module provides four VBAT pins dedicated to the connection with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT\_RF pins for RF part.
- Two VBAT\_BB pins for baseband part.

Table 8: Pin Definition of Power Supply

| Pin Name | Pin No. | I/O | Description                                 | Comment                                                                                                                            |
|----------|---------|-----|---------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------|
| VBAT_BB  | 32, 33  | PI  | Power supply for the module's baseband part | External power supply must be provided with sufficient current of at least 0.8 A. It is recommended to add a TVS diode externally. |
| VBAT_RF  | 52, 53  | PI  | Power supply for the module's RF part       | External power supply must be provided with sufficient current of at least 2.2 A. It is recommended to add a TVS diode externally. |

### 3.4.2. Reference Design for Power Supply

Power design for the module is essential. The power supply of the module should be able to provide sufficient current of at least 3 A. If the voltage difference between input voltage and output voltage is small, it is suggested to use an LDO. If the voltage difference is big, a buck converter is suggested to use.

The following figure illustrates a reference design for +5 V input power supply.

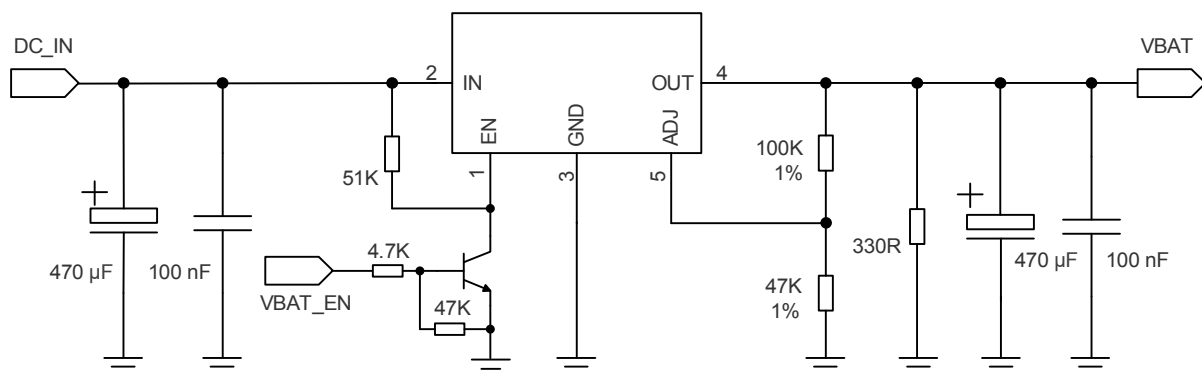


Figure 8: Reference Design of Power Supply

### 3.4.3. Requirements for Voltage Stability

The power supply range of the module is from 3.4 V to 4.3 V. Ensure the input voltage will never drop below 3.4 V.

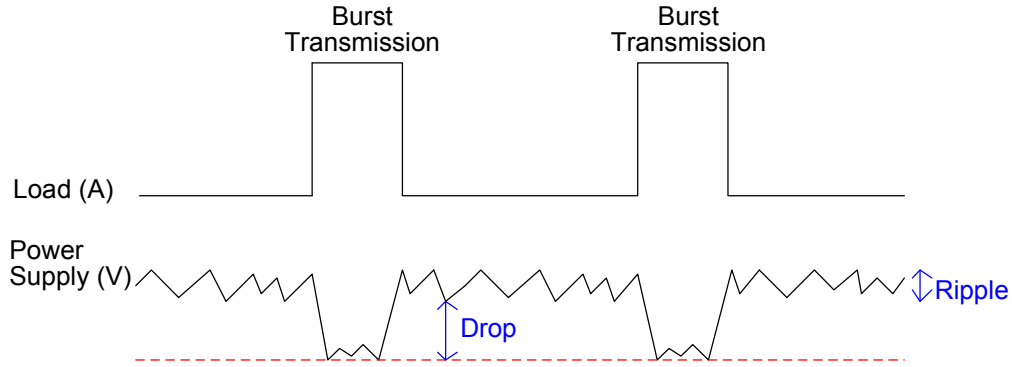


**Figure 9: Power Supply Limits during Burst Transmission**

To decrease voltage's drop, a bypass capacitor of about 100  $\mu\text{F}$  with low ESR ( $\text{ESR} \leq 0.7 \Omega$ ) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved with its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application must be a single voltage source and can be expanded to two sub paths with the star configuration. The width of VBAT\_BB trace should be not less than 1 mm. The width of VBAT\_RF trace should be not less than 2 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, to ensure the stability of the power supply, it is necessary to add a high-power TVS diode at the front end of the power supply. Reference circuit is shown as below:

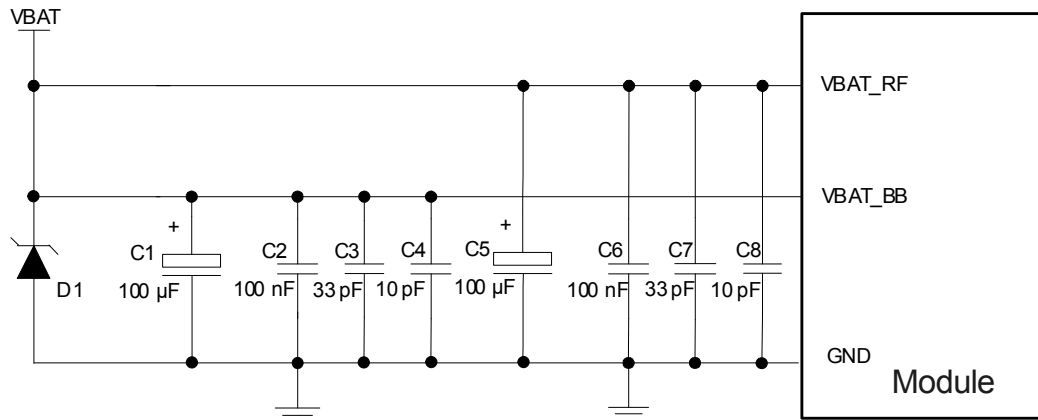


**Figure 10: Star Configuration of the Power Supply**

## 3.5. Turn On

### 3.5.1. Turn On with PWRKEY

Table 9: Pin Definition of PWRKEY

| Pin Name | Pin No. | I/O | Description            | Comment            |
|----------|---------|-----|------------------------|--------------------|
| PWRKEY   | 15      | DI  | Turn on/off the module | VBAT power domain. |

When the module is in power down mode, it can be turned on and enter normal operation mode by driving the PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY.

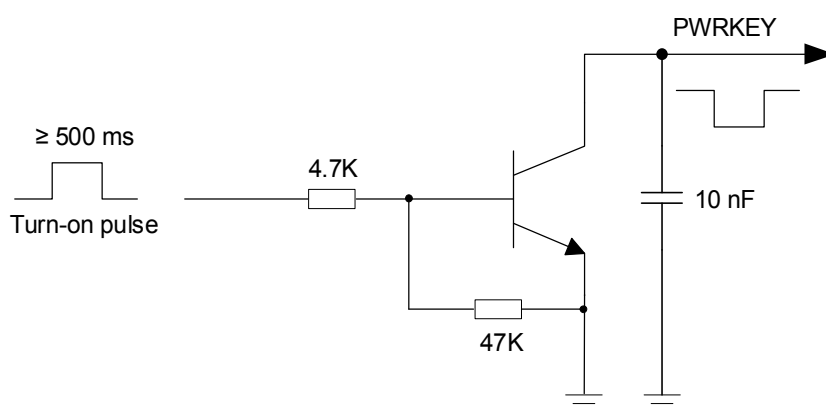


Figure 11: Reference Design of Turning on with Driving Circuit

Another way to control the PWRKEY is by using a button directly. When pressing the button, an electrostatic strike may be generated from finger. Therefore, a TVS diode shall be placed near the button for ESD protection.

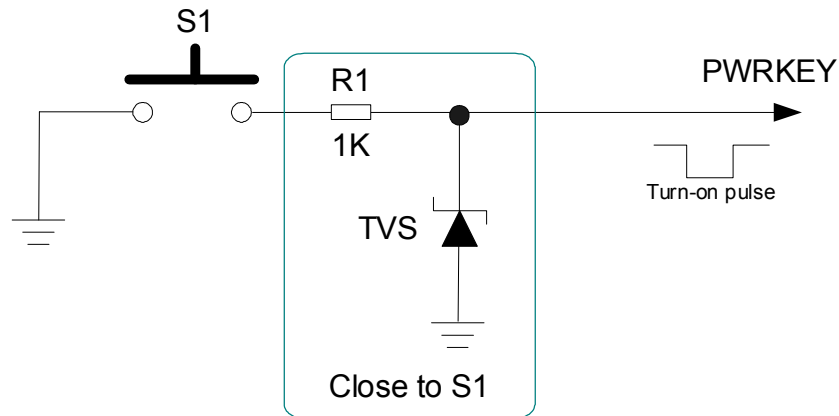


Figure 12: Reference Design of Turning on with a Button

The turn-on scenario is illustrated in the following figure.

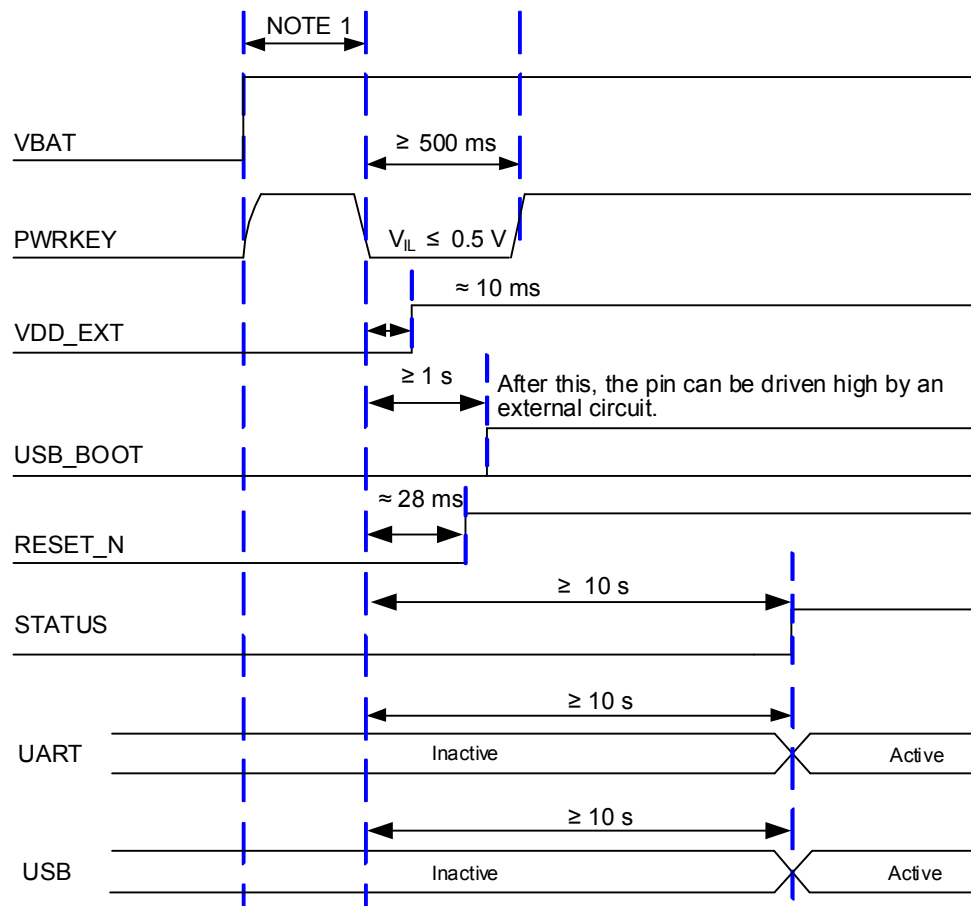


Figure 13: Timing Sequence of Turning on with PWRKEY

**NOTE**

1. Ensure the voltage of VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. If the module needs to turn on automatically but does not need turn off function, PWRKEY can be driven low directly to ground with a recommended 4.7 kΩ resistor.

### 3.6. Turn Off

#### 3.6.1. Turn Off with PWRKEY

Driving PWRKEY low for at least 650 ms, then the module will execute turn-off procedure after the PWRKEY is released.

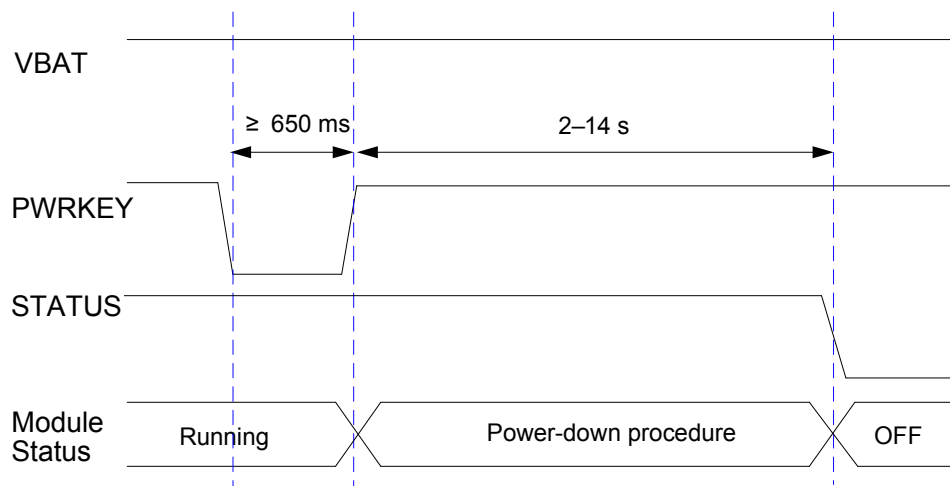


Figure 14: Timing Sequence of Turning off with PWRKEY

#### 3.6.2. Turn Off with AT Command

For proper shutdown procedure, execute **AT+QPOWD**, which has similar timing and effect as turning off the module through driving PWRKEY low. See [document \[2\]](#) for details about **AT+QPOWD**.

**NOTE**

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.
2. When turning off the module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on automatically again after successful turn-off.

### 3.7. Reset

Drive RESET\_N low for at least 300 ms and then release it can reset the module. RESET\_N signal is sensitive to interference, consequently it is recommended to route the trace as short as possible and surround it with ground.

**Table 10: Pin Definition of RESET**

| Pin Name | Pin No. | I/O | Description      | Comment                                                                                  |
|----------|---------|-----|------------------|------------------------------------------------------------------------------------------|
| RESET_N  | 17      | DI  | Reset the module | Active low. 1.8 V power domain.<br>A test point is recommended to be reserved if unused. |

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET\_N.

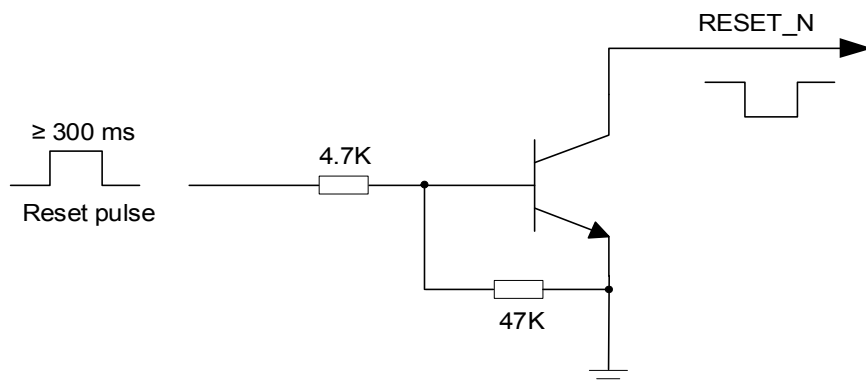


**Figure 15: Reference Design of RESET\_N with Driving Circuit**

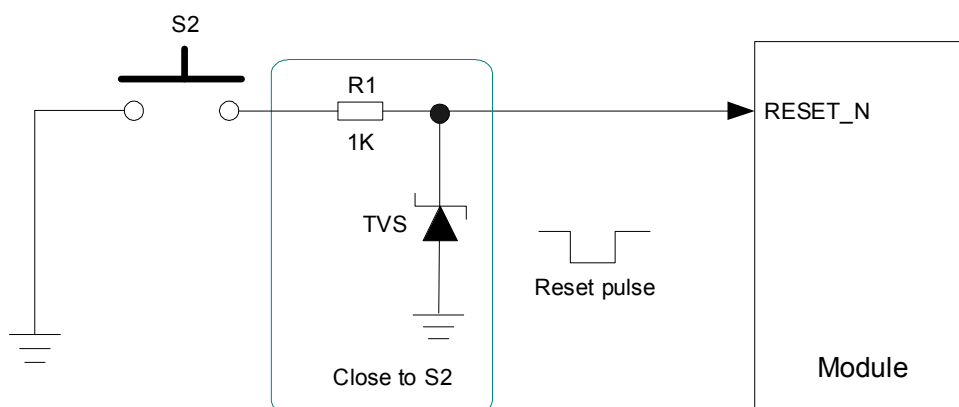


**Figure 16: Reference Design of RESET\_N with a Button**

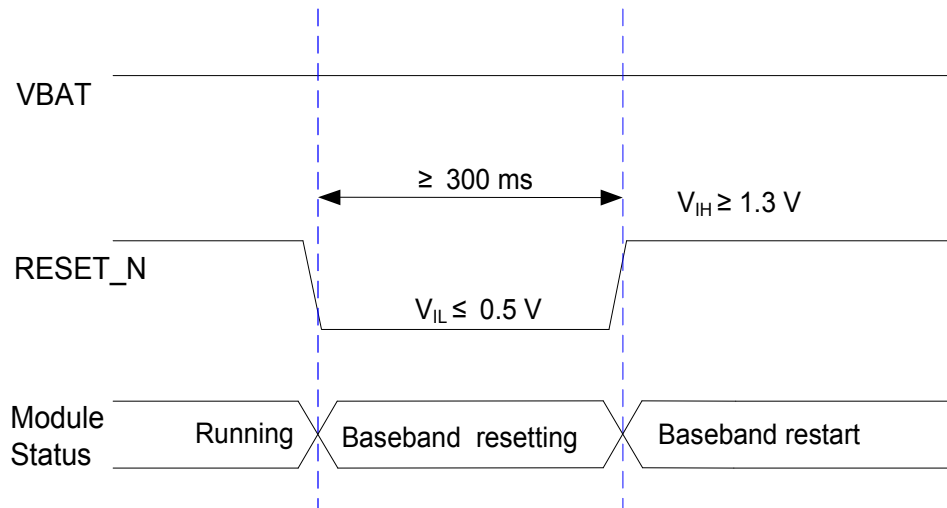


Figure 17: Timing Sequence of RESET\_N

**NOTE**

1. RESET\_N only resets the internal baseband chip of the module and does not reset the power management chip.
2. Use RESET\_N only when you fail to turn off the module with the **AT+QPOWD** and PWRKEY.
3. Ensure the capacitance on PWRKEY and RESET\_N does not exceed 10 nF.

# 4 Application Interfaces

## 4.1. USB Interface

The module provides one USB interface, which complies with USB 2.0 specifications, and supports high-Speed (480 Mbps) and full-Speed (12 Mbps) for USB 2.0. The USB interface supports data transmission, AT command communication, software debugging and firmware upgrade, and only slave mode is supported.

**Table 11: Pin Definition of USB Interface**

| Pin Name | Pin No. | I/O | Description               | Comment                                                             |
|----------|---------|-----|---------------------------|---------------------------------------------------------------------|
| USB_VBUS | 8       | AI  | USB connection detect     | Test point must be reserved.                                        |
| USB_DP   | 9       | AIO | USB differential data (+) | Requires differential impedance of 90 $\Omega$ . USB 2.0 compliant. |
| USB_DM   | 10      | AIO | USB differential data (-) |                                                                     |
|          |         |     |                           | Test points must be reserved.                                       |

Test points must be reserved for software debugging and firmware upgrading in your designs.

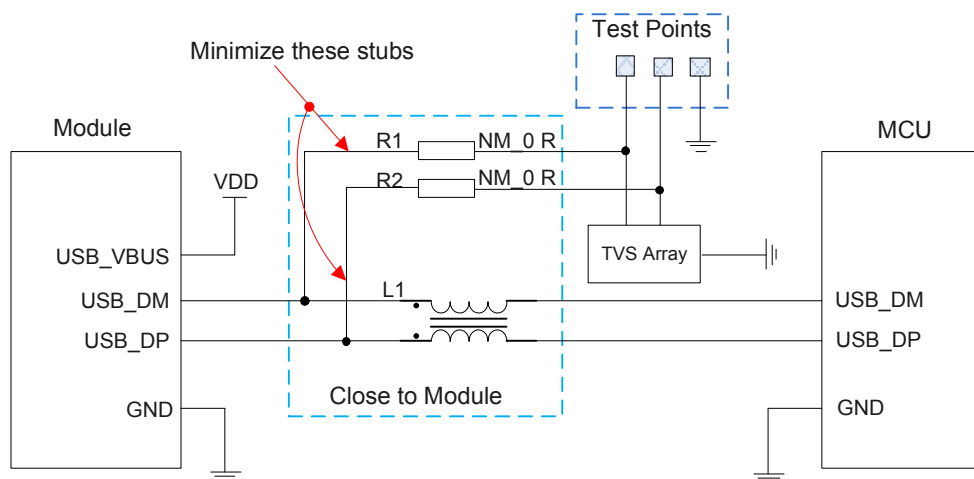


**Figure 18: Reference Design of USB Application**

A common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission. Meanwhile, the 0  $\Omega$  resistors (R1 and R2) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data line signal, L1, R1 and R2 components must be placed close to the module, and also resistors R1 and R2 should be placed close to each other. The extra stubs of trace must be kept as short as possible.

To ensure performance, you should follow the following principles when designing USB interface:

- The impedance of USB differential trace is 90  $\Omega$ . Route USB differential traces in the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below.
- Do not route signal traces under VBAT traces, crystal-oscillators, magnetic devices, sensitive circuits and provide clearance from RF signals, analog signals, and noise signals generated by clock, DC-DC, etc.
- Pay attention to the selection of the ESD protection component on the USB data line. Its parasitic capacitance should not exceed 2 pF and should be placed as close as possible to the USB interface.

For more details about the USB specifications, visit <http://www.usb.org/home>.

## 4.2. USB\_BOOT

The module provides a USB\_BOOT pin. You can pull up USB\_BOOT to 1.8 V or short-circuit VDD\_EXT and USB\_BOOT before turning on the module, the module will enter emergency download mode when turned on. In this mode, the module supports firmware upgrade over USB 2.0 interface.

**Table 12: Pin Definition of USB\_BOOT**

| Pin Name | Pin No. | I/O | Description                                   | Comment                                                                     |
|----------|---------|-----|-----------------------------------------------|-----------------------------------------------------------------------------|
| USB_BOOT | 75      | DI  | Force the module into emergency download mode | 1.8 V power domain. Active high. It is recommended to reserve a test point. |

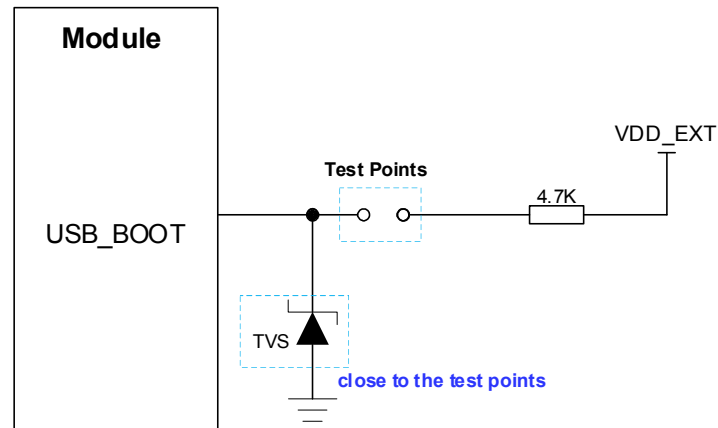


Figure 19: Reference Design of USB\_BOOT

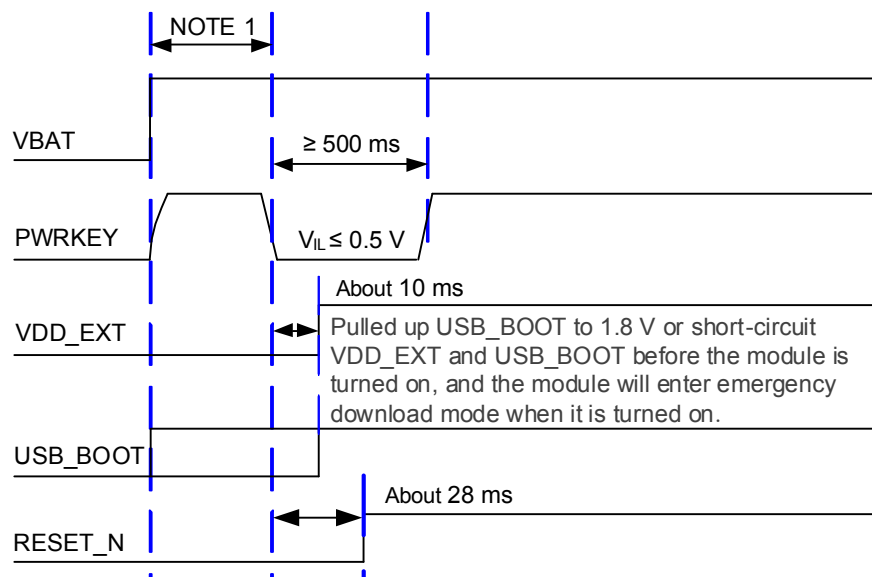


Figure 20: Timing Sequence for Entering Emergency Download Mode

**NOTE**

1. Ensure VBAT is stable before driving PWRKEY low. The time period between powering VBAT up and driving PWRKEY low should be at least 30 ms.
2. When using MCU to control module to enter the emergency download mode, follow the above timing sequence. It is not recommended to pull up USB\_BOOT to 1.8 V before powering up VBAT. Connect the test points as shown in **Figure 19** can manually force the module to enter emergency download mode.

### 4.3. (U)SIM Interfaces

The circuitry of (U)SIM interfaces meet ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V (U)SIM card is supported.

**Table 13: Pin Definition of (U)SIM Interface**

| Pin Name   | Pin No. | I/O | Description                  | Comment                                                                                           |
|------------|---------|-----|------------------------------|---------------------------------------------------------------------------------------------------|
| USIM1_DET  | 42      | DI  | (U)SIM1 card hot-plug detect | 1.8 V power domain. If unused, keep it open.                                                      |
| USIM1_VDD  | 43      | PO  | (U)SIM1 card power supply    | Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module. |
| USIM1_RST  | 44      | DO  | (U)SIM1 card reset           |                                                                                                   |
| USIM1_DATA | 45      | DIO | (U)SIM1 card data            |                                                                                                   |
| USIM1_CLK  | 46      | DO  | (U)SIM1 card clock           |                                                                                                   |
| USIM1_GND  | 47      | -   | Specified ground for (U)SIM1 |                                                                                                   |
| USIM2_DET  | 83      | DI  | (U)SIM2 card hot-plug detect | 1.8 V power domain. If unused, keep it open.                                                      |
| USIM2_CLK  | 84      | DO  | (U)SIM2 card clock           |                                                                                                   |
| USIM2_RST  | 85      | DO  | (U)SIM2 card reset           |                                                                                                   |
| USIM2_DATA | 86      | DIO | (U)SIM2 card data            |                                                                                                   |
| USIM2_VDD  | 87      | PO  | (U)SIM2 card power supply    | Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module. |

The module supports (U)SIM card hot-plug via the USIM\_DET pin, and both high- and low-level detections are supported. The function is disabled by default, and it can be configured via **AT+QSIMDET**. For more details, see **document [2]**.

The following figure illustrates a reference design for (U)SIM card interface with an 8-pin (U)SIM card connector.

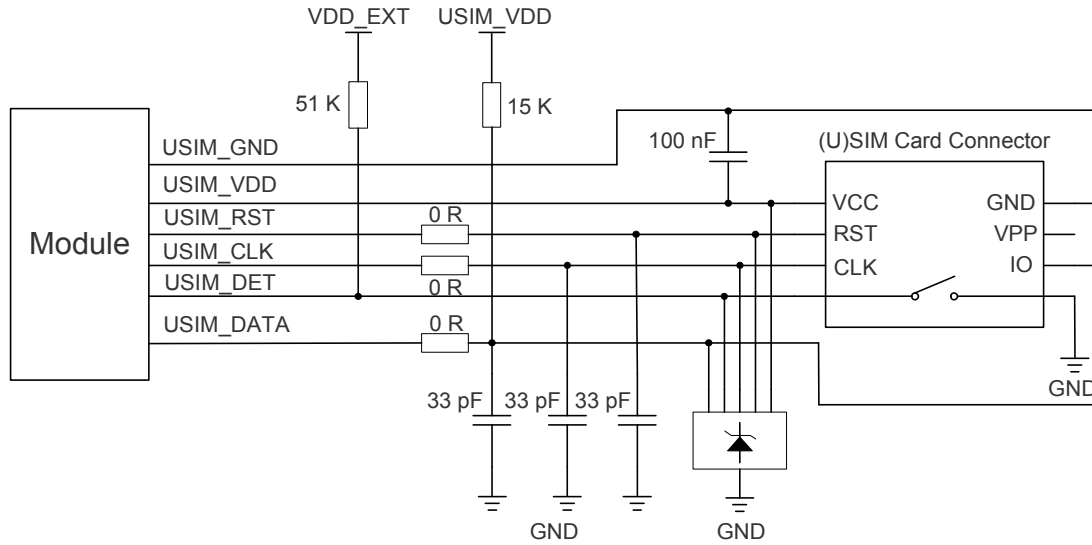


**Figure 21: Reference Design of (U)SIM Interface with an 8-Pin (U)SIM Card Connector**

If (U)SIM card hot-plug detection function is not needed, keep USIM\_DET disconnected.

A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

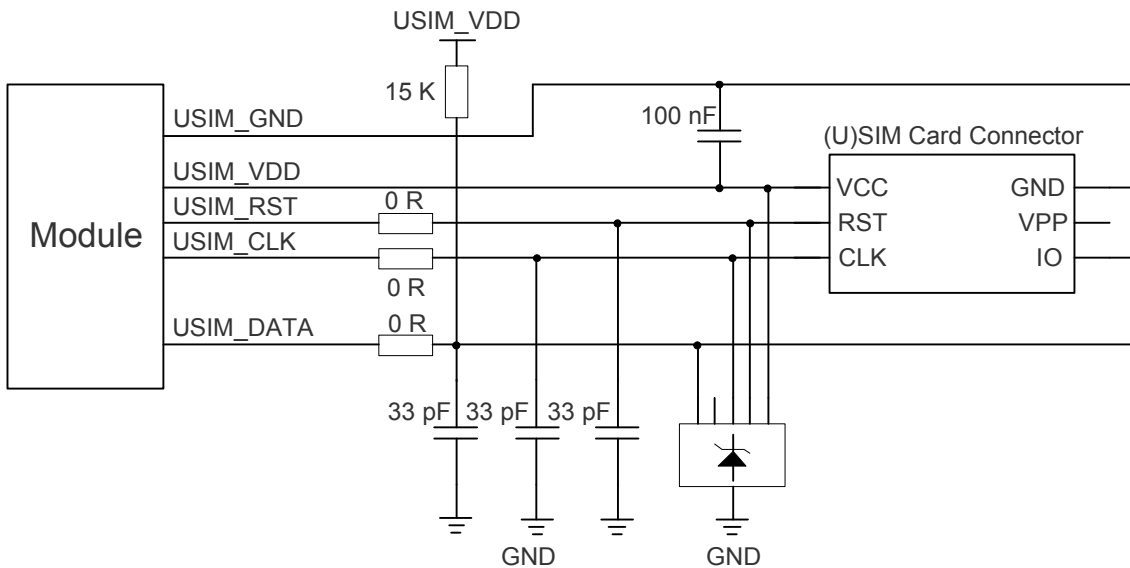


**Figure 22: Reference Design of (U)SIM Interface with a 6-Pin (U)SIM Card Connector**

To enhance the reliability and availability of the (U)SIM card in applications, follow the principles below in the (U)SIM circuit design:

- Place the (U)SIM card connector close to the module. Keep the trace length less than 200 mm if possible. Keep (U)SIM card signals away from RF and VBAT traces.
- Ensure the bypass capacitor between USIM\_VDD and GND is less than 1  $\mu$ F, and place it as close to the (U)SIM card connector as possible.
- Ensure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM\_VDD not less than 0.5 mm to maintain the same electric potential. If the ground is complete on your PCB, USIM\_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM\_DATA and USIM\_CLK, keep them away from each other and shield them with surrounded ground.
- To offer good ESD protection, it is recommended to add a TVS diode array of which parasitic capacitance should be less than 15 pF. The 0  $\Omega$  resistors should be added in series between the module and the (U)SIM card to facilitate debugging. Note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The 33 pF capacitors in parallel on USIM\_DATA, USIM\_CLK and USIM\_RST lines are used for filtering RF interference.
- The pull-up resistor on USIM\_DATA line can improve anti-jamming capability when long layout trace and sensitive occasions are applied, and should be placed close to the (U)SIM card connector.

## 4.4. UART Interfaces

The module provides three UART and the following shows their features:

**Table 14: UART Information**

| UART Type  | Supported Baud Rates (bps)                                             | Default Baud Rates (bps) | Function                                       |
|------------|------------------------------------------------------------------------|--------------------------|------------------------------------------------|
| Main UART  | 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 and 1M | 115200                   | Data transmission and AT command communication |
| Debug UART | 115200                                                                 | 115200                   | Log output                                     |

Pin definition of the UART is as follows:

**Table 15: Pin Definition of UART**

| Pin Name | Pin No. | I/O | Description                       | Comment                                                                  |
|----------|---------|-----|-----------------------------------|--------------------------------------------------------------------------|
| MAIN_DTR | 30      | DI  | Main UART data terminal ready     |                                                                          |
| MAIN_RXD | 34      | DI  | Main UART receive                 | 1.8 V power domain.<br>If unused, keep them open.                        |
| MAIN_TXD | 35      | DO  | Main UART transmit                |                                                                          |
| MAIN_CTS | 36      | DO  | DTE clear to send signal from DCE | 1.8 V power domain.<br>Connect to DTE's CTS.<br>If unused, keep it open. |
| MAIN_RTS | 37      | DI  | DTE request to send signal to DCE | 1.8 V power domain.<br>Connect to DTE's RTS.<br>If unused, keep it open. |
| MAIN_DCD | 38      | DO  | Main UART data carrier detect     | 1.8 V power domain.<br>If unused, keep them open.                        |
| MAIN_RI  | 39      | DO  | Main UART ring indication         |                                                                          |
| DBG_RXD  | 22      | DI  | Debug UART receive                | 1.8 V power domain.<br>Test points must be reserved.                     |
| DBG_TXD  | 23      | DO  | Debug UART transmit               |                                                                          |

The module provides 1.8 V UART interfaces. A voltage-level translator should be used between the module and host's UART if the application is equipped with a 3.3 V UART interface. A voltage-level translator TXS0108EPWR provided by *Texas Instruments* is recommended.

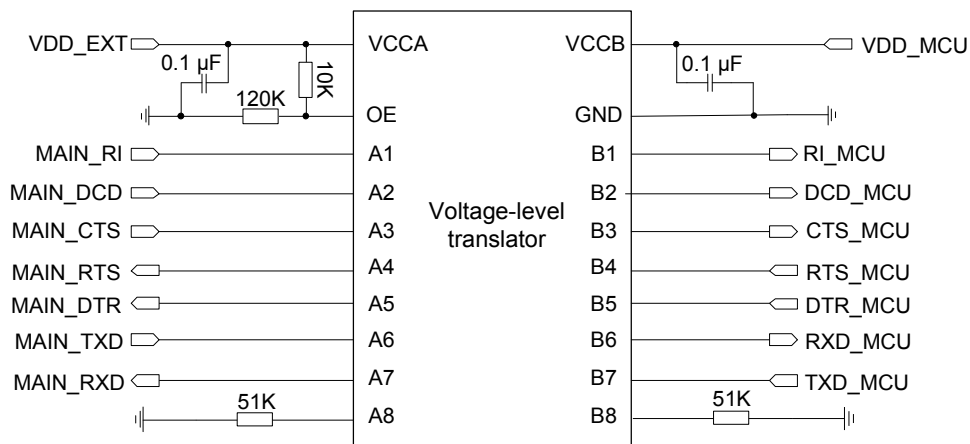


**Figure 23: Reference Design with a Voltage-level Translator**

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

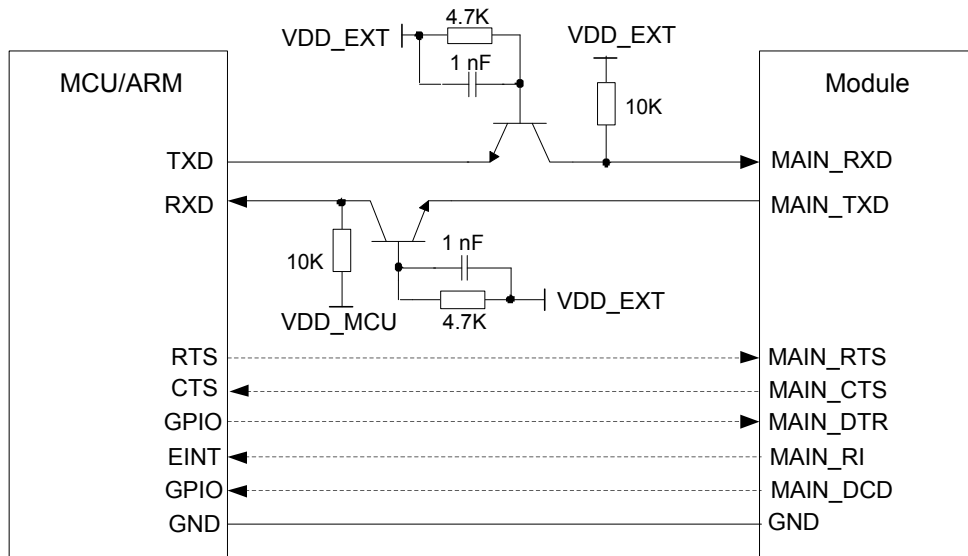


Figure 24: Reference Design with Transistor Circuit

#### NOTE

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS.

## 4.5. PCM and I2C Interfaces

The module provides one Pulse Code Modulation (PCM) digital interface and one I2C interface.

Table 16: Pin Definition of PCM Interface

| Pin Name | Pin No. | I/O | Description         | Comment                                           |
|----------|---------|-----|---------------------|---------------------------------------------------|
| PCM_CLK  | 4       | DO  | PCM clock           |                                                   |
| PCM_SYNC | 5       | DO  | PCM data frame sync | 1.8 V power domain.<br>If unused, keep them open. |
| PCM_DIN  | 6       | DI  | PCM data input      |                                                   |
| PCM_DOUT | 7       | DO  | PCM data output     |                                                   |

**Table 17: Pin Definition of I2C Interface**

| Pin Name | Pin No. | I/O | Description      | Comment                                         |
|----------|---------|-----|------------------|-------------------------------------------------|
| I2C_SCL  | 40      | OD  | I2C serial clock | An external 1.8 V pull-up resistor is required. |
| I2C_SDA  | 41      | OD  | I2C serial data  | If unused, keep them open.                      |

PCM interface supports short frame mode, and module can only be used as a master device.

The module supports 16-bit linear data format. The following figure is the short frame mode timing diagram (PCM\_SYNC = 8 kHz, PCM\_CLK = 2048 kHz).

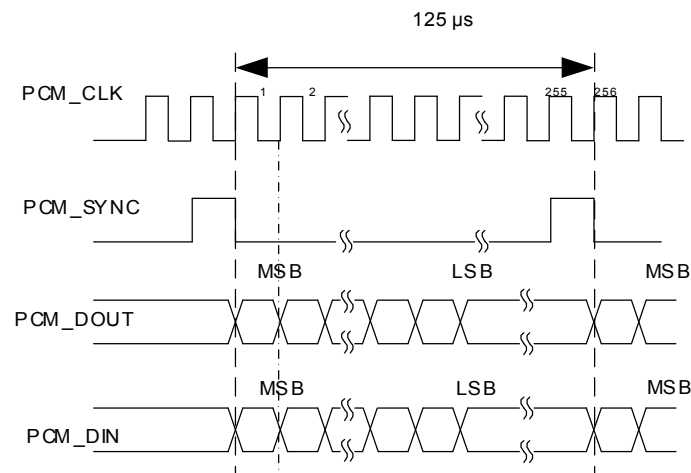


**Figure 25: Timing Sequence of Short Frame Mode**

In short frame mode, data is sampled on the falling edge of PCM\_CLK and transmitted on the rising edge. The PCM\_SYNC falling edge represents the MSB. In this mode, PCM\_CLK supports 256 kHz, 512 kHz, 1024 kHz and 2048 kHz when PCM\_SYNC operates at 8 kHz, and also supports 4096 kHz when PCM\_SYNC operates at 16 kHz.

The default configuration is short frame mode, PCM\_CLK = 2048 kHz, PCM\_SYNC = 8 kHz.

The following figure shows a reference design of I2C and PCM interfaces with an external codec IC.

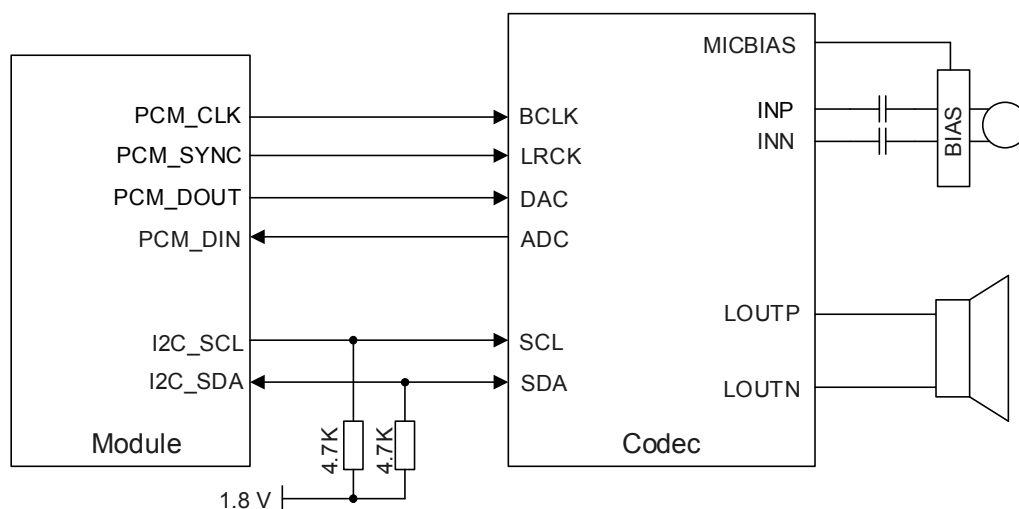


**Figure 26: Reference Design of PCM and I2C Application with Audio Codec**

#### NOTE

1. It is recommended to reserve an RC ( $R = 0 \Omega$ ,  $C = 33 \text{ pF}$ ) circuit on the PCM lines, especially for PCM\_CLK.
2. The module can only be used as a master device in applications related to PCM and I2C interfaces.

## 4.7. ADC Interfaces

The module provides two Analog-to-Digital Converter (ADC) interfaces. To improve the accuracy of ADC, the trace of ADC interfaces should be surrounded by ground.

Table 19: Pin Definition of ADC Interface

| Pin Name | Pin No. | I/O | Description                   | Comment                    |
|----------|---------|-----|-------------------------------|----------------------------|
| ADC0     | 24      | AI  | General-purpose ADC interface | If unused, keep them open. |
| ADC1     | 2       | AI  |                               |                            |

The voltage value on ADC pins can be read via **AT+QADC=<port>**:

- **AT+QADC=0**: read the voltage value on ADC0
- **AT+QADC=1**: read the voltage value on ADC1

For more details about the AT command, see *document [2]*.

Table 20: Characteristics of ADC Interface

| Name               | Min. | Typ. | Max.    | Unit |
|--------------------|------|------|---------|------|
| ADC0 Voltage Range | 0    | -    | VBAT_BB | V    |
| ADC1 Voltage Range | 0    | -    | VBAT_BB | V    |
| ADC Resolution     | -    | 12   | -       | bits |

**NOTE**

1. The input voltage of every ADC interface should not exceed its voltage range.
2. It is prohibited to directly supply any voltage to ADC interface when the module is not powered by the VBAT.
3. If the collected voltage is greater than VBAT\_BB, it is recommended to use a resistor divider circuit input for the ADC pin. When designing it, reserve a 1 nF capacitor at both ends of the grounding divider resistor. The capacitor is not mounted by default.

## 4.8. Indication Signal

Relative interfaces' pin descriptions are as follows:

Table 21: Pin Definition of Indication Signal

| Pin Name   | Pin No. | I/O | Description                                   | Comment                                           |
|------------|---------|-----|-----------------------------------------------|---------------------------------------------------|
| NET_STATUS | 21      | DO  | Indicate the module's network activity status | 1.8 V power domain.<br>If unused, keep them open. |
| STATUS     | 20      | DO  | Indicate the module's operation status        |                                                   |
| MAIN_RI    | 39      | DO  | Main UART ring indication                     |                                                   |

### 4.8.1. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides one network indication pin: NET\_STATUS. The following tables describe pin definition and logic level changes in different network status.

Table 22: Working State of the Network Connection Status/Activity Indication

| Pin Name   | Status                                   | Description                  |
|------------|------------------------------------------|------------------------------|
| NET_STATUS | Flicker slowly (200 ms High/1800 ms Low) | Network searching            |
|            | Flicker slowly (1800 ms High/200 ms Low) | Idle                         |
|            | Flicker quickly (125 ms High/125 ms Low) | Data transmission is ongoing |
|            | Always High                              | Voice calling                |

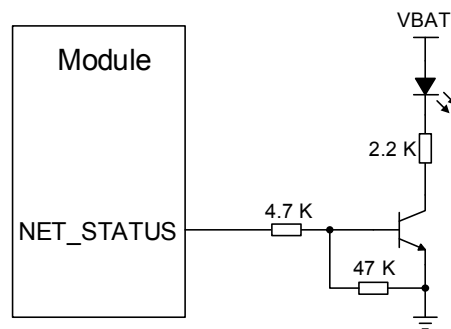


Figure 30: Reference Design of Network Status Indication

#### 4.8.2. STATUS

The STATUS pin indicates the module's operation status. It will output high level when module is turned on successfully.

A reference circuit is shown as below.

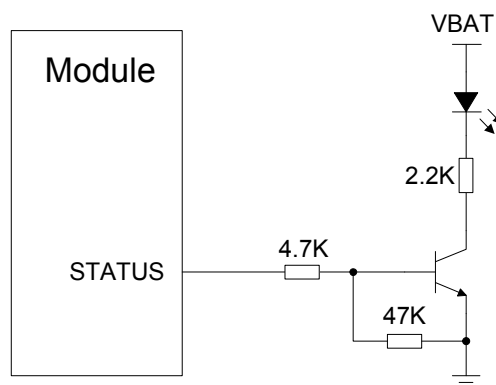


Figure 31: Reference Circuits of STATUS

### 4.8.3. MAIN\_RI

**AT+QCFG="risignalttype","physical"** can be used to configure the indication behavior for MAIN\_RI. No matter on which port (main UART, USB AT port or USB modem port) a URC information is presented, the URC information will trigger the behavior of the MAIN\_RI.

#### NOTE

The **AT+QURCCFG** allows you to set the main UART, USB AT port or USB modem port as the URC information output port. The USB AT port is the URC output port by default.

MAIN\_RI behaviors can be configured flexibly, and the default ones are shown as below:

**Table 23: Behaviors of the MAIN\_RI**

| Module Status                      | MAIN_RI Level Status                                                                                                  |
|------------------------------------|-----------------------------------------------------------------------------------------------------------------------|
| Idle                               | High                                                                                                                  |
| When a new URC information returns | MAIN_RI outputs at least 120 ms low level. After the module outputs the data, the level status will then become high. |

Indication behavior of MAIN\_RI can be configured via several commands, e.g. **AT+QCFG="urc/ri/ring"** can be used to specify the MAIN\_RI behavior when the URC indicating an incoming call is reported. See **document [2]** for details.

# 5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

## 5.1. Cellular Network/Wlan

### 5.1.1. Antenna Interface & Frequency Bands

Table 24: Pin Definition of Main Antenna Interface

| Pin Name   | Pin No. | I/O | Description            | Comment                |
|------------|---------|-----|------------------------|------------------------|
| ANT_MAIN   | 60      | AIO | Main antenna interface | 50 $\Omega$ impedance. |
| AP_WCN_ANT | 57      | AIO | Wlan antenna interface | 50 $\Omega$ impedance. |

#### NOTE

Only passive antennas are supported.

Table 25: Operating Frequency of GLMM24A01

| Operating Frequency | Transmit (MHz) | Receive (MHz) |
|---------------------|----------------|---------------|
| LTE-FDD B1          | 1920–1980      | 2110–2170     |
| LTE-FDD B2          | 1850–1910      | 1930–1990     |
| LTE-FDD B3          | 1710–1785      | 1805–1880     |
| LTE-FDD B4          | 1710–1755      | 2110–2155     |
| LTE-FDD B5          | 824–849        | 869–894       |
| LTE-FDD B7          | 2500–2570      | 2620–2690     |

|             |           |           |
|-------------|-----------|-----------|
| LTE-FDD B8  | 880–915   | 925–960   |
| LTE-FDD B12 | 699–716   | 729–746   |
| LTE-FDD B13 | 777–787   | 746–756   |
| LTE-FDD B17 | 704–716   | 734–746   |
| LTE-FDD B18 | 815–830   | 860–875   |
| LTE-FDD B19 | 830–845   | 875–890   |
| LTE-FDD B20 | 832–862   | 791–821   |
| LTE-FDD B25 | 1850–1915 | 1930–1995 |
| LTE-FDD B26 | 814–849   | 859–894   |
| LTE-FDD B28 | 703–748   | 758–803   |
| LTE-FDD B66 | 1710–1780 | 2110–2200 |
| LTE-TDD B38 | 2570–2620 | 2570–2620 |
| LTE-TDD B41 | 2496–2690 | 2496–2690 |
| WIFI        | 2412–2472 | 2412–2472 |

5.1.2. Transmitting Power  
Table 26: RF Transmitting Power

| Frequency Bands                                                                         | Max. RF Output Power | Min. RF Output Power |
|-----------------------------------------------------------------------------------------|----------------------|----------------------|
| LTE-FDD<br>B1/B2/B3/B4/B5/B7/B8/B12<br>B13/B17/B18/B19/B20/B28/B66<br>LTE-TDD<br>B38/41 | 23dBm±2.7dB          | < -39 dBm            |
| WIFI 11b/g/n                                                                            | 15dBm±3dB            |                      |

### 5.1.3. Receiver Sensitivity

The following table shows conducted RF receiver sensitivity of the module.

**Table 27: Conducted RF Receiver Sensitivity**

| Frequency            | Receiving Sensitivity (Typ.) |           |      | 3GPP Requirement (SIMO) |
|----------------------|------------------------------|-----------|------|-------------------------|
|                      | Primary                      | Diversity | SIMO |                         |
| LTE-FDD B1 (10 MHz)  | -98dBm                       | -         | -    | -96.3dBm                |
| LTE-FDD B2(10 MHz)   | -98dBm                       | -         | -    | -94.3 dBm               |
| LTE-FDD B3 (10 MHz)  | -97 dBm                      | -         | -    | -93.3 dBm               |
| LTE-FDD B4 (10 MHz)  | -97.5 dBm                    | -         | -    | -96.3 dBm               |
| LTE-FDD B5 (10 MHz)  | -97.2dBm                     | -         | -    | -94.3 dBm               |
| LTE-FDD B7 (10 MHz)  | -97 dBm                      | -         | -    | -94.3 dBm               |
| LTE-FDD B8 (10 MHz)  | -99dBm                       | -         | -    | -93.3 dBm               |
| LTE-FDD B12 (10 MHz) | -97.5 dBm                    | -         | -    | -93.3 dBm               |
| LTE-FDD B13 (10 MHz) | -98.5 dBm                    | -         | -    | -93.3 dBm               |
| LTE-FDD B17 (10MHz)  | -97.5 dBm                    | -         | -    | -93.3 dBm               |
| LTE-FDD B18 (10MHz)  | -97 dBm                      | -         | -    | -96.3 dBm               |
| LTE-FDD B19 (10 MHz) | -97.5 dBm                    | -         | -    | -96.3 dBm               |
| LTE-FDD B20 (10 MHz) | -98.5 dBm                    | -         | -    | -93.3 dBm               |
| LTE-FDD B25 (10MHz)  | -96 dBm                      | -         | -    | -93.3 dBm               |
| LTE-FDD B26 (10MHz)  | -97 dBm                      | -         | -    | -93.3 dBm               |
| LTE-FDD B28 (10 MHz) | -98 dBm                      | -         | -    | -94.3 dBm               |
| LTE-FDD B66 (10MHz)  | -97 dBm                      | -         | -    | -94.3 dBm               |
| LTE-FDD B38 (10MHz)  | -96.5dBm                     | -         | -    | -96.3 dBm               |
| LTE-FDD B41 (10MHz)  | -96.5 dBm                    | -         | -    | -94.3 dBm               |

### 5.1.4. Reference Design

The module provides one RF antenna interface for antenna connection.

It is recommended to reserve a  $\pi$ -type matching circuit for better RF performance, and the  $\pi$ -type matching components (C1, R1, and C2) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

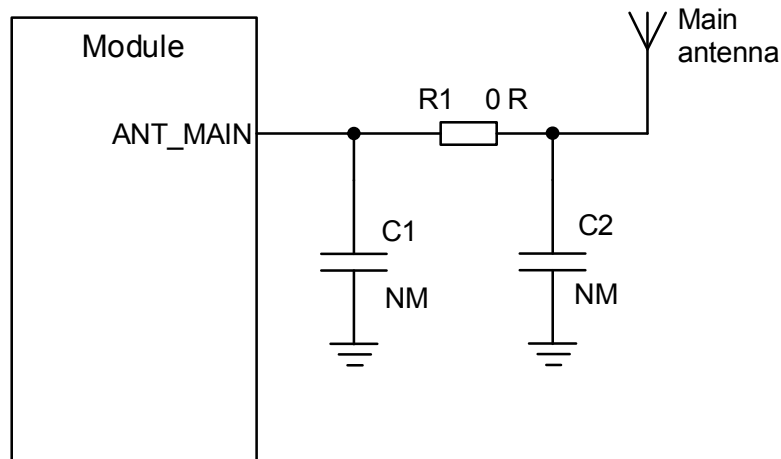


Figure 32: Reference Circuit for RF Antenna Interfaces

## 5.2. Reference Design of RF Routing

For user's PCB, the characteristic impedance of all RF traces should be controlled to  $50\ \Omega$ . The impedance of the RF traces is usually determined by the trace width ( $W$ ), the materials' dielectric constant, the height from the reference ground to the signal layer ( $H$ ), and the spacing between RF traces and grounds ( $S$ ). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

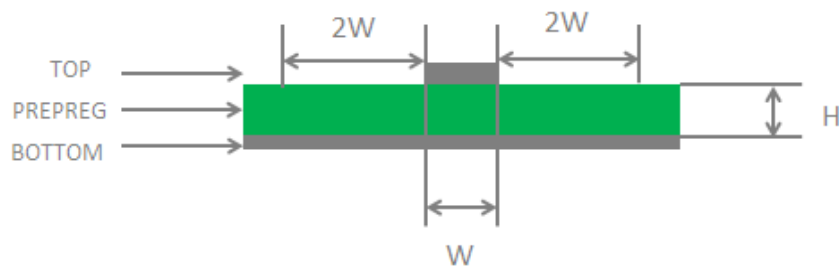


Figure 33: Microstrip Design on a 2-layer PCB

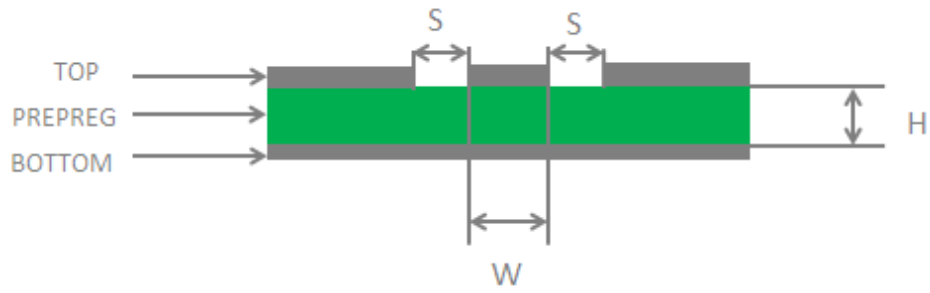


Figure 34: Coplanar Waveguide Design on a 2-layer PCB

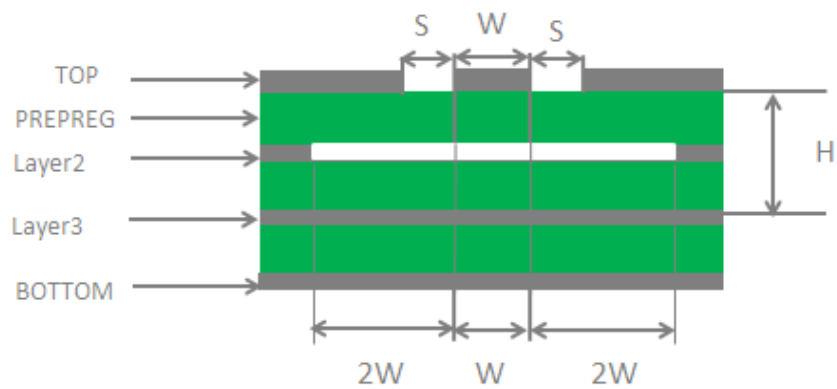


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

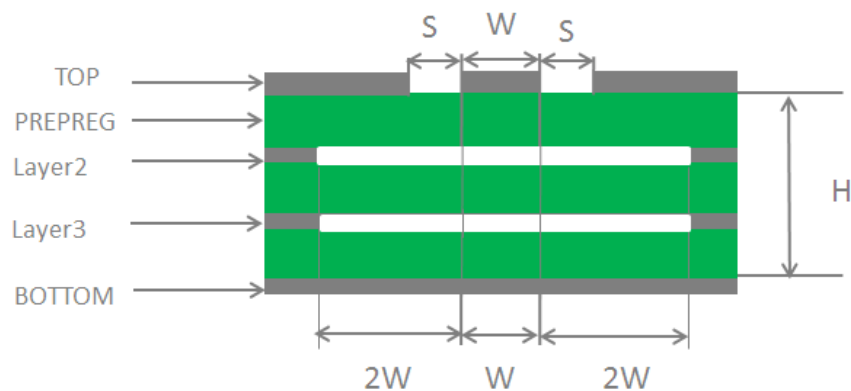


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50  $\Omega$ .
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces ( $2 \times W$ ).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see **document [4]**.

### 5.3. Requirements for Antenna Design

Table 28: Requirements for Antenna Design

| Antenna Type | Requirements                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| LTE/Wlan     | <ul style="list-style-type: none"><li>● VSWR: <math>\leq 2</math></li><li>● Efficiency: <math>&gt; 30\%</math></li><li>● Gain: 1 dBi</li><li>● Max input power: 50 W</li><li>● Input impedance: 50 <math>\Omega</math></li><li>● Polarization: Vertical</li><li>● Cable insertion loss:<ul style="list-style-type: none"><li>&lt; 1 dB: LB (<math>&lt; 1</math> GHz)</li><li>&lt; 1.5 dB: MB (1–2.3 GHz)</li><li>&lt; 2 dB: HB (<math>&gt; 2.3</math> GHz)</li></ul></li></ul> |

## 5.4. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

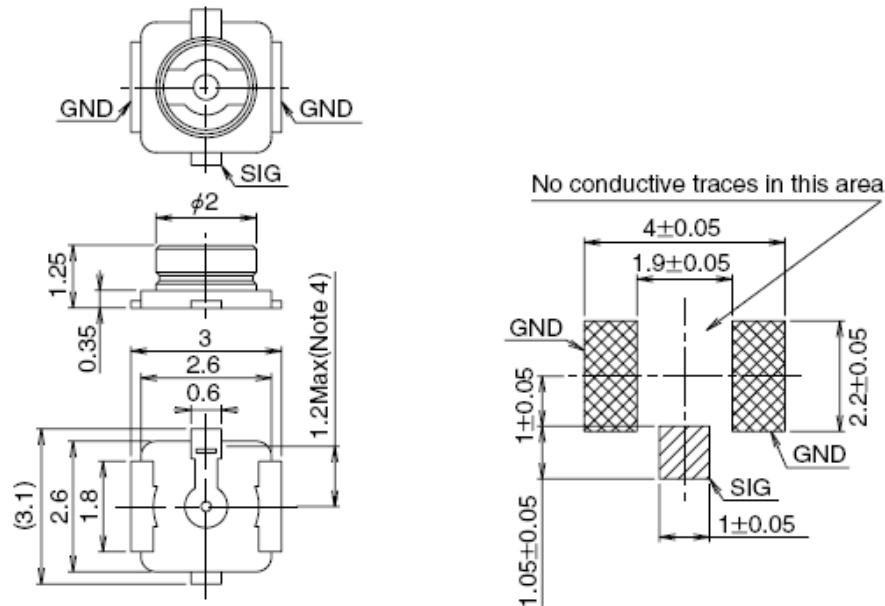


Figure 37: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

| Part No.         | U.FL-LP-040                  | U.FL-LP-066                                     | U.FL-LP(V)-040               | U.FL-LP-062                | U.FL-LP-088                  |
|------------------|------------------------------|-------------------------------------------------|------------------------------|----------------------------|------------------------------|
|                  |                              |                                                 |                              |                            |                              |
| Mated Height     | 2.5mm Max.<br>(2.4mm Nom.)   | 2.5mm Max.<br>(2.4mm Nom.)                      | 2.0mm Max.<br>(1.9mm Nom.)   | 2.4mm Max.<br>(2.3mm Nom.) | 2.4mm Max.<br>(2.3mm Nom.)   |
| Applicable cable | Dia. 0.81mm<br>Coaxial cable | Dia. 1.13mm and<br>Dia. 1.32mm<br>Coaxial cable | Dia. 0.81mm<br>Coaxial cable | Dia. 1mm<br>Coaxial cable  | Dia. 1.37mm<br>Coaxial cable |
| Weight (mg)      | 53.7                         | 59.1                                            | 34.8                         | 45.5                       | 71.7                         |
| RoHS             | YES                          |                                                 |                              |                            |                              |

Figure 38: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors.

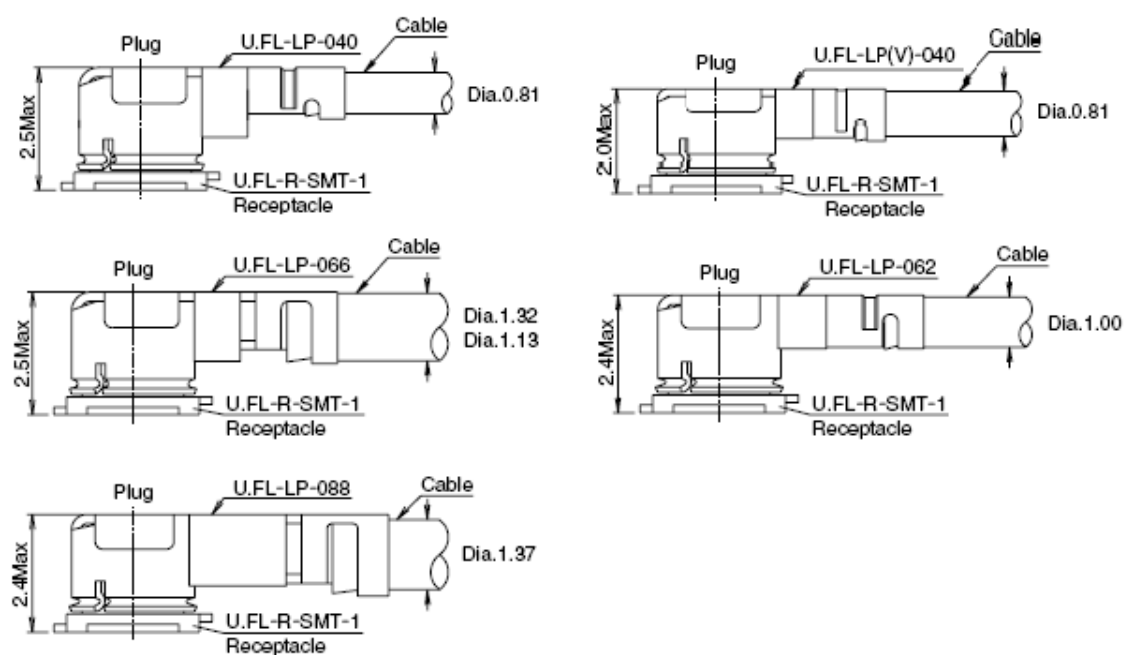


Figure 39: Space Factor of Mated Connectors (Unit: mm)

For more details, visit <http://www.hirose.com>.

# 6 Electrical Characteristics & Reliability

## 6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 29: Absolute Maximum Ratings

| Parameter               | Min. | Max. | Unit |
|-------------------------|------|------|------|
| VBAT_RF/VBAT_BB         | -0.3 | 6.0  | V    |
| USB_VBUS                | -0.3 | 5.5  | V    |
| Peak Current of VBAT_BB | -    | 0.8  | A    |
| Peak Current of VBAT_RF | -    | 2.2  | A    |
| Voltage on Digital Pins | -0.3 | 2.3  | V    |

## 6.2. Power Supply Ratings

Table 30: Power Supply Ratings

| Parameter | Description         | Conditions                                                                 | Min. | Typ. | Max. | Unit |
|-----------|---------------------|----------------------------------------------------------------------------|------|------|------|------|
| VBAT      | VBAT_BB and VBAT_RF | The actual input voltages must stay between the minimum and maximum values | 3.4  | 3.8  | 4.3  | V    |

|                   |                                        |                                |     |     |      |    |
|-------------------|----------------------------------------|--------------------------------|-----|-----|------|----|
|                   | Voltage drop during transmitting burst |                                | -   | -   | 400  | mV |
| I <sub>VBAT</sub> | Peak power consumption                 | At maximum power control level | -   | 2.0 | 2.5  | A  |
| USB_VBUS          | USB connection detection               |                                | 3.0 | 5.0 | 5.25 | V  |

### 6.3. Power Consumption

Table 31: Power Consumption

| Description | Conditions                            | Typ.  | Unit |
|-------------|---------------------------------------|-------|------|
| OFF state   | Power off                             | 29    | μA   |
| Sleep state | <b>AT+CFUN=0</b> (USB disconnected)   | 0.69  | mA   |
|             | LTE-FDD @ PF = 32 (USB disconnected)  | 1.71  | mA   |
|             | LTE-FDD @ PF = 64 (USB disconnected)  | 1.26  | mA   |
|             | LTE-FDD @ PF = 64 (USB suspend)       | 1.43  | mA   |
|             | LTE-FDD @ PF = 128 (USB disconnected) | 1.04  | mA   |
|             | LTE-FDD @ PF = 256 (USB disconnected) | 0.94  | mA   |
|             |                                       |       |      |
| Idle state  | LTE-FDD @ PF = 64 (USB disconnected)  | 20.04 | mA   |
|             | LTE-FDD @ PF = 64 (USB connected)     | 29.18 | mA   |

|                        |             |     |    |
|------------------------|-------------|-----|----|
| LTE data transmission  | LTE-FDD B1  | 456 | mA |
|                        | LTE-FDD B2  | 466 | mA |
|                        | LTE-FDD B3  | 489 | mA |
|                        | LTE-FDD B4  | 411 | mA |
|                        | LTE-FDD B5  | 401 | mA |
|                        | LTE-FDD B7  | 455 | mA |
|                        | LTE-FDD B8  | 407 | mA |
|                        | LTE-FDD B12 | 490 | mA |
|                        | LTE-FDD B13 | 486 | mA |
|                        | LTE-FDD B17 | 477 | mA |
|                        | LTE-FDD B18 | 430 | mA |
|                        | LTE-FDD B19 | 389 | mA |
|                        | LTE-FDD B20 | 405 | mA |
|                        | LTE-FDD B25 | 445 | mA |
|                        | LTE-FDD B26 | 419 | mA |
|                        | LTE-FDD B28 | 408 | mA |
|                        | LTE-FDD B66 | 412 | mA |
|                        | LTE-FDD B38 | 227 | mA |
|                        | LTE-FDD B41 | 230 | mA |
| Wlan data transmission | 11b         | 259 | mA |

## 6.4. Digital I/O Characteristic

Table 32: 1.8 V I/O Requirements

| Parameter | Description         | Min.                  | Max.                  | Unit |
|-----------|---------------------|-----------------------|-----------------------|------|
| $V_{IH}$  | Input high voltage  | $0.7 \times V_{DDIO}$ | $V_{DDIO} + 0.2$      | V    |
| $V_{IL}$  | Input low voltage   | -0.3                  | $0.3 \times V_{DDIO}$ | V    |
| $V_{OH}$  | Output high voltage | $V_{DDIO} - 0.2$      | -                     | V    |
| $V_{OL}$  | Output low voltage  | -                     | 0.2                   | V    |

Table 33: (U)SIM Low-voltage I/O Requirements

| Parameter | Description         | Min.                   | Max.                    | Unit |
|-----------|---------------------|------------------------|-------------------------|------|
| $V_{IH}$  | Input high voltage  | $0.7 \times USIM\_VDD$ | $USIM\_VDD$             | V    |
| $V_{IL}$  | Input low voltage   | 0                      | $0.2 \times USIM\_VDD$  | V    |
| $V_{OH}$  | Output high voltage | $0.7 \times USIM\_VDD$ | $USIM\_VDD$             | V    |
| $V_{OL}$  | Output low voltage  | 0                      | $0.15 \times USIM\_VDD$ | V    |

**Table 34: (U)SIM High-voltage I/O Requirements**

| Parameter       | Description         | Min.           | Max.            | Unit |
|-----------------|---------------------|----------------|-----------------|------|
| V <sub>IH</sub> | Input high voltage  | 0.7 × USIM_VDD | USIM_VDD        | V    |
| V <sub>IL</sub> | Input low voltage   | 0              | 0.15 × USIM_VDD | V    |
| V <sub>OH</sub> | Output high voltage | 0.7 × USIM_VDD | USIM_VDD        | V    |
| V <sub>OL</sub> | Output low voltage  | 0              | 0.15 × USIM_VDD | V    |

## 6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

ESD characteristics of the module's pins are as follows:

**Table 35: Electrostatics Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)**

| Tested Interfaces      | Contact Discharge | Air Discharge | Unit |
|------------------------|-------------------|---------------|------|
| VBAT, GND              | ±8                | ±12           | kV   |
| All Antenna Interfaces | ±5                | ±10           | kV   |
| Other Interfaces       | ±0.5              | ±1            | kV   |

## 6.6. Operating and Storage Temperatures

Table 36: Operating and Storage Temperatures

| Parameter                                | Min. | Typ. | Max. | Unit |
|------------------------------------------|------|------|------|------|
| Operating Temperature Range <sup>3</sup> | -35  | +25  | +75  | °C   |
| Extended Temperature Range <sup>4</sup>  | -40  | -    | +85  | °C   |
| Storage temperature range                | -40  | -    | +95  | °C   |

<sup>3</sup> Within the operating temperature range, the module meets 3GPP specifications.

<sup>4</sup> Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, emergency call, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

# 7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are  $\pm 0.2$  mm unless otherwise specified.

## 7.1. Mechanical Dimensions

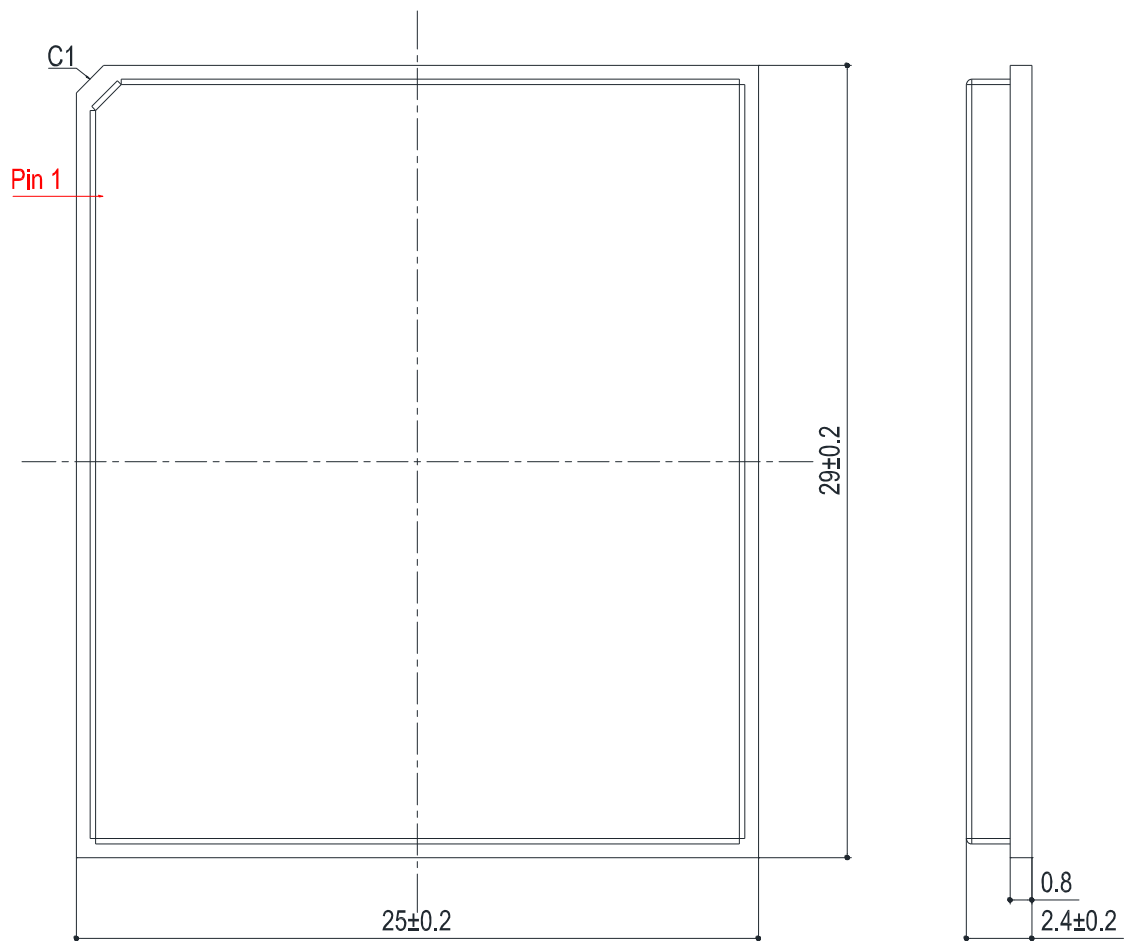


Figure 40: Module Top and Side Dimensions (Unit: mm)

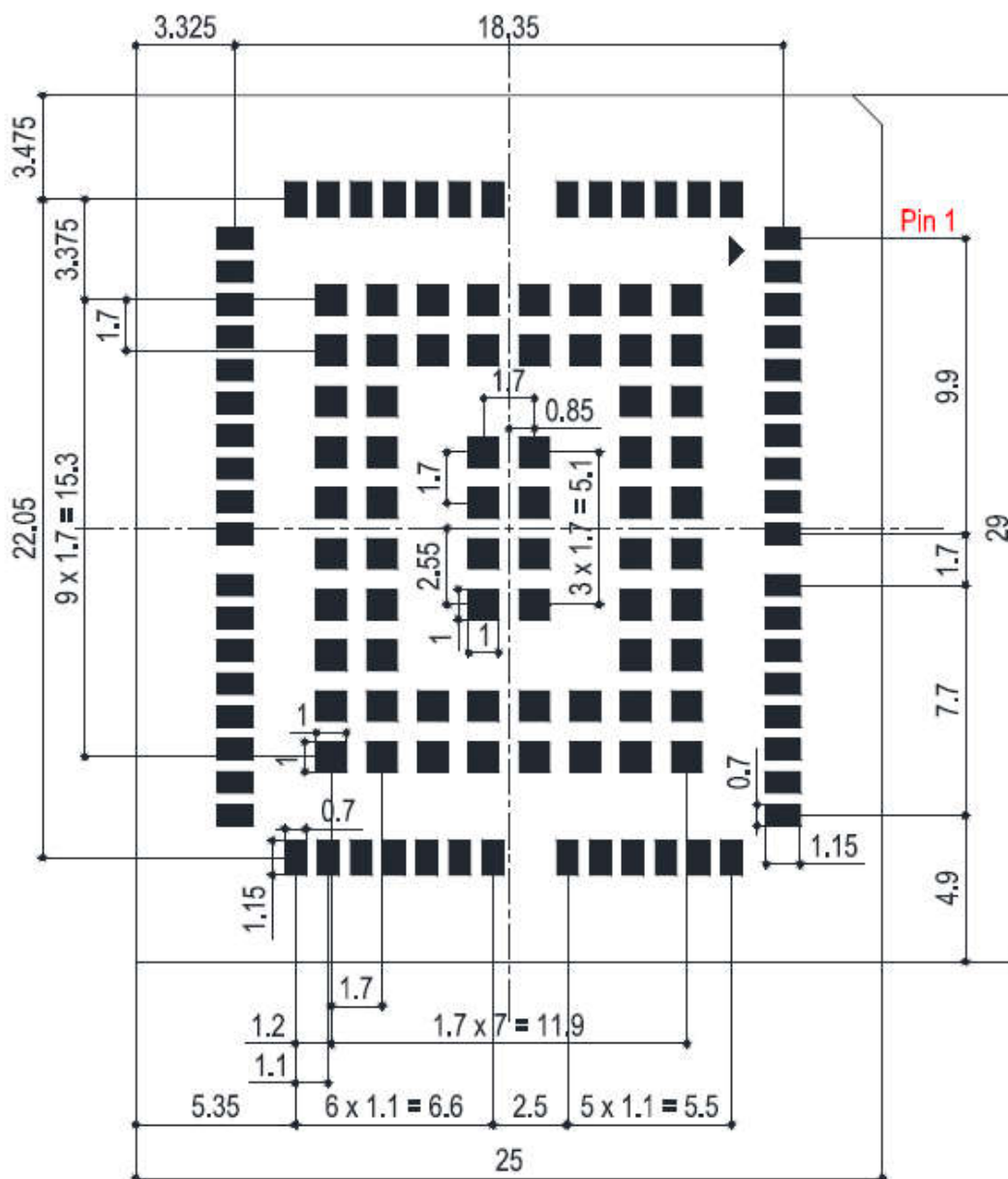
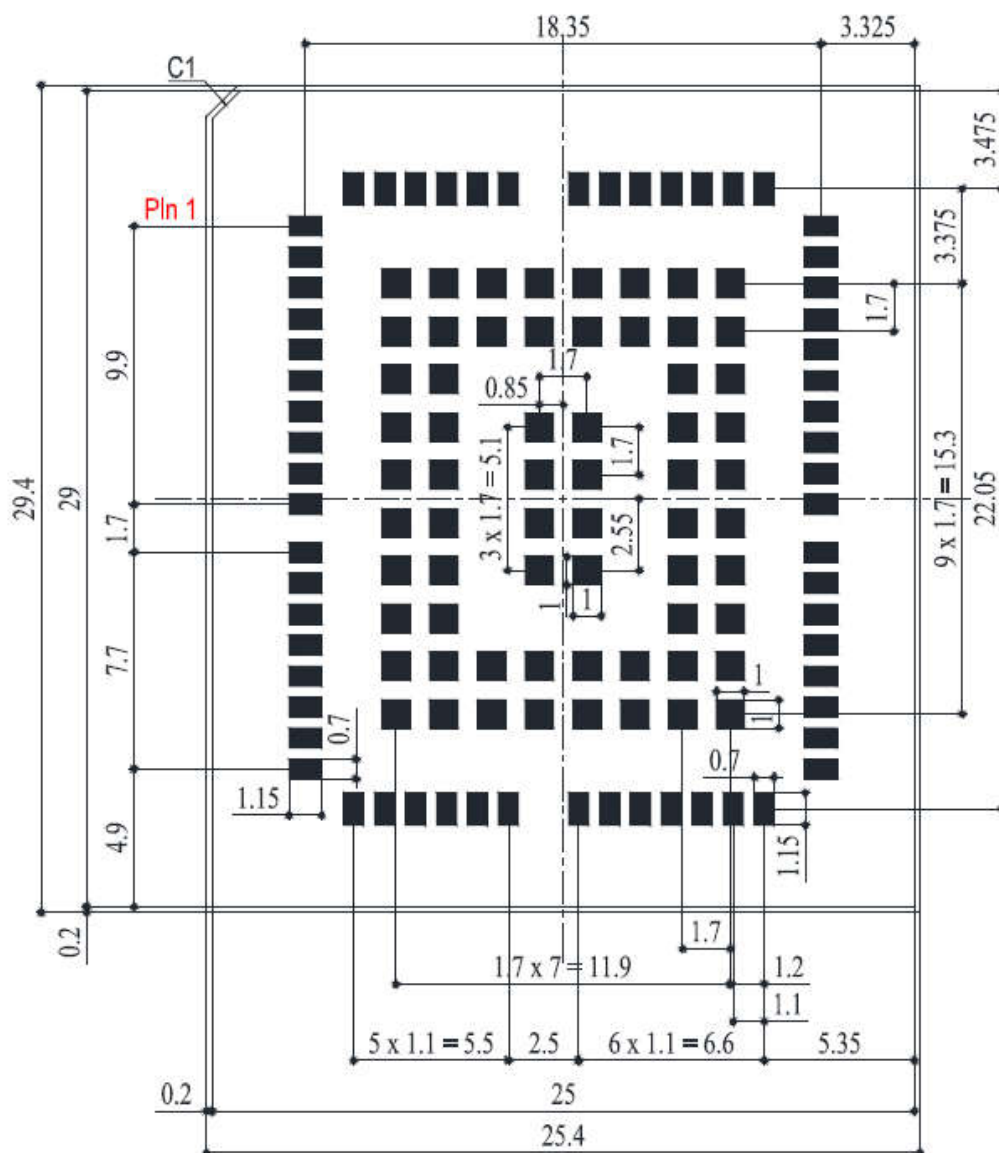


Figure 41: Module Dimensions (Bottom View)

**NOTE**

The package warpage level of the module conforms to the JEITA ED-7306 standard.

## 7.2. Recommended Footprint



Unlabeled tolerance:  $\pm 0.2\text{mm}$

### Figure 42: Recommended Footprint

## NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

### 7.3. Top and Bottom Views

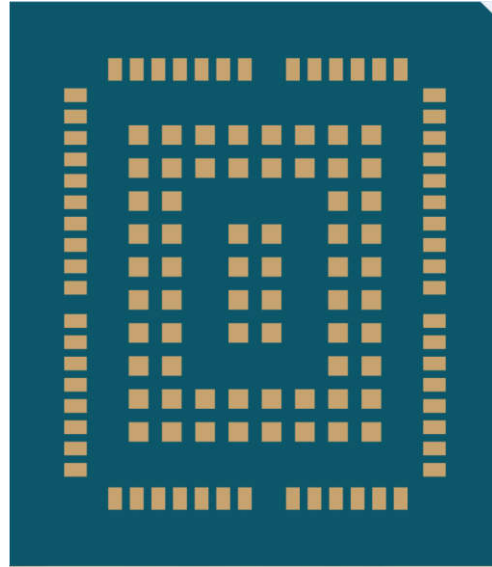


Figure 43: Top & Bottom Views of the Module

#### NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Ucloudlink.

# 8 Storage, Manufacturing & Packaging

## 8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be  $23 \pm 5$  °C and the relative humidity should be 35–60 %.
2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.
3. Floor life: 168 hours <sup>5</sup> in a factory where the temperature is  $23 \pm 5$  °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).
4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:
  - The module is not stored in Recommended Storage Condition;
  - Violation of the third requirement mentioned above;
  - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
  - Before module repairing.
5. If needed, the pre-baking should follow the requirements below:
  - The module should be baked for 8 hours at  $120 \pm 5$  °C;
  - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

---

<sup>5</sup> This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

**NOTE**

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

## 8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, please refer to **document [5]**.

The recommended peak reflow temperature should be 235–246 °C, with 246 °C as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

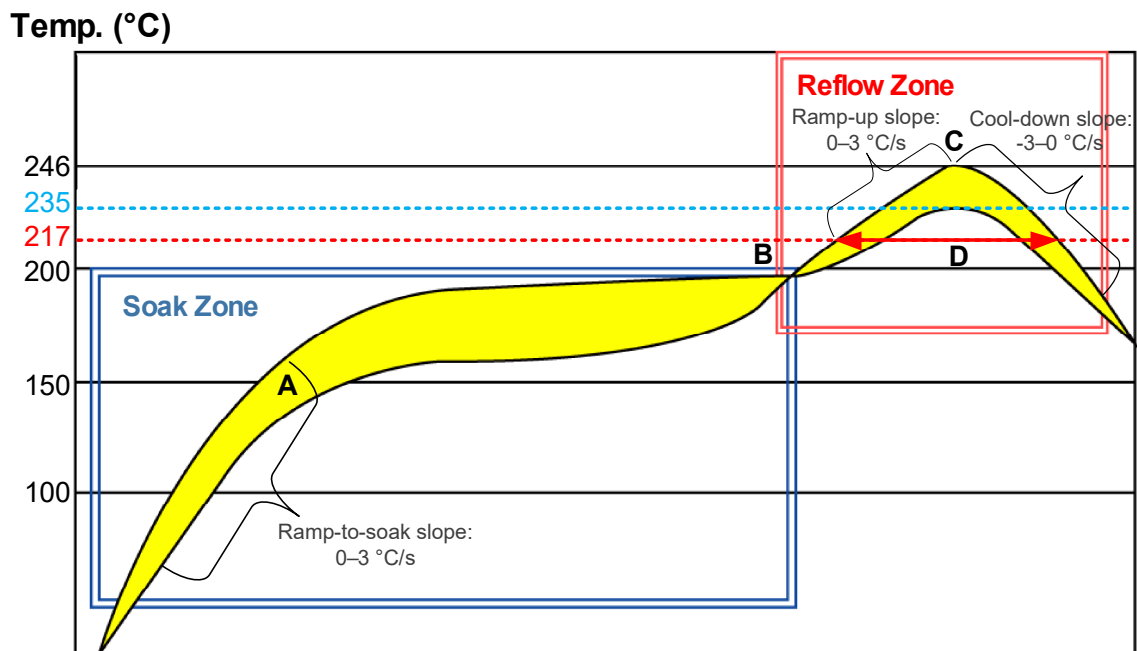


Figure 44: Recommended Reflow Soldering Thermal Profile

Table 37: Recommended Thermal Profile Parameters

| Factor                                         | Recommended Value |
|------------------------------------------------|-------------------|
| <b>Soak Zone</b>                               |                   |
| Ramp-to-soak slope                             | 0–3 °C/s          |
| Soak time (between A and B: 150 °C and 200 °C) | 70–120 s          |
| <b>Reflow Zone</b>                             |                   |
| Ramp-up slope                                  | 0–3 °C/s          |
| Reflow time (D: over 217°C)                    | 40–70 s           |
| Max temperature                                | 235–246 °C        |
| Cool-down slope                                | -3–0 °C/s         |
| <b>Reflow Cycle</b>                            |                   |
| Max reflow cycle                               | 1                 |

**NOTE**

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Due to the complexity of the SMT process, please contact Ucloudlinkl Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in **document [5]**.

### 8.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

#### 8.3.1. Carrier Tape

Dimension details are as follow:

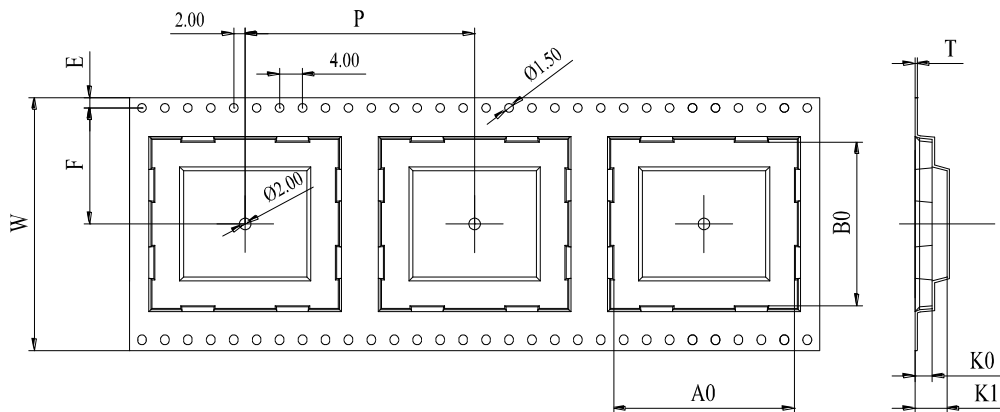


Figure 45: Carrier Tape Dimension Drawing

Table 38: Carrier Tape Dimension Table (Unit: mm)

| W  | P  | T    | A0   | B0   | K0  | K1  | F    | E    |
|----|----|------|------|------|-----|-----|------|------|
| 44 | 32 | 0.35 | 25.5 | 29.5 | 3.2 | 5.8 | 20.2 | 1.75 |

### 8.3.2. Plastic Reel

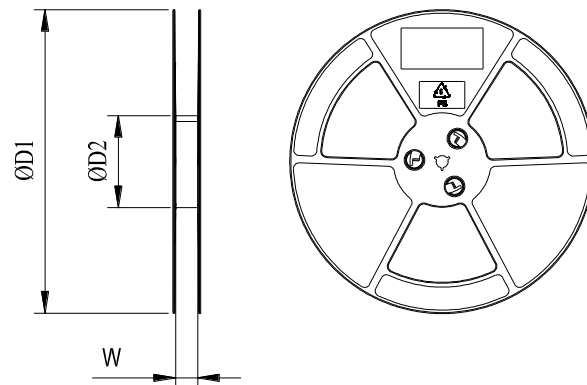


Figure 46: Plastic Reel Dimension Drawing

Table 39: Plastic Reel Dimension Table (Unit: mm)

| ØD1 | ØD2 | W    |
|-----|-----|------|
| 330 | 100 | 44.5 |

### 8.3.3. Mounting Direction

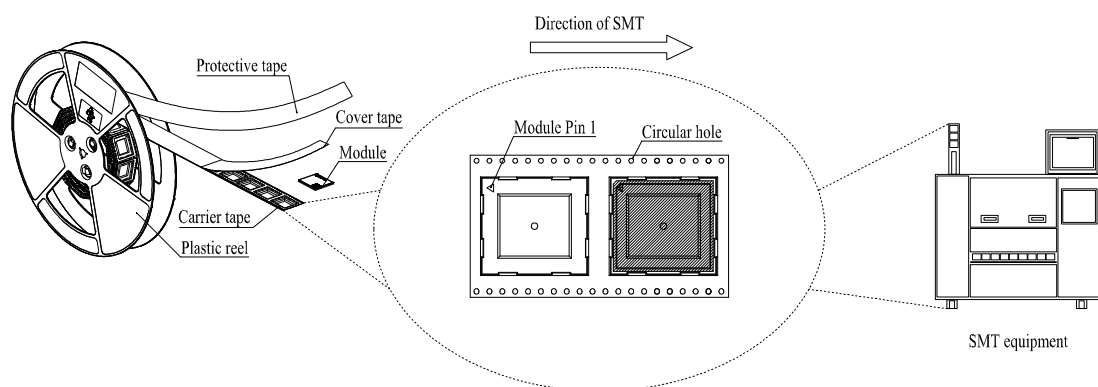
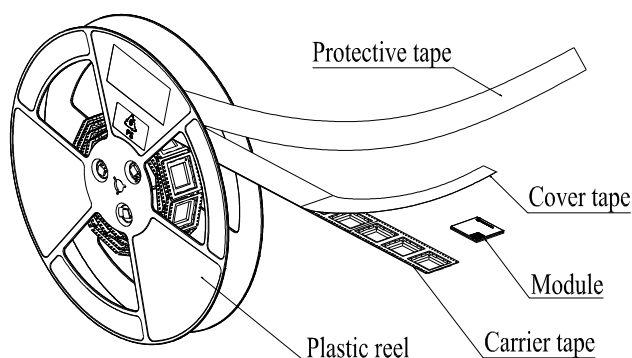


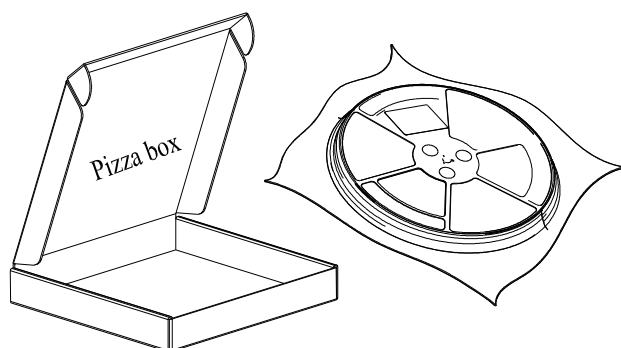
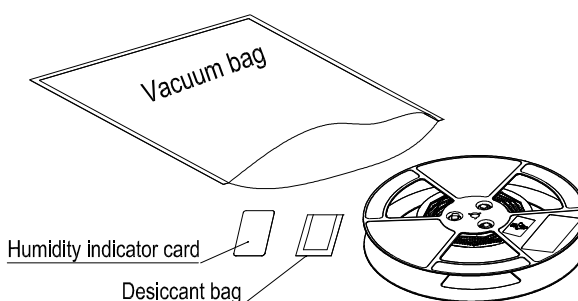
Figure 47: Mounting Direction

### 8.3.4. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.



Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 carton box and seal it. 1 carton box can pack 1000 modules.

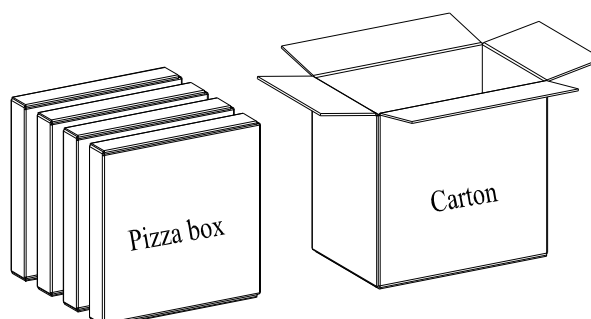


Figure 48: Packaging Process

# 9 Appendix References

**Table 40: Related Documents**

| Document Name                                                        |
|----------------------------------------------------------------------|
| [1] Ucloudlink_UMTS&<br>LTE_EVB_User_Guide                           |
| [2] Ucloudlink_EC200x&EG91xN&EG912Y&EG950A_Series_AT_Commands_Manual |
| [3] Ucloudlink_EC200x&EG91xN&EG912Y_Series_Audio_Application_Note    |
| [4] Ucloudlink_RF_Layout_Application_Note                            |
| [5] Ucloudlink_Module_SMT_Application_Note                           |

**Table 41: Terms and Abbreviations**

| Abbreviation | Description                                 |
|--------------|---------------------------------------------|
| ADC          | Analog-to-Digital Converter                 |
| AMR          | Adaptive Multi-Rate                         |
| AMR-WB       | Adaptive Multi-Rate Wideband                |
| AP           | Application Processor                       |
| bps          | Bits Per Second                             |
| CA           | Carrier Aggregation                         |
| CHAP         | Challenge Handshake Authentication Protocol |
| CMUX         | Connection MUX                              |
| CS           | Coding Scheme                               |
| CTS          | Clear To Send                               |
| DCE          | Data Communications Equipment               |

|       |                                         |
|-------|-----------------------------------------|
| DCS   | Data Coding Scheme                      |
| DFOTA | Delta Firmware Upgrade Over the Air     |
| DL    | Downlink                                |
| DRX   | Discontinuous Reception                 |
| DTE   | Data Terminal Equipment                 |
| DTR   | Data Terminal Ready                     |
| EGSM  | Enhanced GSM                            |
| EFR   | Enhanced Full Rate                      |
| ESD   | Electrostatic Discharge                 |
| ESR   | Equivalent Series Resistance            |
| EVB   | Evaluation Board                        |
| FDD   | Frequency Division Duplex               |
| FILE  | File Protocol                           |
| FR    | Full Rate                               |
| FTP   | File Transfer Protocol                  |
| FTPS  | FTP-SSL: FTP over SSL / FTP Secure      |
| GMSK  | Gaussian Minimum Shift Keying           |
| GPRS  | General Packet Radio Service            |
| GSM   | Global System for Mobile Communications |
| HB    | High Band                               |
| HR    | Half Rate                               |
| HTTP  | Hypertext Transfer Protocol             |
| HTTPS | Hypertext Transfer Protocol Secure      |
| IC    | Integrated Circuit                      |
| I2C   | Inter-Integrated Circuit                |

|      |                                                             |
|------|-------------------------------------------------------------|
| I/O  | Input/Output                                                |
| LB   | Low Band                                                    |
| LDO  | Low-dropout Regulator                                       |
| LED  | Light Emitting Diode                                        |
| LGA  | Land Grid Array                                             |
| LSB  | Least Significant Bit                                       |
| LTE  | Long Term Evolution                                         |
| MB   | Middle Band                                                 |
| MCU  | Microcontroller Unit                                        |
| MLCC | Multi-layer Ceramic Capacitor                               |
| MMS  | Multimedia Messaging Service                                |
| MO   | Mobile Originated                                           |
| MQTT | Message Queuing Telemetry Transport                         |
| MS   | Mobile Station                                              |
| MSB  | Most Significant Bit                                        |
| MT   | Mobile Terminated                                           |
| NITZ | Network Identity and Time Zone / Network Informed Time Zone |
| NTP  | Network Time Protocol                                       |
| PA   | Power Amplifier                                             |
| PAP  | Password Authentication Protocol                            |
| PC   | Personal Computer                                           |
| PCB  | Printed Circuit Board                                       |
| PCM  | Pulse Code Modulation                                       |
| PDA  | Personal Digital Assistant                                  |
| PDU  | Protocol Data Unit                                          |

|        |                                             |
|--------|---------------------------------------------|
| PING   | Packet Internet Groper                      |
| PMIC   | Power Management Integrated Circuit         |
| PPP    | Point-to-Point Protocol                     |
| RAM    | Random Access Memory                        |
| RI     | Ring Indicator                              |
| RF     | Radio Frequency                             |
| Rx     | Receive                                     |
| SIMO   | Single Input Multiple Output                |
| SMD    | Surface Mount Device                        |
| SMS    | Short Message Service                       |
| SMTP   | Simple Mail Transfer Protocol               |
| SMTPS  | Simple Mail Transfer Protocol Secure        |
| SSL    | Secure Sockets Layer                        |
| STB    | Set Top Box                                 |
| TCP    | Transmission Control Protocol               |
| TDD    | Time Division Duplexing                     |
| THD    | Total Harmonic Distortion                   |
| Tx     | Transmit                                    |
| TVS    | Transient Voltage Suppressor                |
| UART   | Universal Asynchronous Receiver/Transmitter |
| UDP    | User Datagram Protocol                      |
| UL     | Uplink                                      |
| URC    | Unsolicited Result Code                     |
| USB    | Universal Serial Bus                        |
| (U)SIM | Universal Subscriber Identity Module        |

|                  |                             |
|------------------|-----------------------------|
| V <sub>BAT</sub> | Voltage at Battery (Pin)    |
| V <sub>max</sub> | Maximum Voltage             |
| V <sub>nom</sub> | Nominal Voltage             |
| V <sub>min</sub> | Minimum Voltage             |
| V <sub>IH</sub>  | High-level Input Voltage    |
| V <sub>IL</sub>  | Low-level Input Voltage     |
| V <sub>OH</sub>  | High-level Output Voltage   |
| V <sub>OL</sub>  | Low-level Output Voltage    |
| V <sub>SWR</sub> | Voltage Standing Wave Ratio |

### **FCC Radiation Exposure Statement**

The modular can be installed or integrated in mobile or fix devices only. This modular cannot be installed in any portable device, for example, USB dongle like transmitters is forbidden.

This modular complies with FCC RF radiation exposure limits set forth for an uncontrolled environment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. This modular must be installed and operated with a minimum distance of 20 cm between the radiator and user body.

If the FCC identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following: "Contains Transmitter Module FCC ID: 2BB6E-GLMM24A01 or Contains FCC ID: 2BB6E-GLMM24A01".

When the module is installed inside another device, the user manual of this device must contain below warning statements:

1. This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference, and
- (2) This device must accept any interference received, including interference that may cause undesired operation.

2. Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. The devices must be installed and used in strict accordance with the manufacturer's instructions as described in the user documentation that comes with the product.

The host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

The end user manual shall include all required regulatory information/warning as shown in this manual, include: This product must be installed and operated with a minimum distance of 20 cm between the radiator and user body.

### **FCC Statement**

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.

- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

To assure continued compliance, any changes or modifications not expressly approved by the party.

Responsible for compliance could void the user's authority to operate this equipment. (Example- use only shielded interface cables when connecting to computer or peripheral devices).

External Antenna Info:

Manufacturer: Quectel Wireless Solutions Co., Ltd.

Antenna Type:

2.4G WIFI: Chip Antenna

LTE: FPC Antenna

Antenna Gain:

2.4G WIFI: -4.99dBi

LTE: 700–960MHz: -6.56dBi, 1710–2690MHz: 0.84dBi