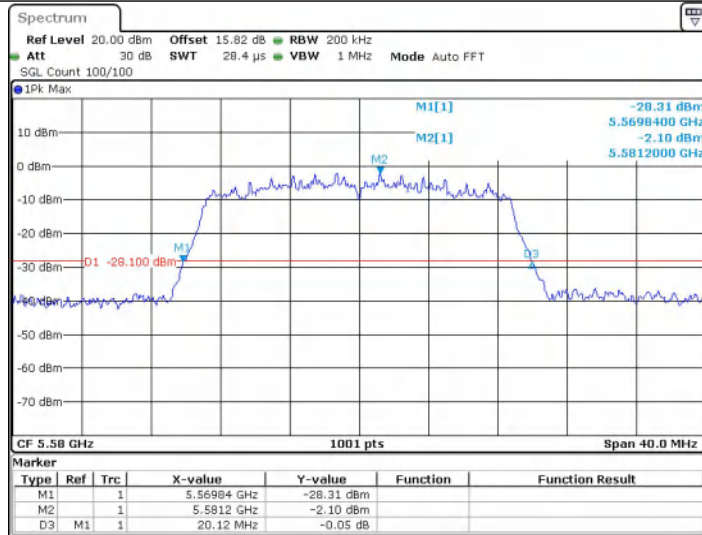
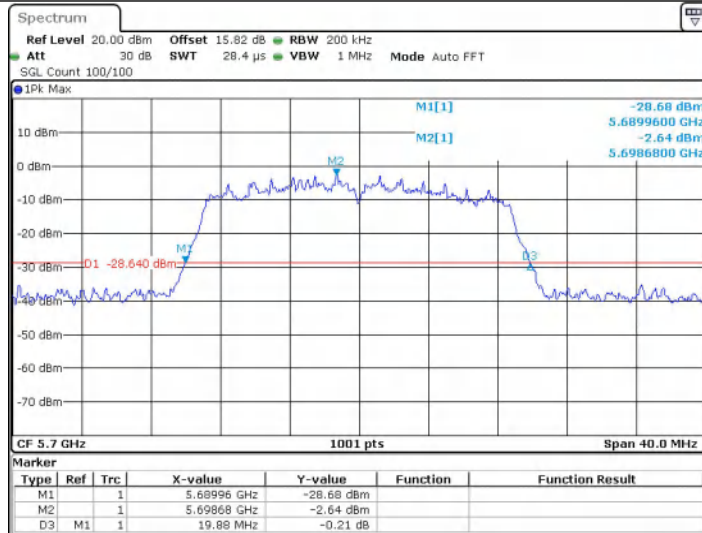


11AC20SISO_Ant2_5580



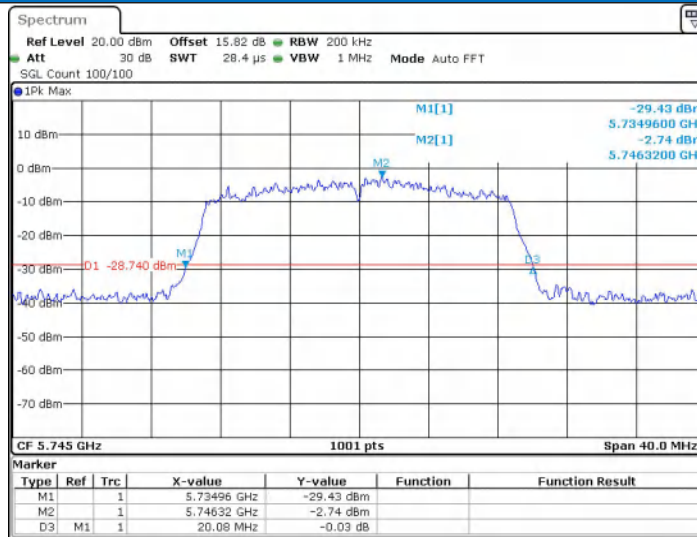
Date: 11 DEC 2025 15:46:06

11AC20SISO_Ant2_5700



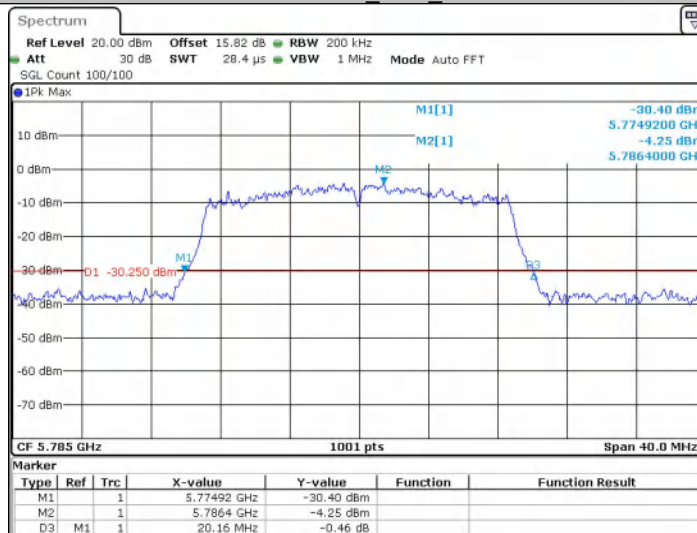
Date: 11 DEC 2025 15:47:51

11AC20SISO_Ant2_5745



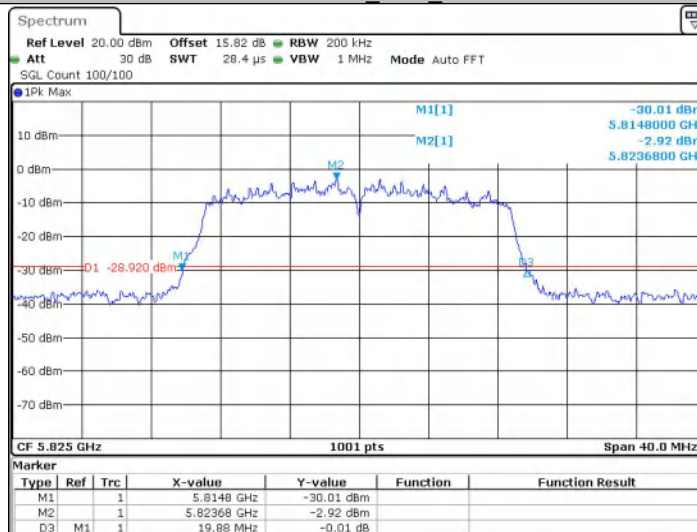
Date: 11 DEC 2025 15:52:26

11AC20SISO_Ant2_5785



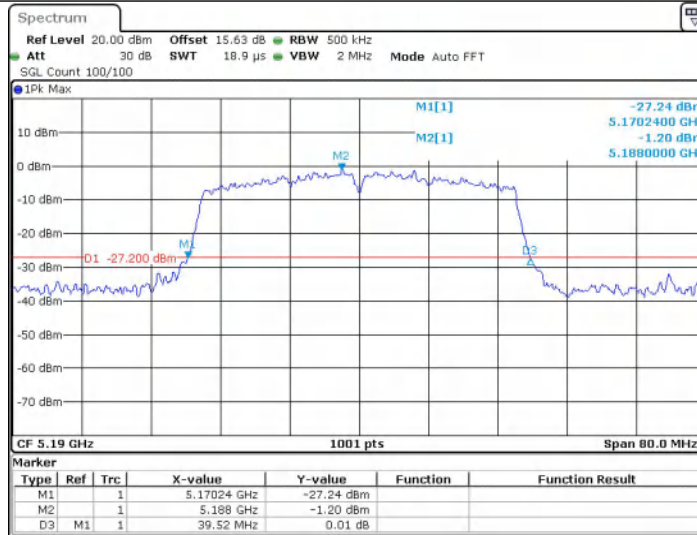
Date: 11 DEC 2025 15:54:54

11AC20SISO_Ant2_5825



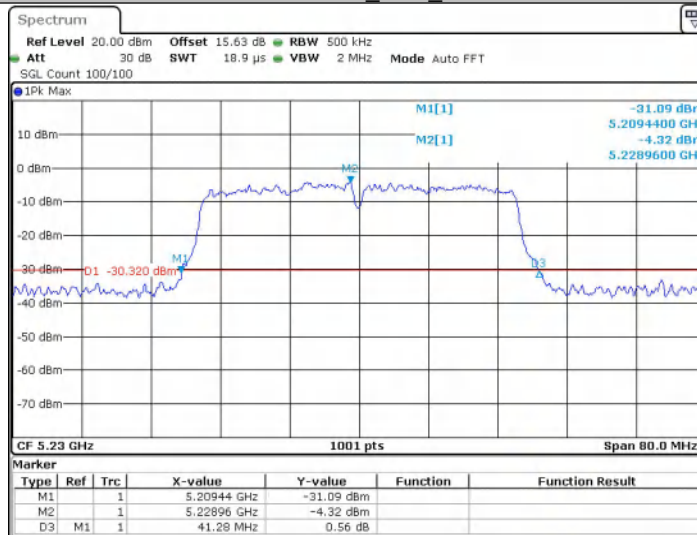
Date: 11 DEC 2025 16:10:35

11AC40SISO_Ant2_5190



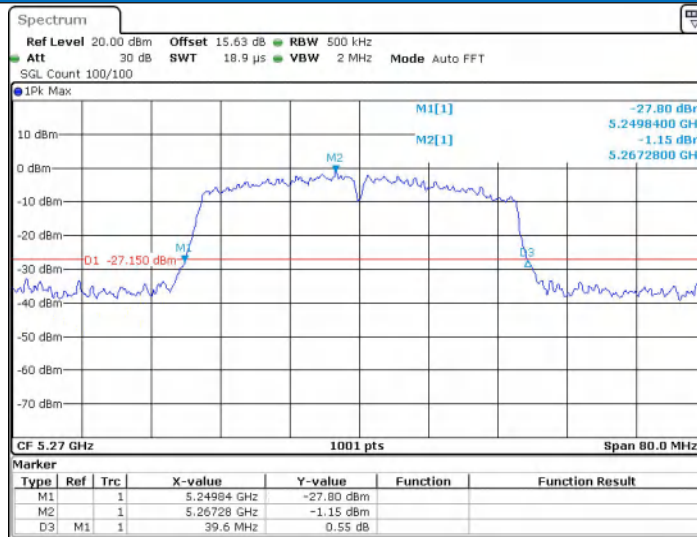
Date: 11 DEC 2025 16:12:02

11AC40SISO_Ant2_5230



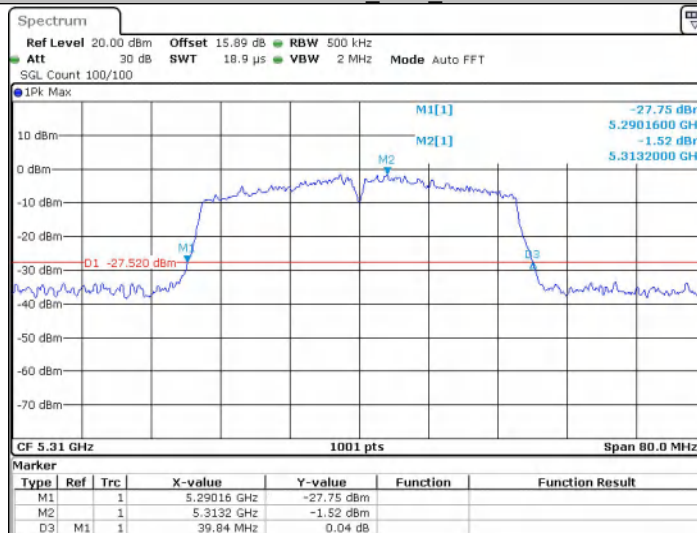
Date: 11 DEC 2025 16:13:50

11AC40SISO_Ant2_5270



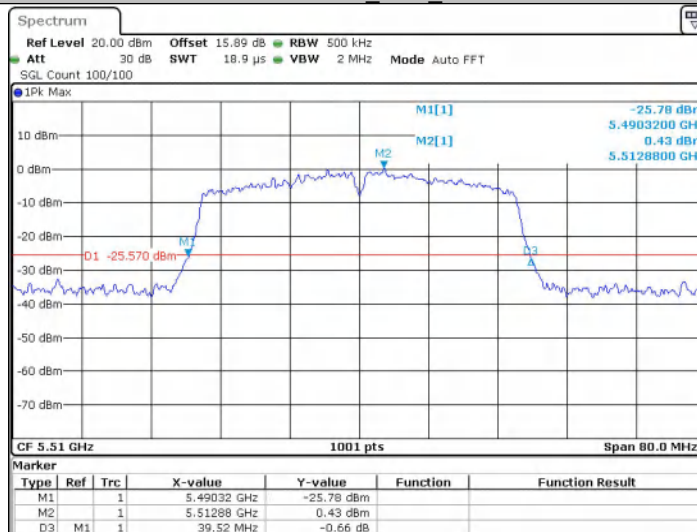
Date: 11 DEC 2025 16:15:15

11AC40SISO_Ant2_5310



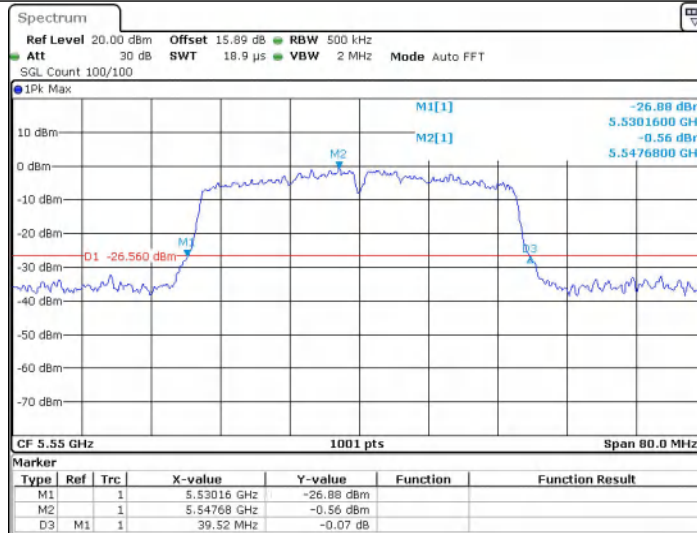
Date: 11 DEC 2025 16:16:13

11AC40SISO_Ant2_5510



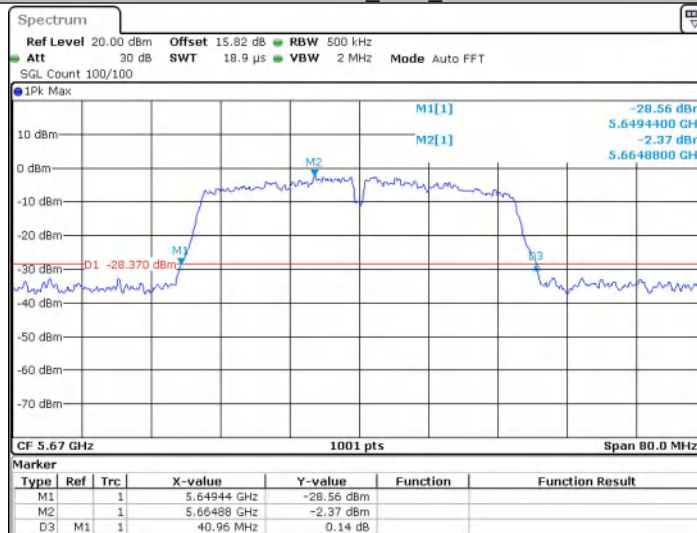
Date: 11 DEC 2025 16:17:10

11AC40SISO_Ant2_5550



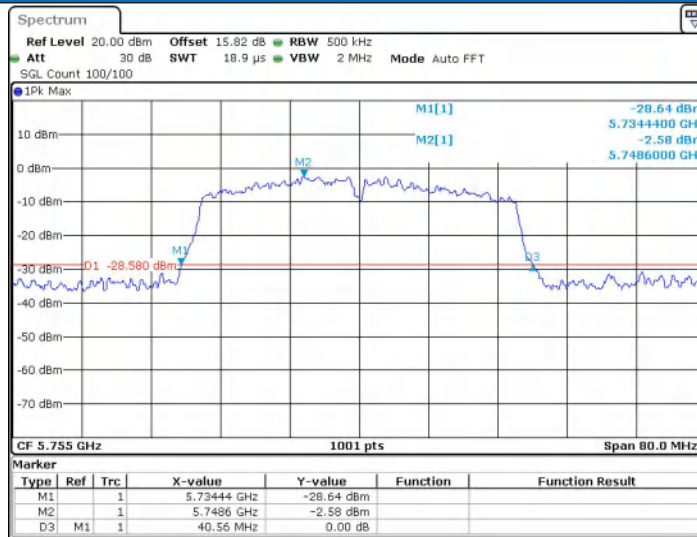
Date: 11 DEC 2025 16:18:08

11AC40SISO_Ant2_5670



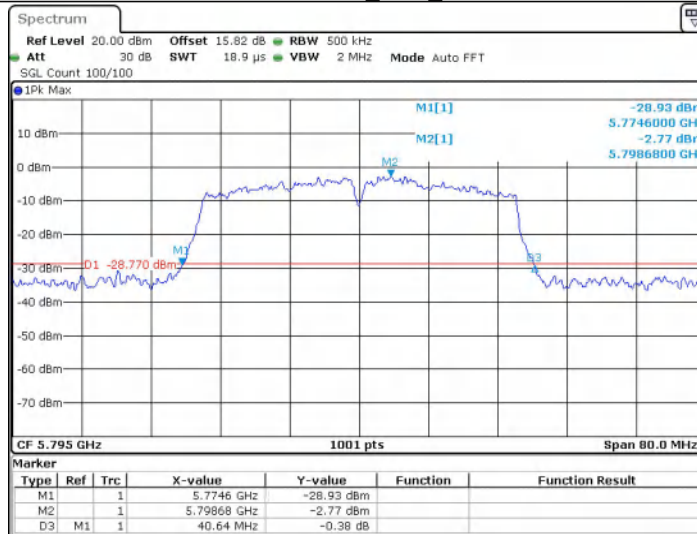
Date: 11 DEC 2025 16:20:09

11AC40SISO_Ant2_5755



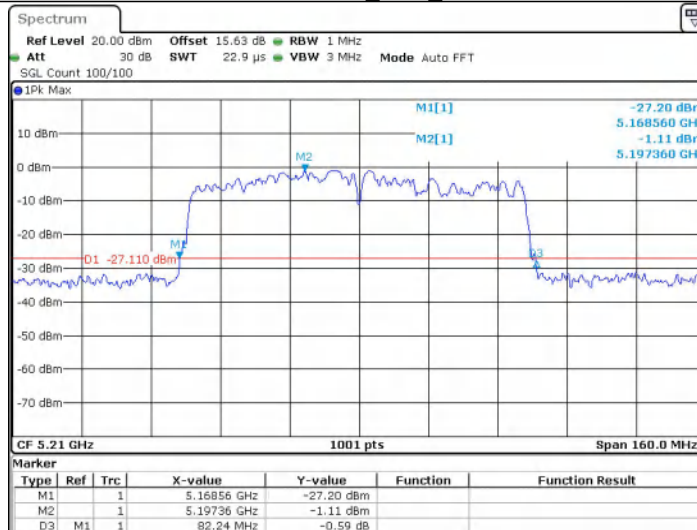
Date: 11 DEC 2025 16:21:41

11AC40SISO_Ant2_5795



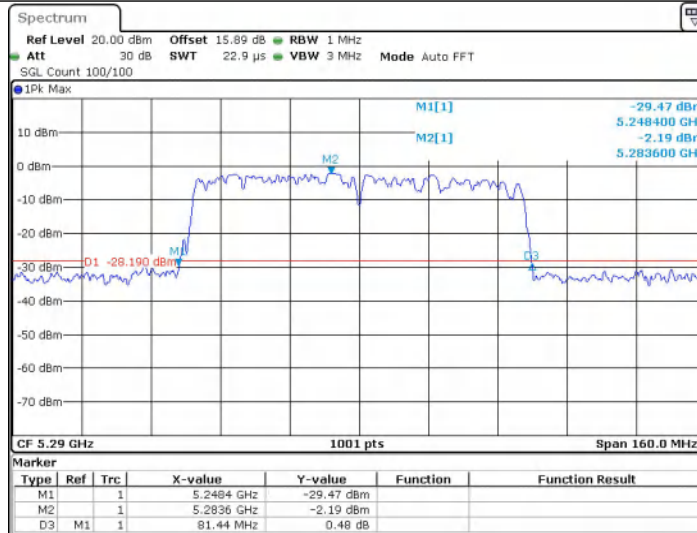
Date: 11 DEC 2025 16:25:39

11AC80SISO_Ant2_5210



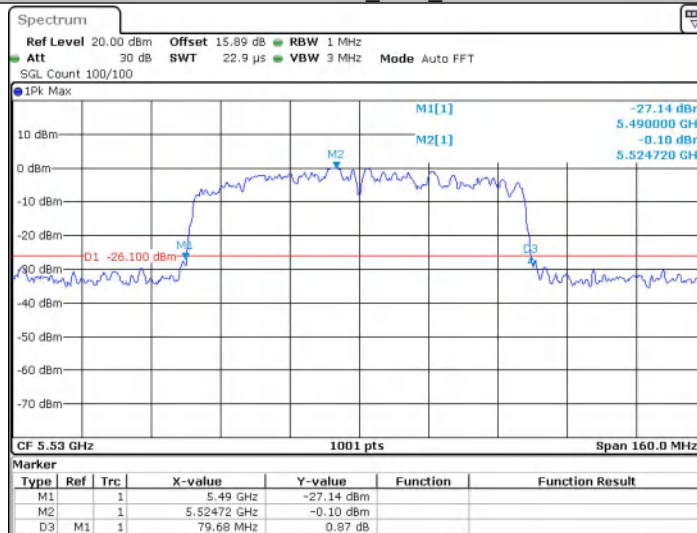
Date: 11 DEC 2025 16:27:48

11AC80SISO_Ant2_5290



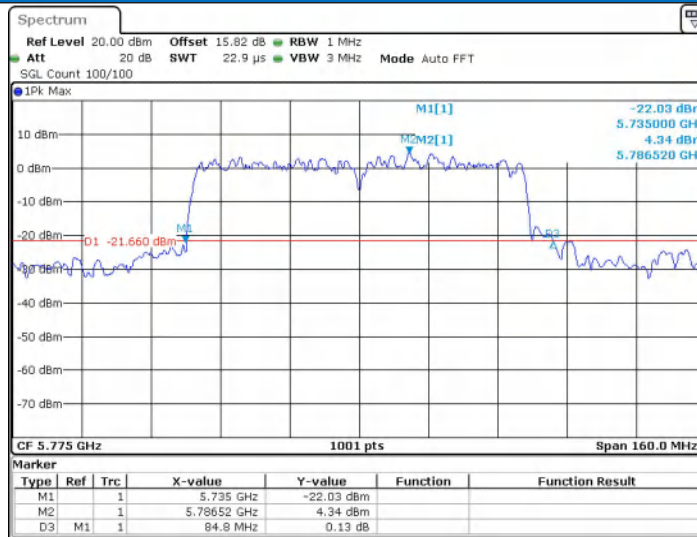
Date: 11 DEC 2025 16:29:14

11AC80SISO_Ant2_5530



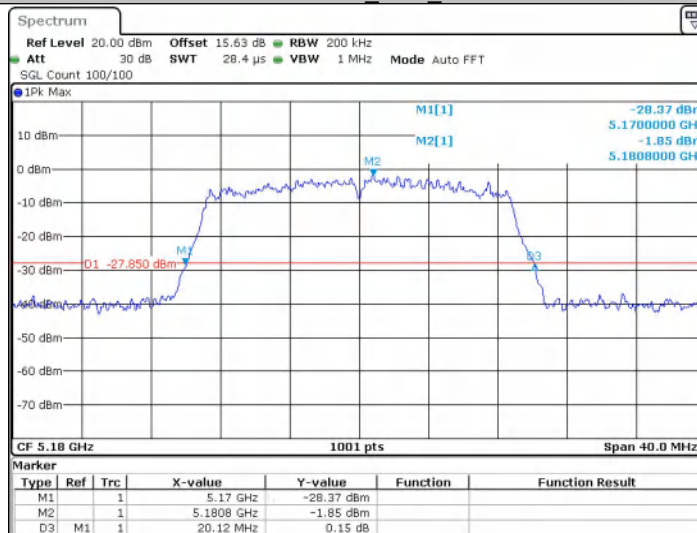
Date: 11 DEC 2025 16:30:29

11AC80SISO_Ant2_5775



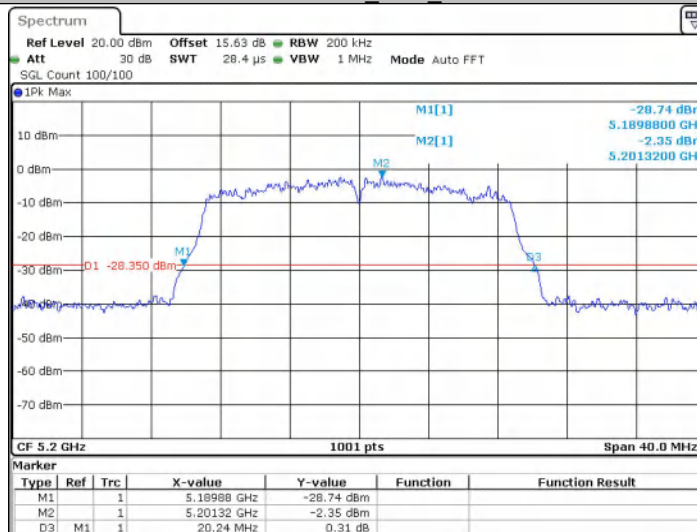
Date: 22 JAN 2026 10:49:12

11AX20SISO_Ant2_5180



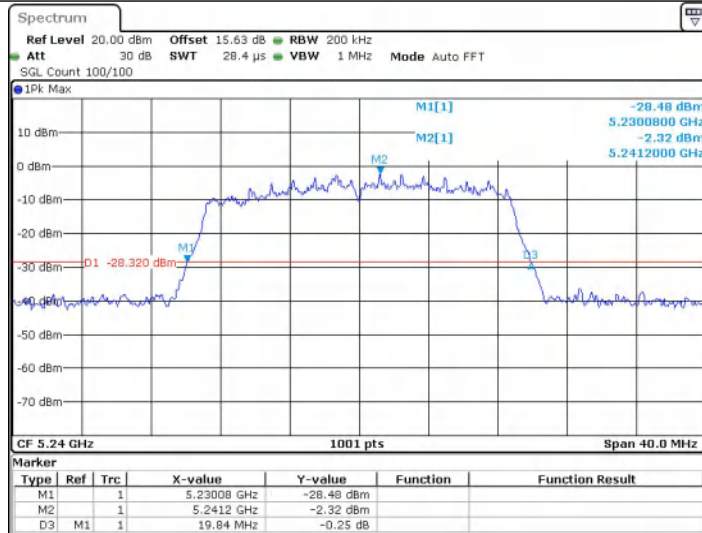
Date: 11 DEC 2025 16:36:45

11AX20SISO_Ant2_5200



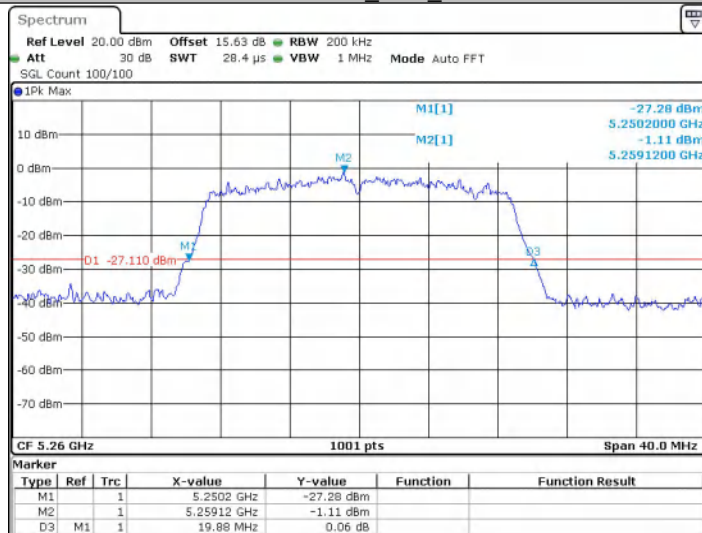
Date: 11 DEC 2025 16:37:40

11AX20SISO_Ant2_5240



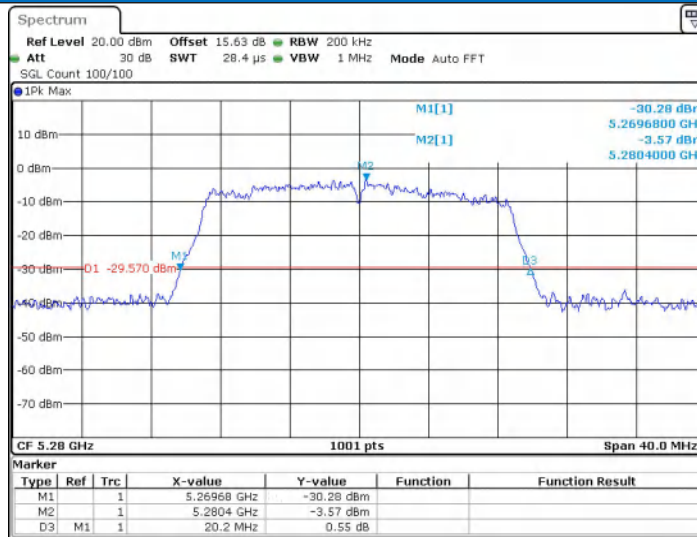
Date: 11 DEC 2025 16:38:49

11AX20SISO_Ant2_5260



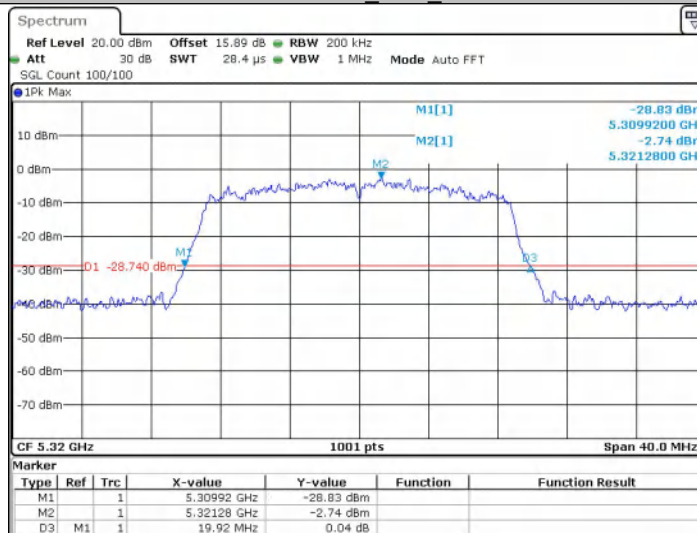
Date: 11 DEC 2025 16:39:49

11AX20SISO_Ant2_5280



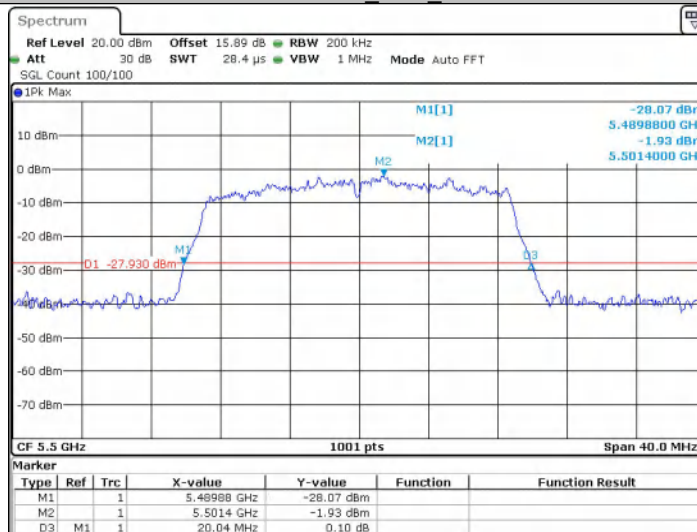
Date: 11 DEC 2025 16:40:47

11AX20SISO_Ant2_5320



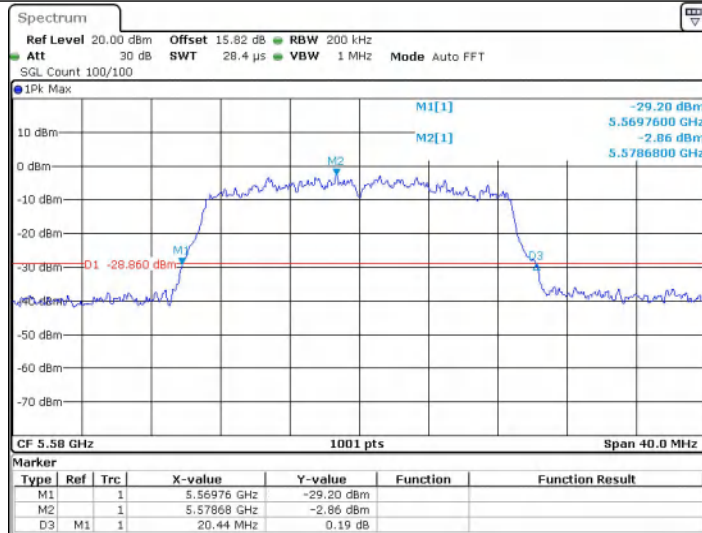
Date: 11 DEC 2025 16:41:43

11AX20SISO_Ant2_5500



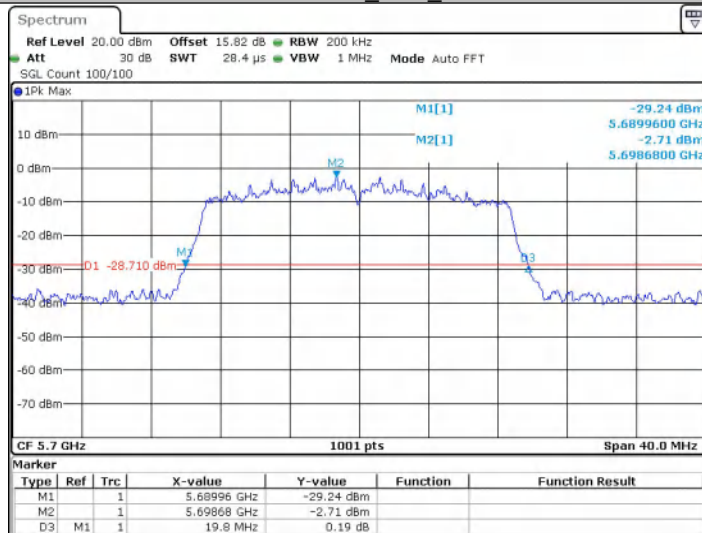
Date: 11 DEC 2025 16:42:36

11AX20SISO_Ant2_5580



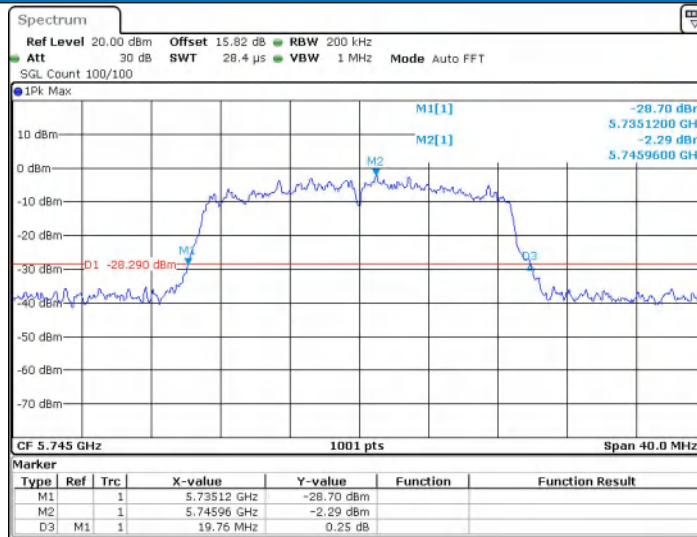
Date: 11 DEC 2025 16:43:29

11AX20SISO_Ant2_5700



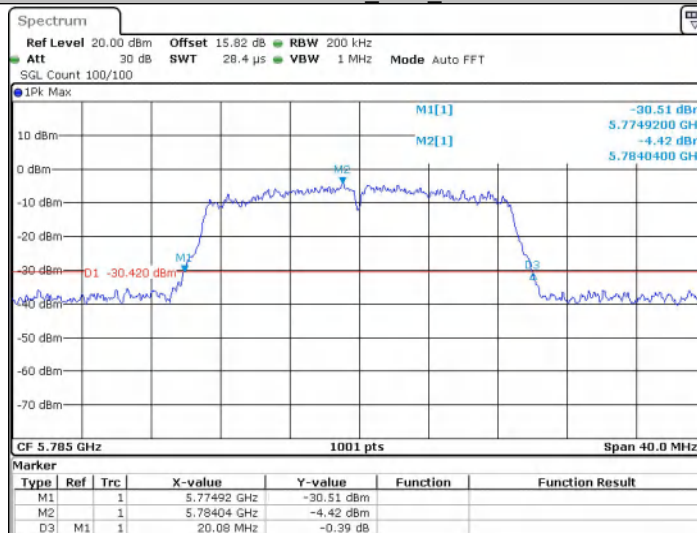
Date: 11 DEC 2025 16:44:31

11AX20SISO_Ant2_5745



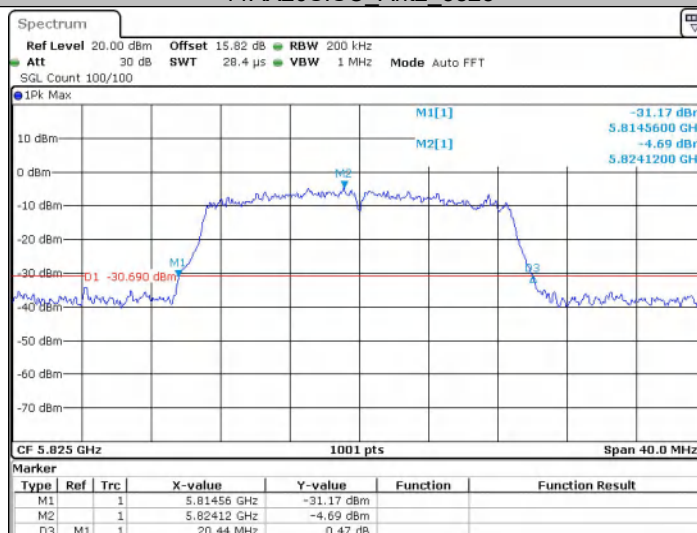
Date: 11 DEC 2025 16:45:54

11AX20SISO_Ant2_5785



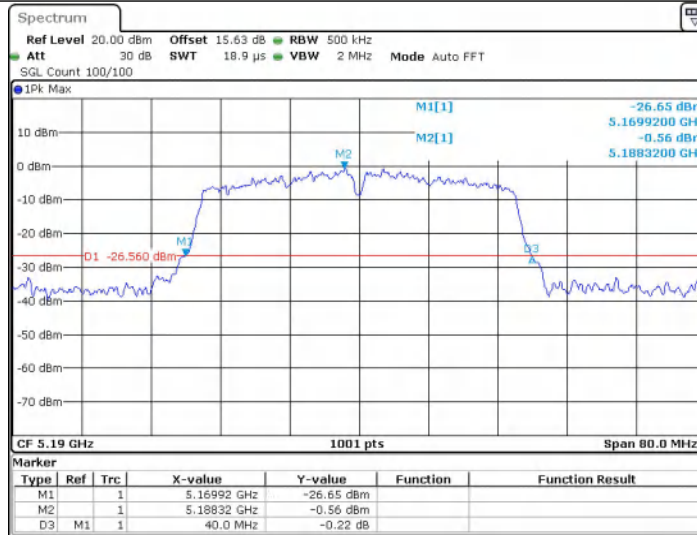
Date: 11 DEC 2025 16:47:01

11AX20SISO_Ant2_5825



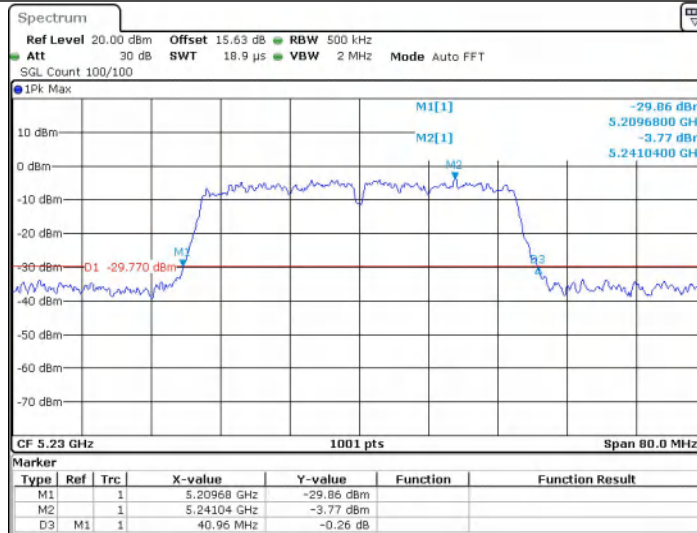
Date: 11 DEC 2025 16:49:38

11AX40SISO_Ant2_5190



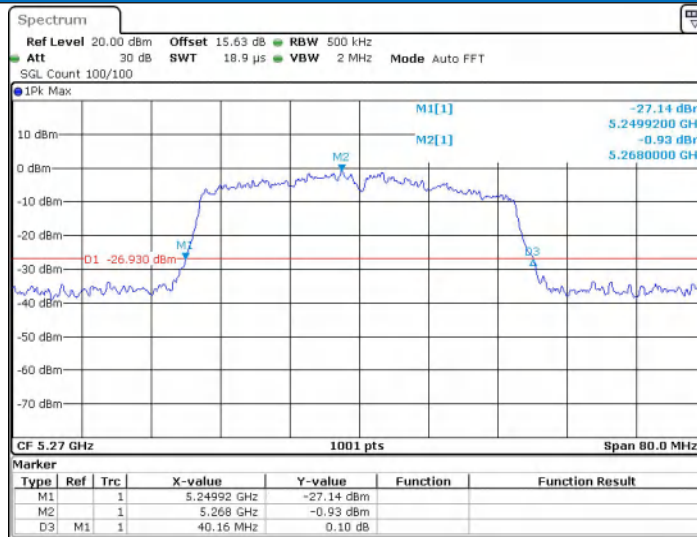
Date: 11 DEC 2025 16:53:52

11AX40SISO_Ant2_5230



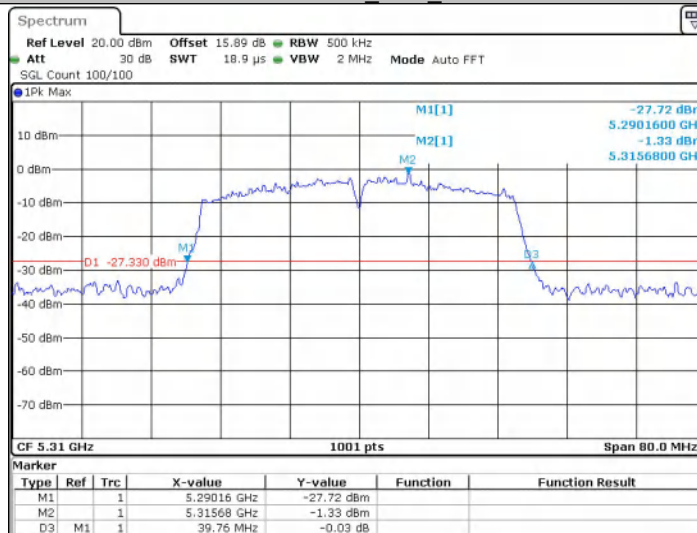
Date: 11 DEC 2025 16:54:47

11AX40SISO_Ant2_5270



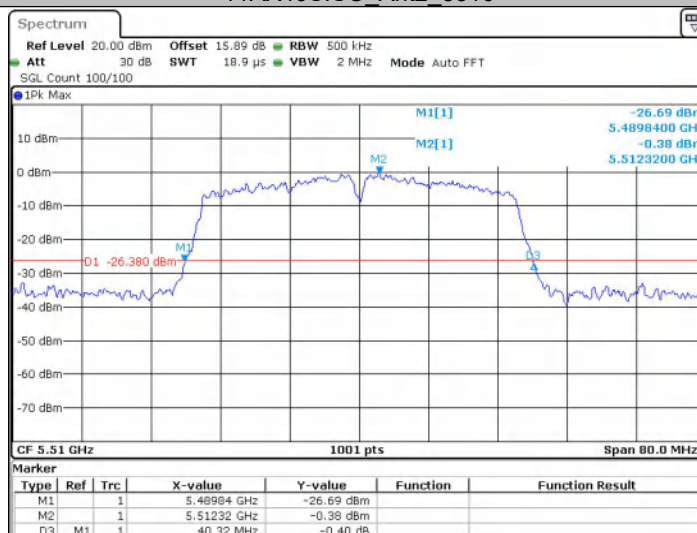
Date: 11 DEC 2025 16:56:57

11AX40SISO_Ant2_5310



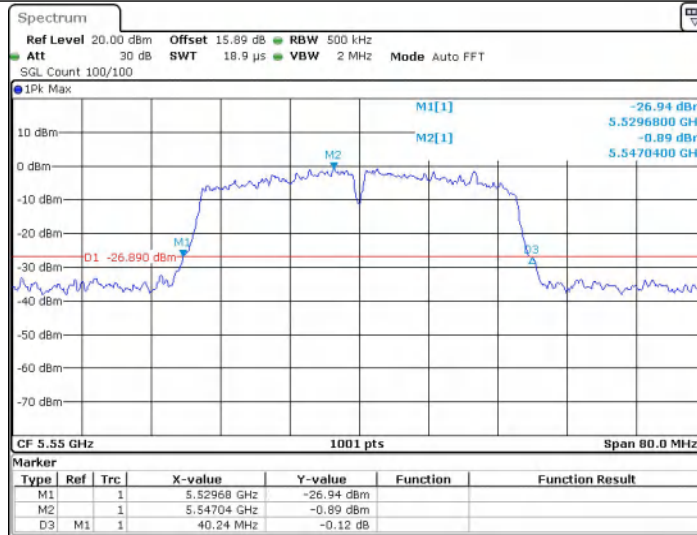
Date: 11 DEC 2025 16:57:54

11AX40SISO_Ant2_5510



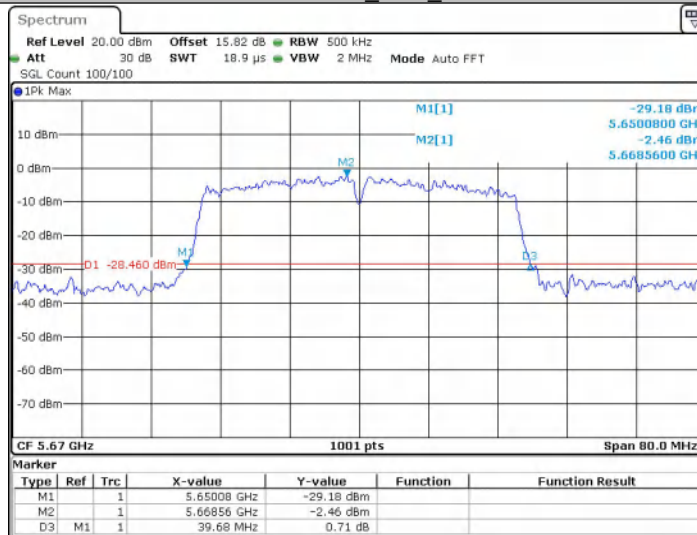
Date: 11 DEC 2025 16:58:55

11AX40SISO_Ant2_5550



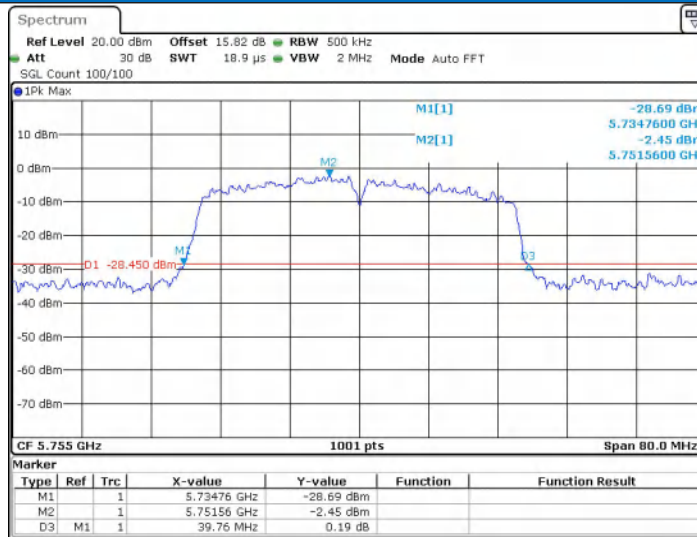
Date: 11 DEC 2025 17:01:29

11AX40SISO_Ant2_5670



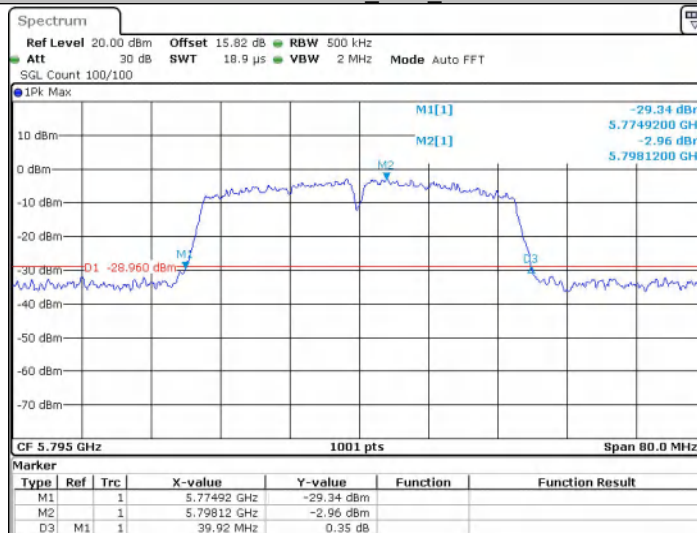
Date: 11 DEC 2025 17:03:57

11AX40SISO_Ant2_5755



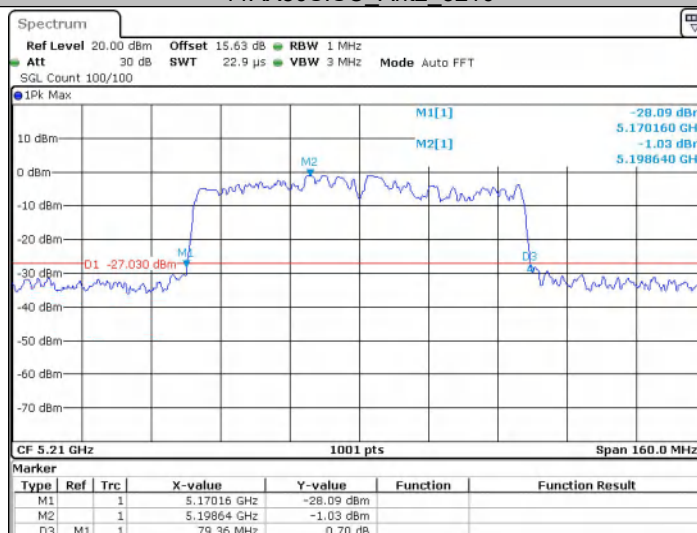
Date: 11 DEC 2025 17:05:02

11AX40SISO_Ant2_5795



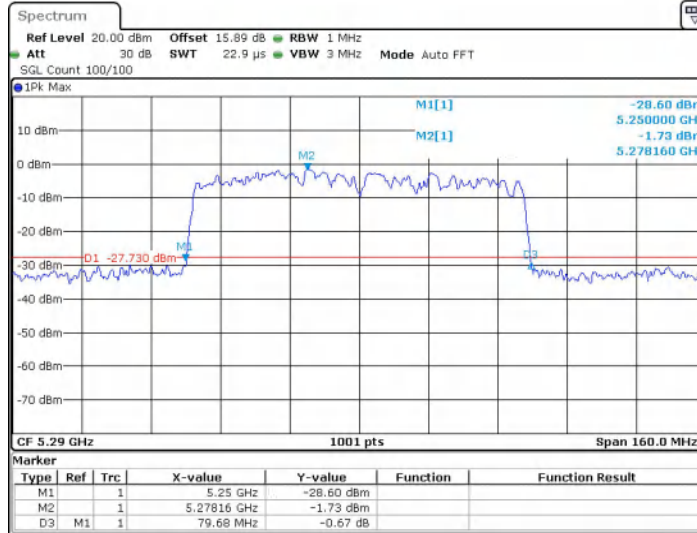
Date: 11 DEC 2025 17:06:15

11AX80SISO_Ant2_5210



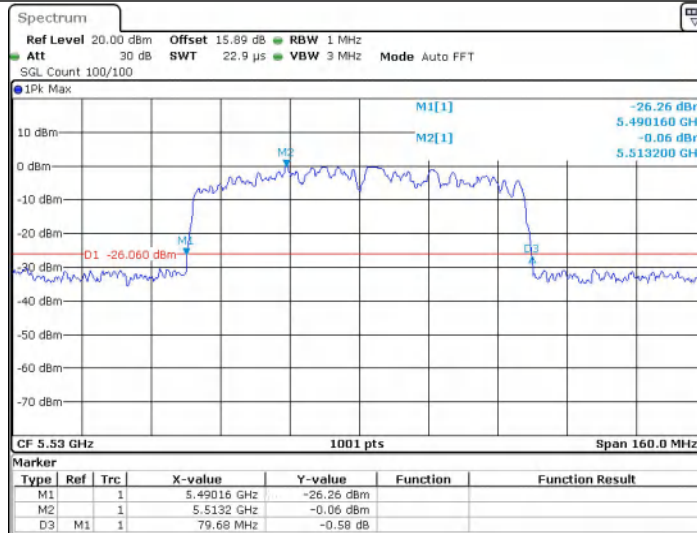
Date: 11 DEC 2025 17:07:29

11AX80SISO_Ant2_5290



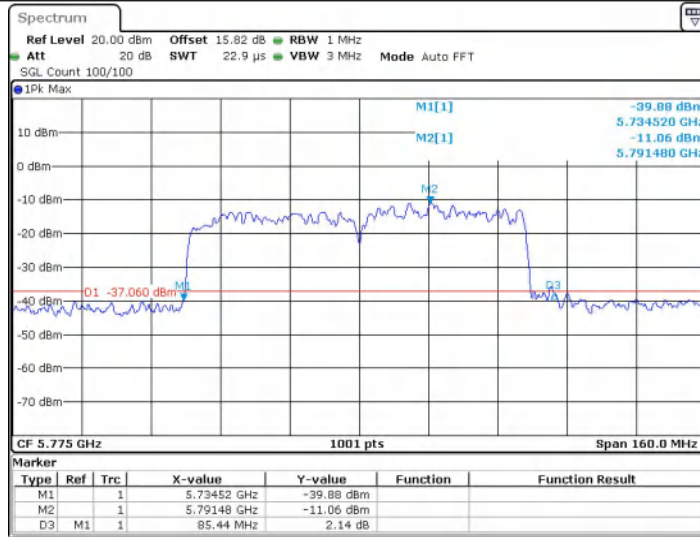
Date: 11 DEC 2025 17:08:41

11AX80SISO_Ant2_5530



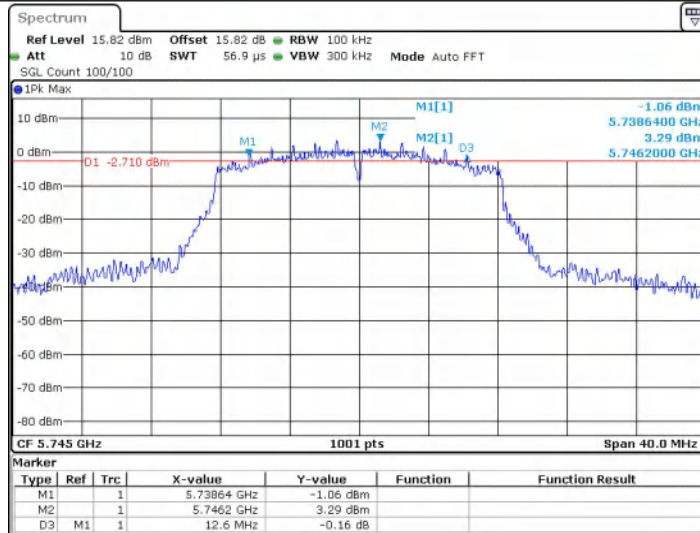
Date: 11 DEC 2025 17:09:59

11AX80SISO_Ant2_5775



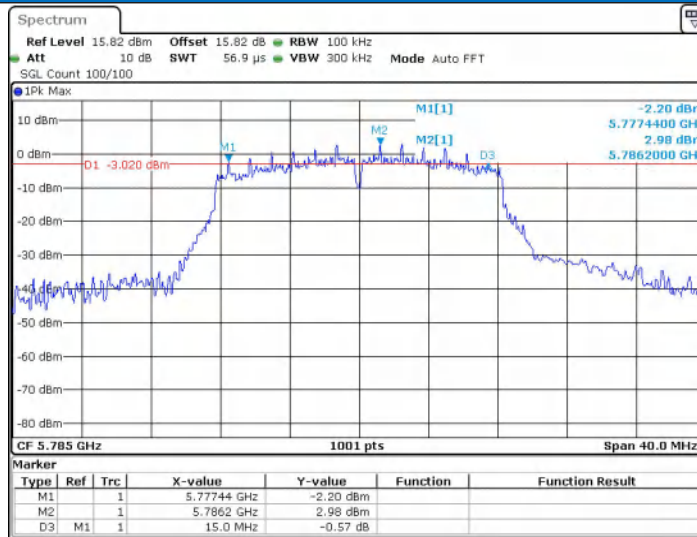
Date: 22 JAN 2026 11:12:34

11A_Ant2_5745



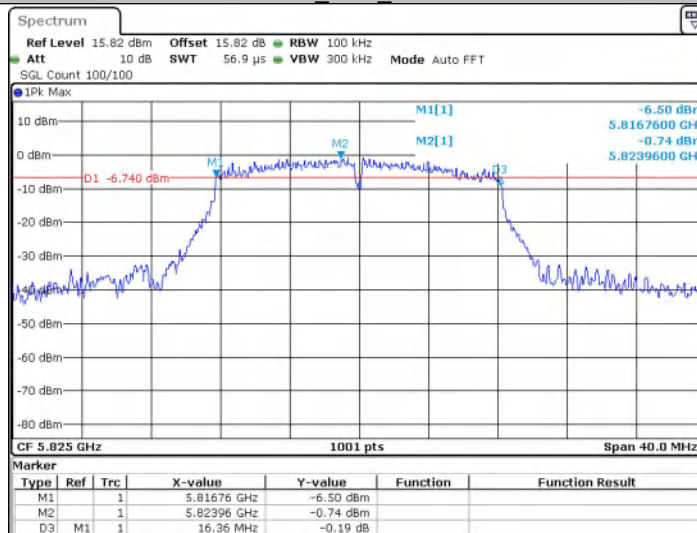
Date: 20 JAN 2026 14:49:07

11A_Ant2_5785



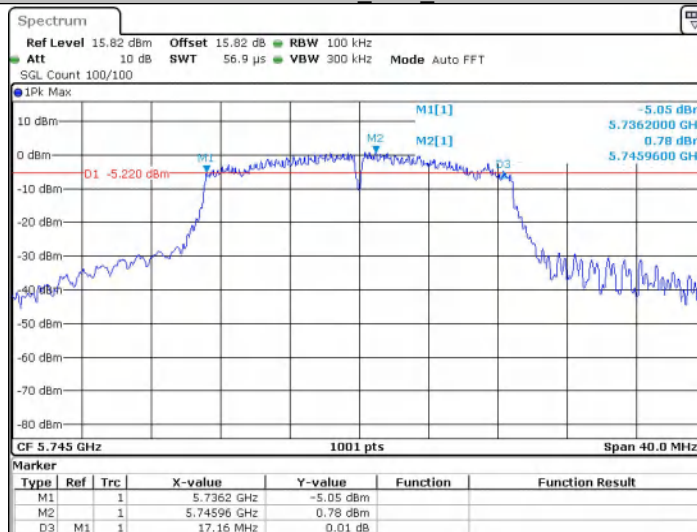
Date: 20 JAN 2026 14:50:54

11A_Ant2_5825



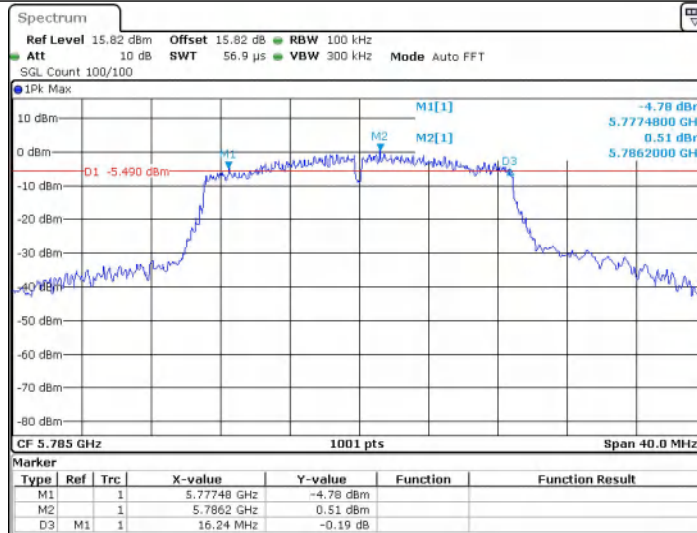
Date: 20 JAN 2026 14:51:28

11N20SISO_Ant2_5745



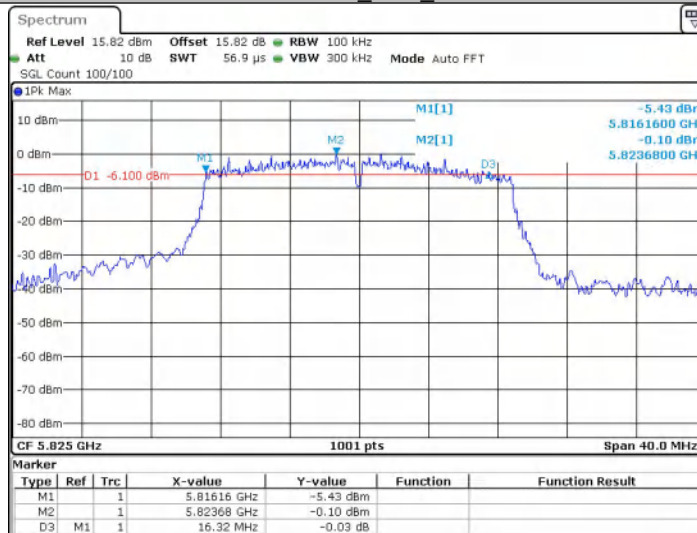
Date: 20 JAN 2026 15:04:27

11N20SISO_Ant2_5785



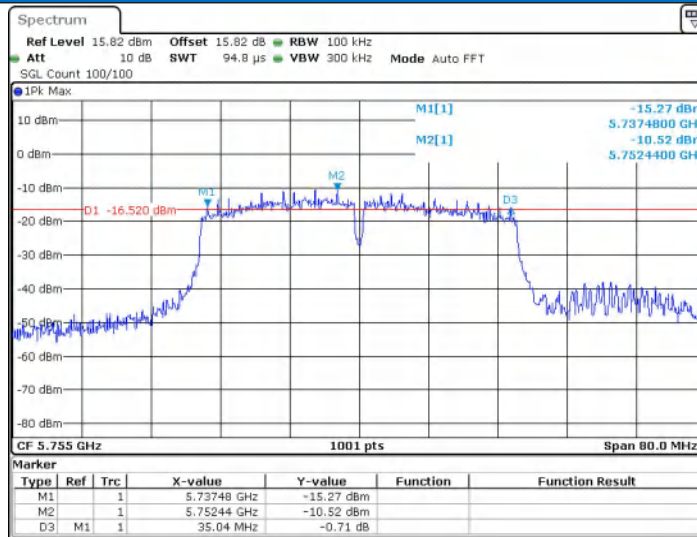
Date: 20 JAN 2026 15:06:18

11N20SISO_Ant2_5825



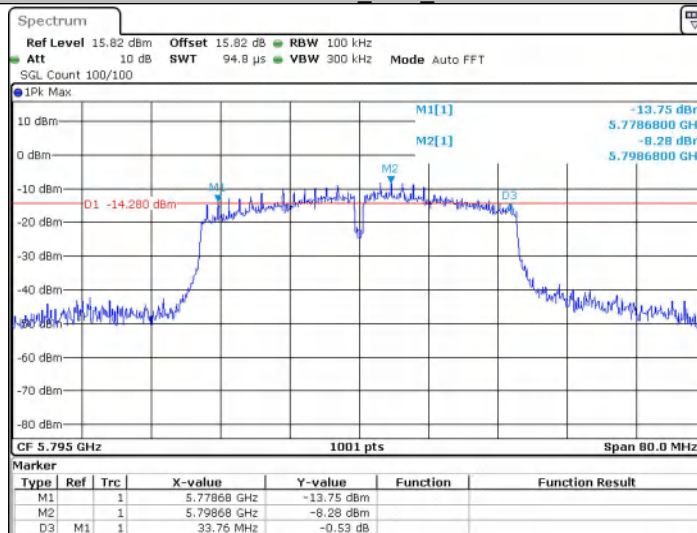
Date: 20 JAN 2026 15:06:52

11N40SISO_Ant2_5755



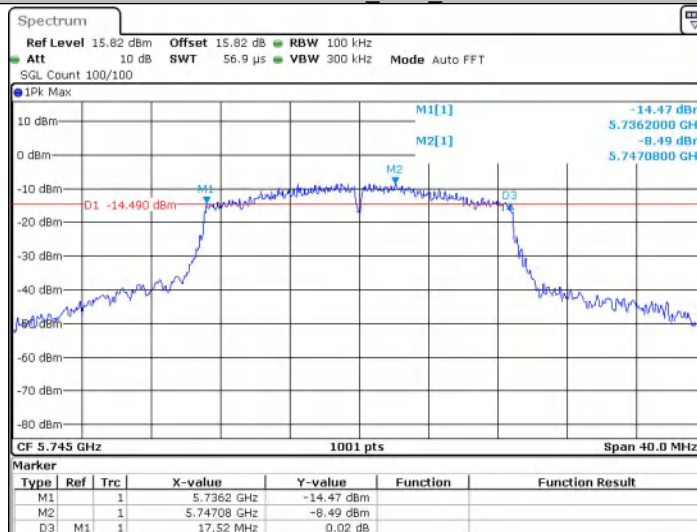
Date: 21 JAN 2026 16:16:22

11N40SISO_Ant2_5795



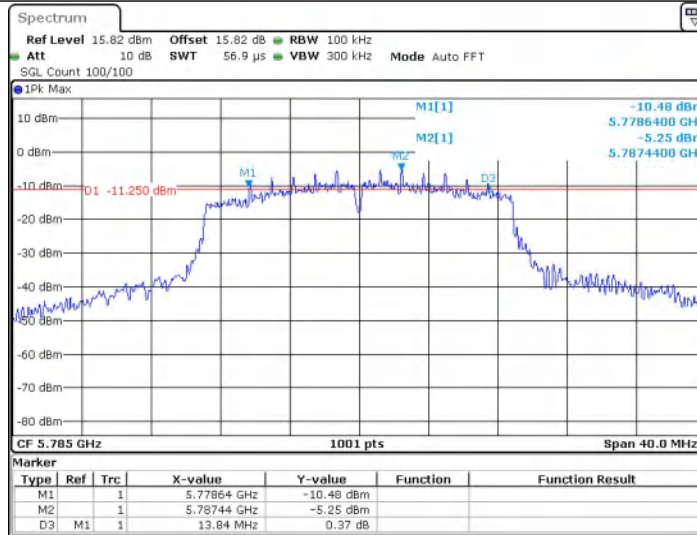
Date: 21 JAN 2026 16:17:00

11AC20SISO_Ant2_5745



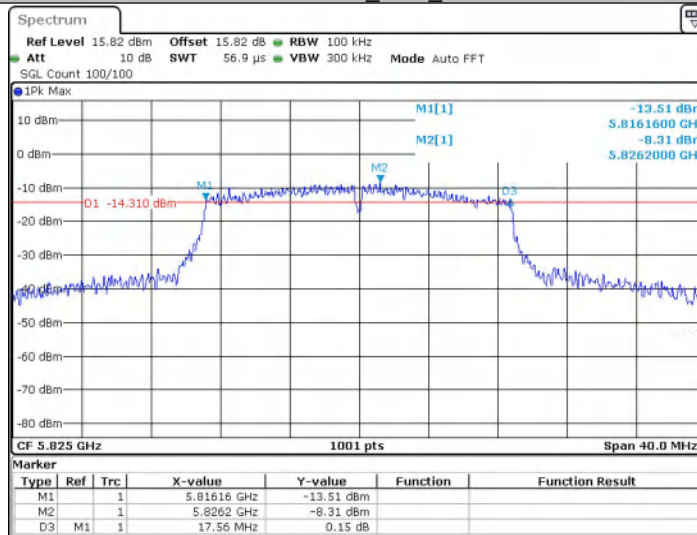
Date: 21 JAN 2026 16:22:57

11AC20SISO_Ant2_5785



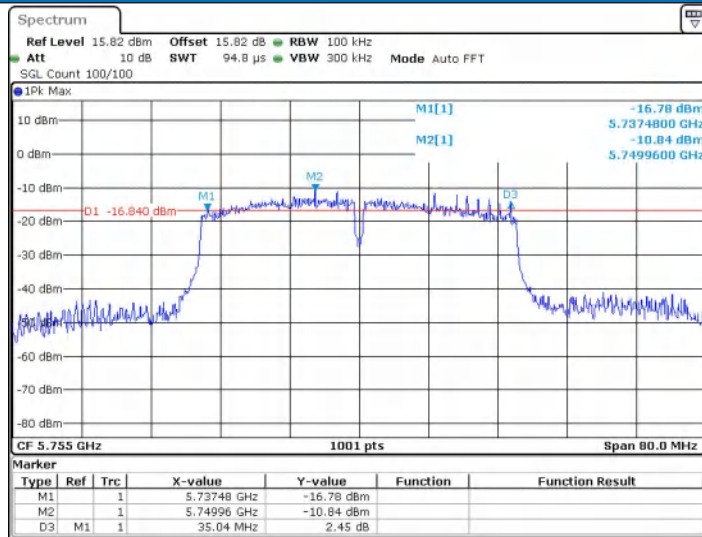
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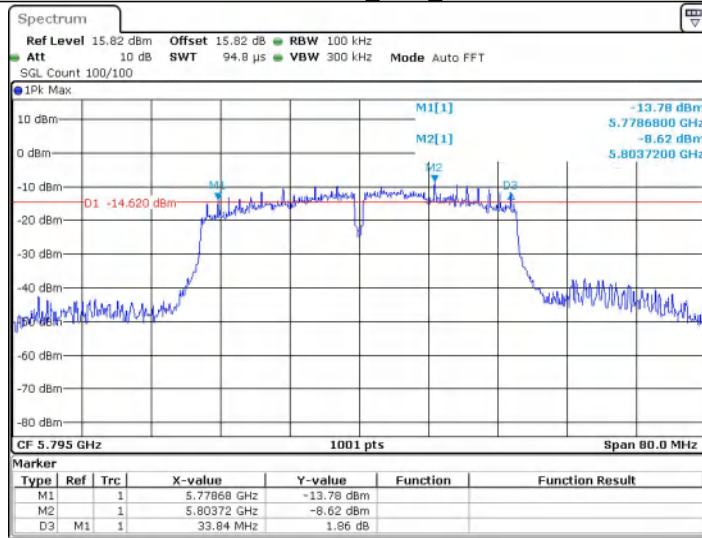


Date: 21 JAN 2026 16:24:14

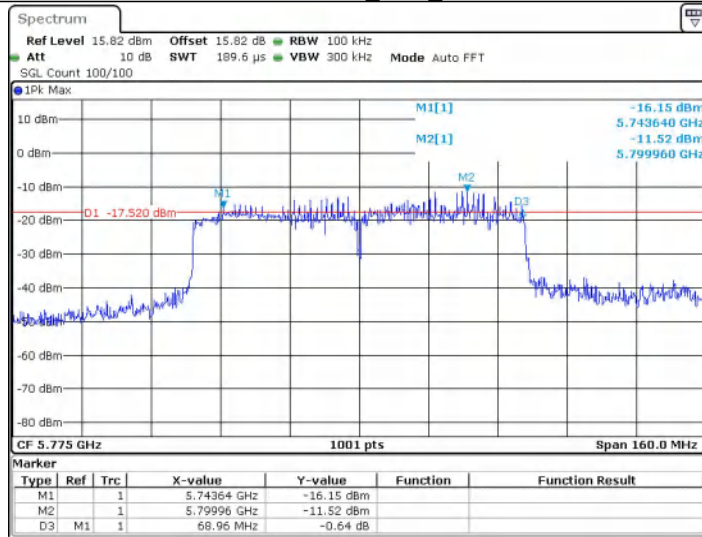
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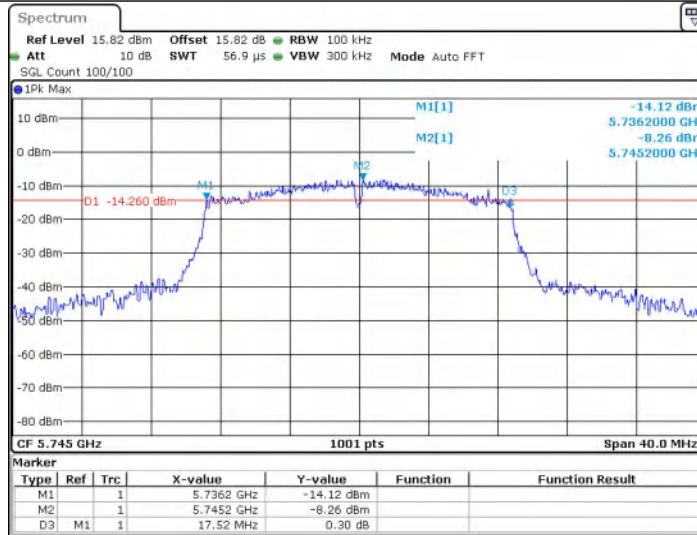
11AC40SISO_Ant2_5795



11AC80SISO_Ant2_5775

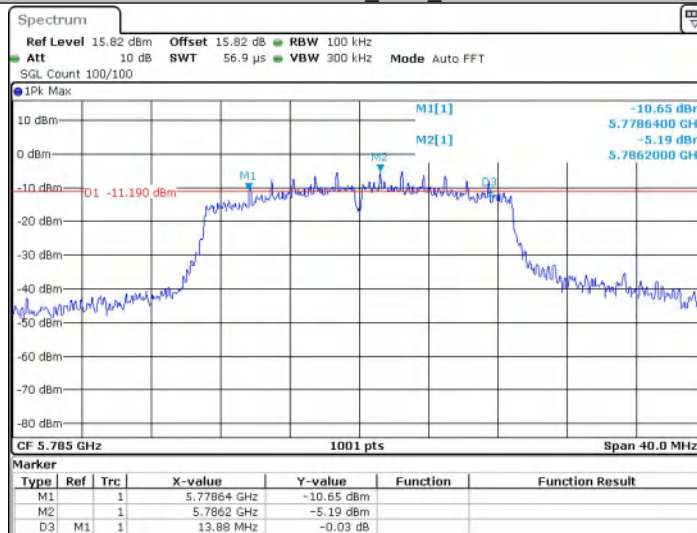


11AX20SISO_Ant2_5745



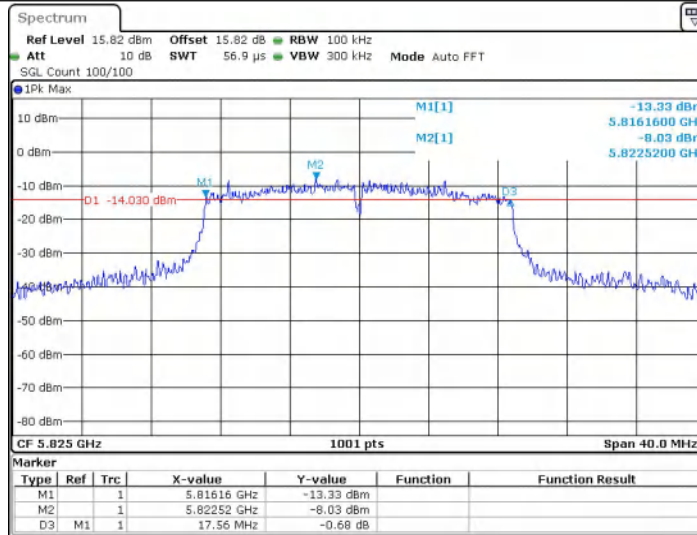
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11AX20SISO_Ant2_5785



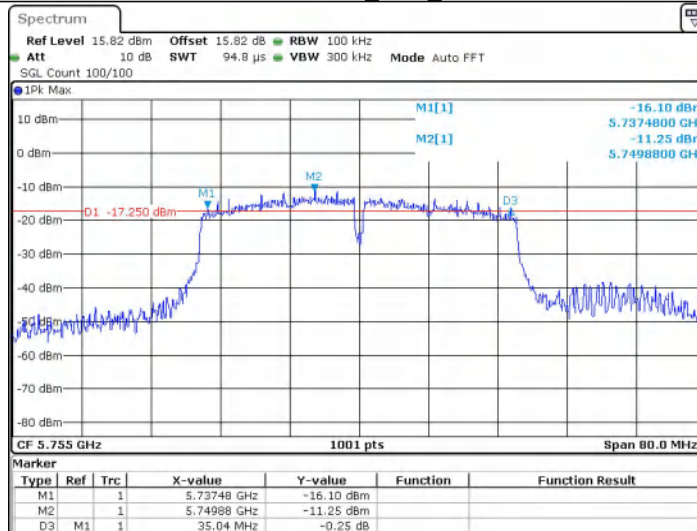
Date: 21 JAN 2026 16:58:58

11AX20SISO_Ant2_5825



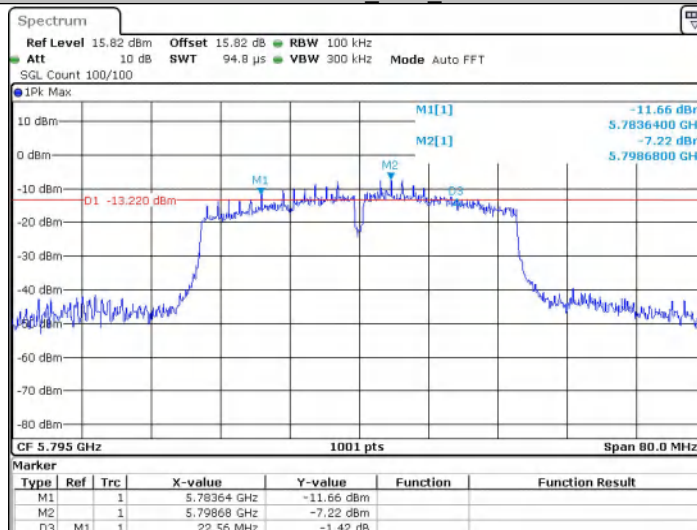
Date: 21 JAN 2026 17:00:28

11AX40SISO_Ant2_5755



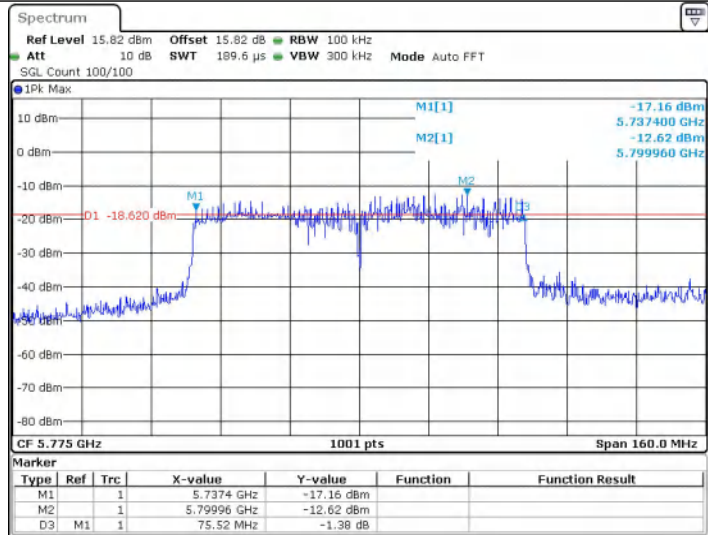
Date: 21 JAN 2026 17:07:26

11AX40SISO_Ant2_5795



Date: 21 JAN 2026 17:08:14

11AX80SISO_Ant2_5775



Date: 21 JAN 2026 17:12:10

Appendix B): Maximum Conduct Output Power

1.Duty Cycle (x)

Test Requirement KDB 789033 D02 II B 1

Test Method: KDB 789033 II B 1

Test Procedure:

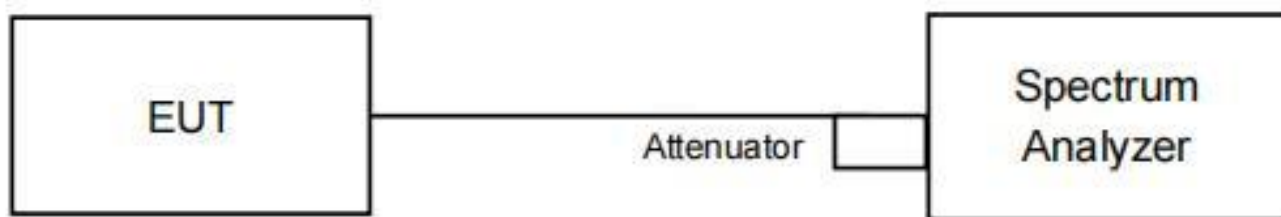
Set RBW = 20MHz

Set VBW = 40MHz

Set detector = peak.

Set span =0Hz

Test Setup Diagram

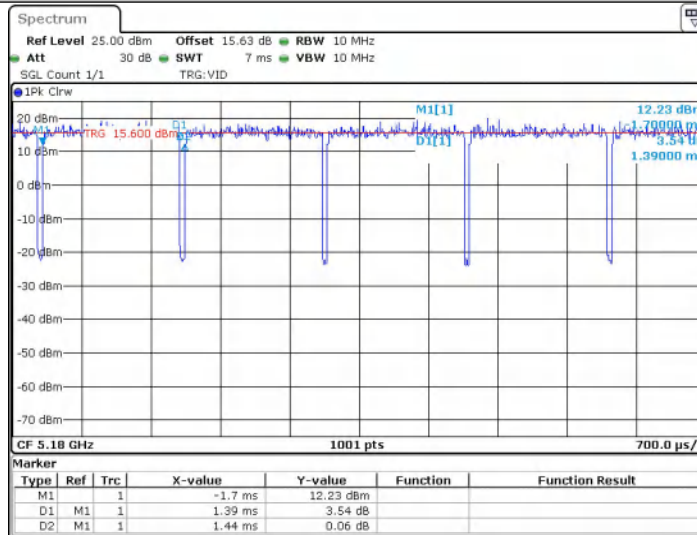


Measurement Data

Ant1:

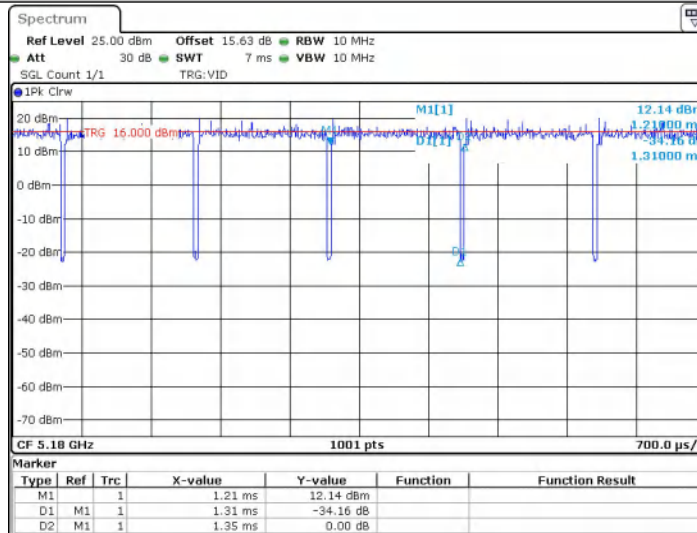
Test Mode	Antenna	Duty Cycle[%]	10log(1/x) Factor[dB]
11A	Ant1	96.53	0.15
11N20	Ant1	97.04	0.13
11N40	Ant1	94.20	0.26
11AC20	Ant1	96.32	0.16
11AC40	Ant1	92.86	0.32
11AC80	Ant1	89.19	0.50
11AX20	Ant1	97.06	0.13
11AX40	Ant1	94.29	0.26
11AX80	Ant1	88.89	0.51

11A



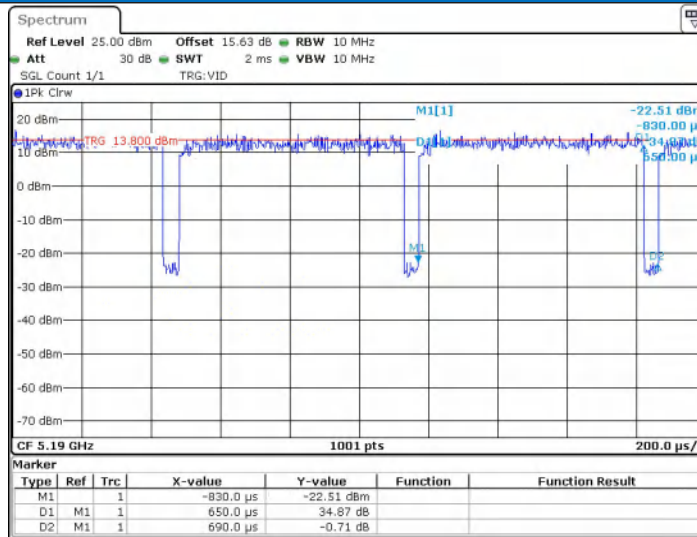
Date: 12 DEC 2025 16:53:15

11N20



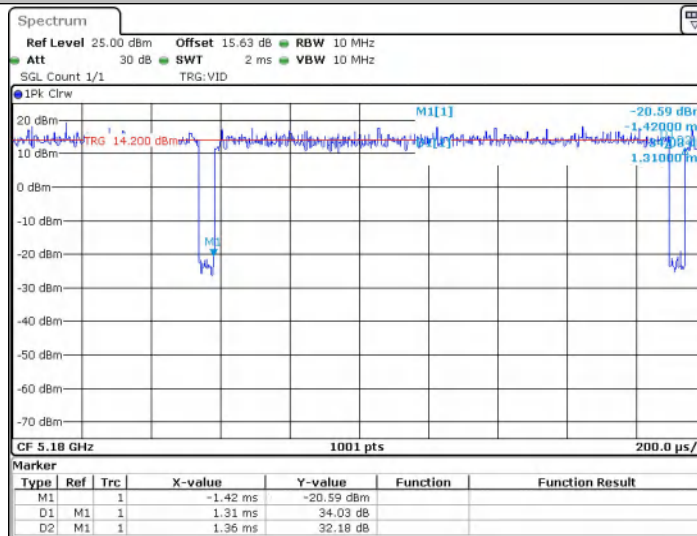
Date: 12 DEC 2025 17:25:29

11N40



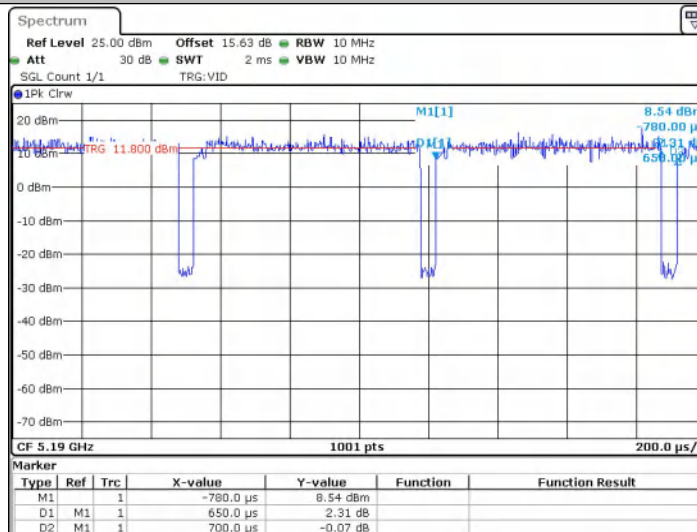
Date: 12 DEC 2025 17:45:40

11AC20



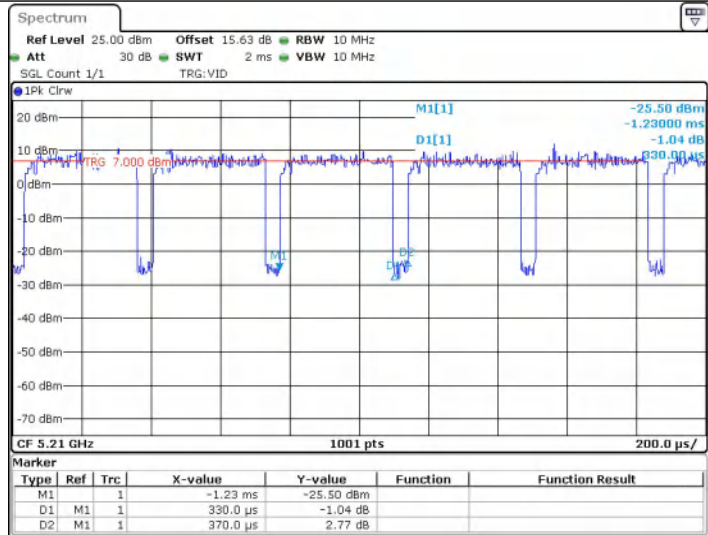
Date: 13 DEC 2025 13:55:11

11AC40

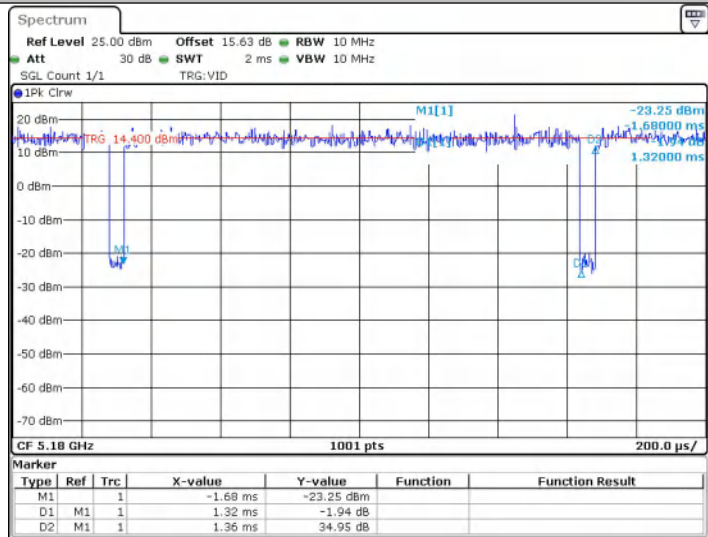


Date: 13 DEC 2025 14:15:07

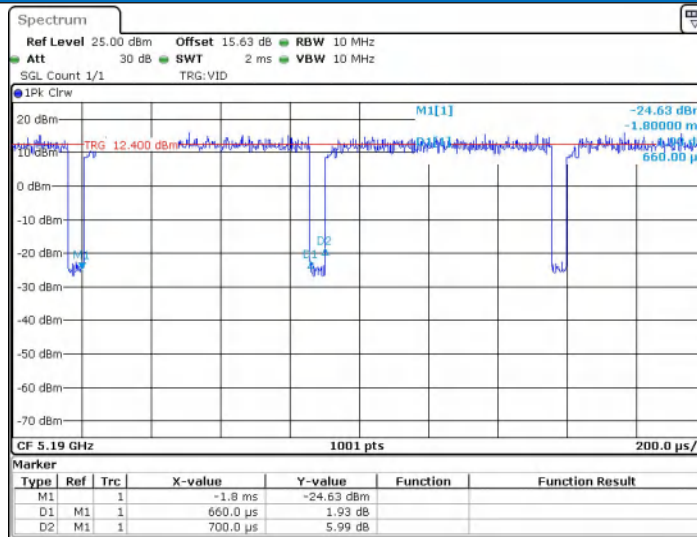
11AC80



11AX20

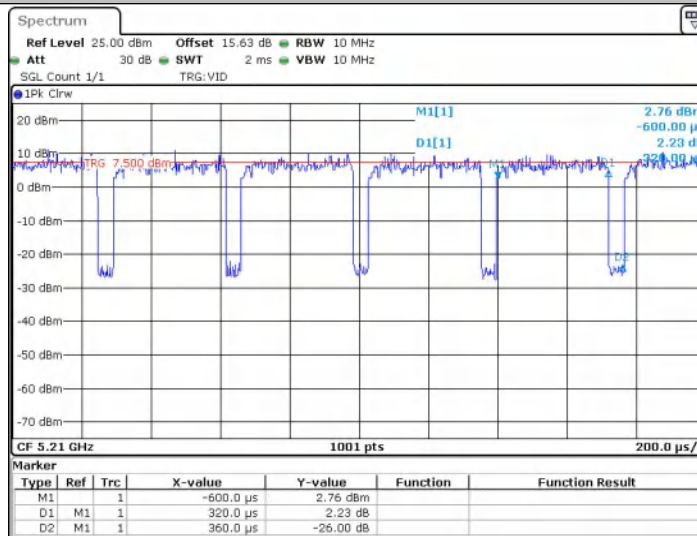


11AX40



Date: 13 DEC 2025 15:01:53

11AX80

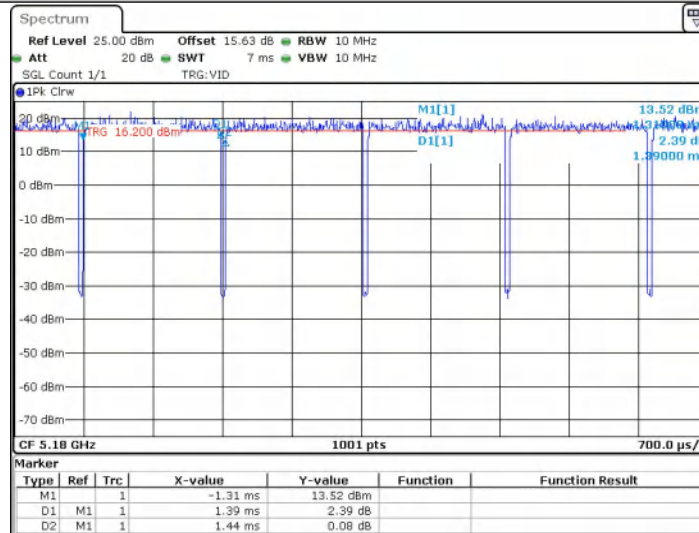


Date: 13 DEC 2025 15:30:28

Ant2:

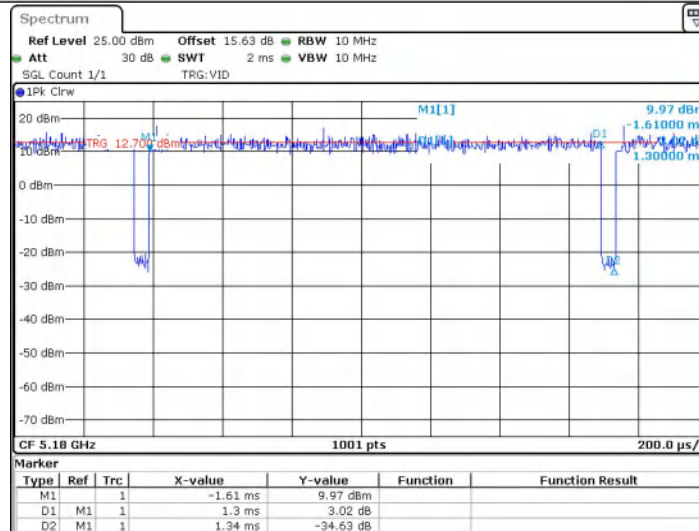
Test Mode	Antenna	Duty Cycle[%]	10log(1/x) Factor[dB]
11A	Ant1	96.53	0.15
11N20	Ant1	97.01	0.13
11N40	Ant1	92.75	0.33
11AC20	Ant1	96.30	0.16
11AC40	Ant1	94.20	0.26
11AC80	Ant1	97.25	0.12
11AX20	Ant1	96.27	0.17
11AX40	Ant1	92.86	0.32
11AX80	Ant1	97.25	0.12

11A



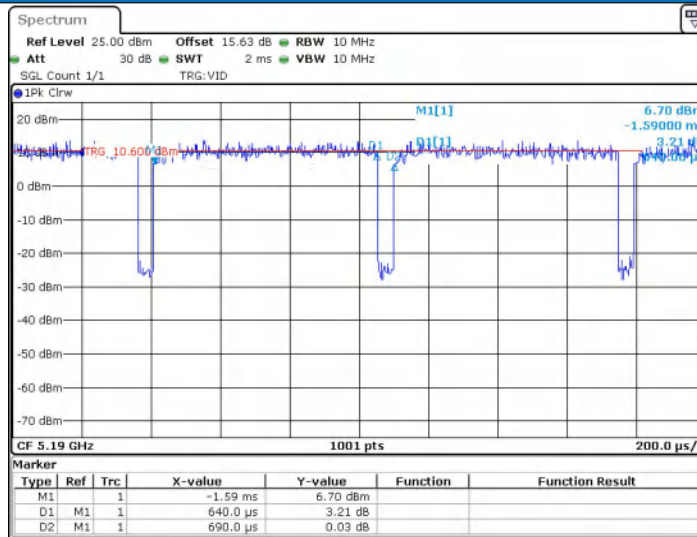
Date: 15 DEC 2025 15:01:59

11N20



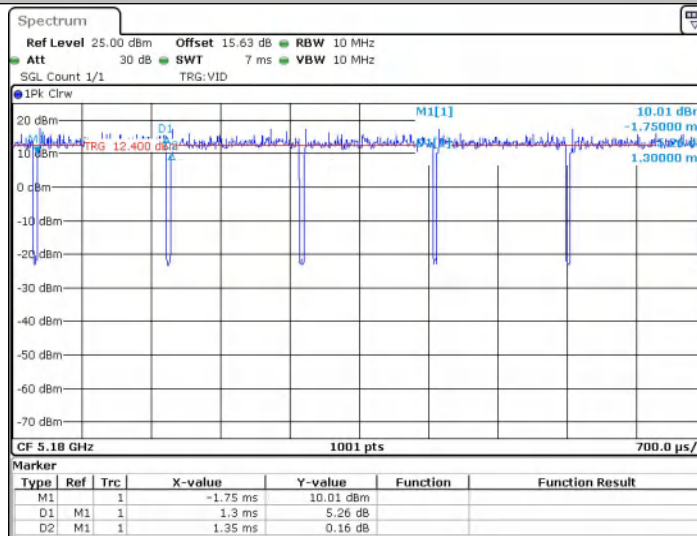
Date: 11 DEC 2025 14:59:34

11N40



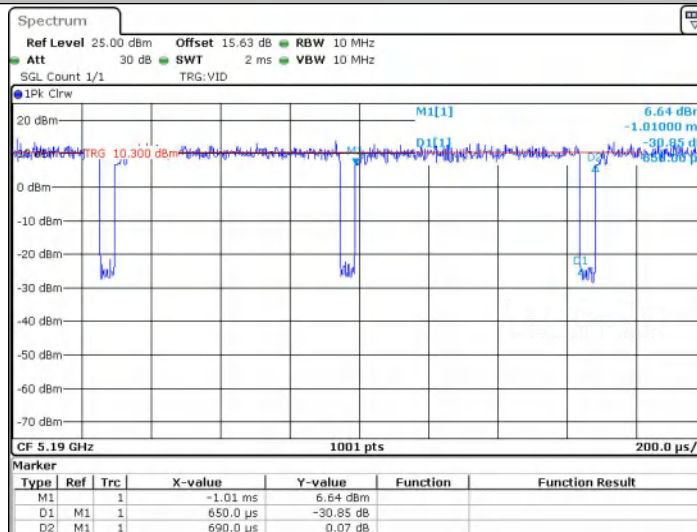
Date: 11 DEC 2025 15:21:04

11AC20



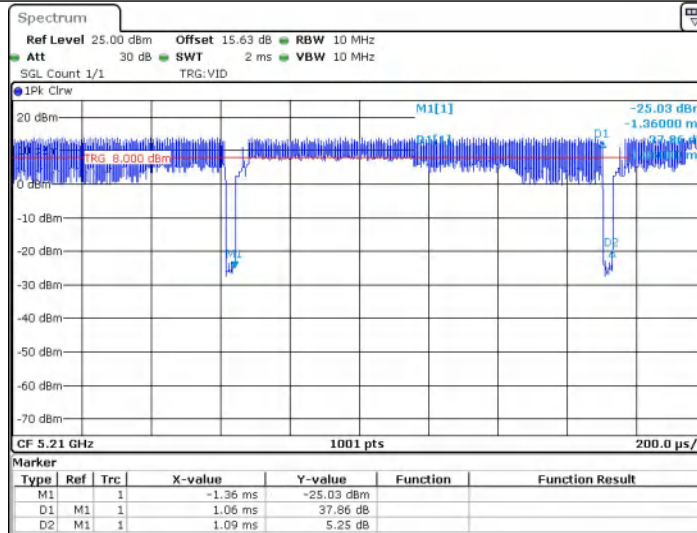
Date: 11 DEC 2025 15:37:47

11AC40



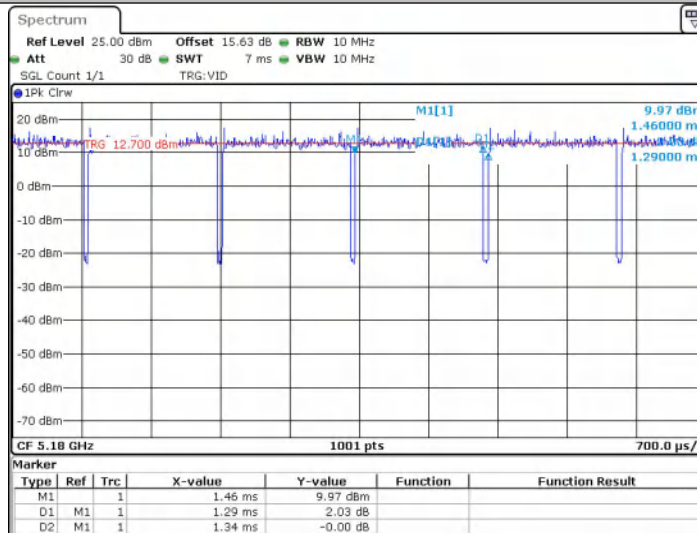
Date: 11 DEC 2025 16:12:24

11AC80



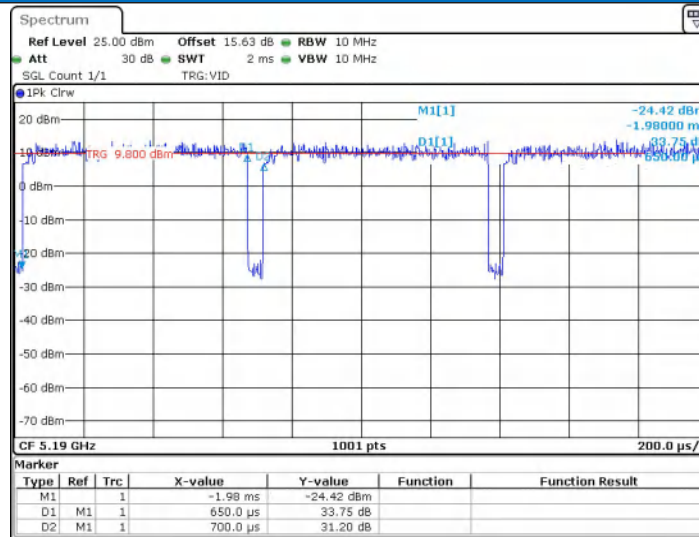
Date: 11 DEC 2025 16:28:19

11AX20



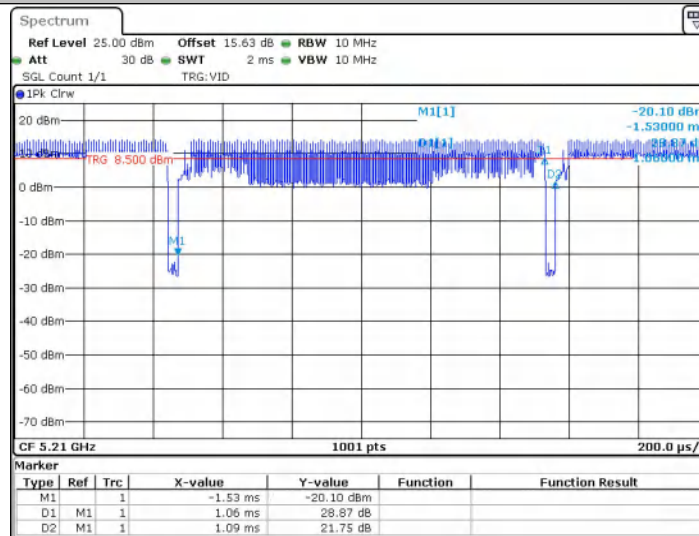
Date: 11 DEC 2025 16:37:07

11AX40



Date: 11 DEC 2025 16:54:13

11AX80



Date: 11 DEC 2025 17:08:00

Note:

Transmitting in full-bandwidth single-user mode (Full RU) with all kinds of modulations, and at the lowest, middle, and highest data rates across the channel.

2. Maximum Conducted Output Power

Test Requirement 47 CFR Part 15, Subpart C 15.407 (a)

Test Method: KDB 789033 D02 II E

Limit:

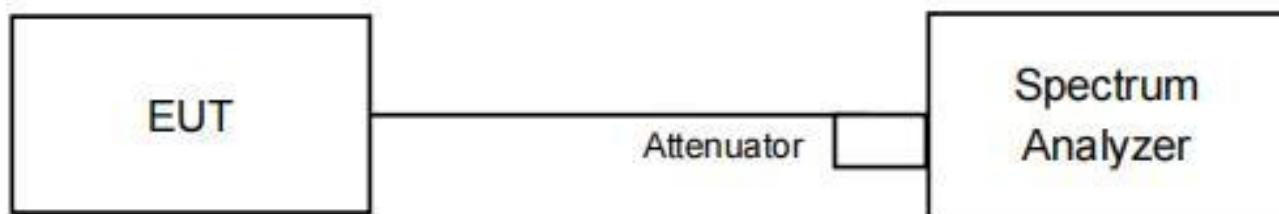
Frequency band(MHz)	Limit
5150-5250	$\leq 1\text{W}(30\text{dBm})$ for master device
	$\leq 250\text{mW}(24\text{dBm})$ for client device
5250-5350	$\leq 250\text{mW}(24\text{dBm})$ for client device or $11\text{dBm}+10\log B^*$
5470-5725	$\leq 250\text{mW}(24\text{dBm})$ for client device or $11\text{dBm}+10\log B^*$
5725-5850	$\leq 1\text{W}(30\text{dBm})$
Remark:	* Where B is the 26dB emission bandwidth in MHz. The maximum conducted output power must be measured over any interval of continuous transmission using instrumentation calibrated in terms of an rms-equivalent voltage.

Test Procedure:

Method SA-2 (trace averaging across on and off times of the EUT transmissions, followed by duty cycle correction).

- (1) Set RBW = 1 MHz.
- (2) Set VBW $\geq$ 3 MHz.
- (3) Detector = power average
- (4) Sweep time = auto.
- (5) Add duty cycle to the measured average power.

Test Setup Diagram



Measurement Data

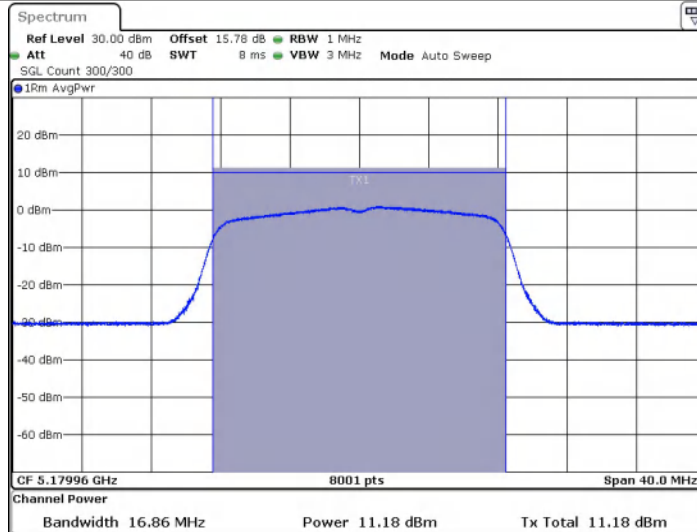
Ant1:

Test Mode	Antenna	Freq(MHz)	Result [dBm]	Limit [dBm]	Verdict	
11A	Ant1	5180	11.18	≤24	PASS	
		5200	10.91	≤24	PASS	
		5240	9.27	≤24	PASS	
		5260	11.08	≤24	PASS	
		5280	8.83	≤24	PASS	
		5320	10.35	≤24	PASS	
		5500	10.21	≤24	PASS	
		5580	8.35	≤24	PASS	
		5700	9.15	≤24	PASS	
		5745	7.54	≤30	PASS	
		5785	6.00	≤30	PASS	
		5825	5.71	≤30	PASS	
11N20SISO	Ant1	5180	11.00	≤24	PASS	
		5200	10.68	≤24	PASS	
		5240	9.08	≤24	PASS	
		5260	10.84	≤24	PASS	
		5280	8.60	≤24	PASS	
		5320	10.11	≤24	PASS	
		5500	9.76	≤24	PASS	
		5580	8.16	≤24	PASS	
		5700	9.14	≤24	PASS	
		5745	7.35	≤30	PASS	
		5785	5.84	≤30	PASS	
		5825	5.66	≤30	PASS	
11N40SISO	Ant1	5190	10.90	≤24	PASS	
		5230	8.47	≤24	PASS	
		5270	10.15	≤24	PASS	
		5310	9.57	≤24	PASS	
		5510	10.64	≤24	PASS	
		5550	9.57	≤24	PASS	
		5670	8.09	≤24	PASS	
		5755	5.45	≤30	PASS	
		5795	6.26	≤30	PASS	

11AC20SIS O	Ant1	5180	10.41	≤24	PASS	
		5200	9.83	≤24	PASS	
		5240	8.59	≤24	PASS	
		5260	10.52	≤24	PASS	
		5280	8.18	≤24	PASS	
		5320	9.85	≤24	PASS	
		5500	9.93	≤24	PASS	
		5580	8.17	≤24	PASS	
		5700	9.14	≤24	PASS	
		5745	7.41	≤30	PASS	
		5785	5.84	≤30	PASS	
		5825	5.65	≤30	PASS	
11AC40SIS O	Ant1	5190	10.48	≤24	PASS	
		5230	8.02	≤24	PASS	
		5270	9.59	≤24	PASS	
		5310	9.09	≤24	PASS	
		5510	10.63	≤24	PASS	
		5550	9.81	≤24	PASS	
		5670	8.36	≤24	PASS	
		5755	5.71	≤30	PASS	
		5795	6.49	≤30	PASS	
11AC80SIS O	Ant1	5210	9.33	≤24	PASS	
		5290	9.49	≤24	PASS	
		5530	10.32	≤24	PASS	
		5775	5.60	≤30	PASS	
11AX20SIS O	Ant1	5180	10.62	≤24	PASS	
		5200	10.21	≤24	PASS	
		5240	8.59	≤24	PASS	
		5260	10.55	≤24	PASS	
		5280	8.27	≤24	PASS	
		5320	10.00	≤24	PASS	
		5500	10.06	≤24	PASS	
		5580	8.38	≤24	PASS	
		5700	9.13	≤24	PASS	
		5745	7.66	≤30	PASS	
		5785	6.00	≤30	PASS	
		5825	5.64	≤30	PASS	

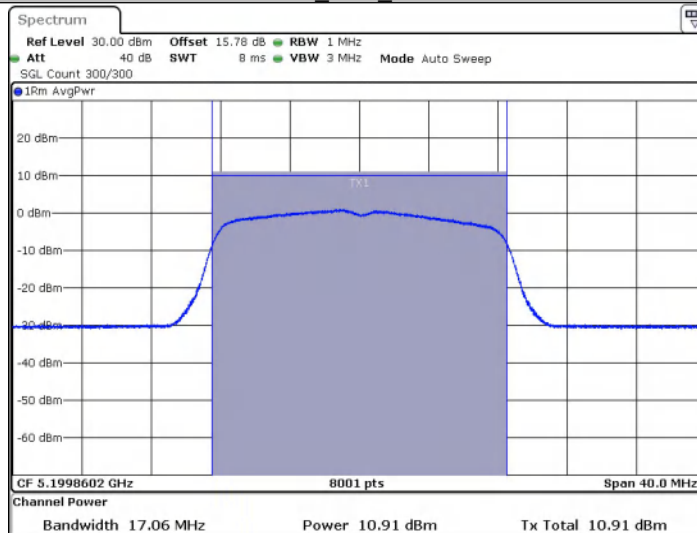
11AX40SIS O	Ant1	5190	10.40	≤24	PASS	
		5230	8.05	≤24	PASS	
		5270	9.72	≤24	PASS	
		5310	9.53	≤24	PASS	
		5510	10.92	≤24	PASS	
		5550	9.54	≤24	PASS	
		5670	7.85	≤24	PASS	
		5755	5.44	≤30	PASS	
		5795	6.40	≤30	PASS	
11AX80SIS O	Ant1	5210	8.92	≤24	PASS	
		5290	9.01	≤24	PASS	
		5530	10.16	≤24	PASS	
		5775	5.76	≤30	PASS	

11A_Ant1_5180



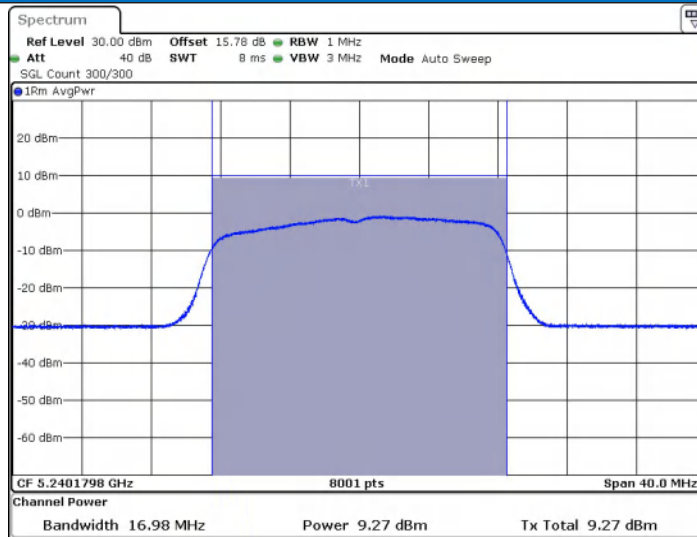
Date: 12 DEC 2025 16:53:26

11A_Ant1_5200



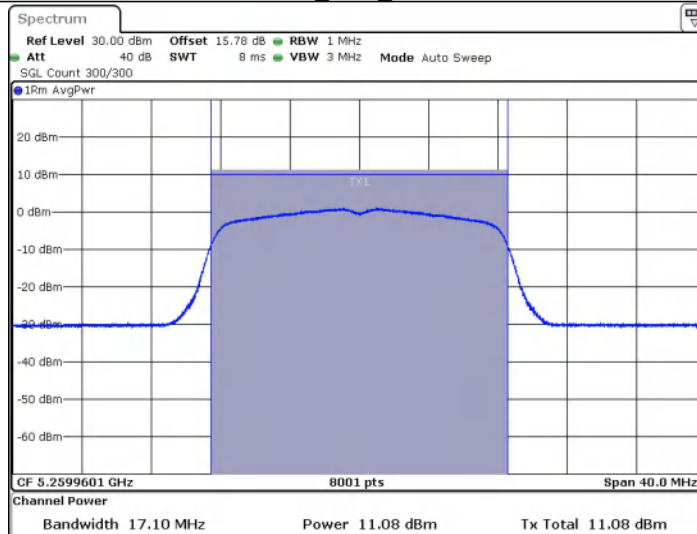
Date: 12 DEC 2025 16:56:38

11A_Ant1_5240



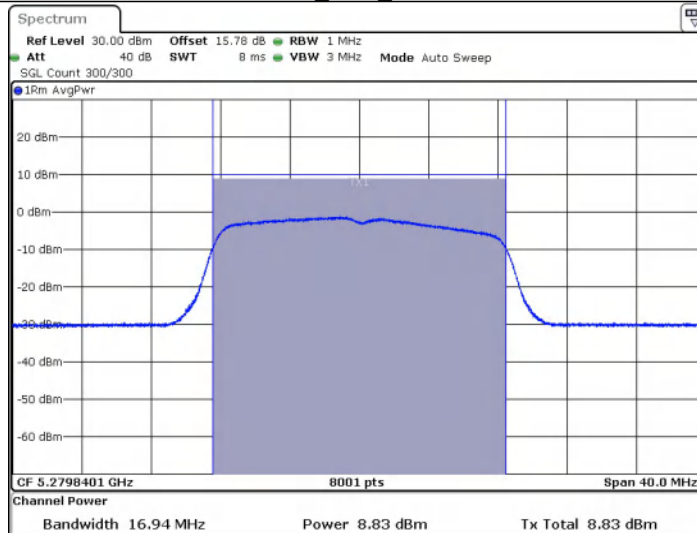
Date: 12 DEC 2025 16:57:44

11A_Ant1_5260



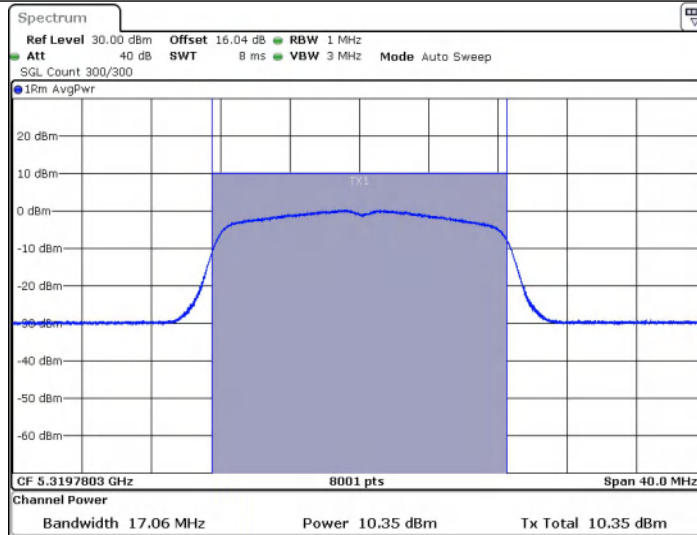
Date: 12 DEC 2025 17:01:16

11A_Ant1_5280



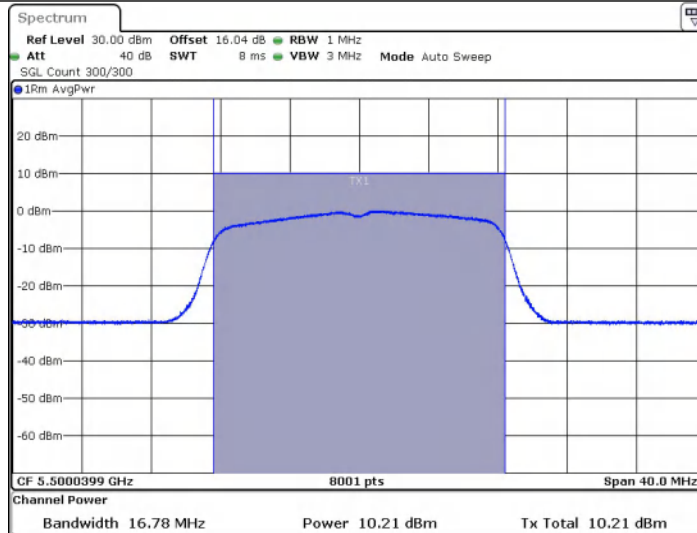
Date: 12 DEC 2025 17:02:40

11A_Ant1_5320



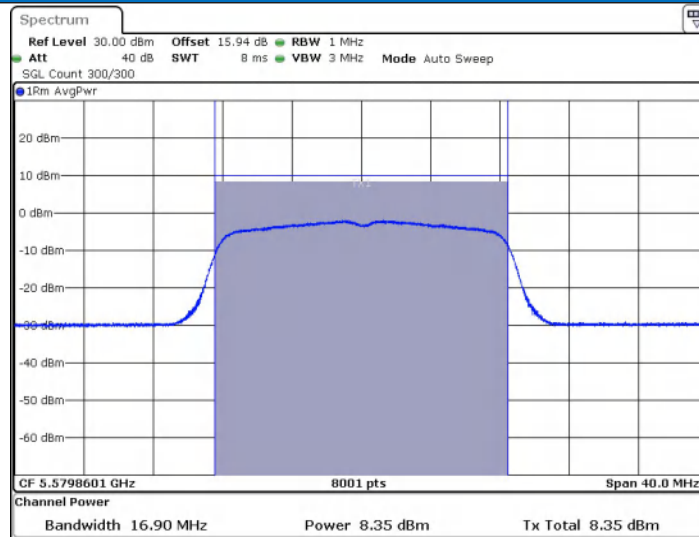
Date: 12 DEC 2025 17:04:12

11A_Ant1_5500



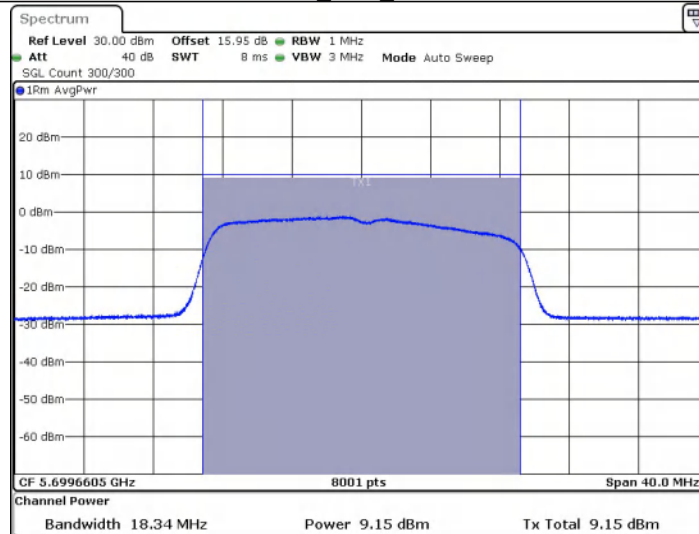
Date: 12 DEC 2025 17:07:18

11A_Ant1_5580



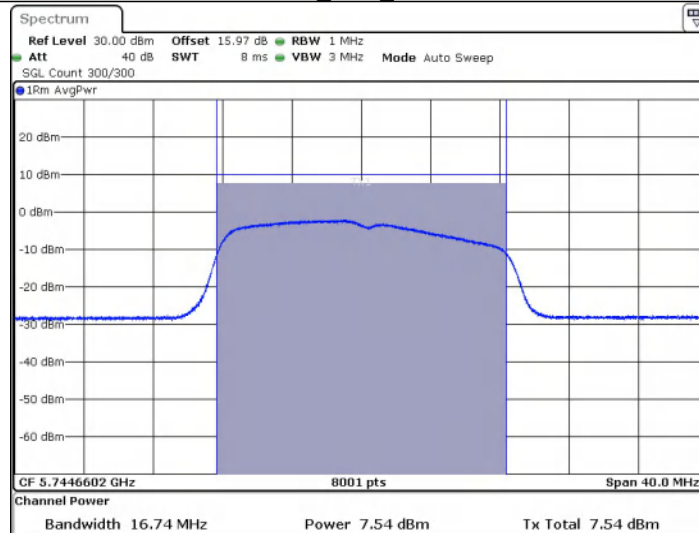
Date: 12 DEC 2025 17:14:06

11A_Ant1_5700



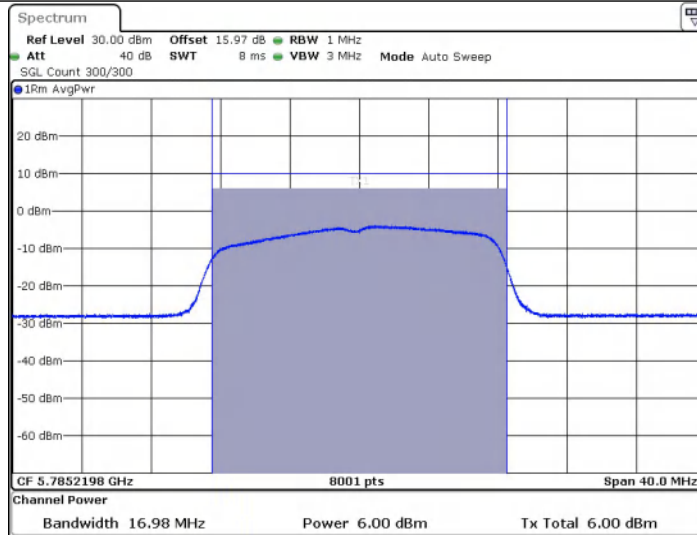
Date: 13 DEC 2025 15:46:28

11A_Ant1_5745



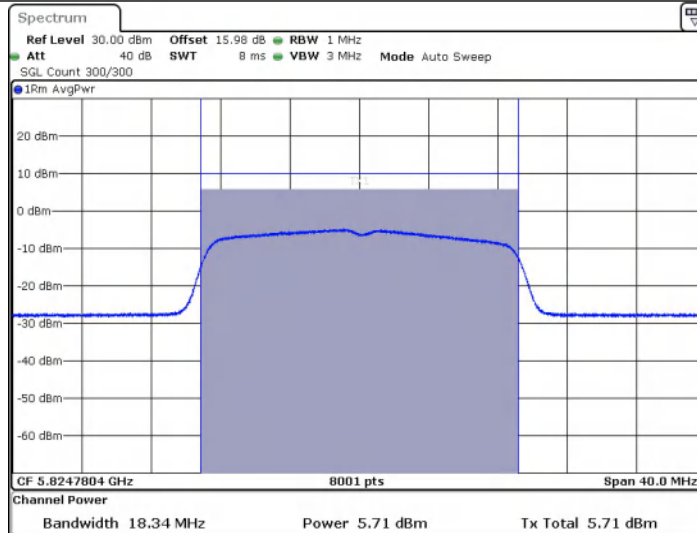
Date: 12 DEC 2025 17:17:20

11A_Ant1_5785



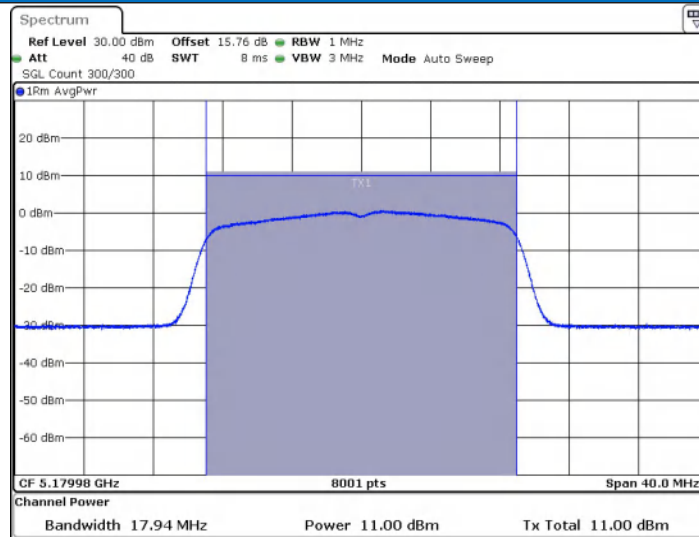
Date: 12 DEC 2025 17:21:24

11A_Ant1_5825



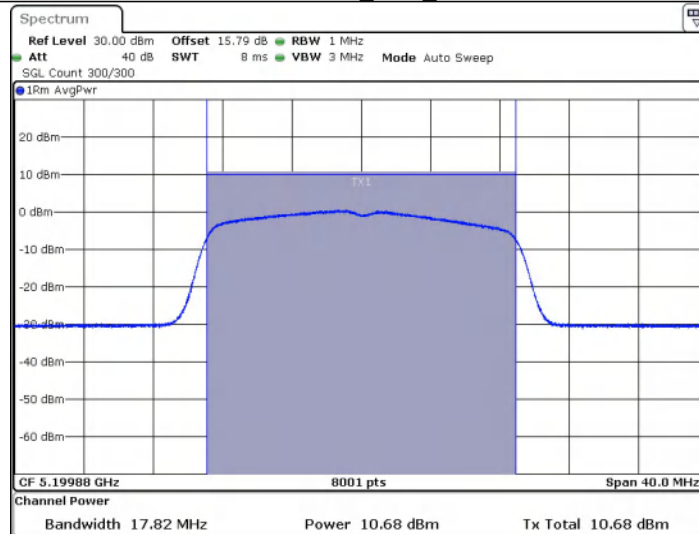
Date: 13 DEC 2025 15:53:57

11N20SISO_Ant1_5180



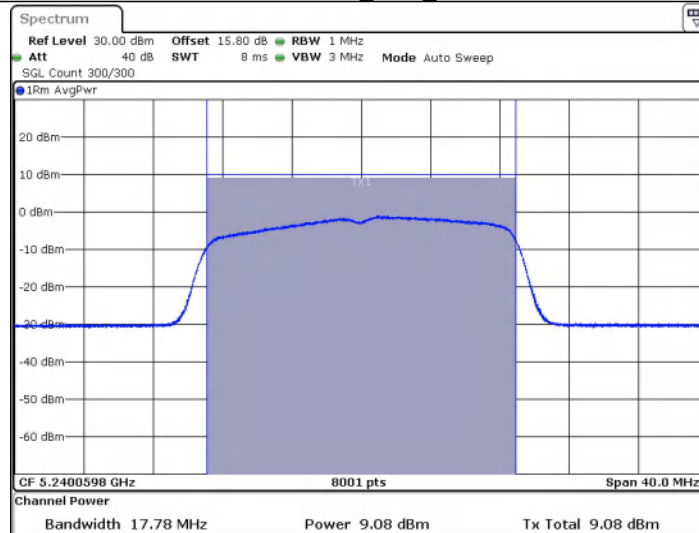
Date: 12.DEC.2025 17:25:39

11N20SISO_Ant1_5200



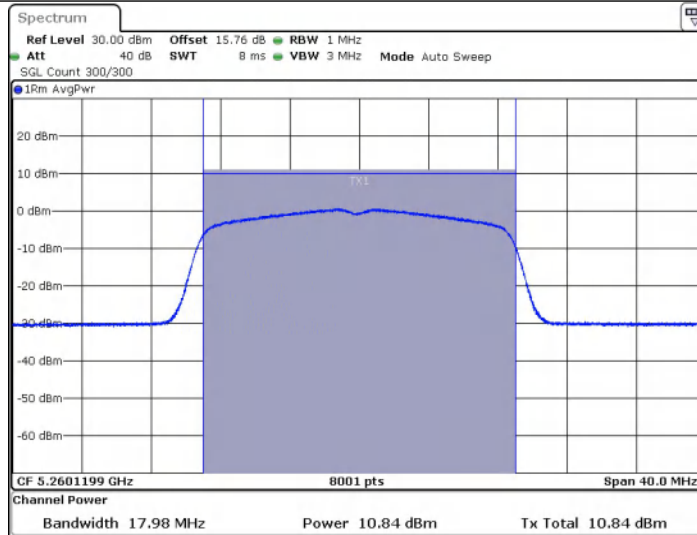
Date: 12.DEC.2025 17:27:45

11N20SISO_Ant1_5240



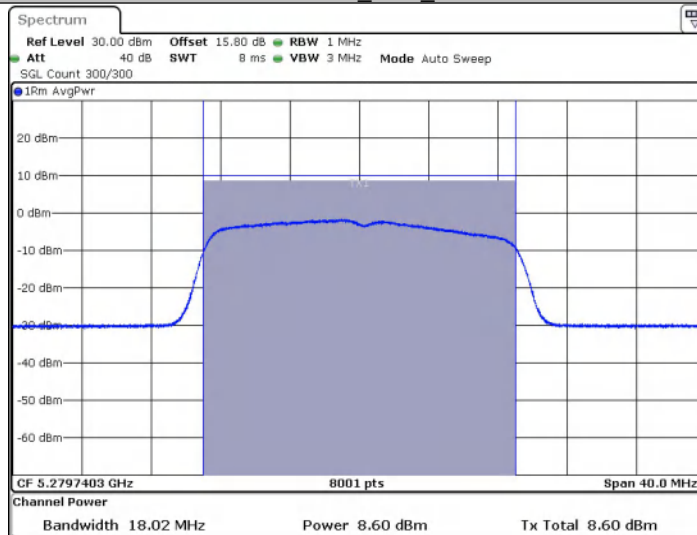
Date: 12.DEC.2025 17:29:04

11N20SISO_Ant1_5260



Date: 12 DEC 2025 17:31:05

11N20SISO_Ant1_5280



Date: 12 DEC 2025 17:32:52

11N20SISO_Ant1_5320