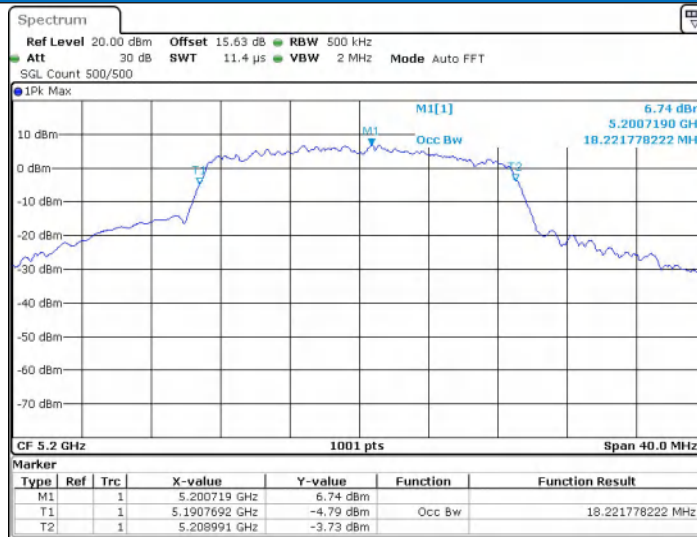
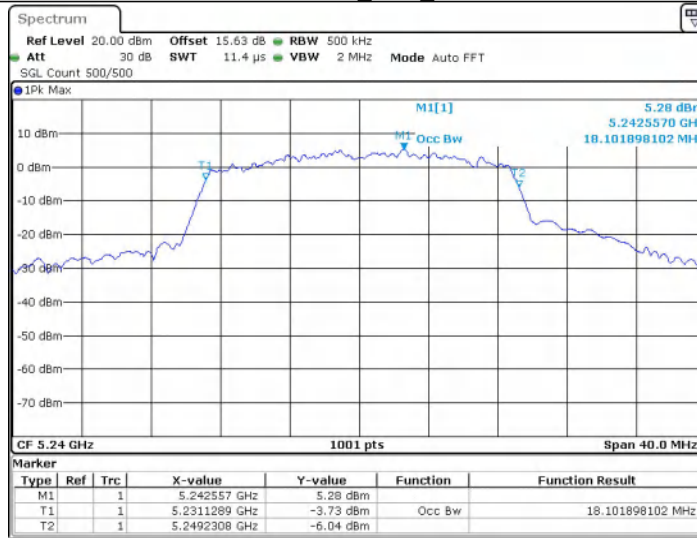
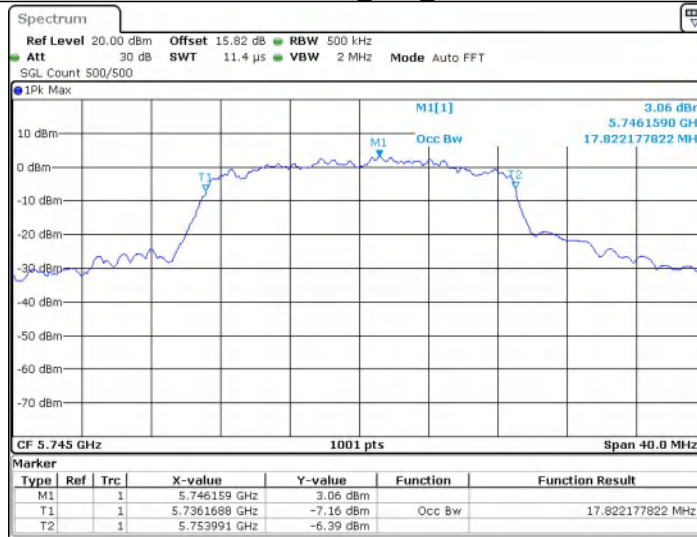




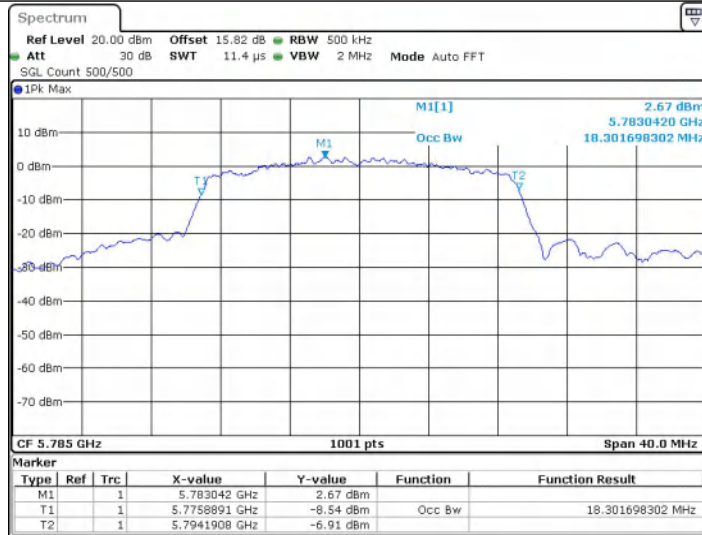
11N20SISO_Ant2_5240



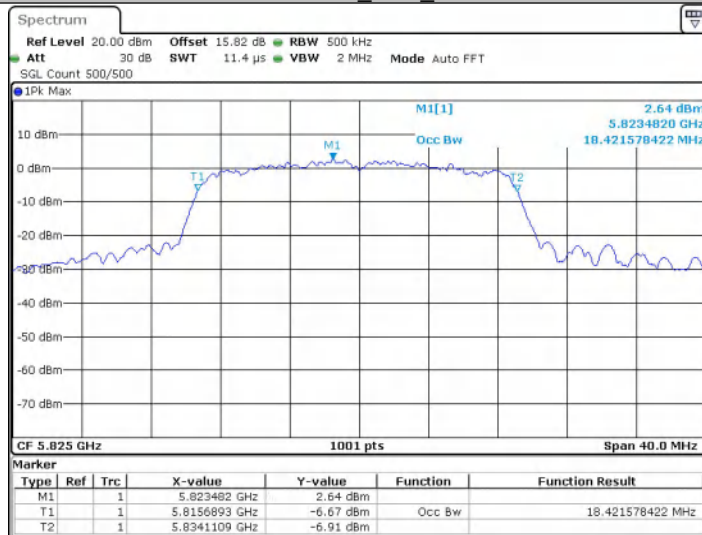
11N20SISO_Ant2_5745



11N20SISO_Ant2_5785



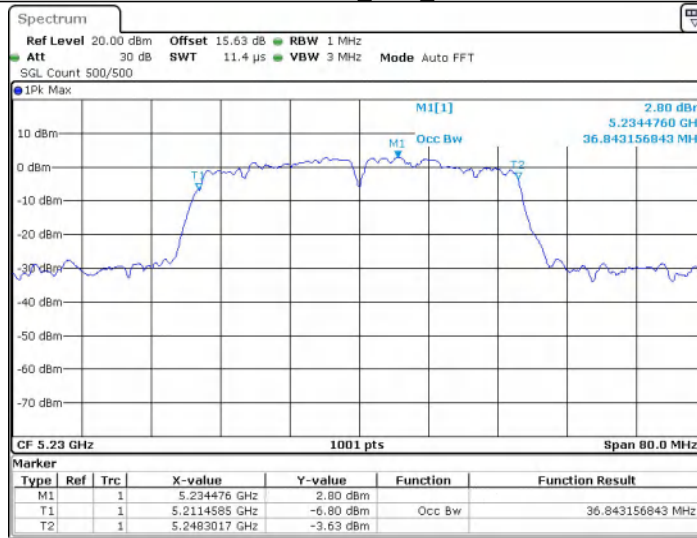
11N20SISO_Ant2_5825



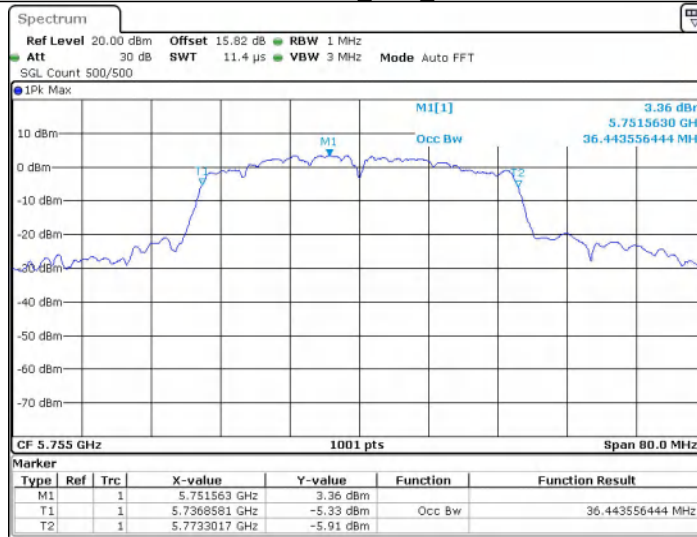
11N40SISO_Ant2_5190



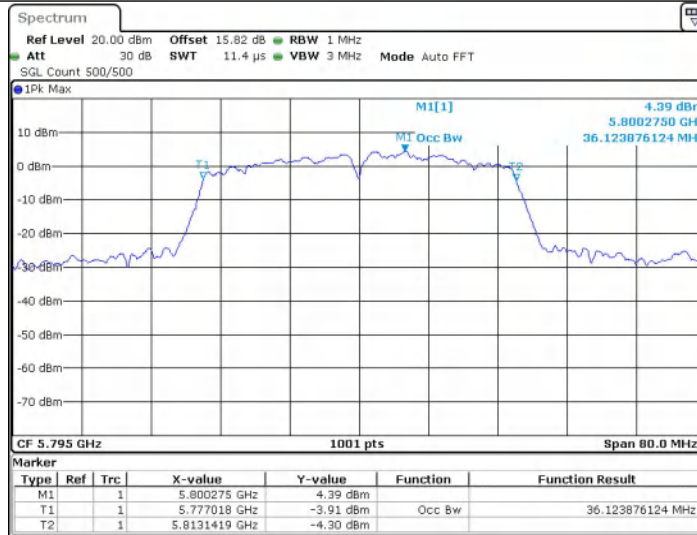
11N40SISO_Ant2_5230



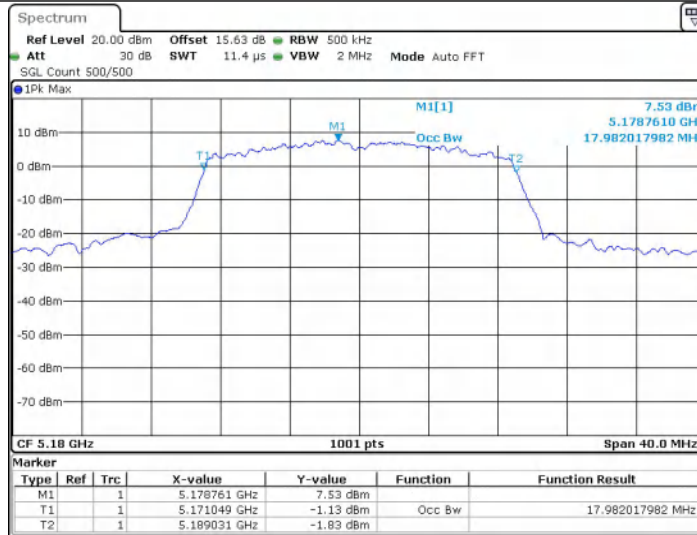
11N40SISO_Ant2_5755



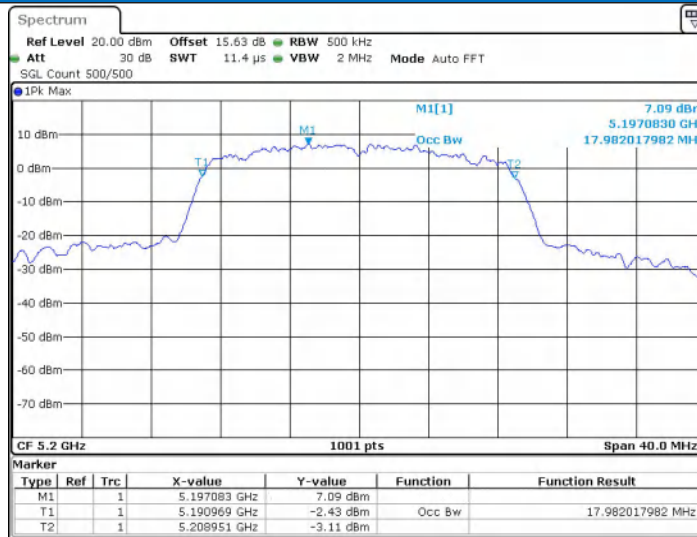
11N40SISO_Ant2_5795



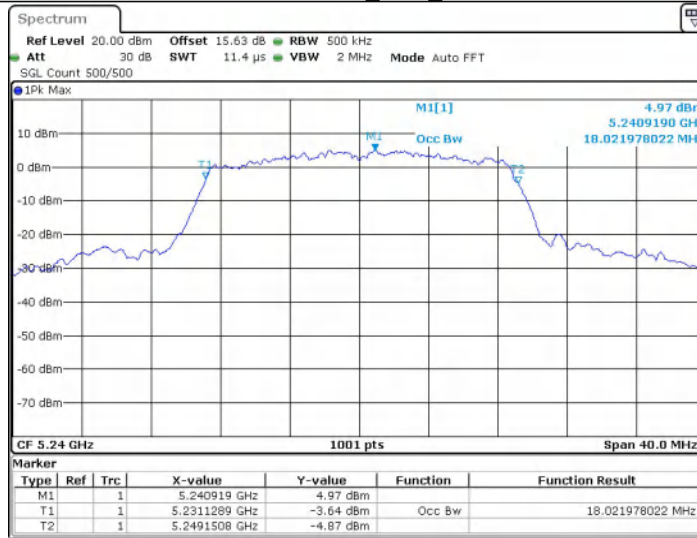
11AC20SISO_Ant2_5180



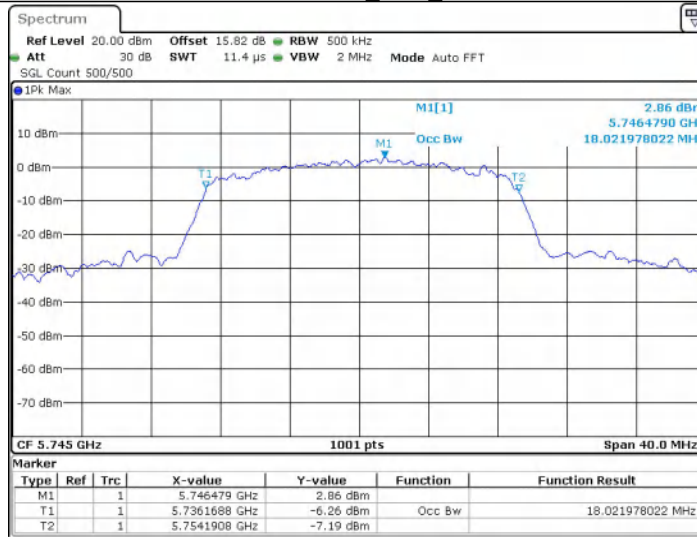
11AC20SISO_Ant2_5200



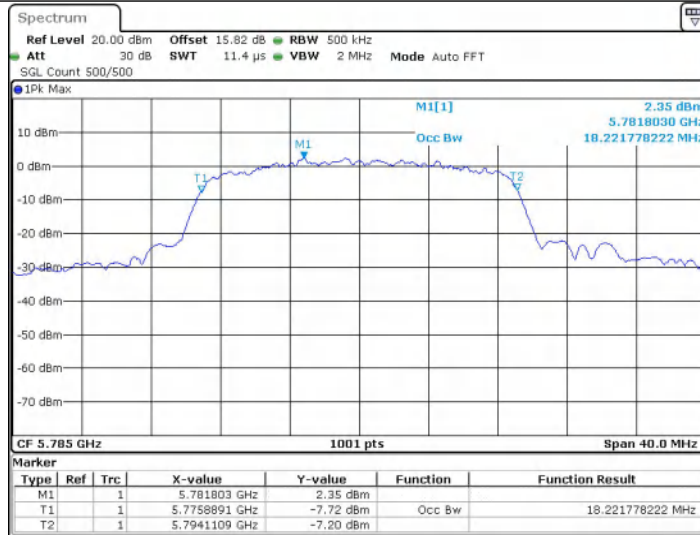
11AC20SISO_Ant2_5240



11AC20SISO_Ant2_5745

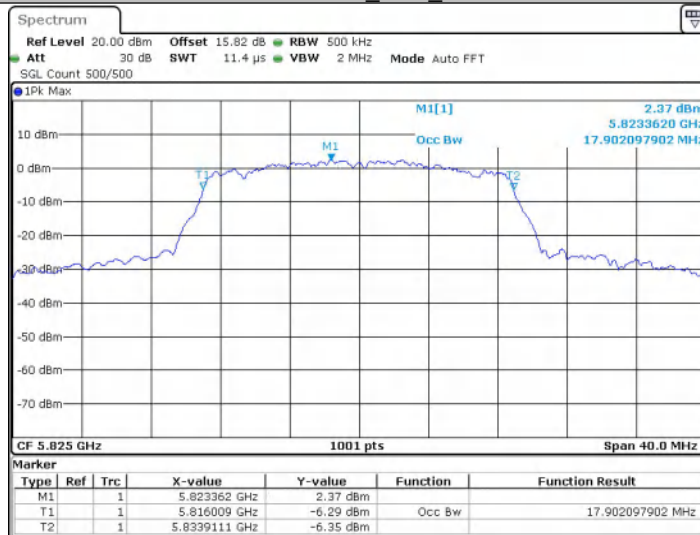


11AC20SISO_Ant2_5785



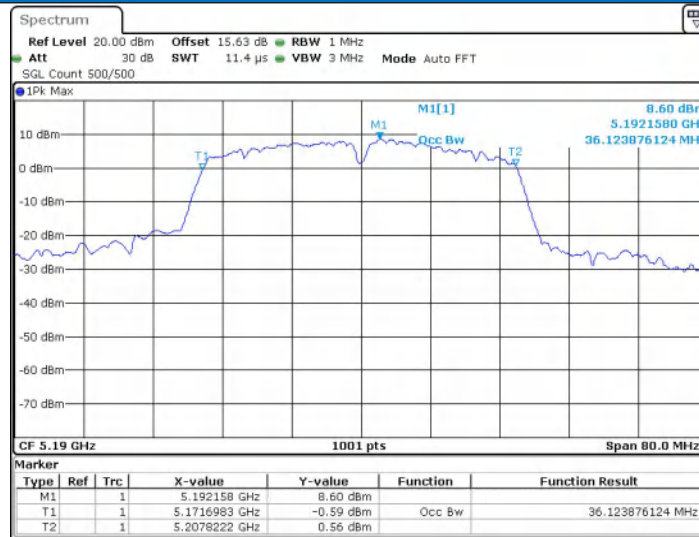
Date: 24 DEC 2025 20:38:51

11AC20SISO_Ant2_5825

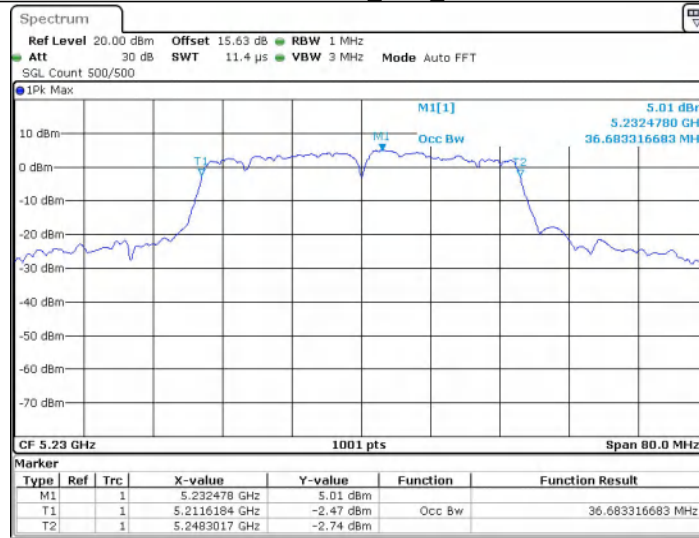


Date: 24 DEC 2025 20:40:07

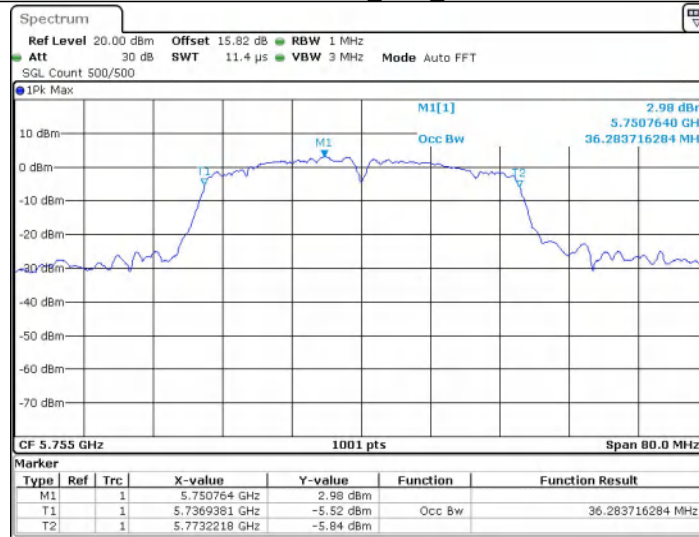
11AC40SISO_Ant2_5190



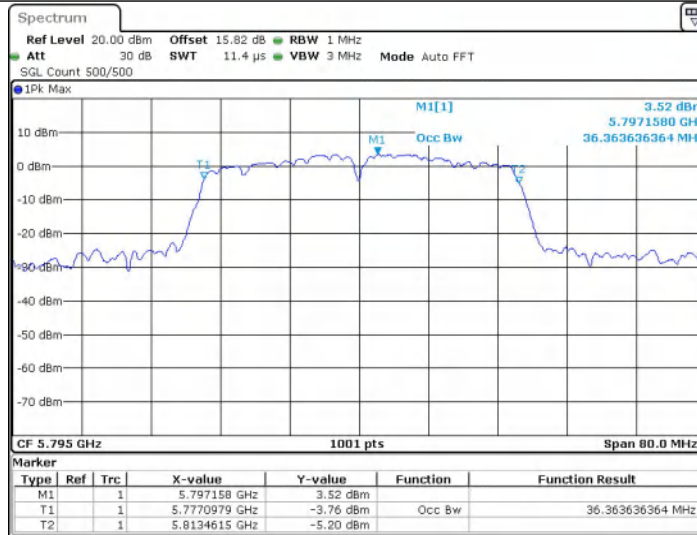
11AC40SISO_Ant2_5230



11AC40SISO_Ant2_5755

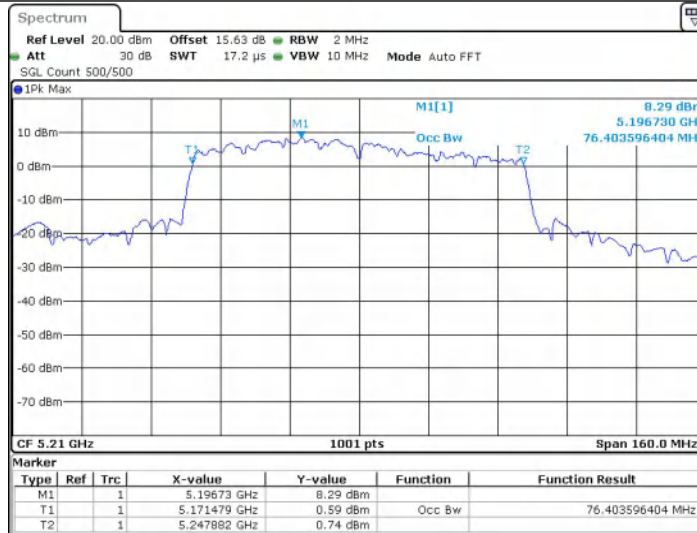


11AC40SISO_Ant2_5795



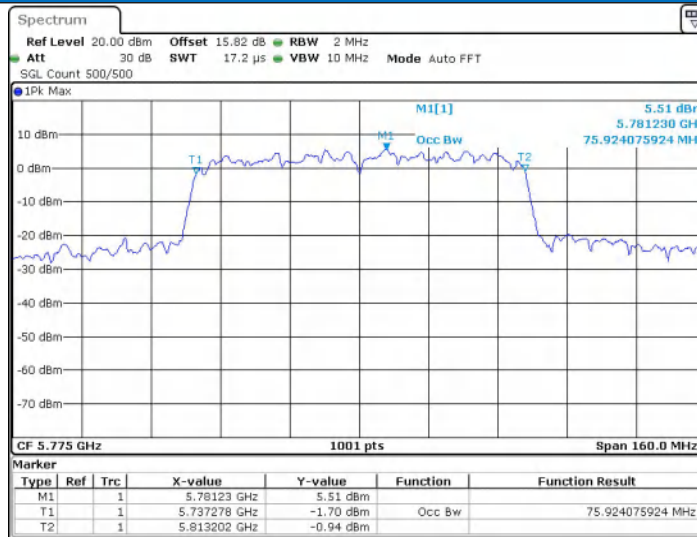
Date: 24 DEC 2025 20:48:25

11AC80SISO_Ant2_5210



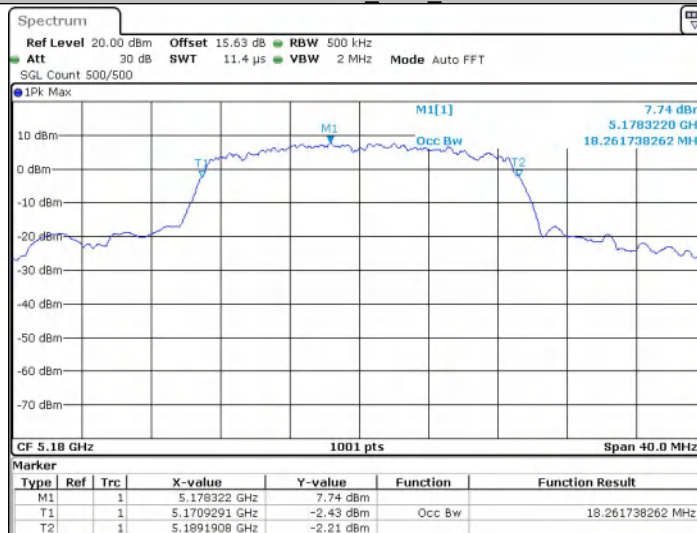
Date: 25 DEC 2025 10:43:01

11AC80SISO_Ant2_5775



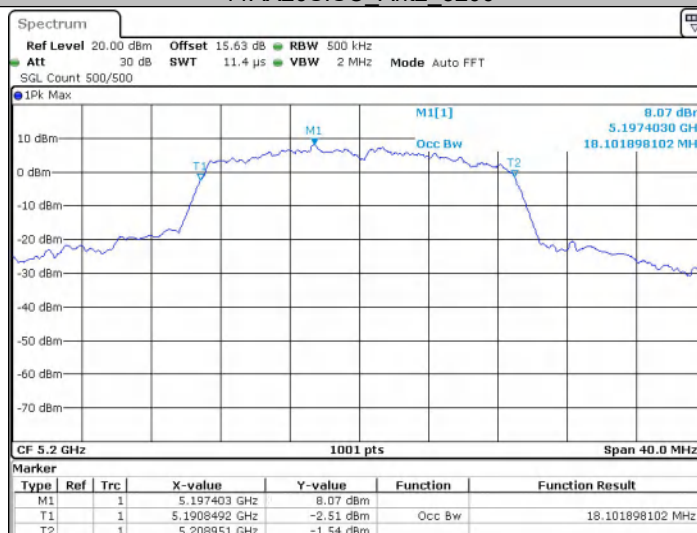
Date: 25 DEC 2025 10:46:13

11AX20SISO_Ant2_5180



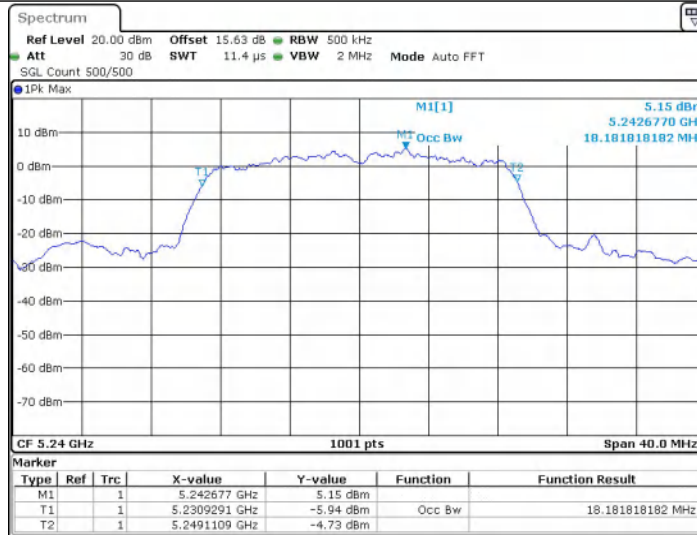
Date: 25 DEC 2025 10:48:17

11AX20SISO_Ant2_5200



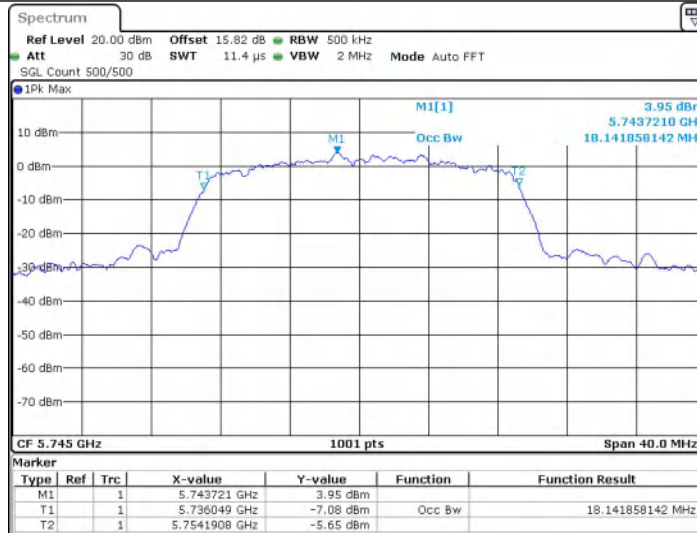
Date: 25 DEC 2025 10:50:33

11AX20SISO_Ant2_5240



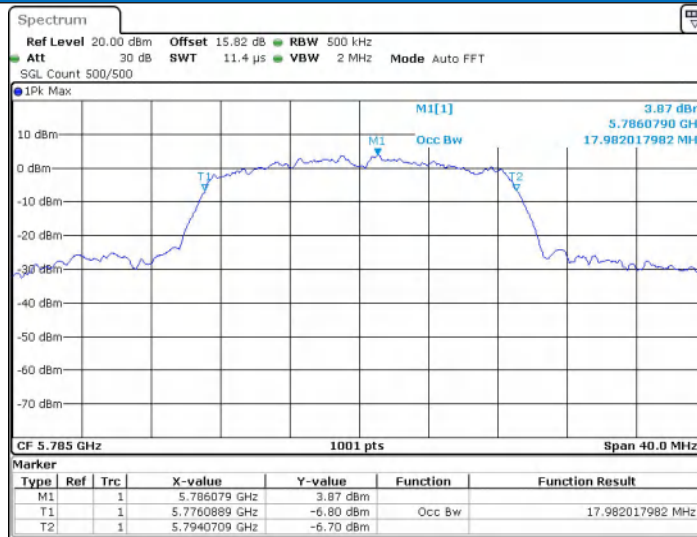
Date: 25 DEC 2025 10:51:45

11AX20SISO_Ant2_5745

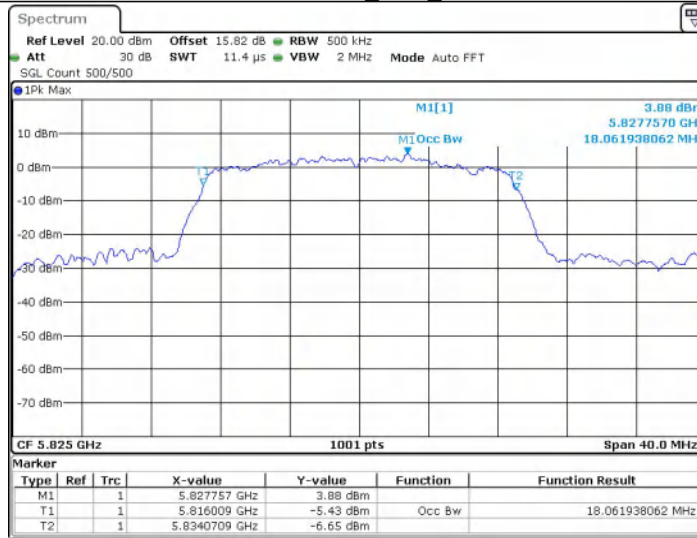


Date: 25 DEC 2025 10:53:33

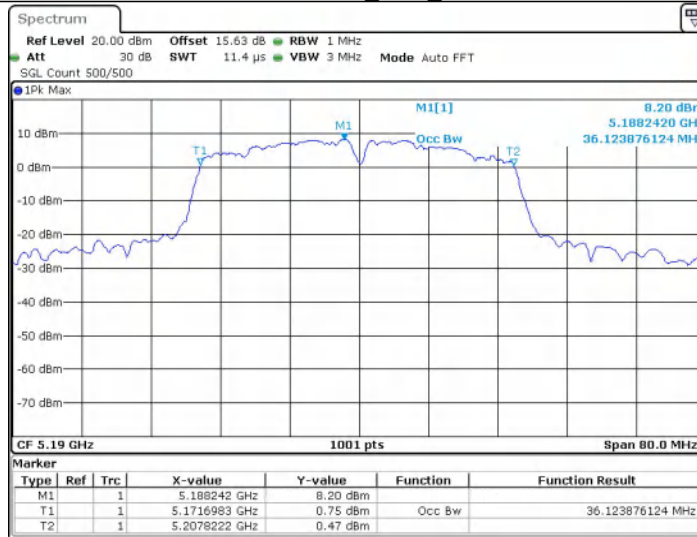
11AX20SISO_Ant2_5785



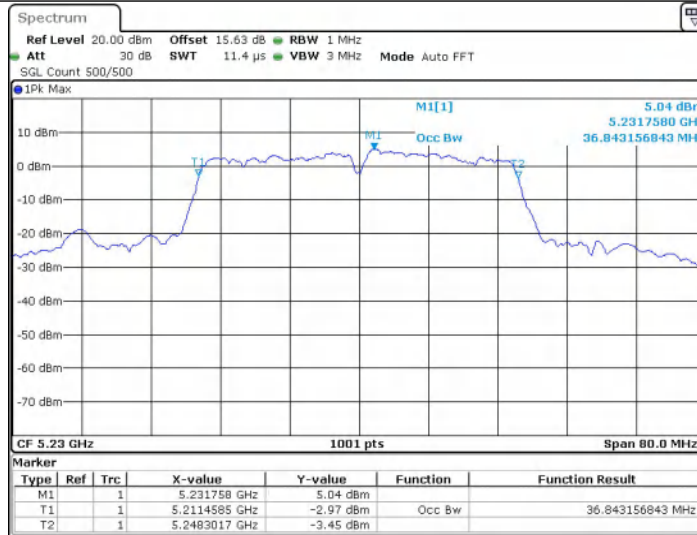
11AX20SISO_Ant2_5825



11AX40SISO_Ant2_5190

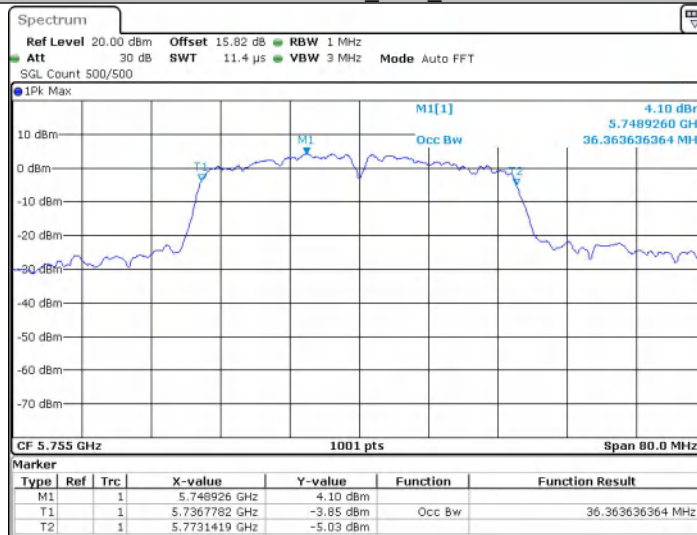


11AX40SISO_Ant2_5230



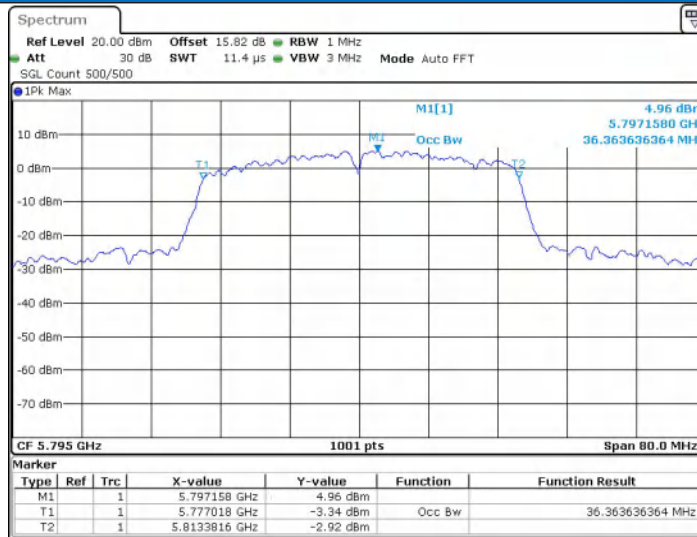
Date: 25 DEC 2025 11:03:29

11AX40SISO_Ant2_5755



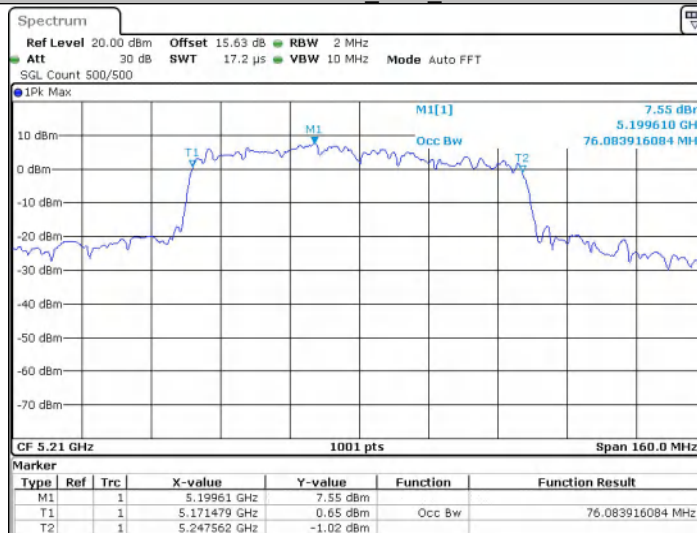
Date: 25 DEC 2025 11:05:22

11AX40SISO_Ant2_5795



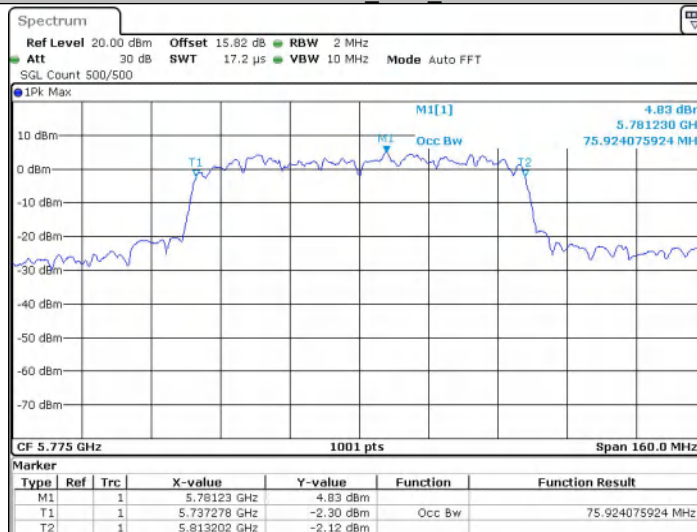
Date: 25 DEC 2025 11:09:13

11AX80SISO_Ant2_5210



Date: 25 DEC 2025 11:11:27

11AX80SISO_Ant2_5775



Date: 25 DEC 2025 11:14:12

Appendix B): Maximum Conduct Output Power

1.Duty Cycle (x)

Test Requirement KDB 789033 D02 II B 1

Test Method: KDB 789033 II B 1

Test Procedure:

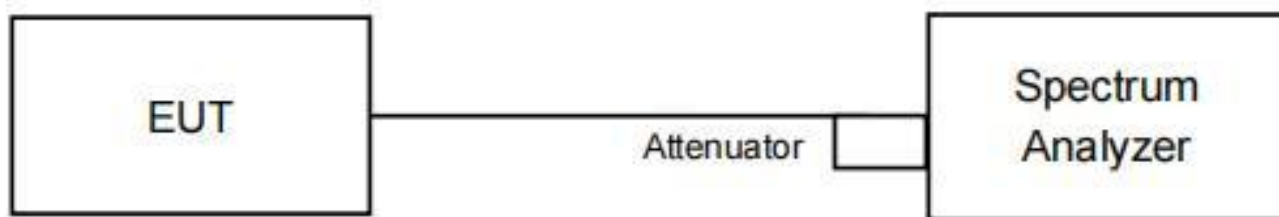
Set RBW = 20MHz

Set VBW = 40MHz

Set detector = peak.

Set span =0Hz

Test Setup Diagram

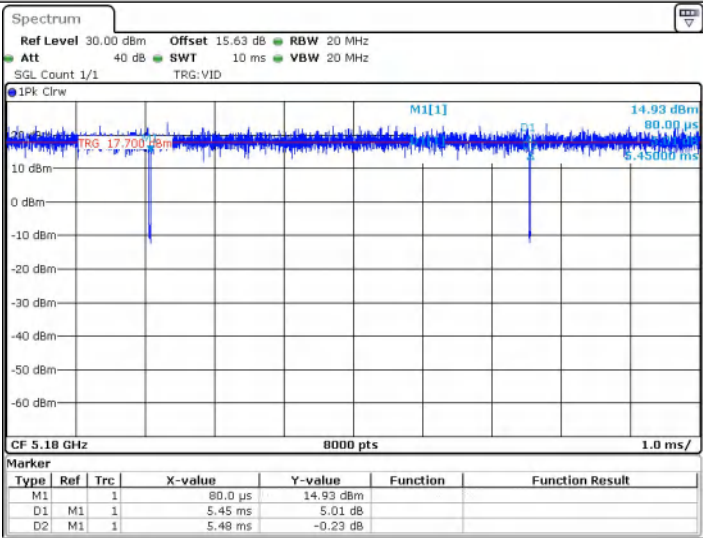


Measurement Data

ANT1:

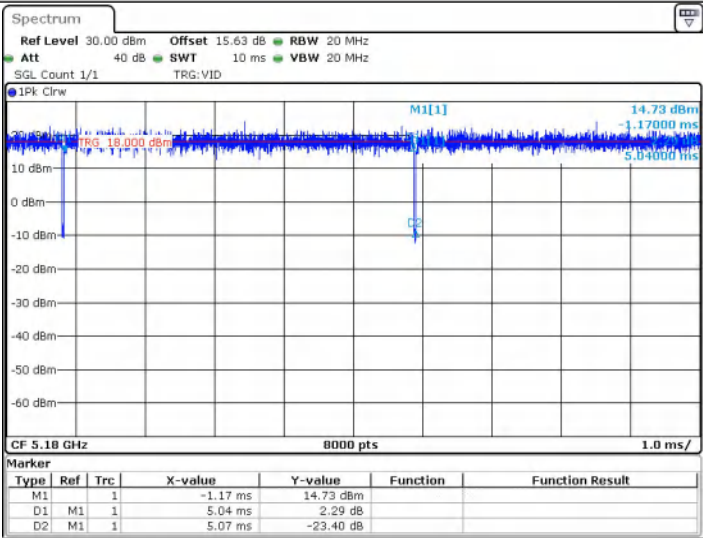
Test Mode	Antenna	Duty Cycle[%]	10log(1/x) Factor[dB]
11A	Ant1	99.45	0.02
11N20	Ant1	99.41	0.03
11N40	Ant1	99.19	0.04
11AC20	Ant1	99.41	0.03
11AC40	Ant1	98.79	0.05
11AC80	Ant1	88.89	0.51
11AX20	Ant1	96.30	0.16
11AX40	Ant1	92.86	0.32
11AX80	Ant1	86.49	0.63

11A



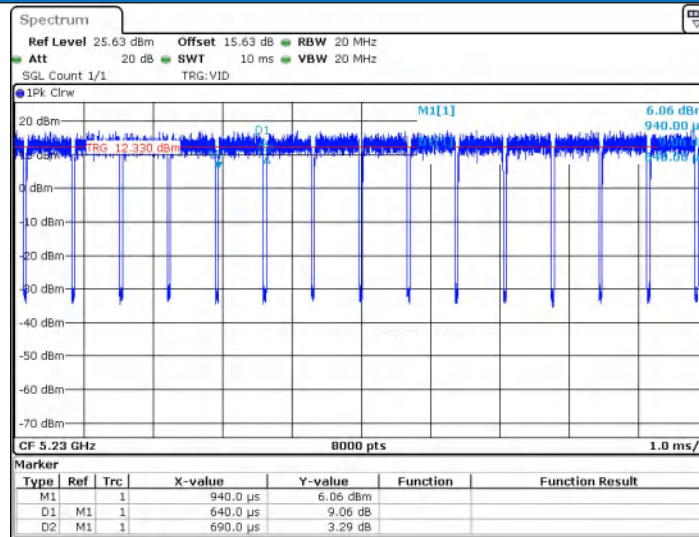
Date: 23 DEC 2025 17:04:28

11N20



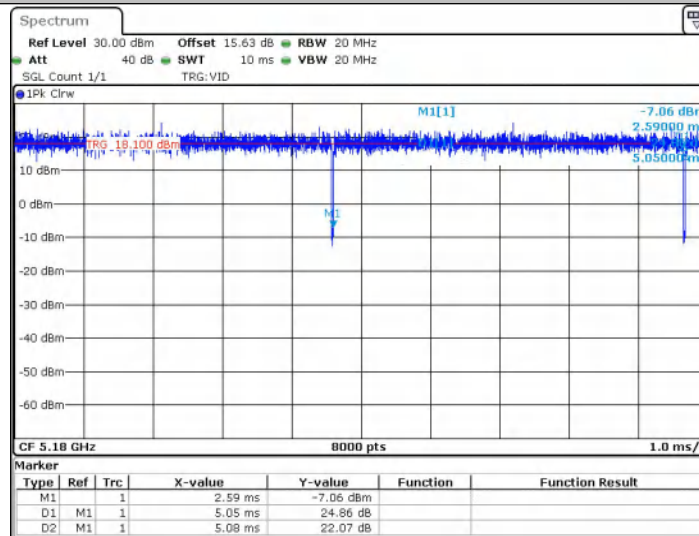
Date: 23 DEC 2025 17:31:56

11N40



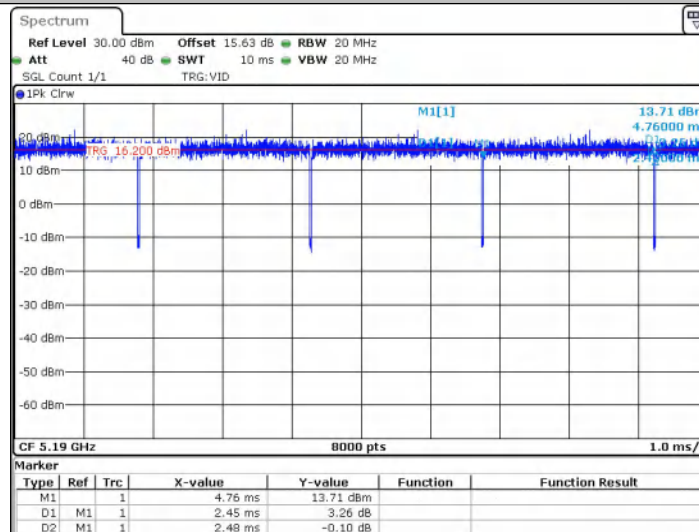
Date: 25 DEC 2025 14:39:12

11AC20



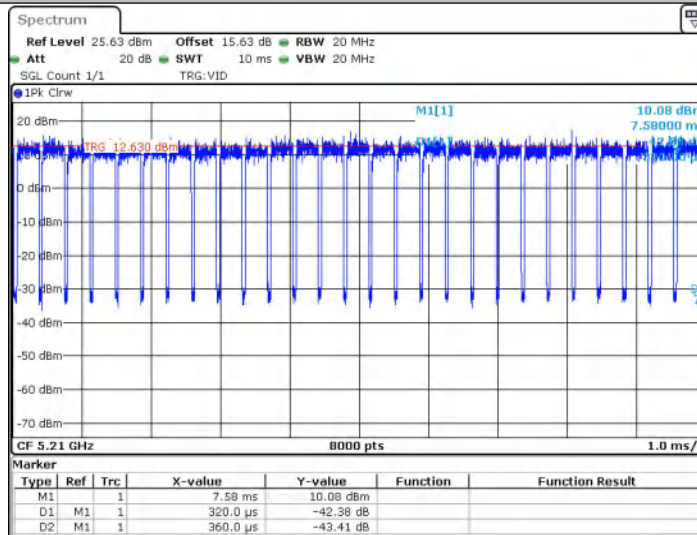
Date: 23 DEC 2025 18:40:36

11AC40



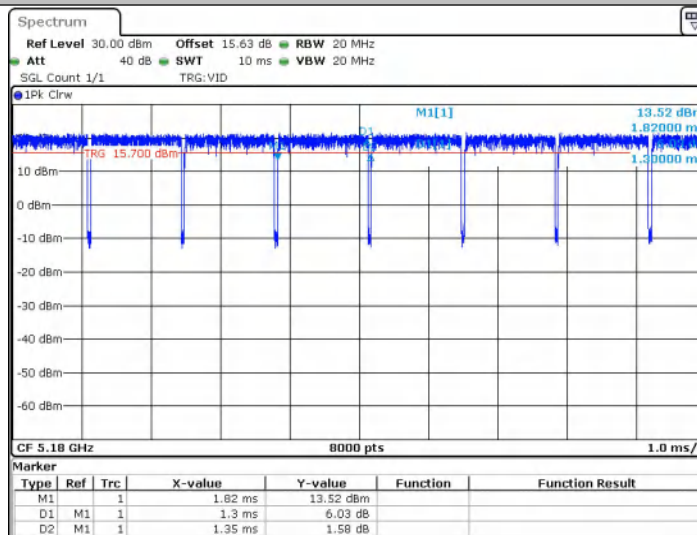
Date: 23 DEC 2025 18:53:38

11AC80



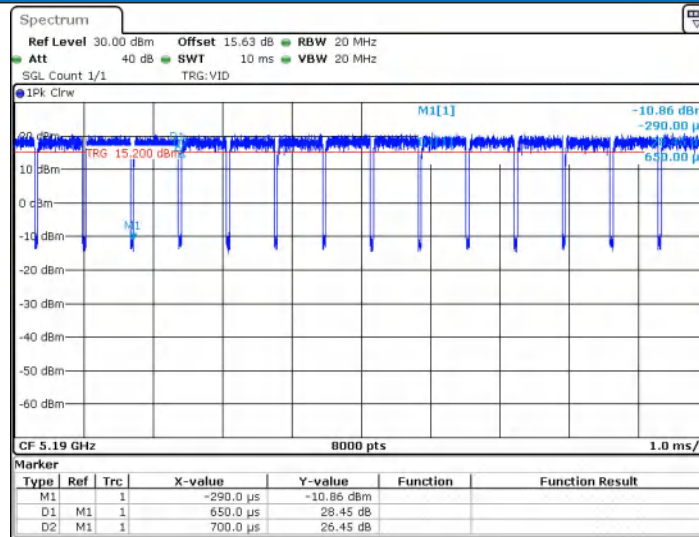
Date: 25 DEC 2025 11:46:50

11AX20



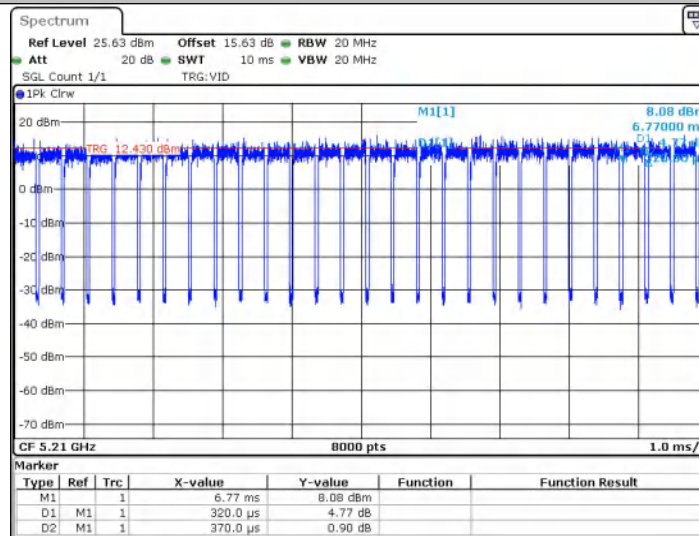
Date: 24 DEC 2025 17:31:29

11AX40



Date: 24 DEC 2025 17:54:10

11AX80

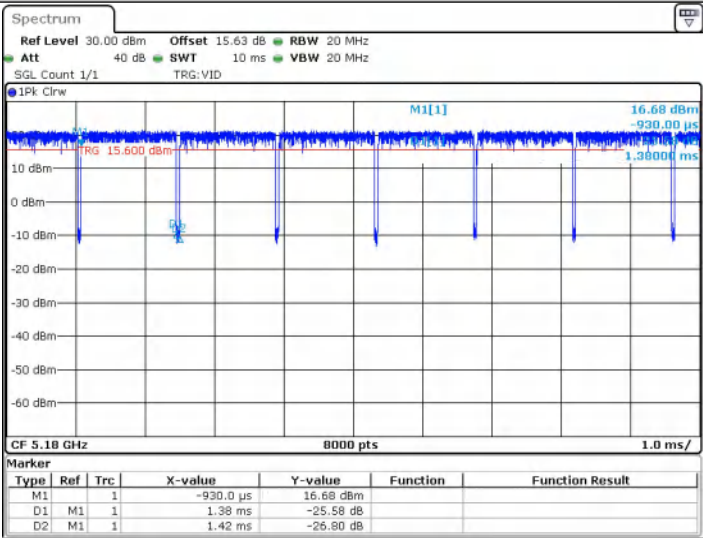


Date: 25 DEC 2025 11:56:56

ANT2:

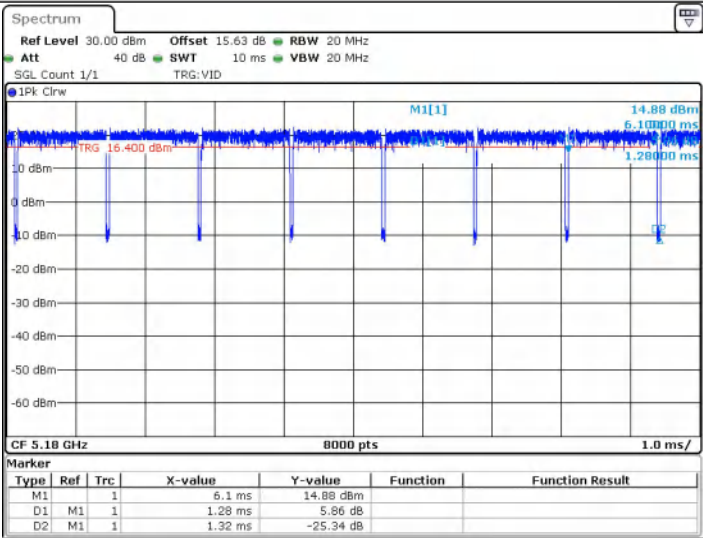
Test Mode	Antenna	Duty Cycle[%]	10log(1/x) Factor[dB]
11A	Ant1	97.18	0.12
11N20	Ant1	96.97	0.13
11N40	Ant1	92.75	0.33
11AC20	Ant1	96.30	0.16
11AC40	Ant1	94.20	0.26
11AC80	Ant1	88.89	0.51
11AX20	Ant1	96.30	0.16
11AX40	Ant1	92.75	0.33
11AX80	Ant1	86.49	0.63

11A



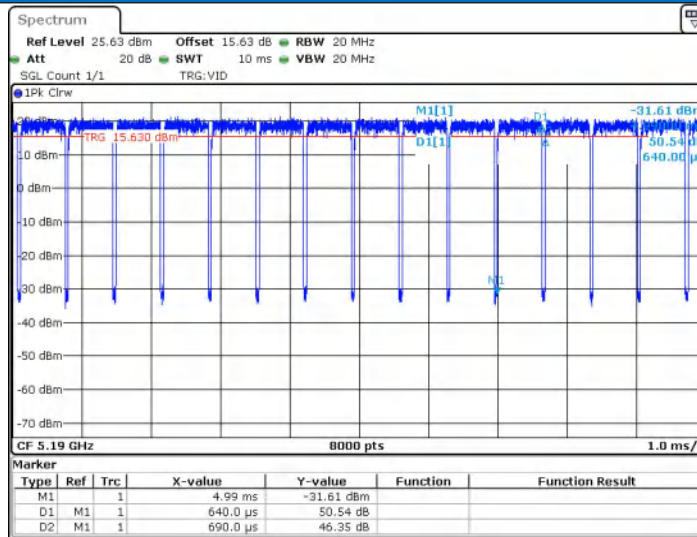
Date: 24 DEC 2025 19:37:19

11N20



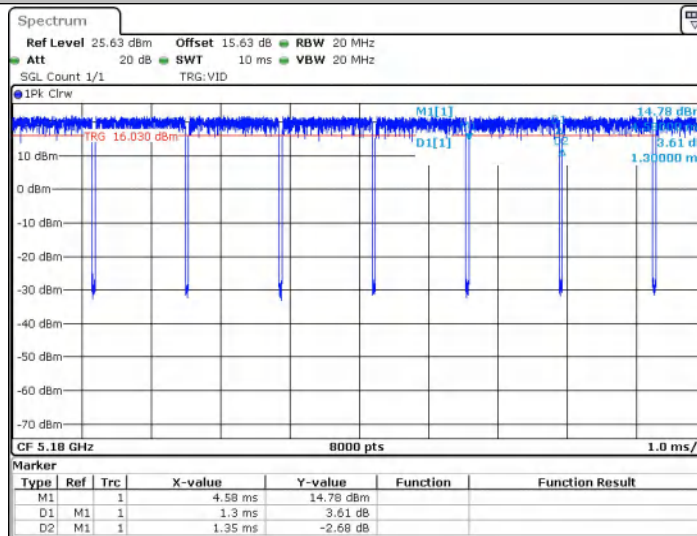
Date: 24 DEC 2025 19:52:57

11N40



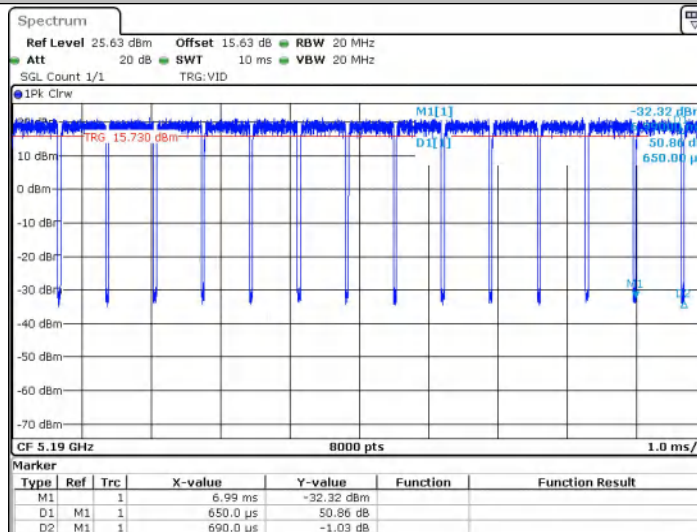
Date: 24 DEC 2025 20:20:38

11AC20



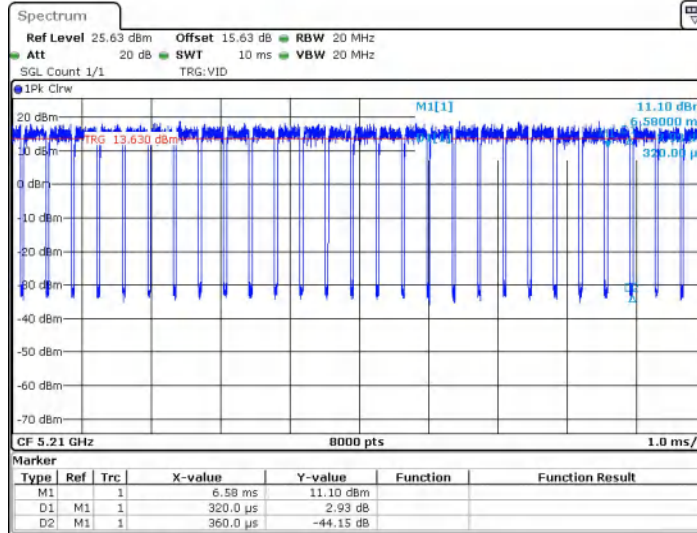
Date: 24 DEC 2025 20:30:30

11AC40



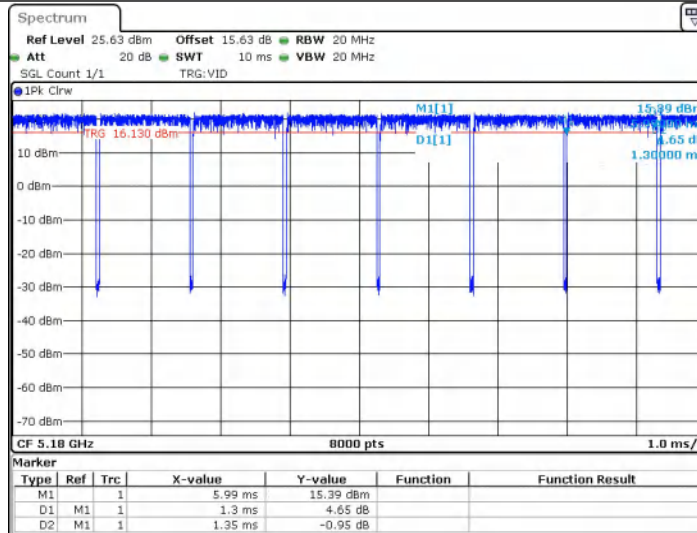
Date: 24 DEC 2025 20:41:52

11AC80



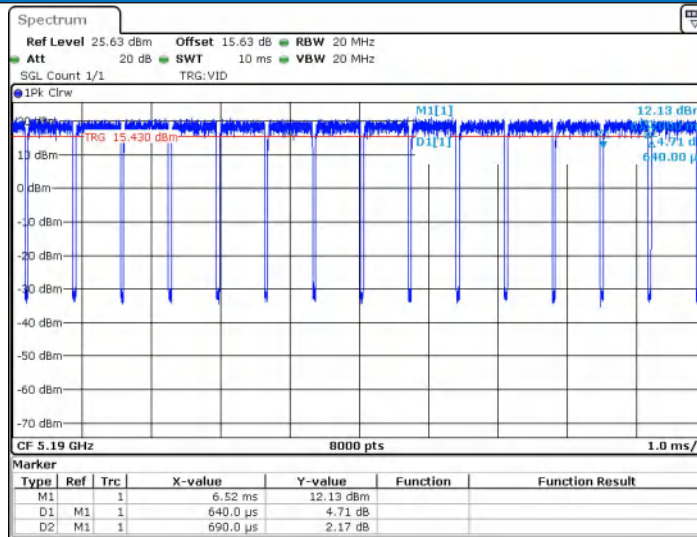
Date: 25 DEC 2025 10:43:13

11AX20



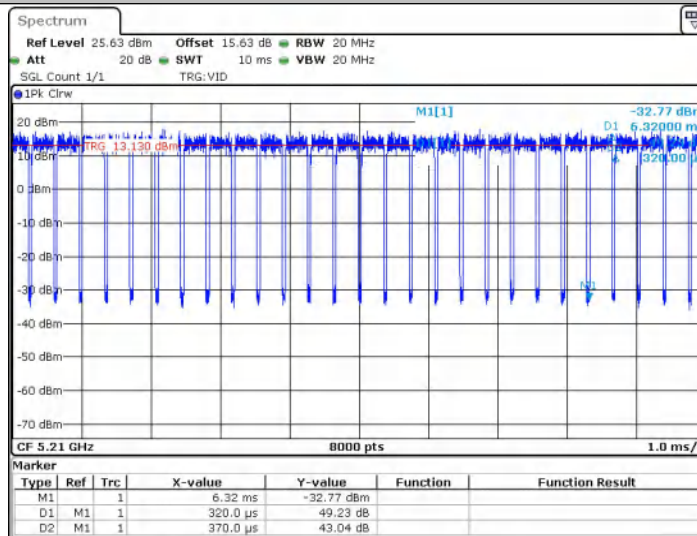
Date: 25 DEC 2025 10:48:29

11AX40



Date: 25 DEC 2025 11:00:40

11AX80



Date: 25 DEC 2025 11:11:40

2. Maximum Conducted Output Power

Test Requirement 47 CFR Part 15, Subpart C 15.407 (a)

Test Method: KDB 789033 D02 II E

Limit:

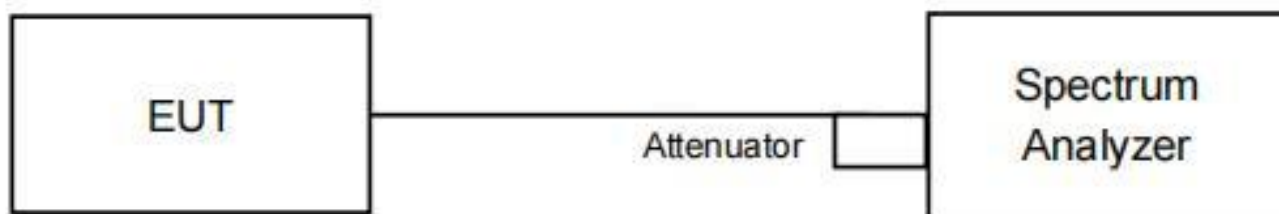
Frequency band(MHz)	Limit
5150-5250	$\leq 1\text{W}(30\text{dBm})$ for master device
	$\leq 250\text{mW}(24\text{dBm})$ for client device
5250-5350	$\leq 250\text{mW}(24\text{dBm})$ for client device or $11\text{dBm}+10\log B^*$
5470-5725	$\leq 250\text{mW}(24\text{dBm})$ for client device or $11\text{dBm}+10\log B^*$
5725-5850	$\leq 1\text{W}(30\text{dBm})$
Remark:	* Where B is the 26dB emission bandwidth in MHz. The maximum conducted output power must be measured over any interval of continuous transmission using instrumentation calibrated in terms of an rms-equivalent voltage.

Test Procedure:

Method SA-2 (trace averaging across on and off times of the EUT transmissions, followed by duty cycle correction).

- (1) Set RBW = 1 MHz.
- (2) Set VBW ≥ 3 MHz.
- (3) Detector = power average
- (4) Sweep time = auto.
- (5) Add duty cycle to the measured average power.

Test Setup Diagram



Measurement Data

Ant1:

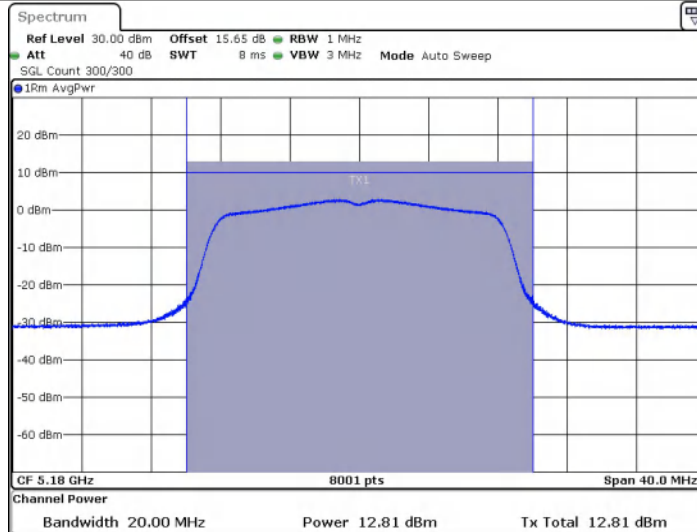
Test Mode	Antenna	Freq(MHz)	Result [dBm]	Limit [dBm]	Verdict
11A	Ant1	5180	12.81	≤23.98	PASS
		5200	12.62	≤23.98	PASS
		5240	11.20	≤23.98	PASS
		5745	10.61	≤30.00	PASS
		5785	8.59	≤30.00	PASS
		5825	8.77	≤30.00	PASS
11N20SISO	Ant1	5180	12.69	≤23.98	PASS
		5200	12.36	≤23.98	PASS
		5240	11.03	≤23.98	PASS
		5745	10.28	≤30.00	PASS
		5785	8.31	≤30.00	PASS
		5825	8.61	≤30.00	PASS
11N40SISO	Ant1	5190	11.77	≤23.98	PASS
		5230	8.61	≤23.98	PASS
		5755	9.05	≤30.00	PASS
		5795	8.71	≤30.00	PASS
11AC20SISO	Ant1	5180	12.86	≤23.98	PASS
		5200	12.45	≤23.98	PASS
		5240	11.14	≤23.98	PASS
		5745	10.42	≤30.00	PASS
		5785	8.44	≤30.00	PASS
		5825	8.71	≤30.00	PASS
11AC40SISO	Ant1	5190	11.89	≤23.98	PASS
		5230	10.17	≤23.98	PASS
		5755	9.00	≤30.00	PASS
		5795	8.90	≤30.00	PASS
11AC80SISO	Ant1	5210	10.25	≤23.98	PASS
		5775	9.24	≤30.00	PASS
11AX20SISO	Ant1	5180	14.10	≤23.98	PASS
		5200	13.21	≤23.98	PASS
		5240	11.09	≤23.98	PASS
		5745	9.18	≤30.00	PASS
		5785	9.16	≤30.00	PASS

		5825	9.51	≤30.00	PASS
11AX40SIS O	Ant1	5190	13.61	≤23.98	PASS
		5230	7.67	≤23.98	PASS
		5755	9.12	≤30.00	PASS
		5795	10.10	≤30.00	PASS
11AX80SIS O	Ant1	5210	9.63	≤23.98	PASS
		5775	6.81	≤30.00	PASS

Note:

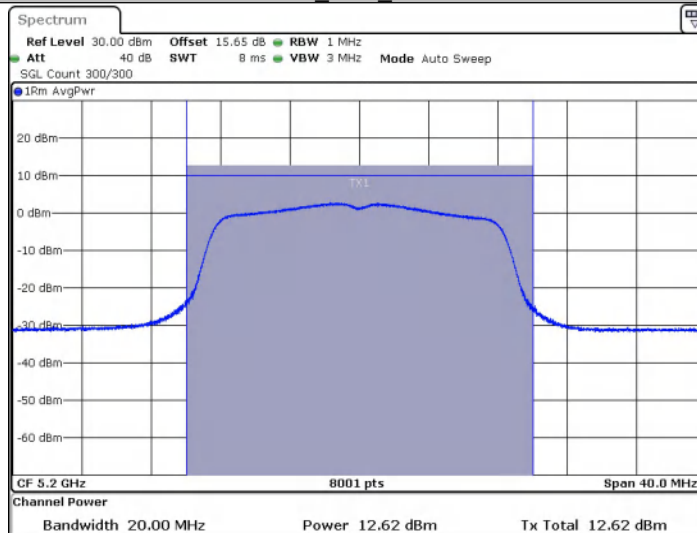
Transmitting in full-bandwidth single-user mode (Full RU) with all kinds of modulations, and at the lowest, middle, and highest data rates across the channel.

11A_Ant1_5180



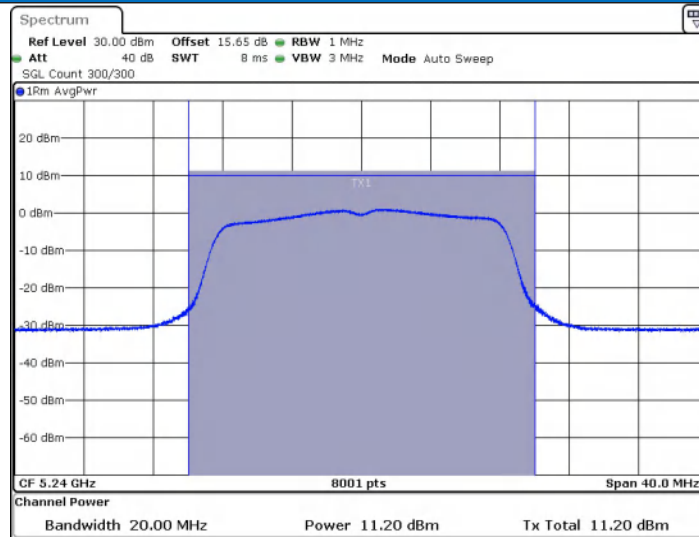
Date: 23 DEC 2025 17:04:37

11A_Ant1_5200



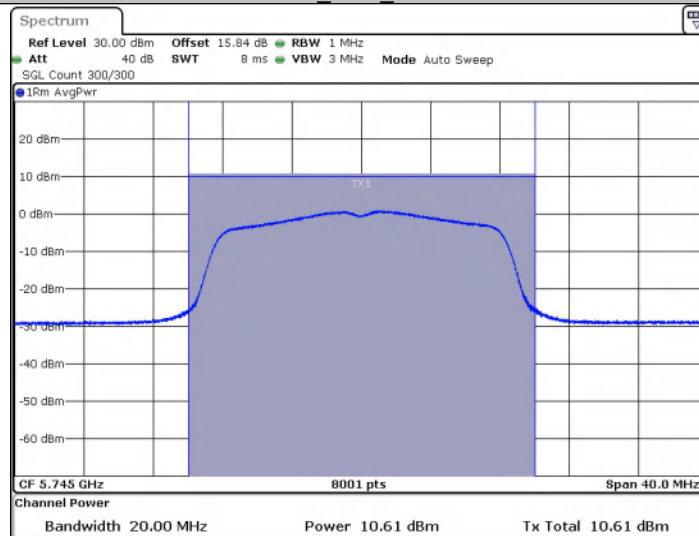
Date: 23 DEC 2025 17:07:07

11A_Ant1_5240



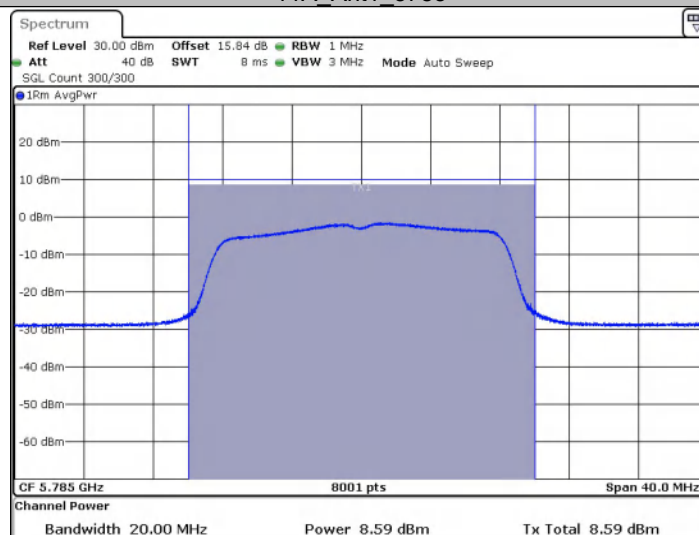
Date: 23 DEC 2025 17:08:28

11A_Ant1_5745



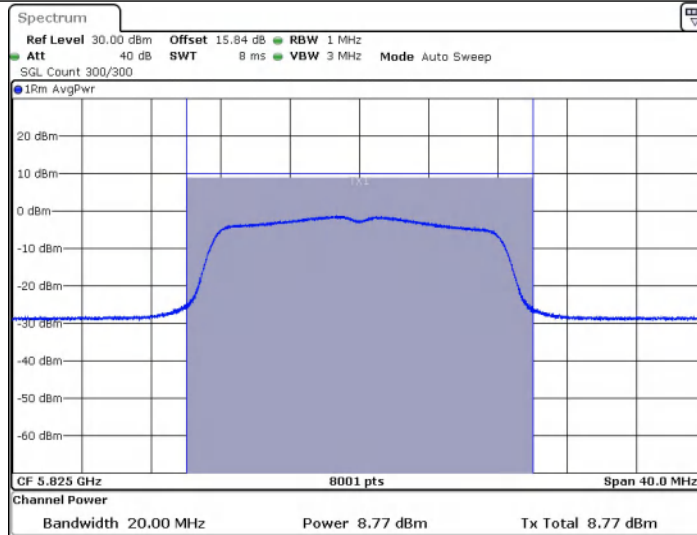
Date: 23 DEC 2025 17:11:18

11A_Ant1_5785



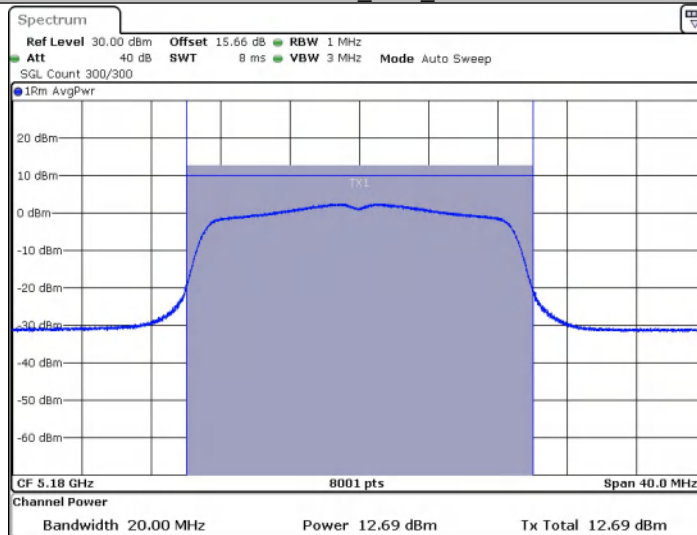
Date: 23 DEC 2025 17:13:26

11A_Ant1_5825



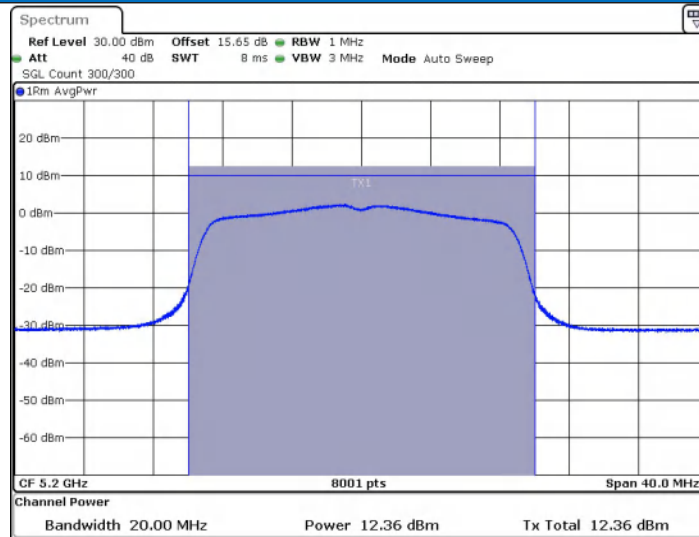
Date: 23 DEC 2025 17:18:34

11N20SISO_Ant1_5180



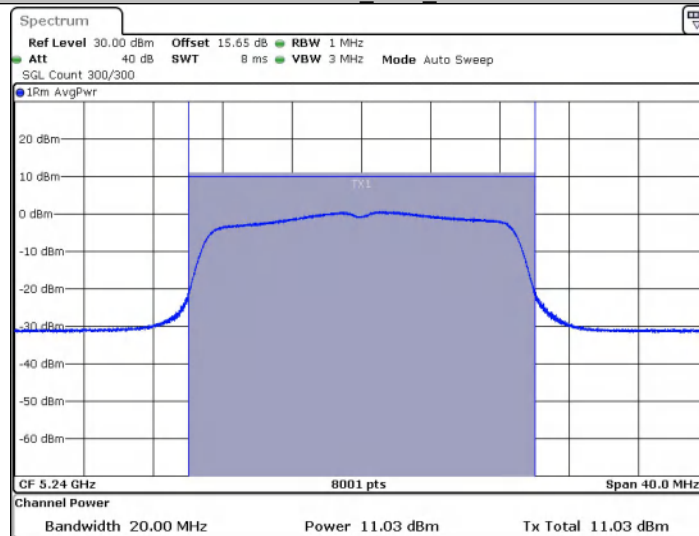
Date: 23 DEC 2025 17:32:06

11N20SISO_Ant1_5200



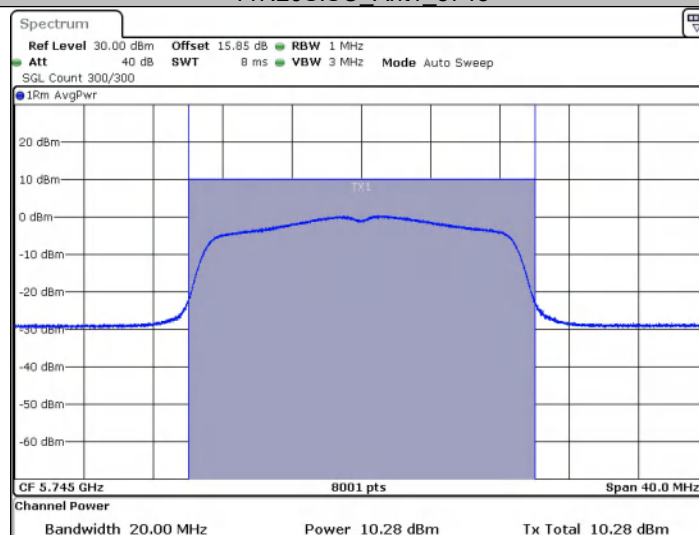
Date: 23 DEC 2025 17:34:59

11N20SISO_Ant1_5240



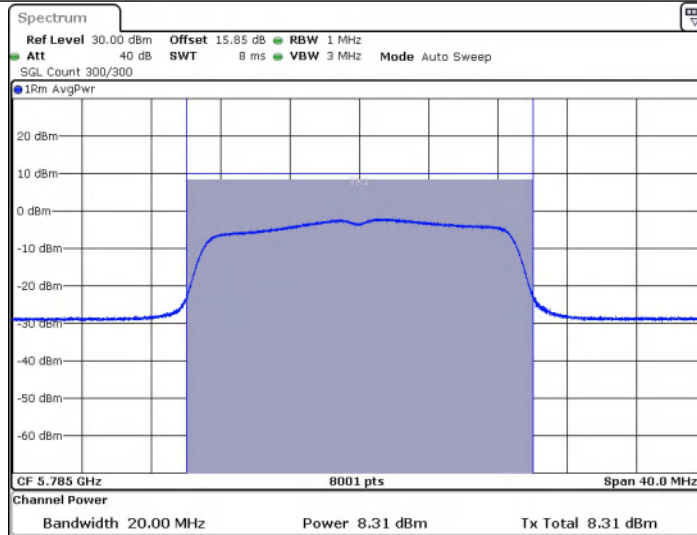
Date: 23 DEC 2025 17:37:36

11N20SISO_Ant1_5745



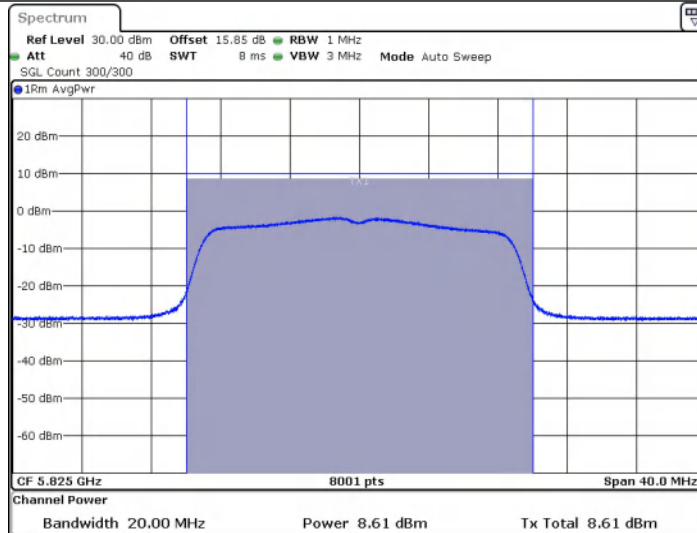
Date: 23 DEC 2025 17:39:25

11N20SISO_Ant1_5785



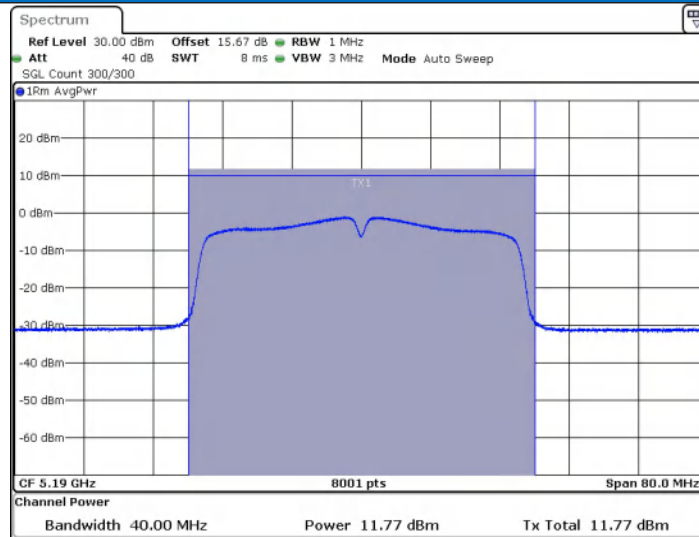
Date: 23 DEC 2025 17:42:38

11N20SISO_Ant1_5825



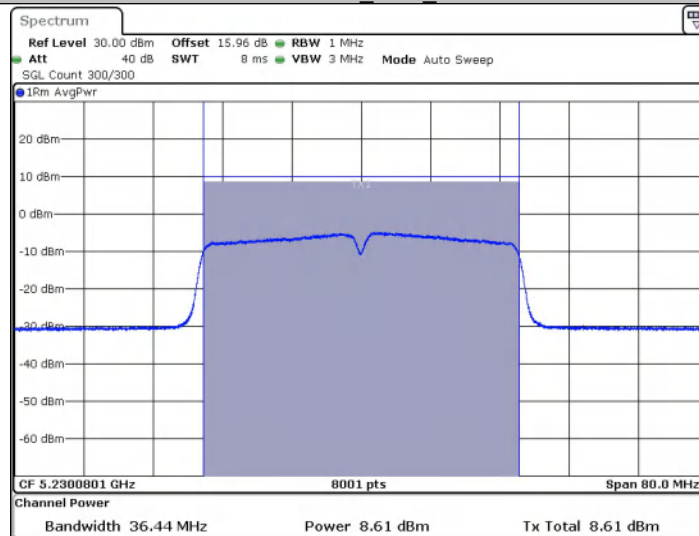
Date: 23 DEC 2025 17:45:51

11N40SISO_Ant1_5190



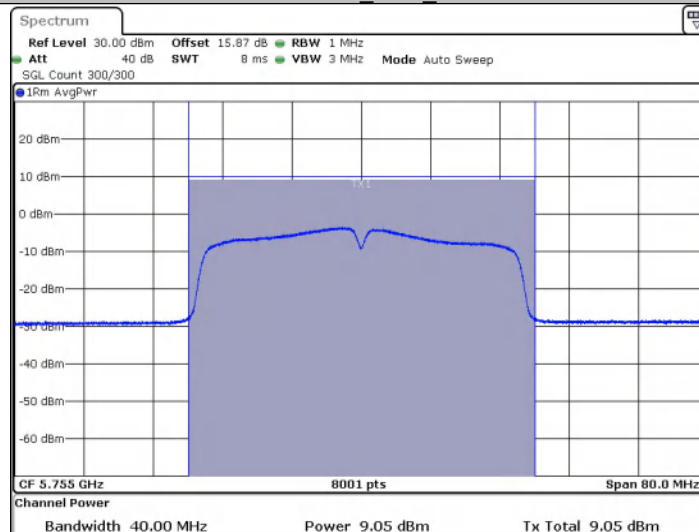
Date: 23 DEC 2025 17:47:37

11N40SISO_Ant1_5230



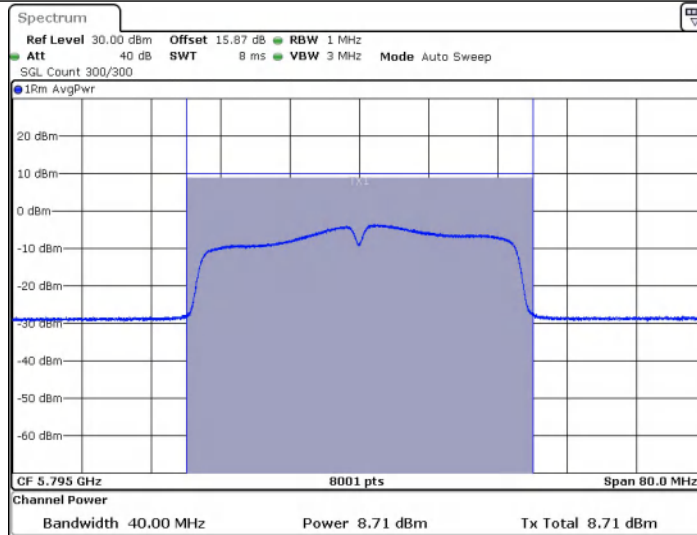
Date: 25 DEC 2025 14:39:22

11N40SISO_Ant1_5755



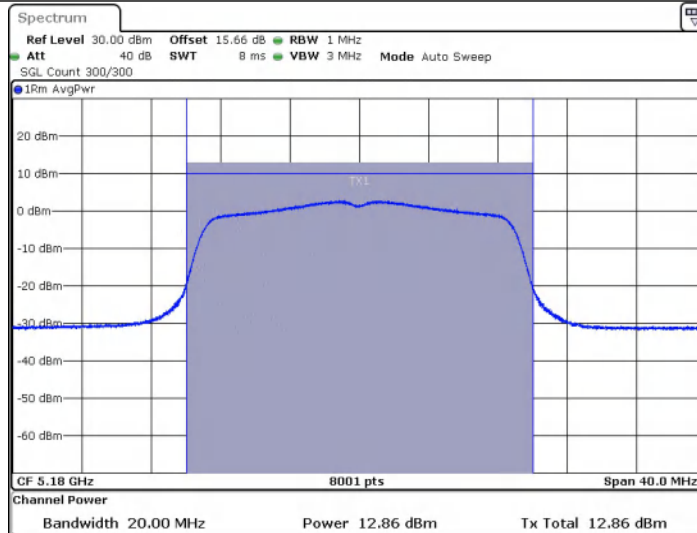
Date: 23 DEC 2025 18:36:45

11N40SISO_Ant1_5795



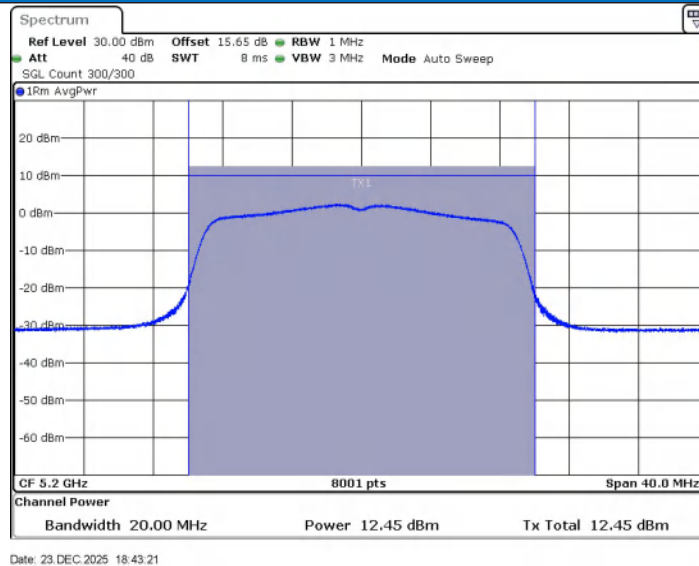
Date: 23 DEC 2025 18:39:04

11AC20SISO_Ant1_5180

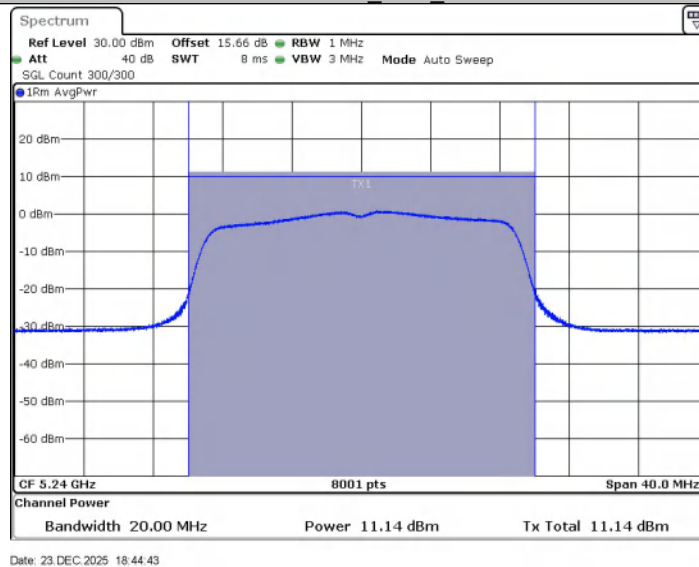


Date: 23 DEC 2025 18:40:45

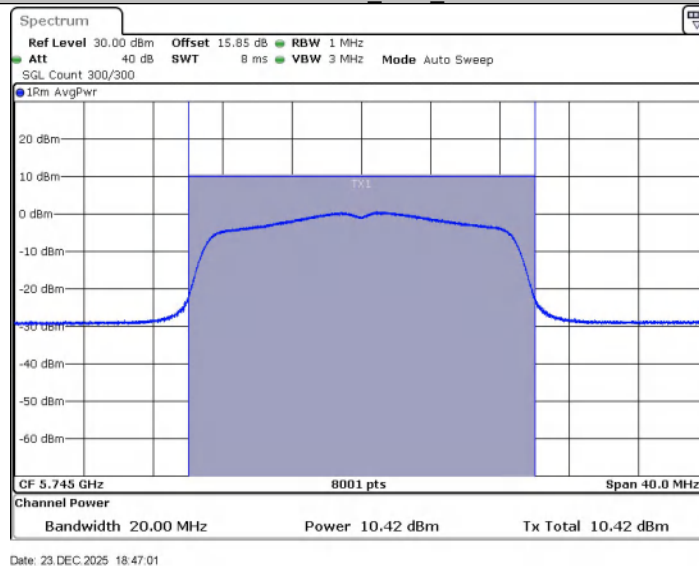
11AC20SISO_Ant1_5200



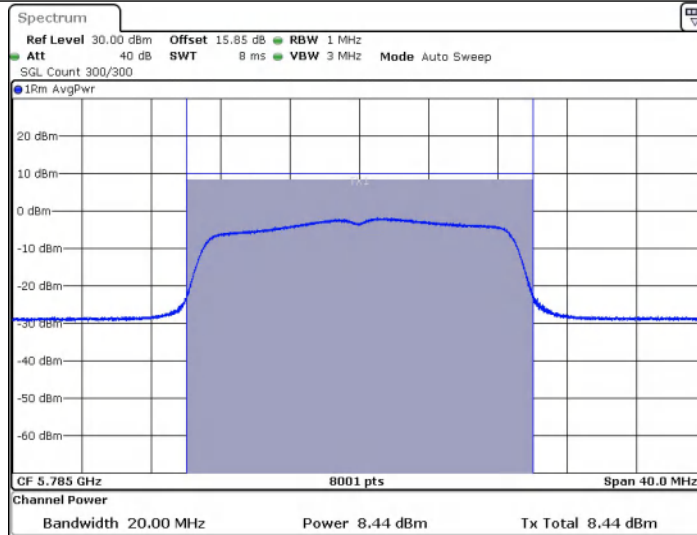
11AC20SISO_Ant1_5240



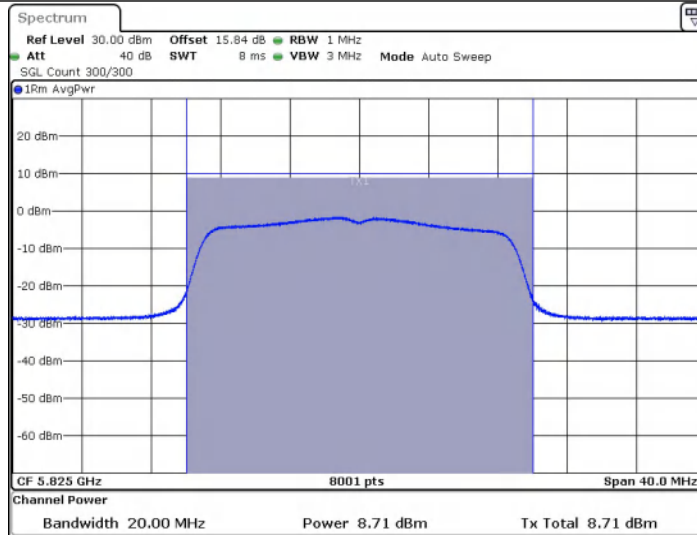
11AC20SISO_Ant1_5745



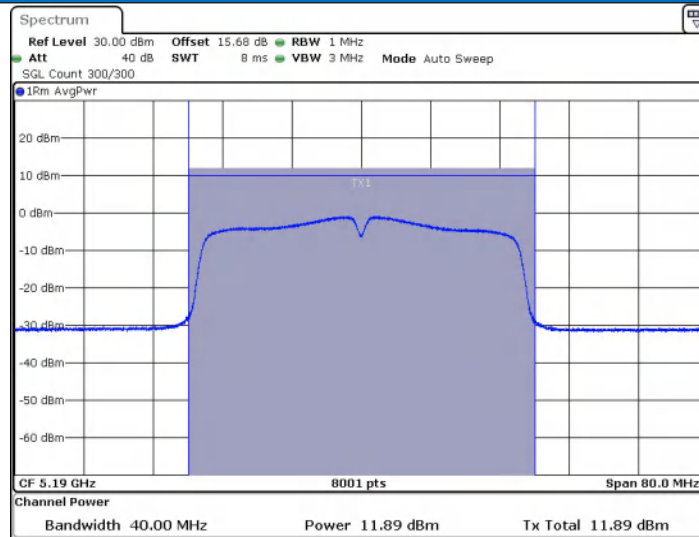
11AC20SISO_Ant1_5785



11AC20SISO_Ant1_5825

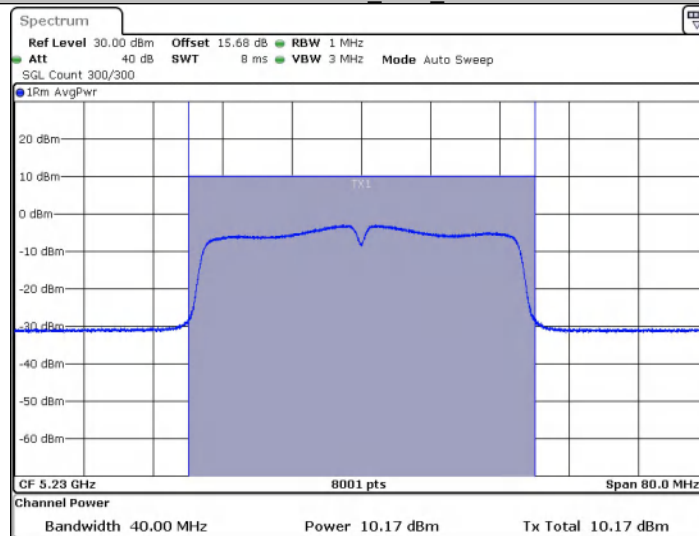


11AC40SISO_Ant1_5190



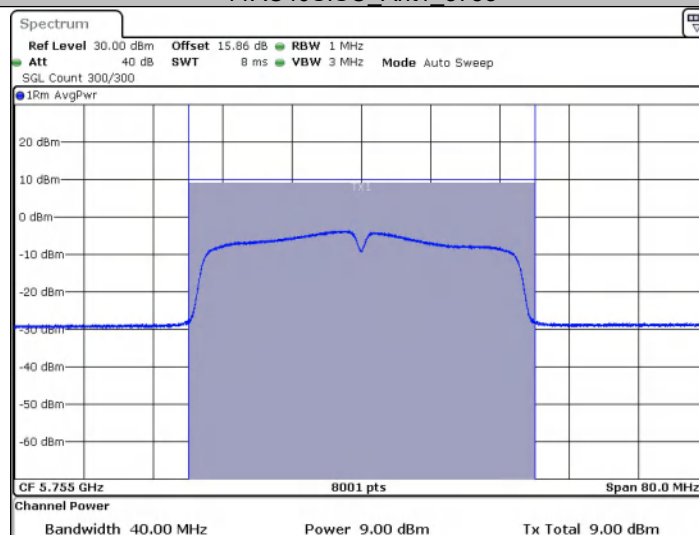
Date: 23 DEC 2025 18:53:48

11AC40SISO_Ant1_5230



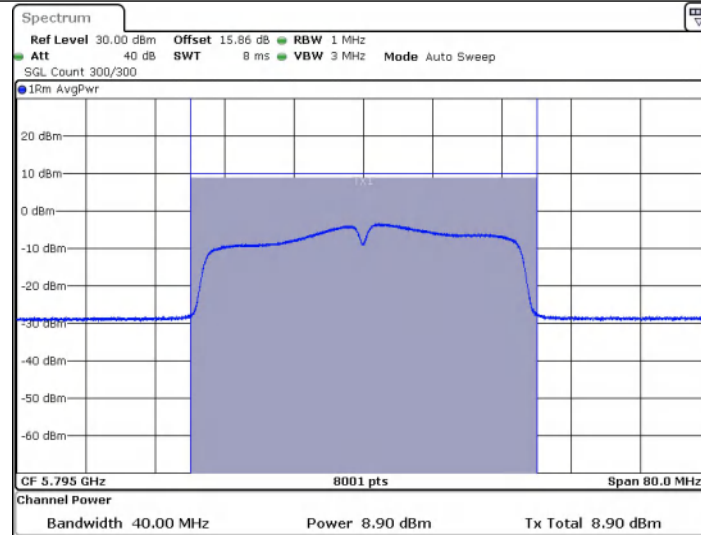
Date: 23 DEC 2025 18:56:33

11AC40SISO_Ant1_5755



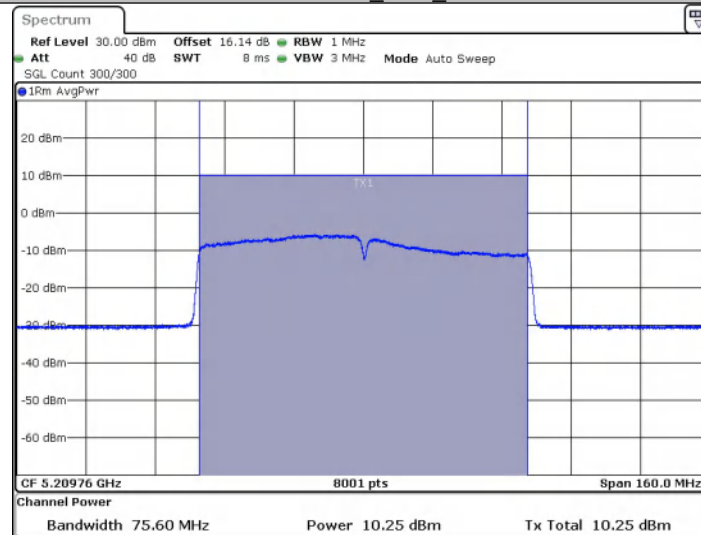
Date: 23 DEC 2025 18:58:50

11AC40SISO_Ant1_5795



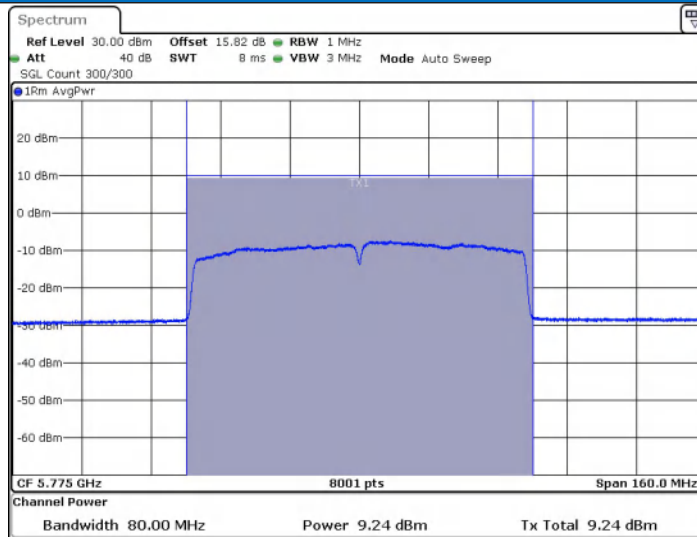
Date: 23 DEC 2025 19:00:45

11AC80SISO_Ant1_5210



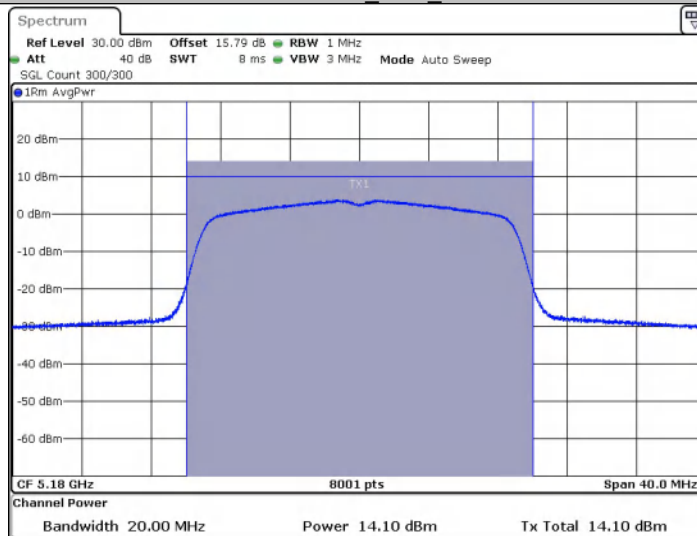
Date: 25 DEC 2025 11:47:00

11AC80SISO_Ant1_5775



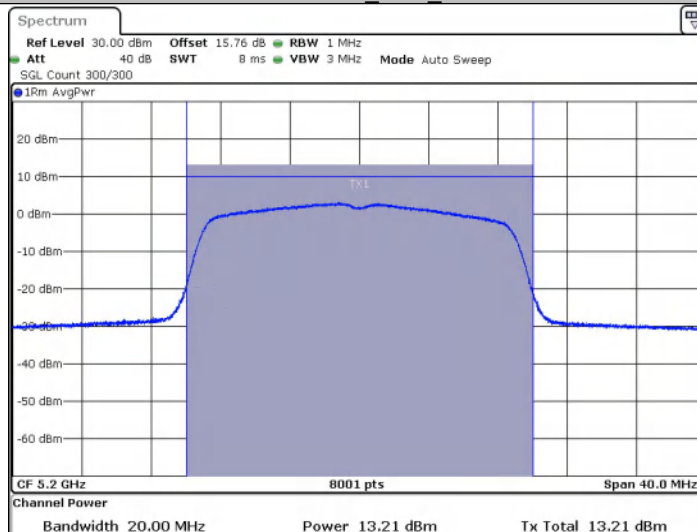
Date: 24 DEC 2025 17:28:28

11AX20SISO_Ant1_5180



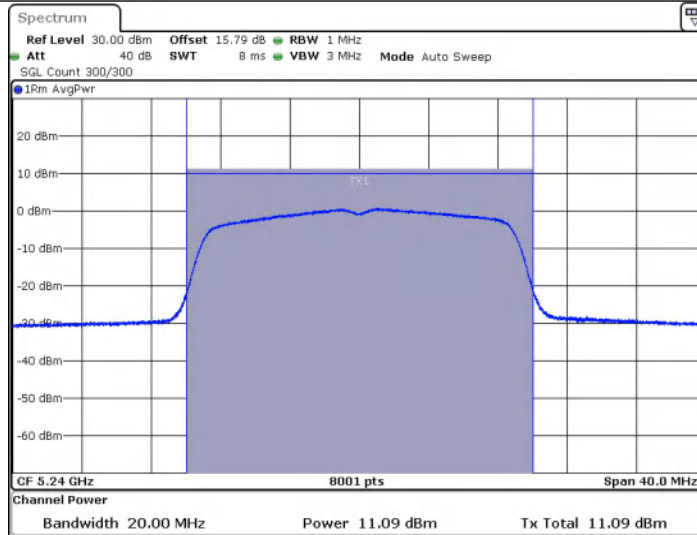
Date: 24 DEC 2025 17:31:39

11AX20SISO_Ant1_5200

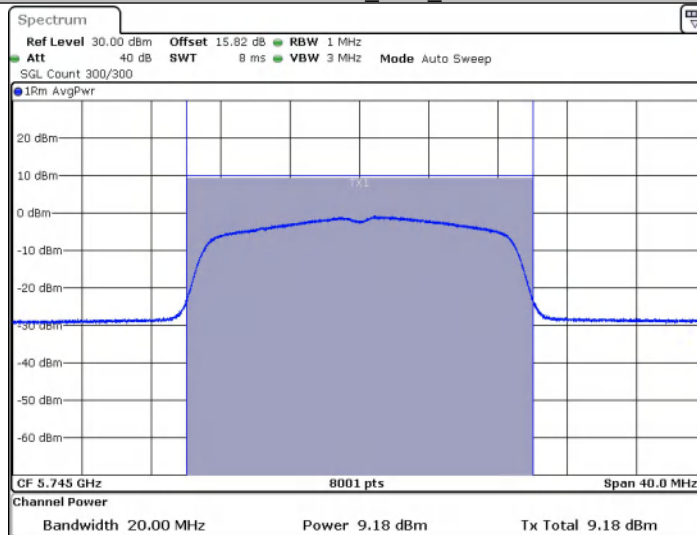


Date: 24 DEC 2025 17:40:59

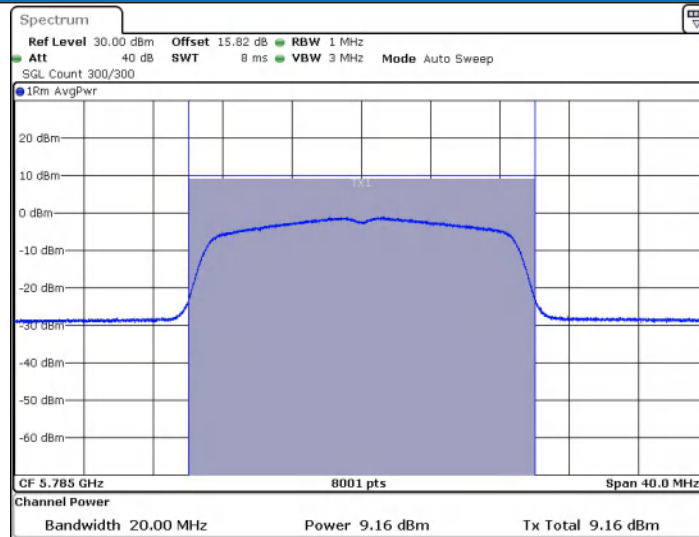
11AX20SISO_Ant1_5240



11AX20SISO_Ant1_5745

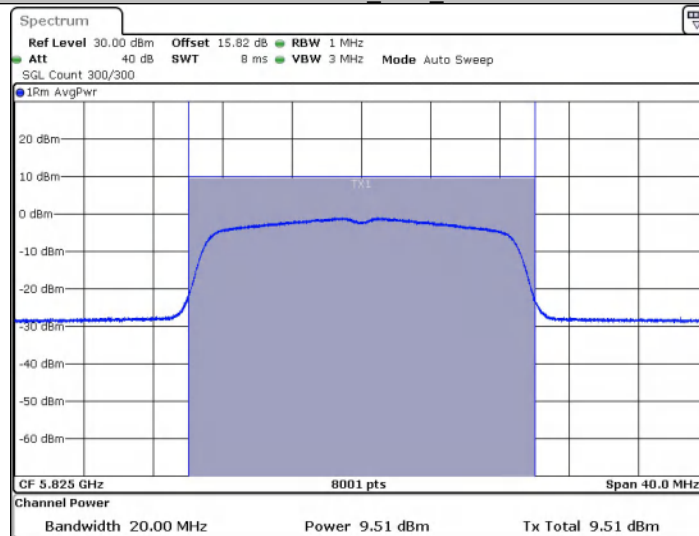


11AX20SISO_Ant1_5785



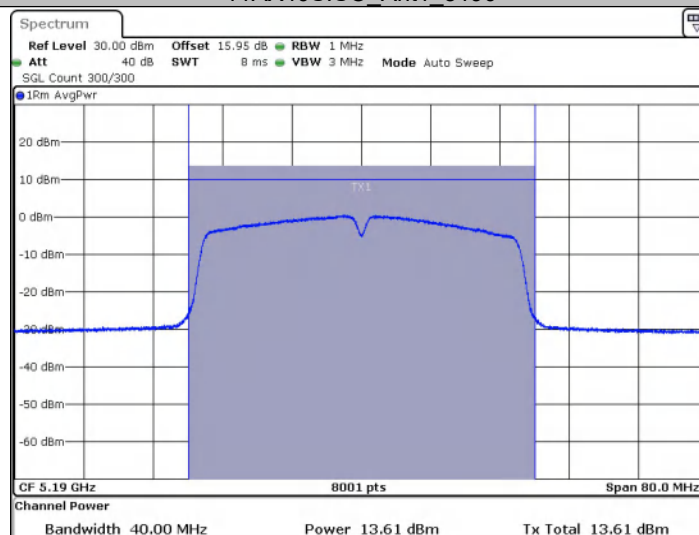
Date: 24 DEC 2025 17:50:53

11AX20SISO_Ant1_5825



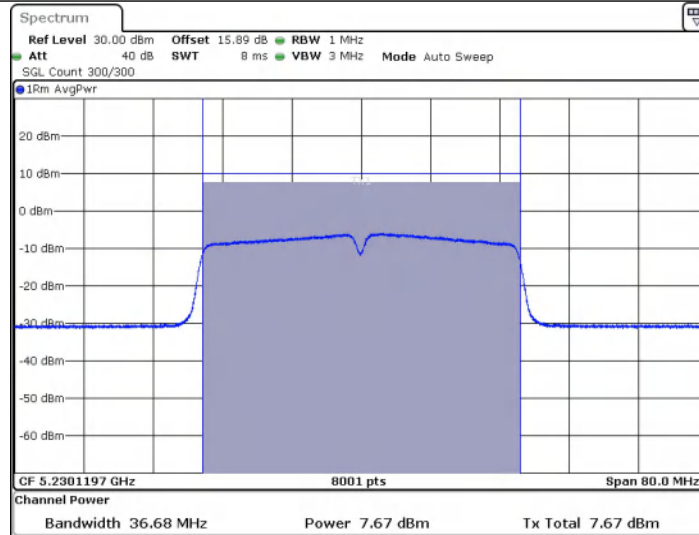
Date: 24 DEC 2025 17:52:03

11AX40SISO_Ant1_5190



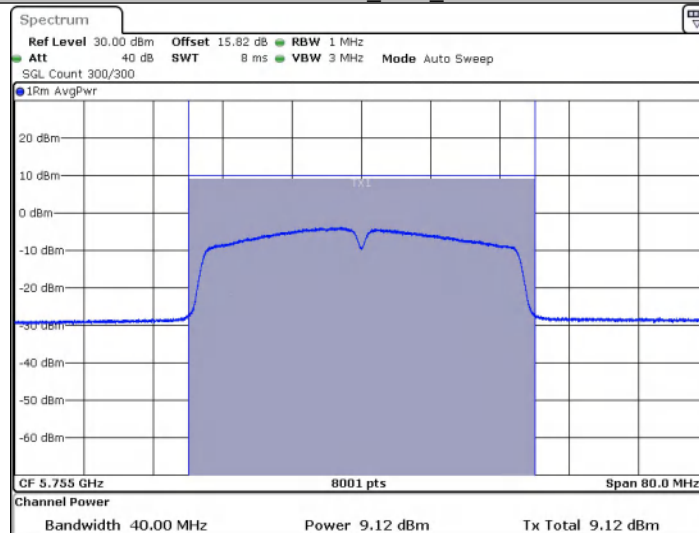
Date: 24 DEC 2025 17:54:19

11AX40SISO_Ant1_5230



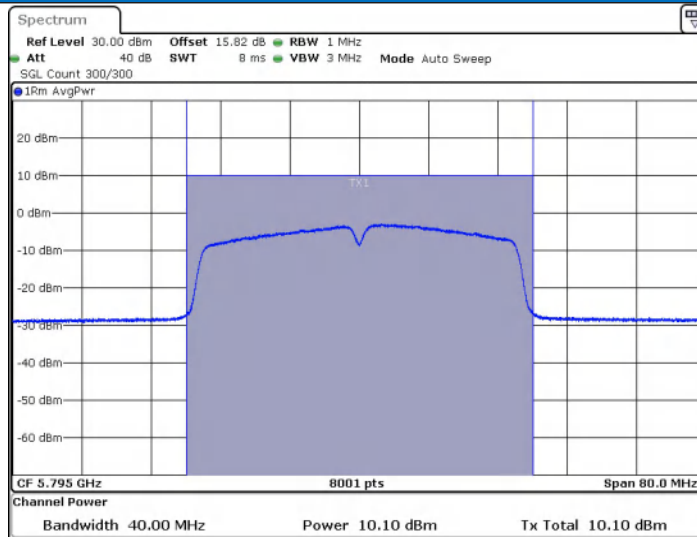
Date: 25 DEC 2025 11:53:06

11AX40SISO_Ant1_5755



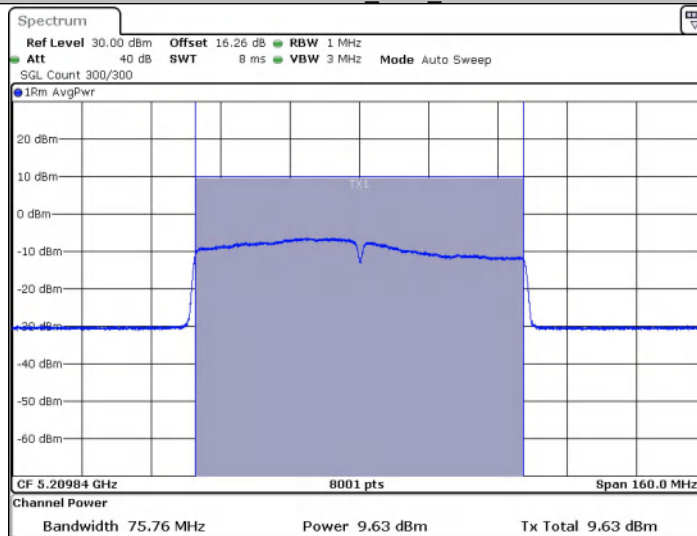
Date: 24 DEC 2025 18:47:41

11AX40SISO_Ant1_5795



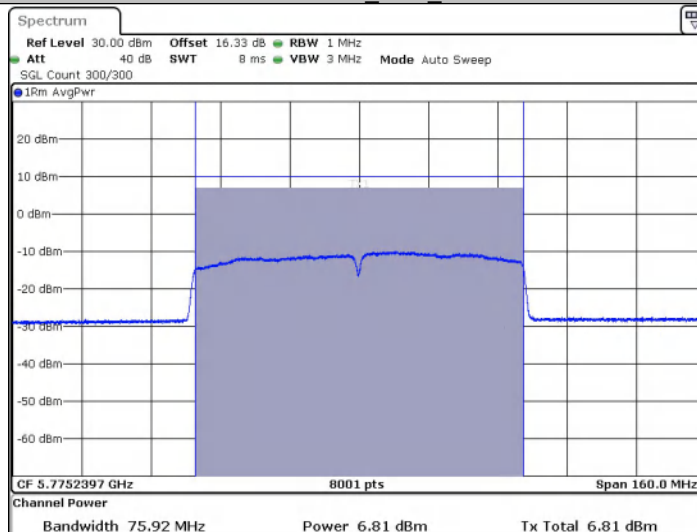
Date: 24 DEC 2025 18:50:26

11AX80SISO_Ant1_5210



Date: 25 DEC 2025 11:57:06

11AX80SISO_Ant1_5775



Date: 25 DEC 2025 12:01:39

Remark:

$Av.Power = Meas.Level + 10 \log (1/duty \text{ cycle})$

$E.i.r.p = Av.Power + G$,

G = antenna gain in dBi.

Ant2:

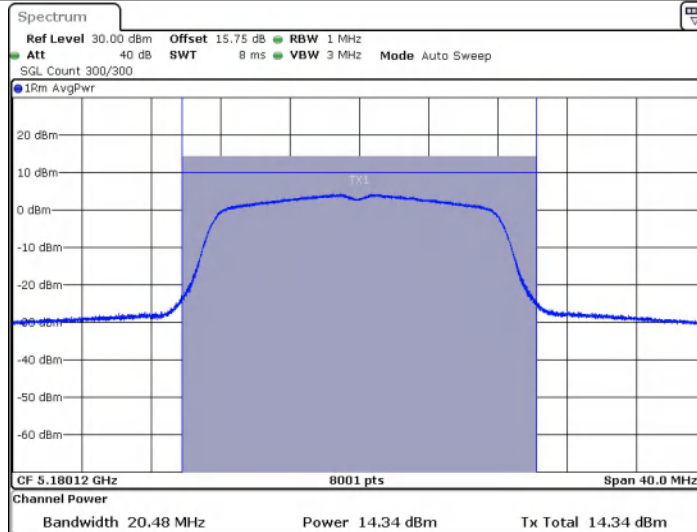
Test Mode	Antenna	Freq(MHz)	Result [dBm]	Limit [dBm]	Verdict
11A	Ant2	5180	14.34	≤23.98	PASS
		5200	13.52	≤23.98	PASS
		5240	11.13	≤23.98	PASS
		5745	9.47	≤30.00	PASS
		5785	9.22	≤30.00	PASS
		5825	9.55	≤30.00	PASS
11N20SISO	Ant2	5180	14.19	≤23.98	PASS
		5200	13.57	≤23.98	PASS
		5240	11.44	≤23.98	PASS
		5745	9.04	≤30.00	PASS
		5785	9.17	≤30.00	PASS
		5825	9.25	≤30.00	PASS
11N40SISO	Ant2	5190	14.08	≤23.98	PASS
		5230	8.08	≤23.98	PASS
		5755	9.10	≤30.00	PASS
		5795	9.76	≤30.00	PASS
11AC20SISO	Ant2	5180	14.41	≤23.98	PASS
		5200	13.73	≤23.98	PASS
		5240	11.75	≤23.98	PASS
		5745	8.90	≤30.00	PASS
		5785	8.99	≤30.00	PASS
		5825	9.08	≤30.00	PASS
11AC40SISO	Ant2	5190	14.06	≤23.98	PASS
		5230	10.98	≤23.98	PASS
		5755	8.66	≤30.00	PASS
		5795	9.64	≤30.00	PASS
11AC80SISO	Ant2	5210	13.44	≤23.98	PASS
		5775	10.86	≤30.00	PASS
11AX20SISO	Ant2	5180	14.67	≤23.98	PASS
		5200	13.92	≤23.98	PASS
		5240	11.01	≤23.98	PASS
		5745	9.87	≤30.00	PASS
		5785	9.85	≤30.00	PASS
		5825	9.96	≤30.00	PASS

11AX40SIS O	Ant2	5190	13.89	≤ 23.98	PASS
		5230	10.67	≤ 23.98	PASS
		5755	9.94	≤ 30.00	PASS
		5795	10.92	≤ 30.00	PASS
11AX80SIS O	Ant2	5210	12.54	≤ 23.98	PASS
		5775	10.22	≤ 30.00	PASS

Note:

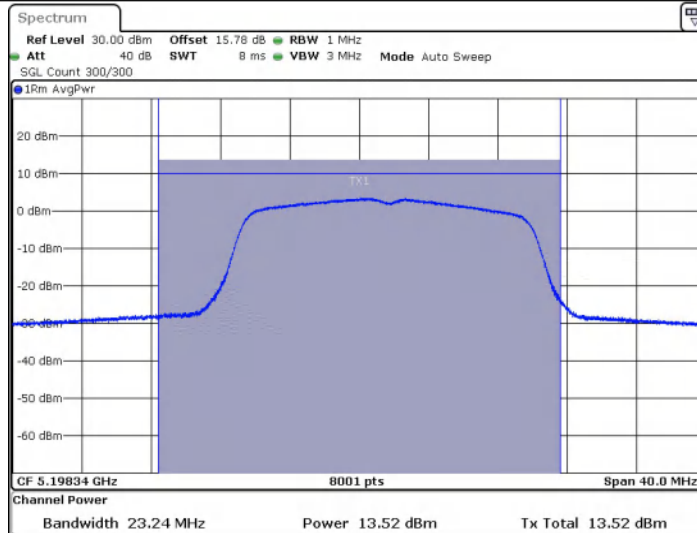
Transmitting in full-bandwidth single-user mode (Full RU) with all kinds of modulations, and at the lowest, middle, and highest data rates across the channel.

11A_Ant2_5180



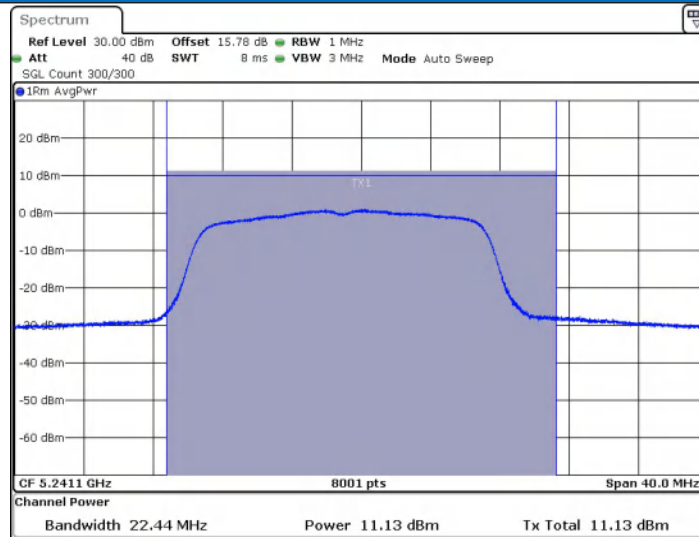
Date: 24 DEC 2025 19:37:28

11A_Ant2_5200



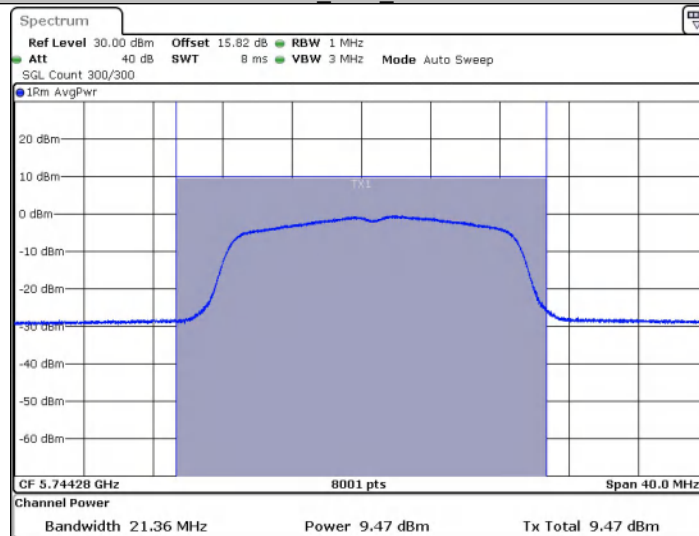
Date: 24 DEC 2025 19:40:47

11A_Ant2_5240



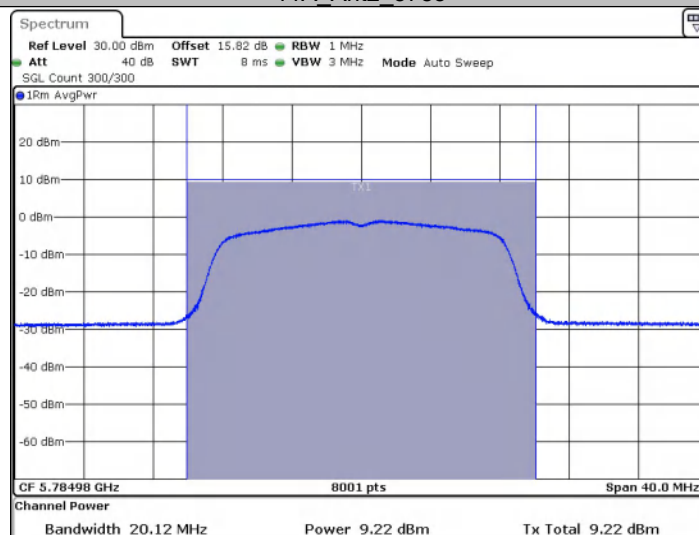
Date: 24 DEC 2025 19:41:48

11A_Ant2_5745



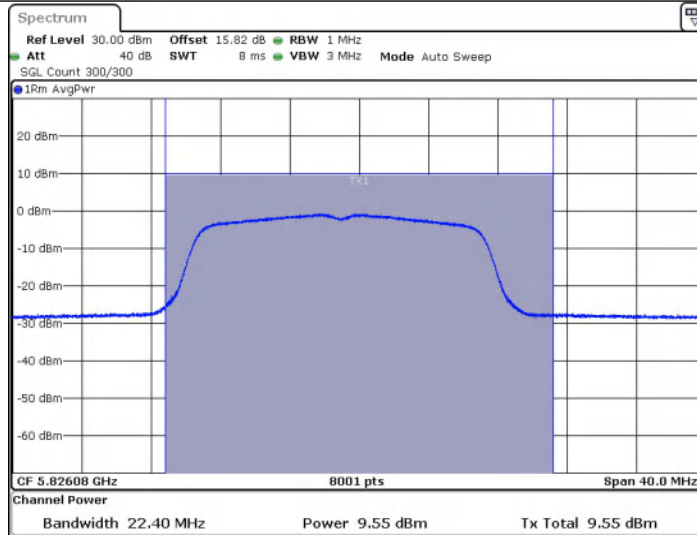
Date: 24 DEC 2025 19:43:24

11A_Ant2_5785



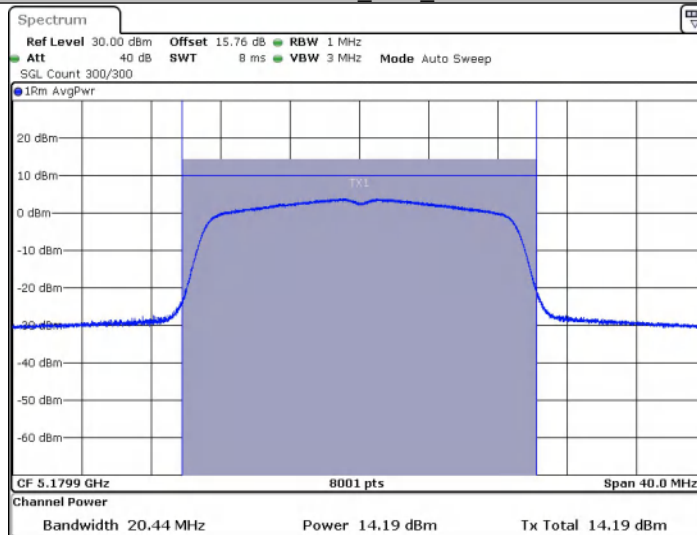
Date: 24 DEC 2025 19:49:35

11A_Ant2_5825



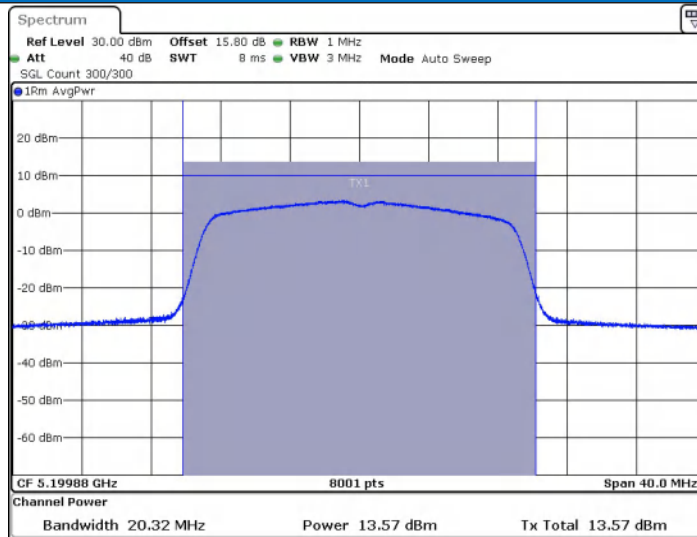
Date: 24 DEC 2025 19:51:33

11N20SISO_Ant2_5180



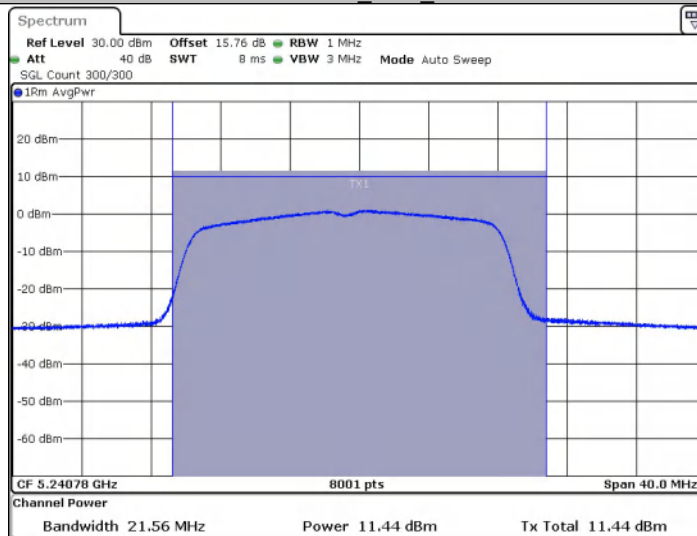
Date: 24 DEC 2025 19:53:06

11N20SISO_Ant2_5200



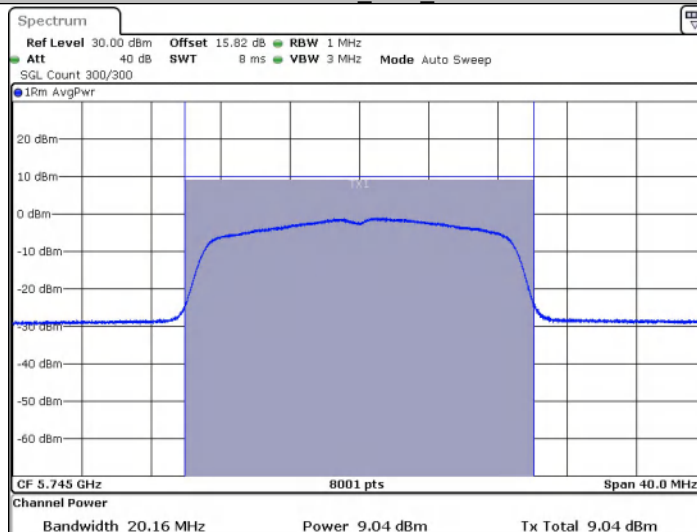
Date: 24 DEC 2025 19:55:55

11N20SISO_Ant2_5240



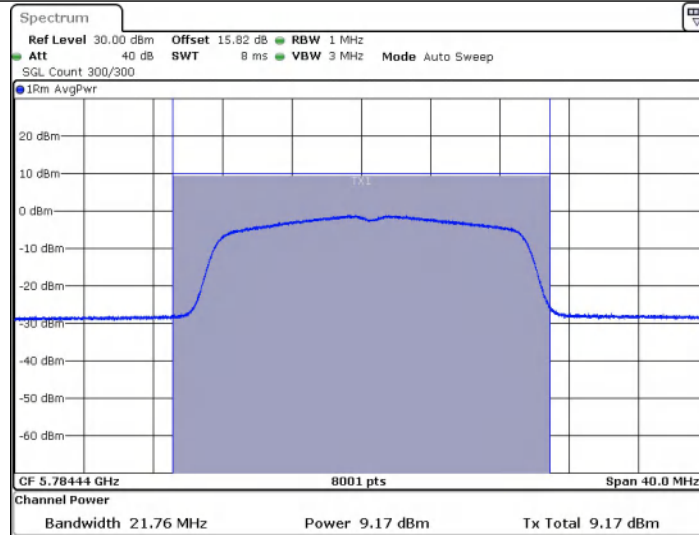
Date: 24 DEC 2025 19:57:48

11N20SISO_Ant2_5745



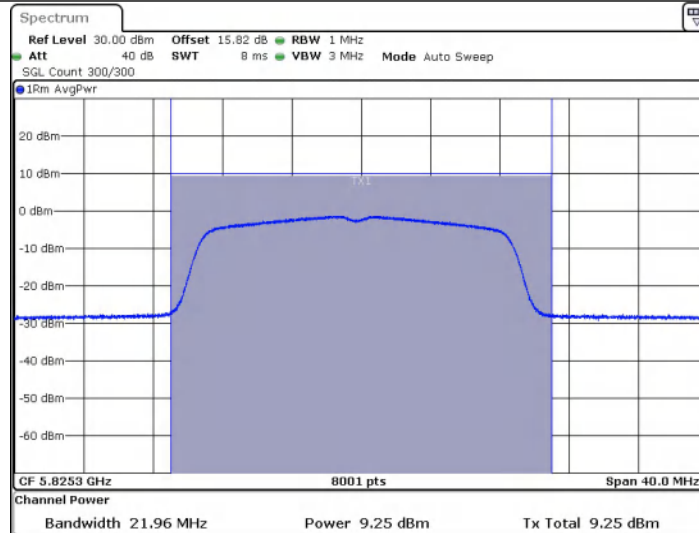
Date: 24 DEC 2025 19:59:23

11N20SISO_Ant2_5785



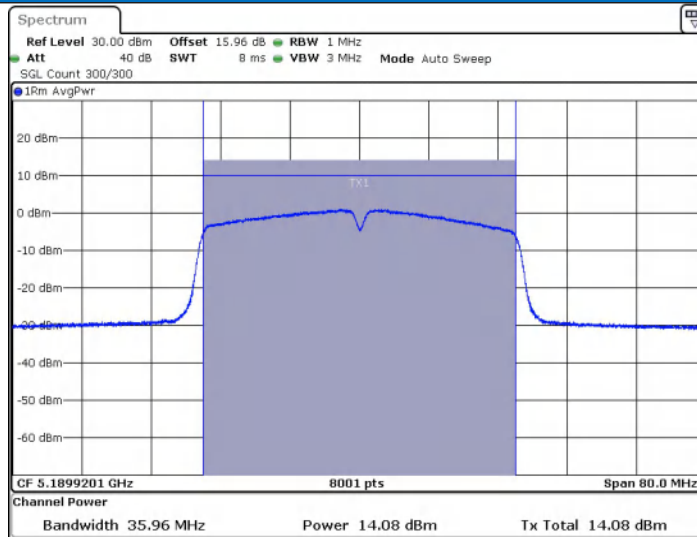
Date: 24 DEC 2025 20:01:51

11N20SISO_Ant2_5825



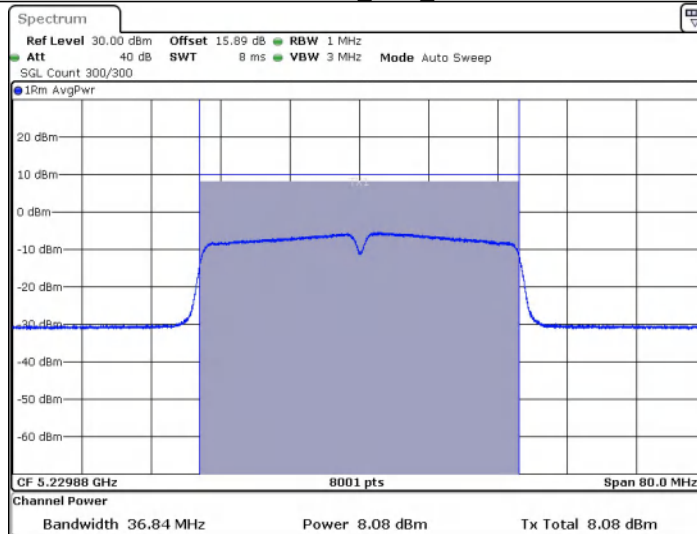
Date: 24 DEC 2025 20:03:47

11N40SISO_Ant2_5190



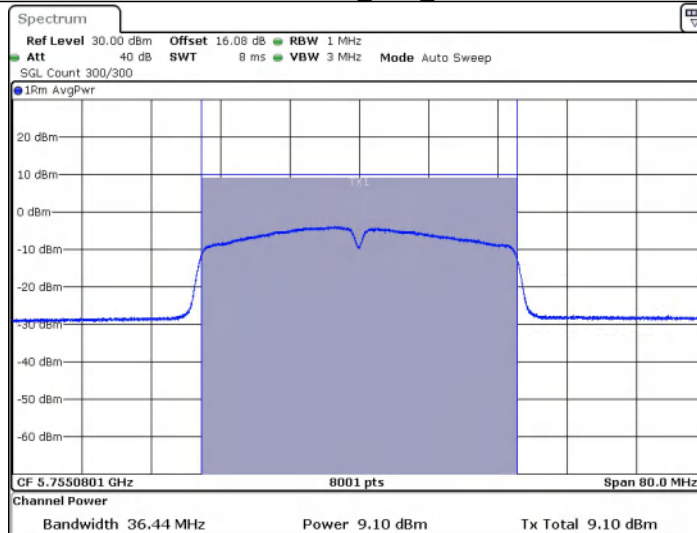
Date: 24 DEC 2025 20:20:48

11N40SISO_Ant2_5230



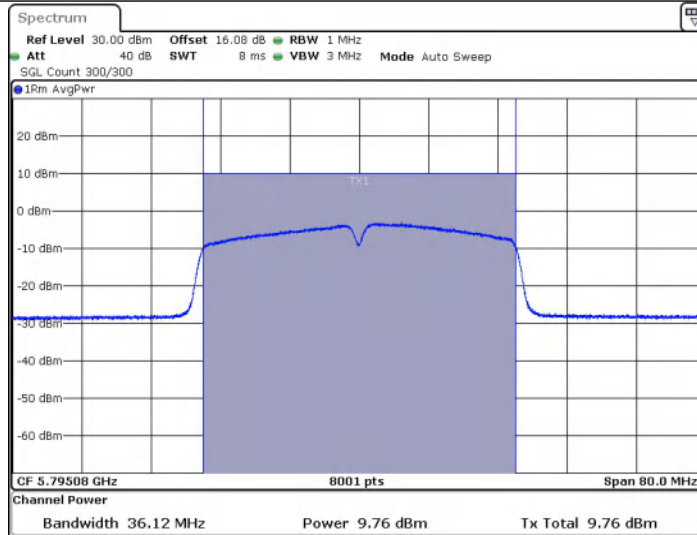
Date: 25 DEC 2025 14:25:49

11N40SISO_Ant2_5755



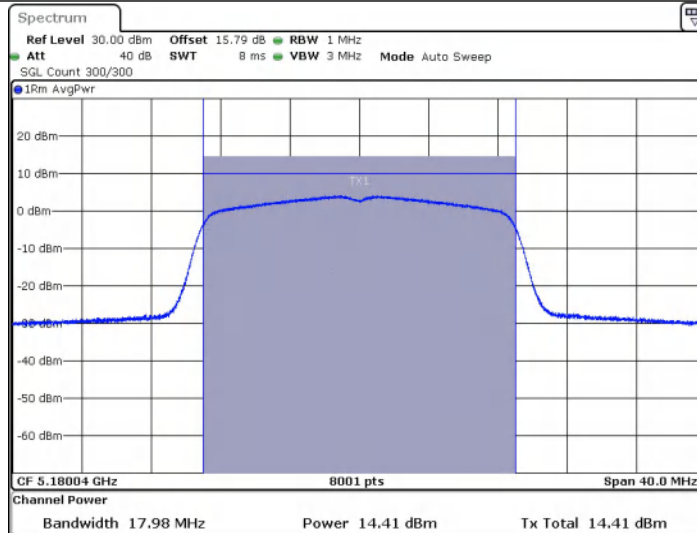
Date: 24 DEC 2025 20:26:57

11N40SISO_Ant2_5795



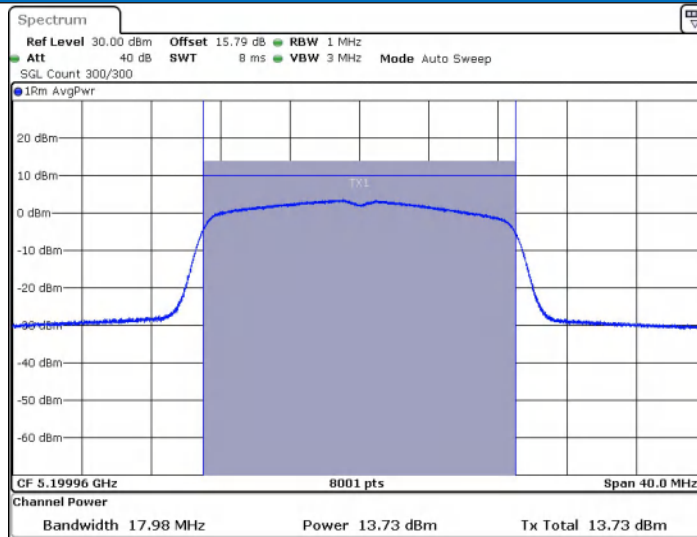
Date: 24 DEC 2025 20:28:53

11AC20SISO_Ant2_5180



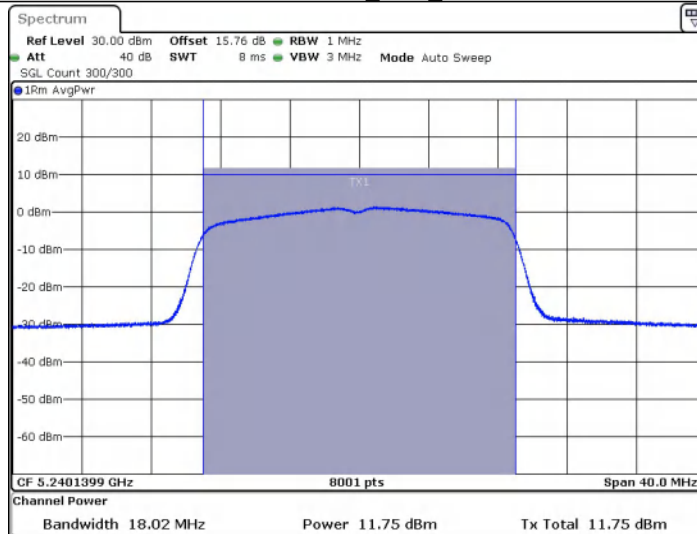
Date: 24 DEC 2025 20:30:39

11AC20SISO_Ant2_5200



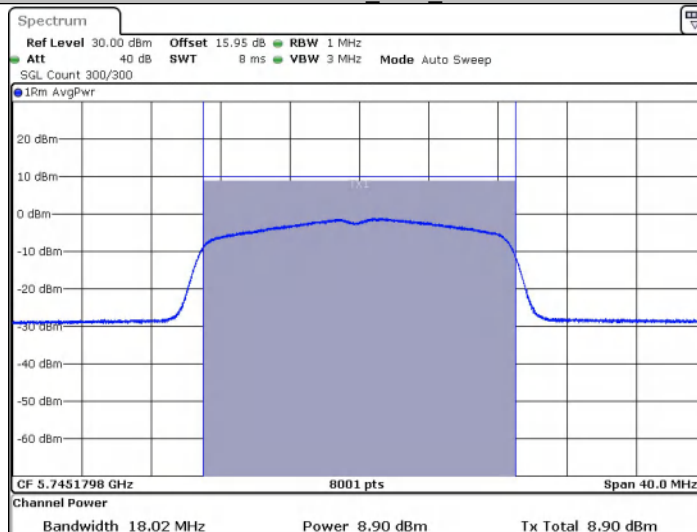
Date: 24 DEC 2025 20:35:08

11AC20SISO_Ant2_5240



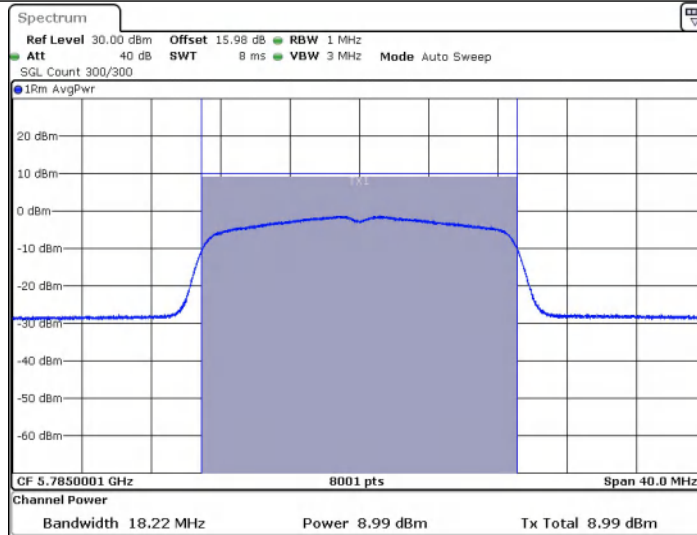
Date: 24 DEC 2025 20:36:09

11AC20SISO_Ant2_5745



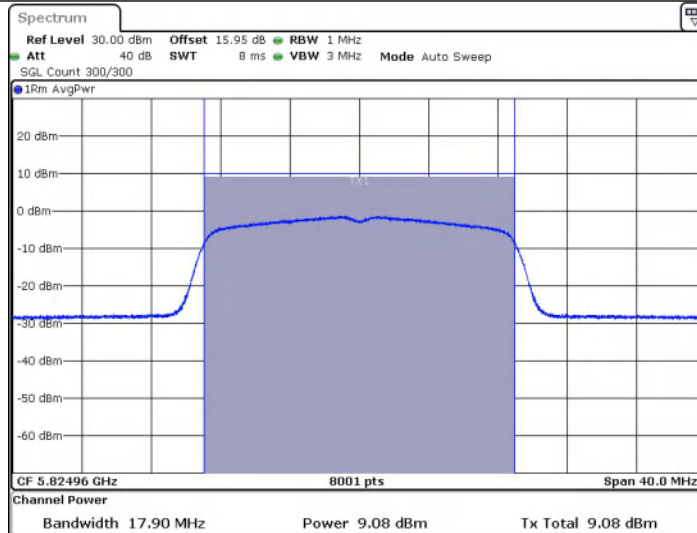
Date: 24 DEC 2025 20:37:41

11AC20SISO_Ant2_5785



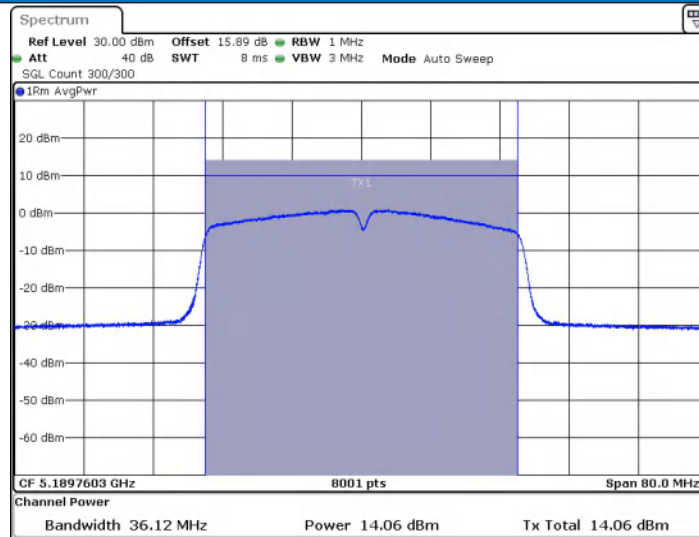
Date: 24 DEC 2025 20:39:13

11AC20SISO_Ant2_5825



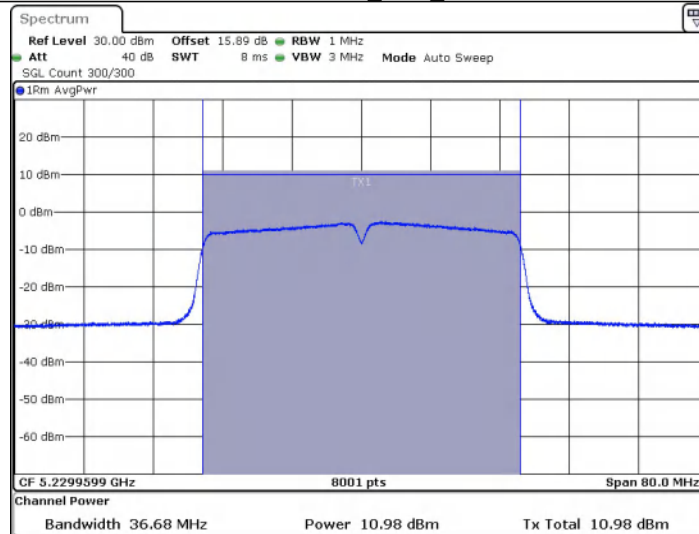
Date: 24 DEC 2025 20:40:28

11AC40SISO_Ant2_5190



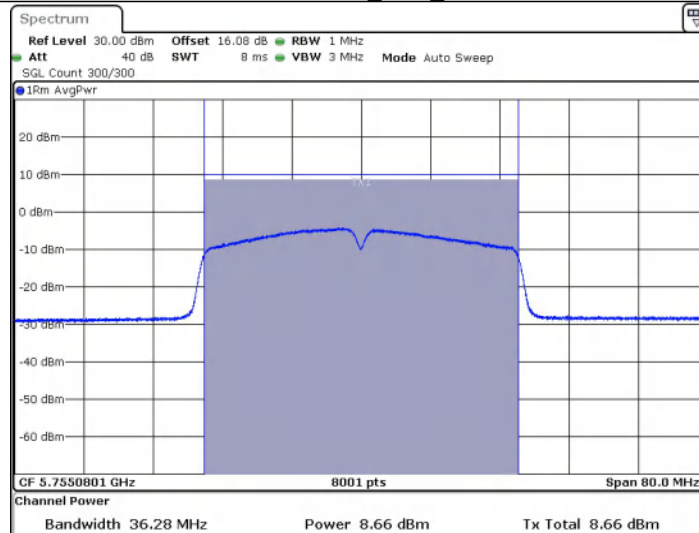
Date: 24 DEC 2025 20:42:02

11AC40SISO_Ant2_5230



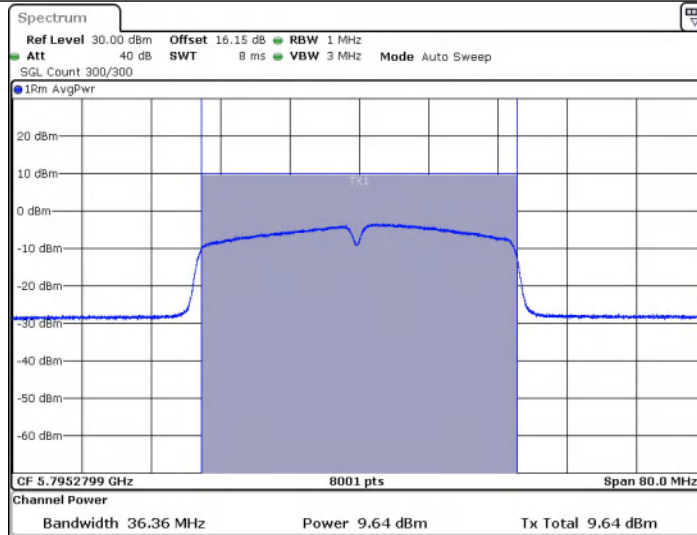
Date: 24 DEC 2025 20:44:21

11AC40SISO_Ant2_5755



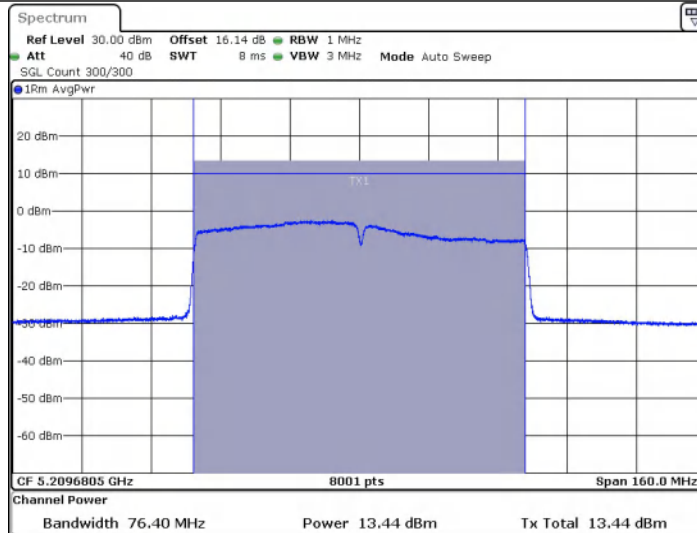
Date: 24 DEC 2025 20:47:03

11AC40SISO_Ant2_5795



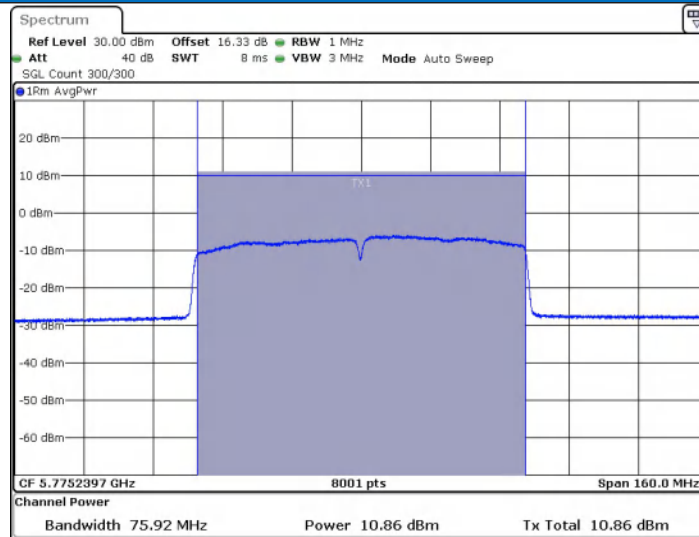
Date: 24 DEC 2025 20:48:47

11AC80SISO_Ant2_5210



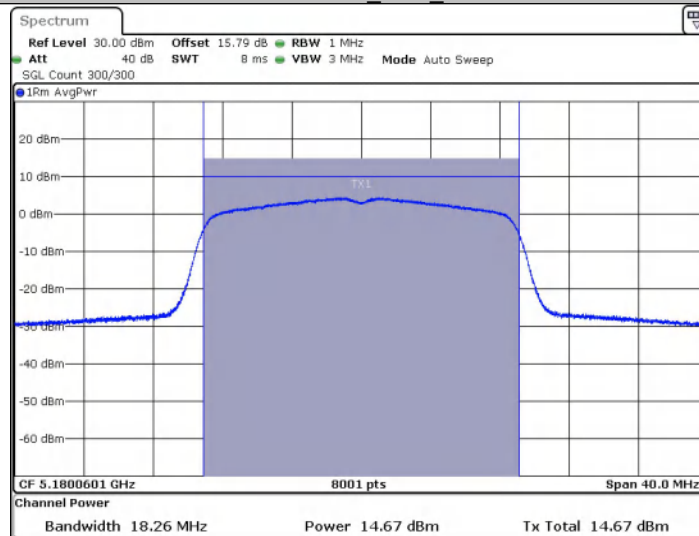
Date: 25 DEC 2025 10:43:24

11AC80SISO_Ant2_5775



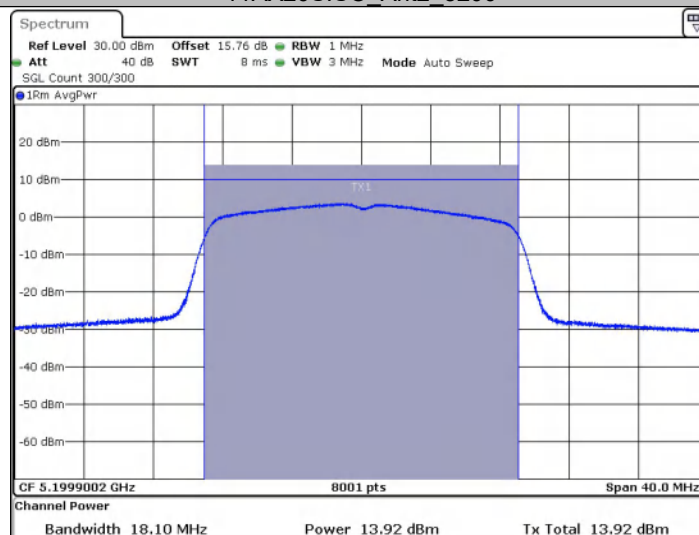
Date: 25 DEC 2025 10:46:36

11AX20SISO_Ant2_5180



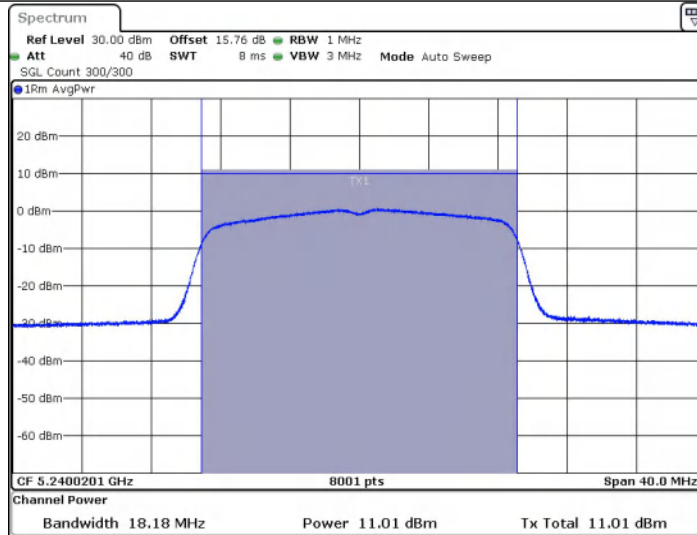
Date: 25 DEC 2025 10:48:39

11AX20SISO_Ant2_5200



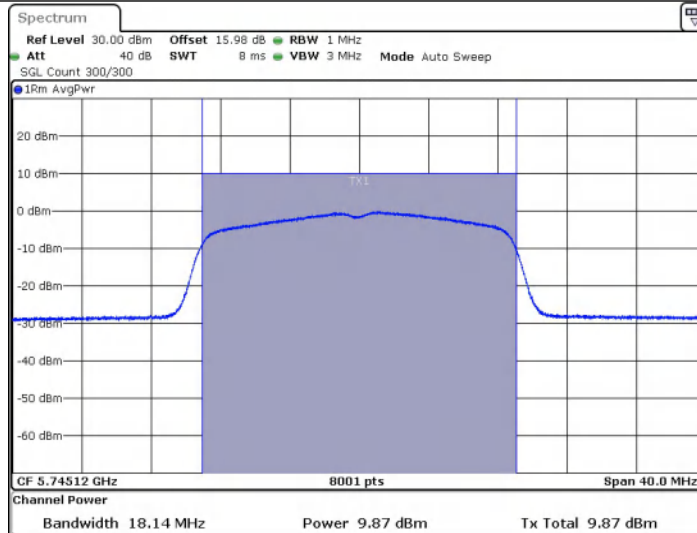
Date: 25 DEC 2025 10:50:54

11AX20SISO_Ant2_5240



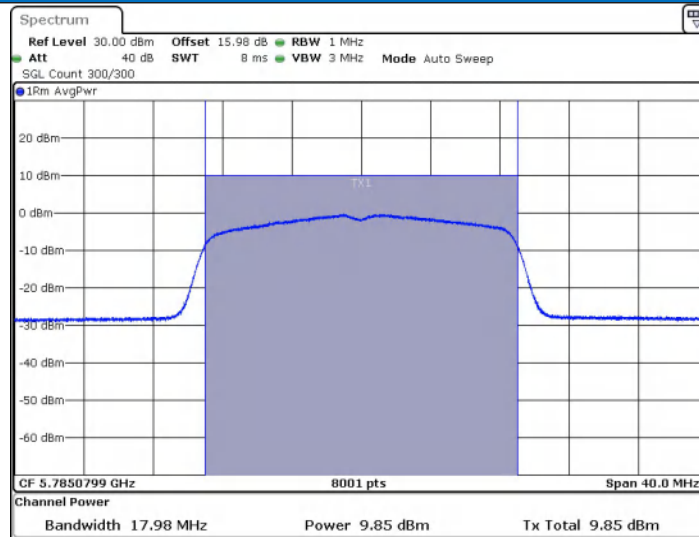
Date: 25 DEC 2025 10:52:06

11AX20SISO_Ant2_5745



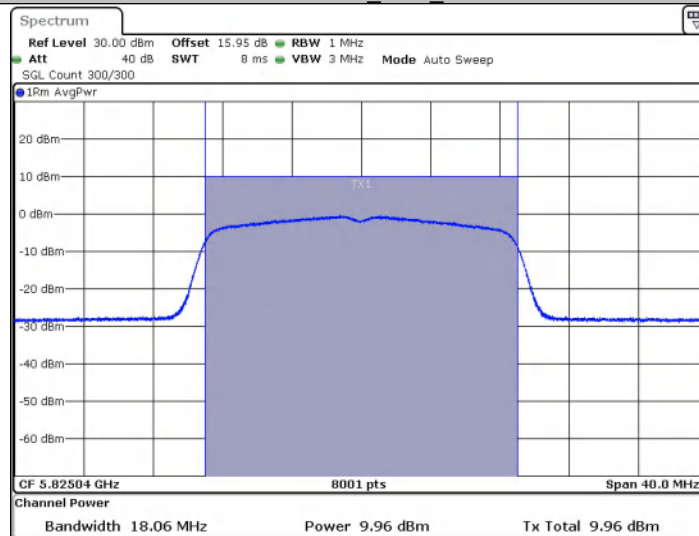
Date: 25 DEC 2025 10:53:55

11AX20SISO_Ant2_5785



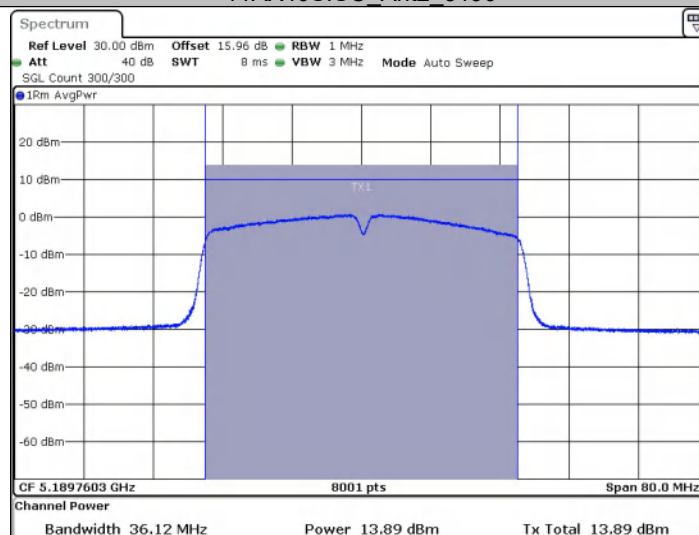
Date: 25 DEC 2025 10:55:28

11AX20SISO_Ant2_5825



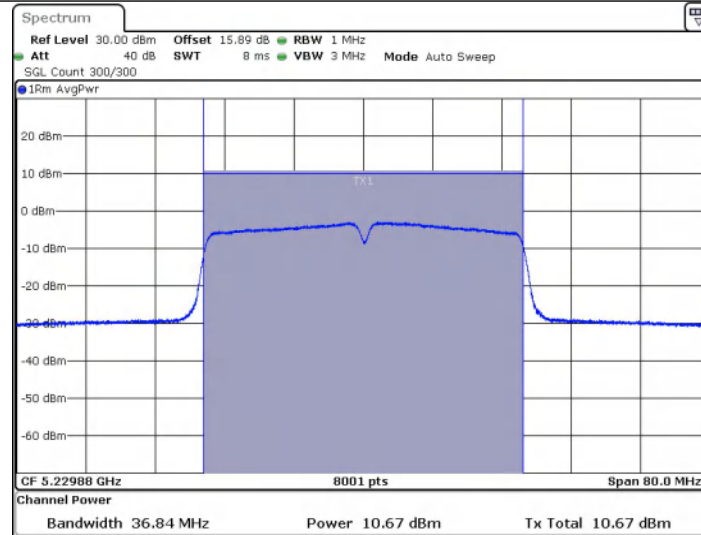
Date: 25 DEC 2025 10:57:35

11AX40SISO_Ant2_5190

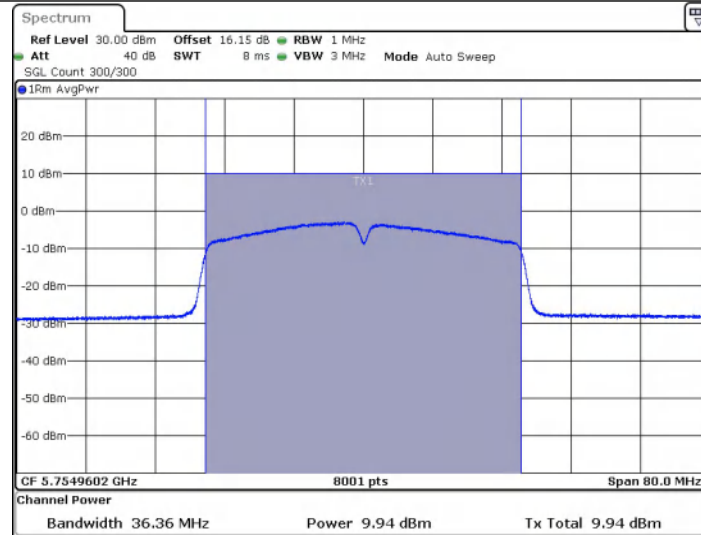


Date: 25 DEC 2025 11:00:49

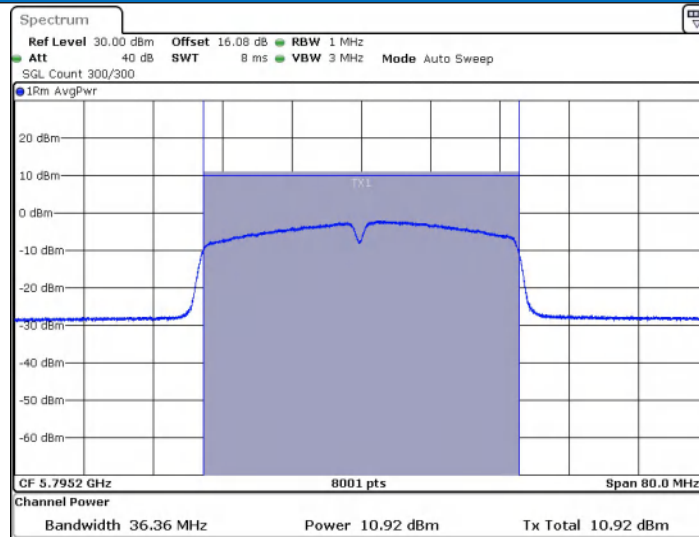
11AX40SISO_Ant2_5230



11AX40SISO_Ant2_5755

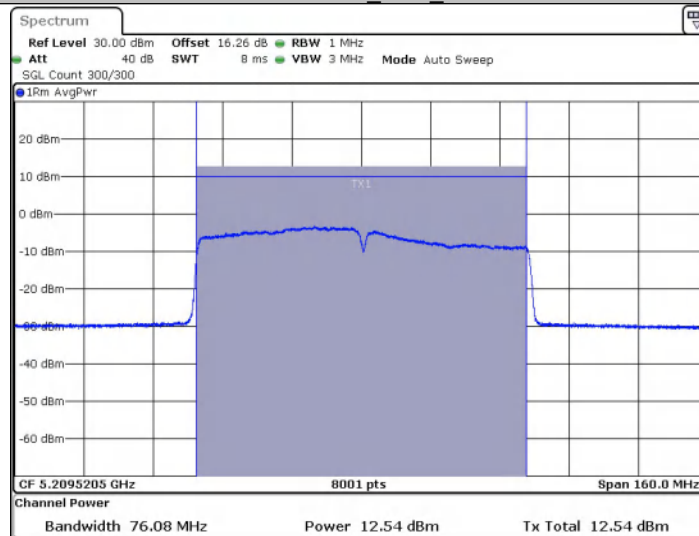


11AX40SISO_Ant2_5795



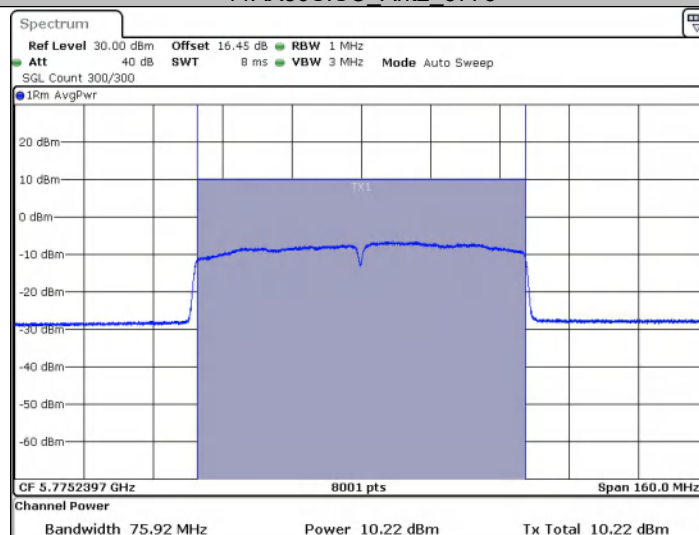
Date: 25 DEC 2025 11:09:34

11AX80SISO_Ant2_5210



Date: 25 DEC 2025 11:11:50

11AX80SISO_Ant2_5775



Date: 25 DEC 2025 11:14:35

Ant1+Ant2:

Test Mode	Antenna	Freq(MHz)	Result [dBm]	Limit [dBm]	Verdict
11N20MIM O	Ant1	5180	16.51	≤23.98	PASS
		5200	16.02	≤23.98	PASS
		5240	14.25	≤23.98	PASS
		5745	12.71	≤30.00	PASS
		5785	11.77	≤30.00	PASS
		5825	11.95	≤30.00	PASS
11N40MIM O	Ant1	5190	16.09	≤23.98	PASS
		5230	11.36	≤23.98	PASS
		5755	12.09	≤30.00	PASS
		5795	12.28	≤30.00	PASS
11AC20MI MO	Ant1	5180	16.71	≤23.98	PASS
		5200	16.15	≤23.98	PASS
		5240	14.47	≤23.98	PASS
		5745	12.74	≤30.00	PASS
		5785	11.73	≤30.00	PASS
		5825	11.91	≤30.00	PASS
11AC40MI MO	Ant1	5190	16.12	≤23.98	PASS
		5230	13.60	≤23.98	PASS
		5755	11.84	≤30.00	PASS
		5795	12.30	≤30.00	PASS
11AC80MI MO	Ant1	5210	15.14	≤23.98	PASS
		5775	13.14	≤30.00	PASS
11AX20MIM O	Ant1	5180	17.40	≤23.98	PASS
		5200	16.59	≤23.98	PASS
		5240	14.06	≤23.98	PASS
		5745	12.55	≤30.00	PASS
		5785	12.53	≤30.00	PASS
		5825	12.75	≤30.00	PASS
11AX40MIM O	Ant1	5190	16.76	≤23.98	PASS
		5230	12.43	≤23.98	PASS
		5755	12.56	≤30.00	PASS
		5795	13.54	≤30.00	PASS
11AX80MIM O	Ant1	5210	14.33	≤23.98	PASS
		5775	11.85	≤30.00	PASS

Remark:

$Av.Power = Meas.Level + 10 \log (1/duty\ cycle)$

$E.i.r.p = Av.Power + G,$

G = antenna gain in dBi.

Appendix C): Maximum Power Spectral Density

Test Requirement 47 CFR Part 15, Subpart C 15.407 (a)

Test Method: KDB 789033 D02 II F

Test Procedure:

For 5150-5725MHz:

1. Connect EUT RF output port to the Spectrum Analyzer through an RF attenuator
2. Set the EUT Work on operation frequency individually.
3. Set RBW = 1MHz.
4. Set the VBW $\geq 3 \times$ RBW. Detector = Peak. Trace mode = max hold.

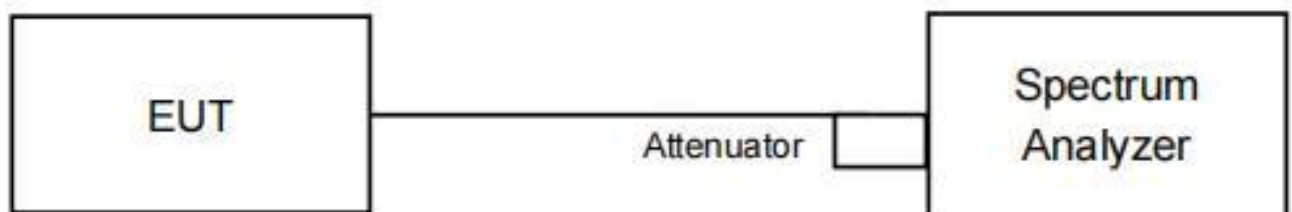
For 5725-5850MHz:

1. Connect EUT RF output port to the Spectrum Analyzer through an RF attenuator
2. Set the EUT Work on operation frequency individually.
3. Set RBW = 500KHz.
4. Set the VBW $\geq 3 \times$ RBW. Detector = Peak. Trace mode = max hold.

Limit:

Frequency band(MHz)	Limit
5150-5250	$\leq 17\text{dBm}$ in 1MHz for master device
	$\leq 11\text{dBm}$ in 1MHz for client device
5250-5350	$\leq 11\text{dBm}$ in 1MHz for client device
5470-5725	$\leq 11\text{dBm}$ in 1MHz for client device
5725-5850	$\leq 30\text{dBm}$ in 500 kHz
Remark:	The maximum power spectral density is measured as a conducted emission by direct connection of a calibrated test instrument to the equipment under test.

Test Setup Diagram



Result Table

ANT1:

TestMode	Freq(MHz)	Result [dBm/MHz]	Limit[dBm/MHz]	Verdict
11A	5180	2.88	≤11.00	PASS
	5200	2.49	≤11.00	PASS
	5240	1.22	≤11.00	PASS
	5745	-1.84	≤30.00	PASS
	5785	-4.34	≤30.00	PASS
	5825	-4.05	≤30.00	PASS
11N20SISO	5180	2.27	≤11.00	PASS
	5200	2.62	≤11.00	PASS
	5240	0.87	≤11.00	PASS
	5745	-2.43	≤30.00	PASS
	5785	-5.09	≤30.00	PASS
	5825	-4.71	≤30.00	PASS
11N40SISO	5190	-1.24	≤11.00	PASS
	5230	-5.10	≤11.00	PASS
	5755	-6.59	≤30.00	PASS
	5795	-6.80	≤30.00	PASS
11AC20SISO	5180	2.08	≤11.00	PASS
	5200	2.08	≤11.00	PASS
	5240	0.72	≤11.00	PASS
	5745	-2.40	≤30.00	PASS
	5785	-4.96	≤30.00	PASS
	5825	-4.18	≤30.00	PASS
11AC40SISO	5190	-0.98	≤11.00	PASS
	5230	-2.76	≤11.00	PASS
	5755	-6.74	≤30.00	PASS
	5795	-6.71	≤30.00	PASS
11AC80SISO	5210	-5.89	≤11.00	PASS
	5775	-9.90	≤30.00	PASS
11AX20SISO	5180	3.65	≤11.00	PASS
	5200	2.80	≤11.00	PASS
	5240	0.97	≤11.00	PASS
	5745	-3.98	≤30.00	PASS
	5785	-3.69	≤30.00	PASS
	5825	-3.48	≤30.00	PASS

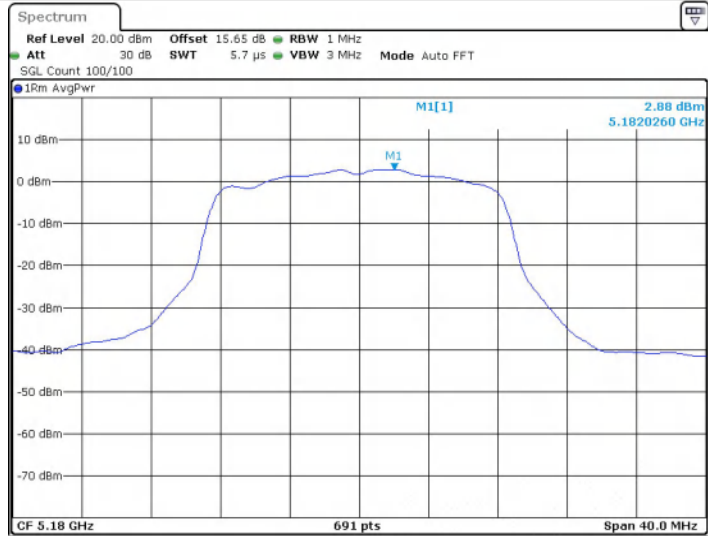
11AX40SISO	5190	0.44	≤ 11.00	PASS
	5230	-5.72	≤ 11.00	PASS
	5755	-6.98	≤ 30.00	PASS
	5795	-5.91	≤ 30.00	PASS
11AX80SISO	5210	-6.06	≤ 11.00	PASS
	5775	-12.91	≤ 30.00	PASS

Remark:

PSD = Meas PSD + Duty Cycle Factor

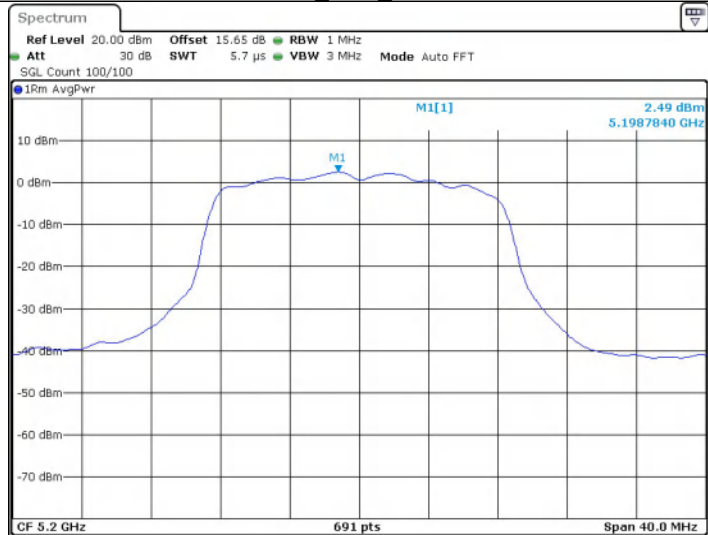
Transmitting in full-bandwidth single-user mode (Full RU) with all kinds of modulations, and at the lowest, middle, and highest data rates across the channel.

11A_Ant1_5180



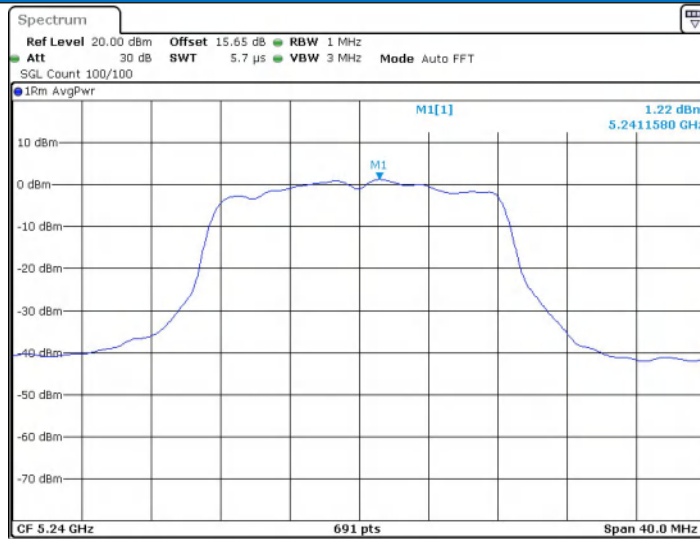
Date: 23.DEC.2025 17:04:43

11A_Ant1_5200



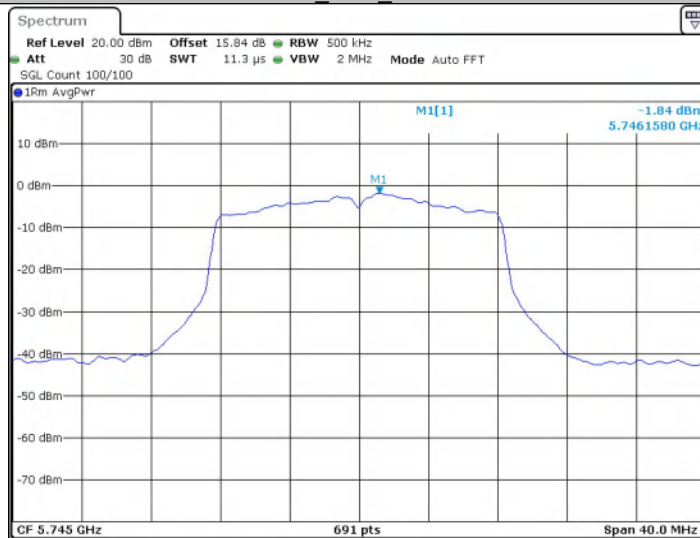
Date: 23.DEC.2025 17:07:12

11A_Ant1_5240



Date: 23.DEC.2025 17:08:34

11A_Ant1_5745



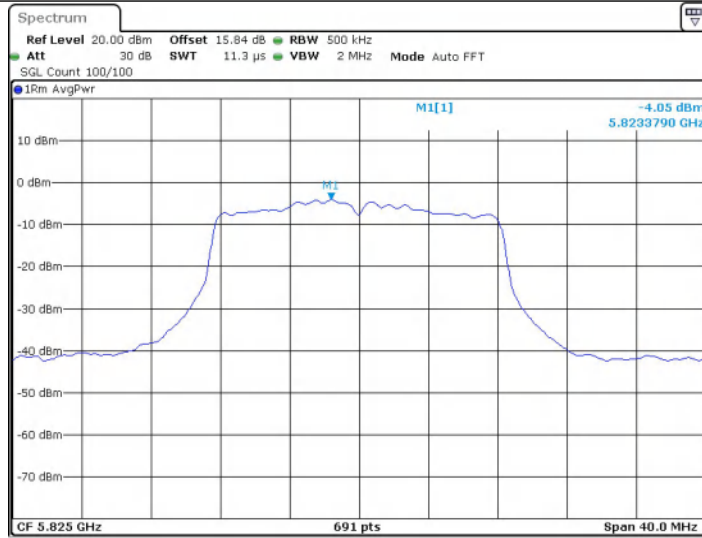
Date: 23.DEC.2025 17:11:24

11A_Ant1_5785



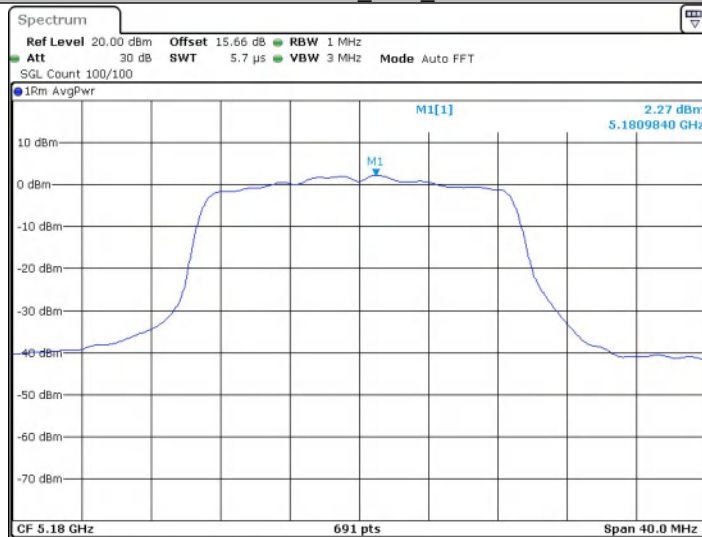
Date: 23.DEC.2025 17:13:32

11A_Ant1_5825



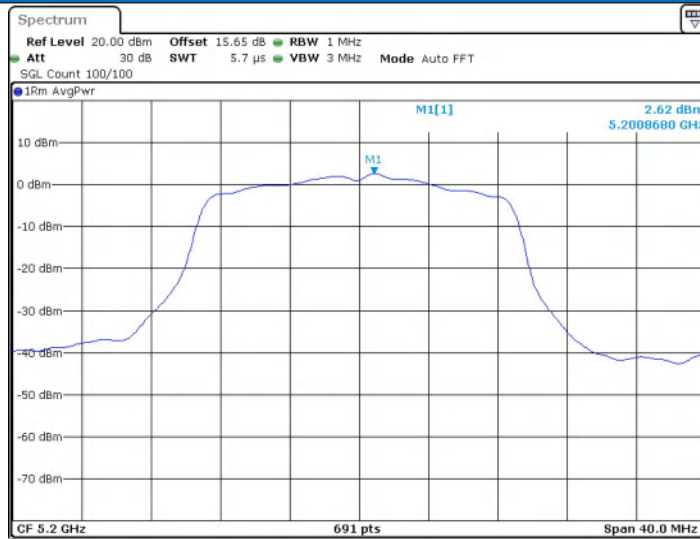
Date: 23 DEC 2025 17:18:40

11N20SISO_Ant1_5180



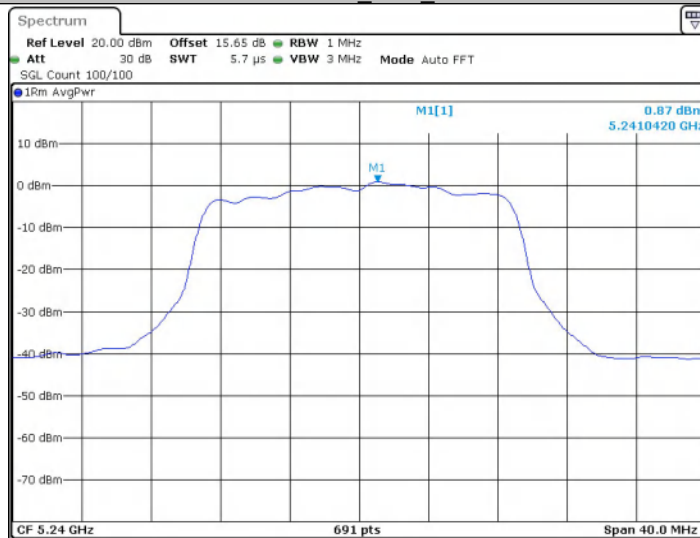
Date: 23 DEC 2025 17:32:12

11N20SISO_Ant1_5200



Date: 23.DEC.2025 17:35:05

11N20SISO_Ant1_5240



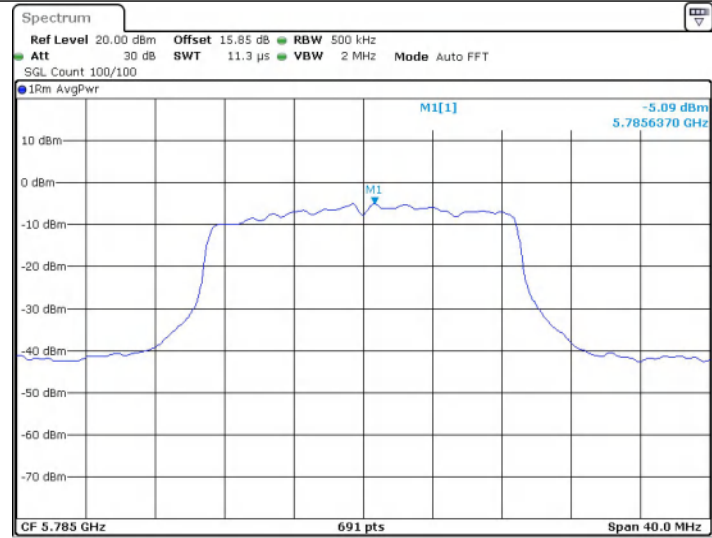
Date: 23.DEC.2025 17:37:42

11N20SISO_Ant1_5745



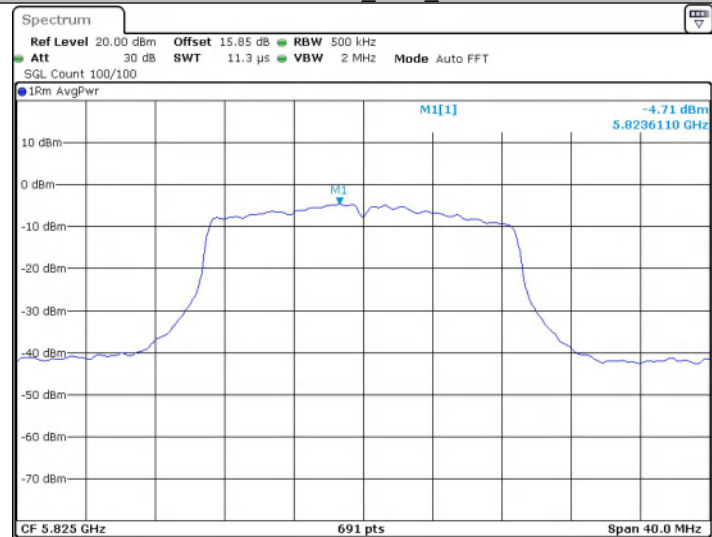
Date: 23.DEC.2025 17:39:31

11N20SISO_Ant1_5785



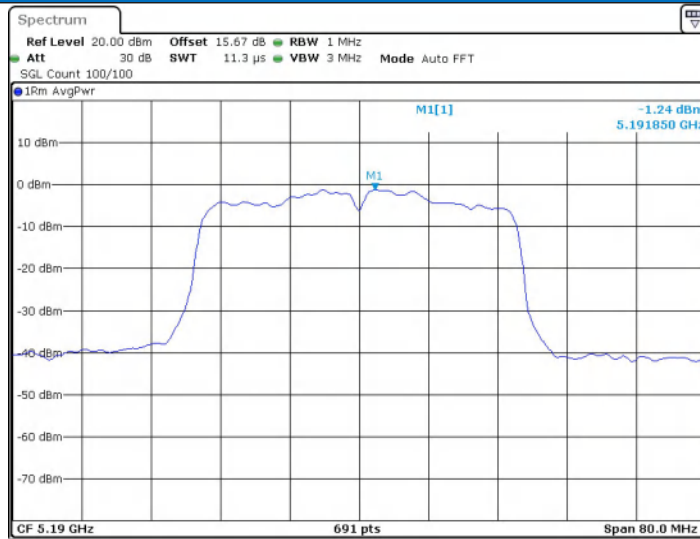
Date: 23 DEC 2025 17:42:43

11N20SISO_Ant1_5825



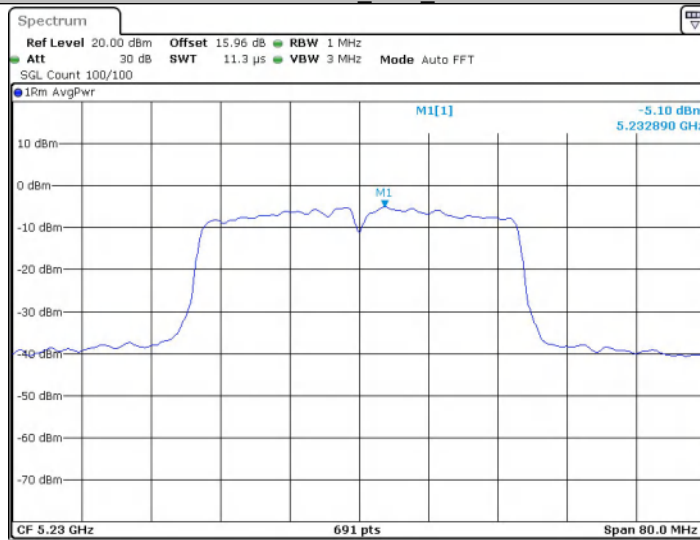
Date: 23 DEC 2025 17:45:57

11N40SISO_Ant1_5190



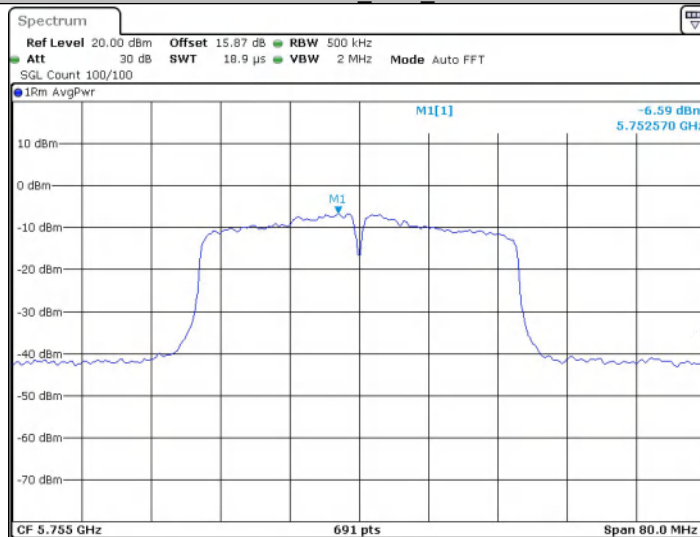
Date: 23 DEC 2025 17:47:43

11N40SISO_Ant1_5230



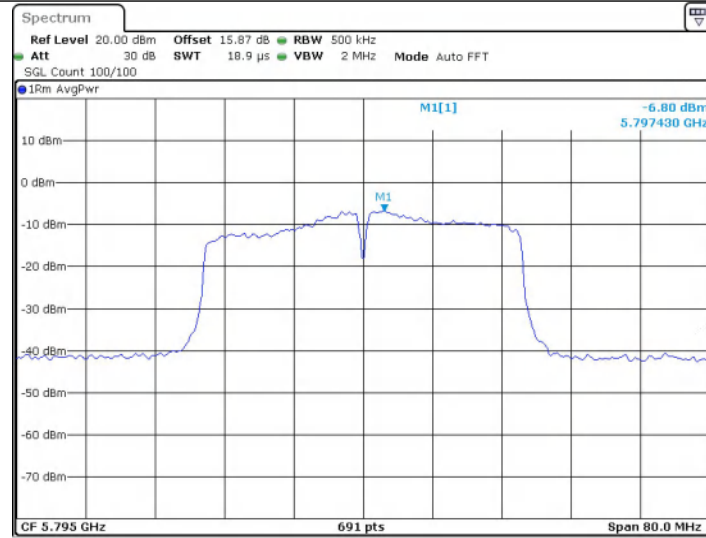
Date: 25 DEC 2025 14:39:28

11N40SISO_Ant1_5755



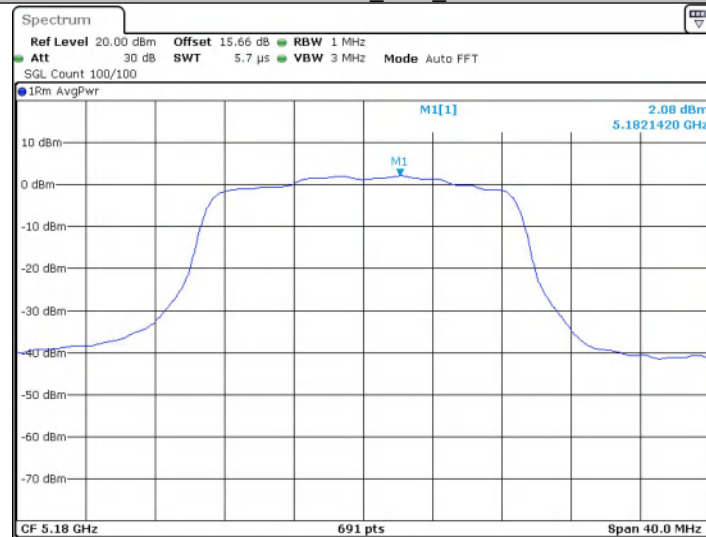
Date: 23 DEC 2025 18:36:51

11N40SISO_Ant1_5795



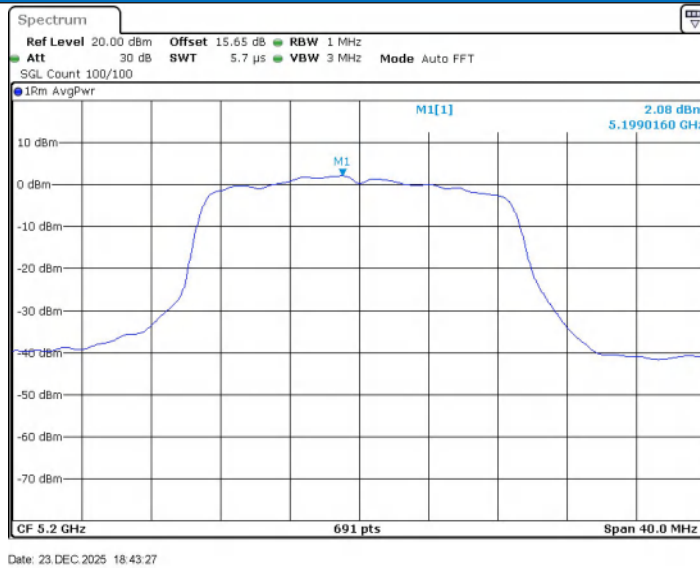
Date: 23 DEC 2025 18:39:10

11AC20SISO_Ant1_5180

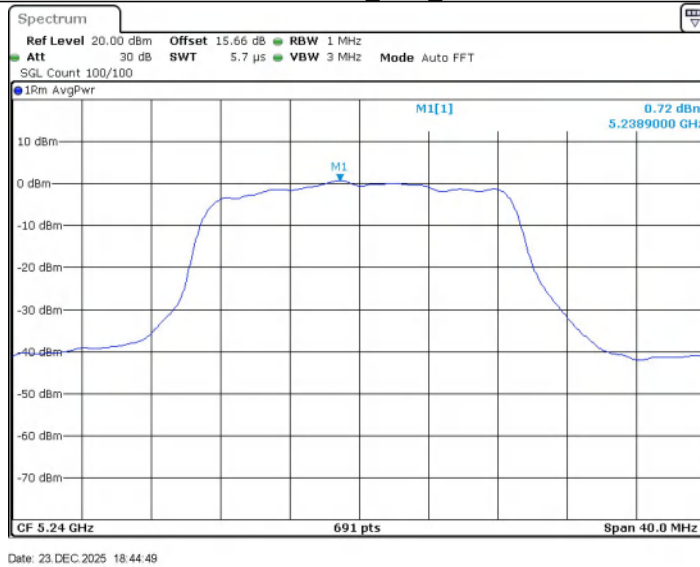


Date: 23 DEC 2025 18:40:51

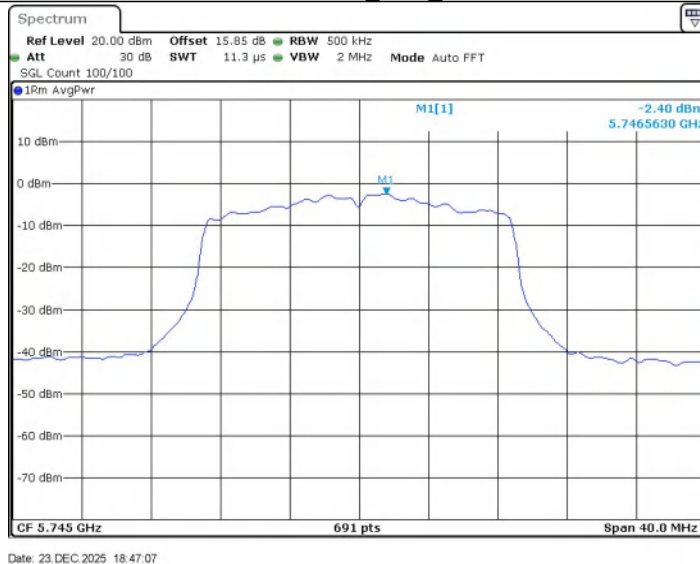
11AC20SISO_Ant1_5200



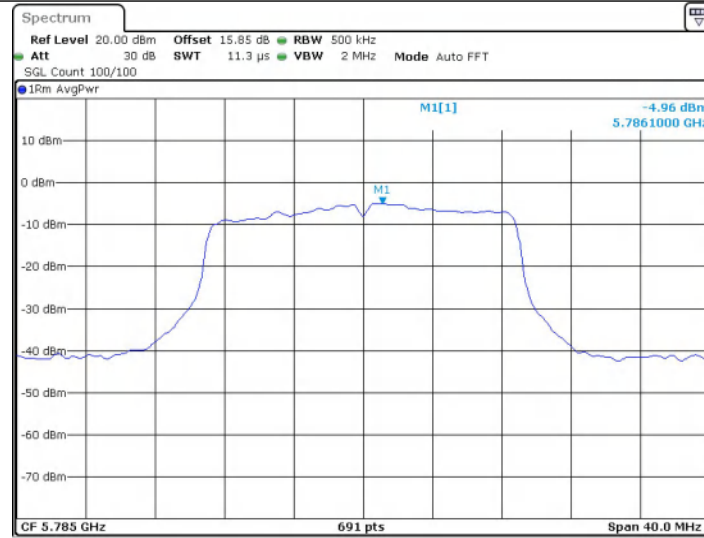
11AC20SISO_Ant1_5240



11AC20SISO_Ant1_5745

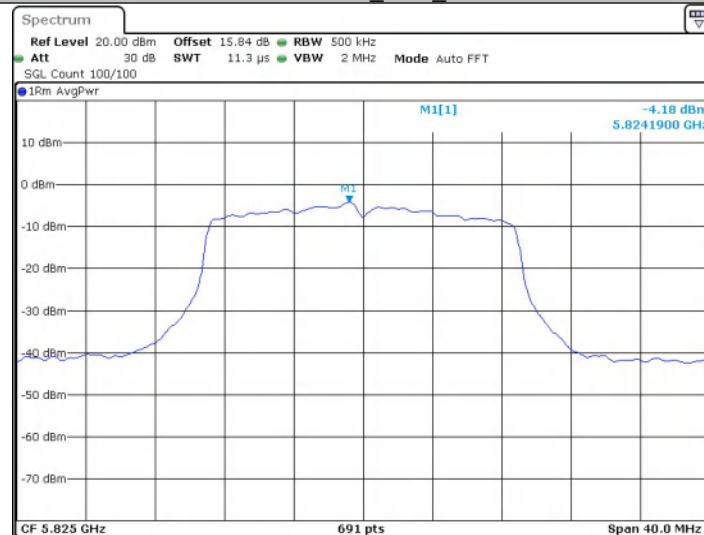


11AC20SISO_Ant1_5785



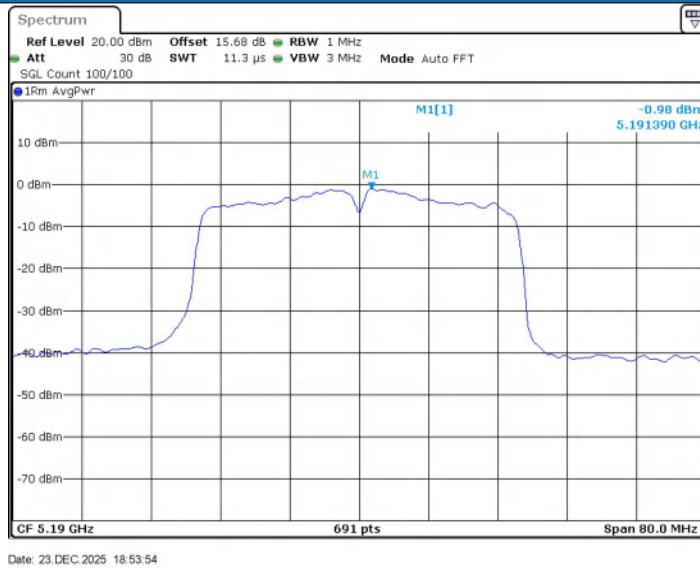
Date: 23 DEC 2025 18:50:15

11AC20SISO_Ant1_5825

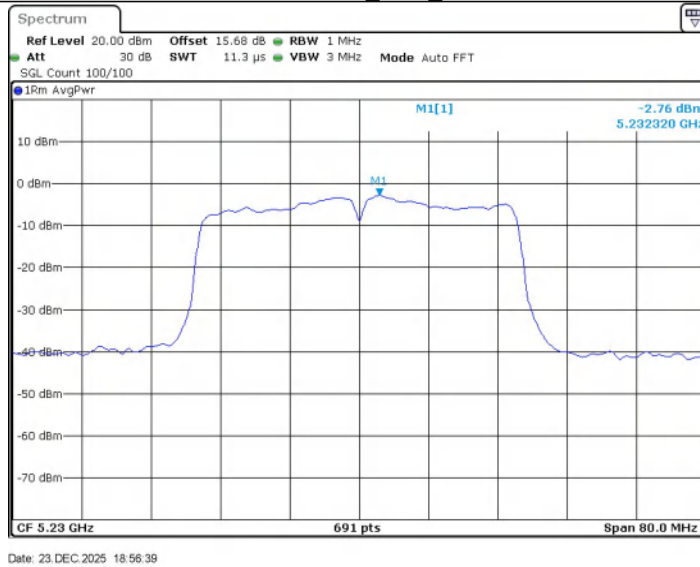


Date: 23 DEC 2025 18:51:23

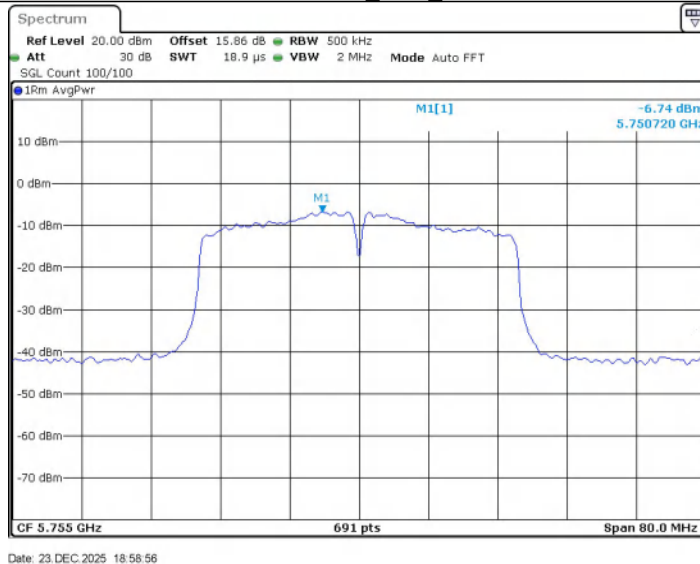
11AC40SISO_Ant1_5190



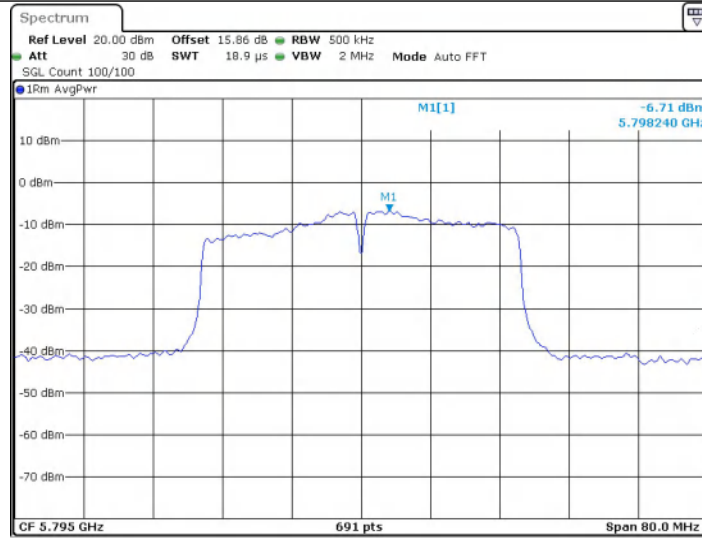
11AC40SISO_Ant1_5230



11AC40SISO_Ant1_5755

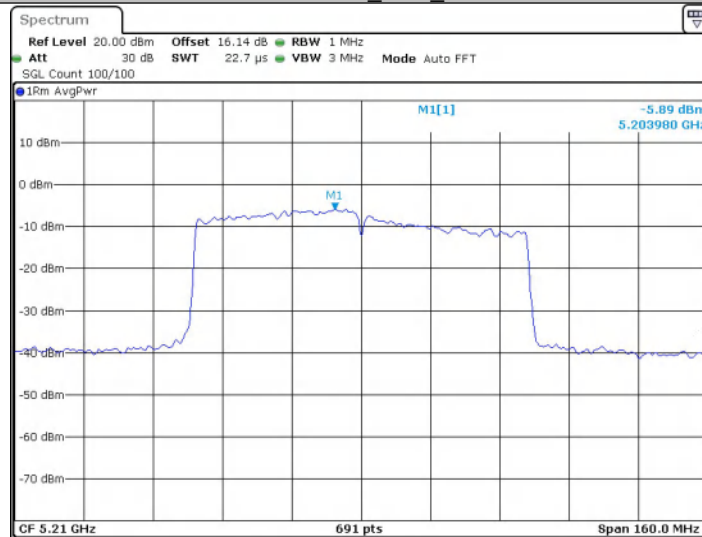


11AC40SISO_Ant1_5795



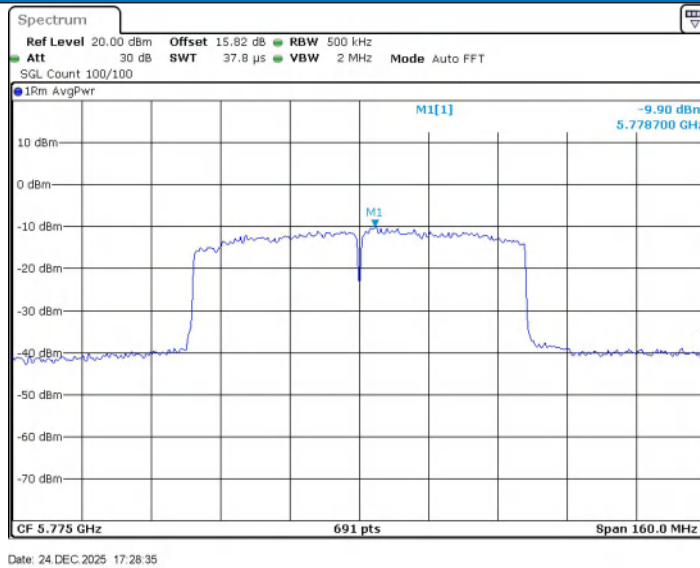
Date: 23 DEC 2025 19:00:51

11AC80SISO_Ant1_5210

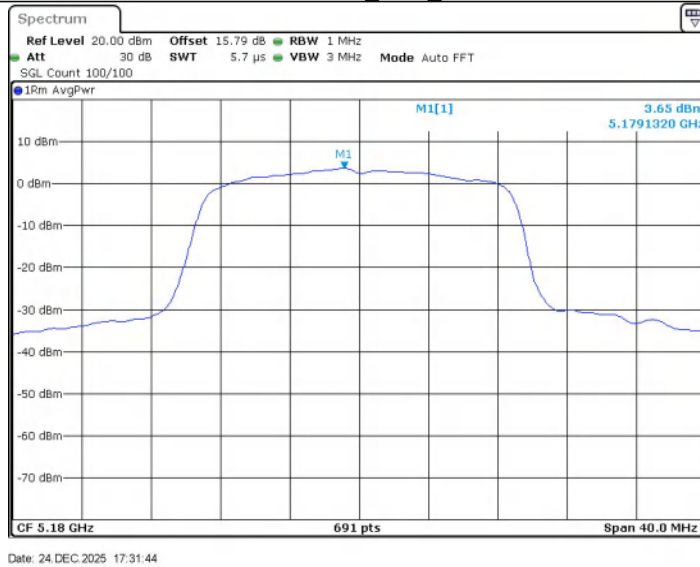


Date: 25 DEC 2025 11:47:07

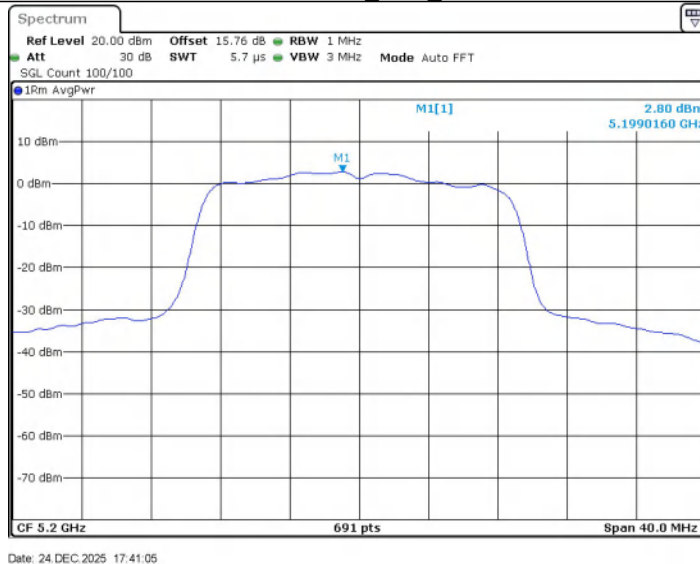
11AC80SISO_Ant1_5775



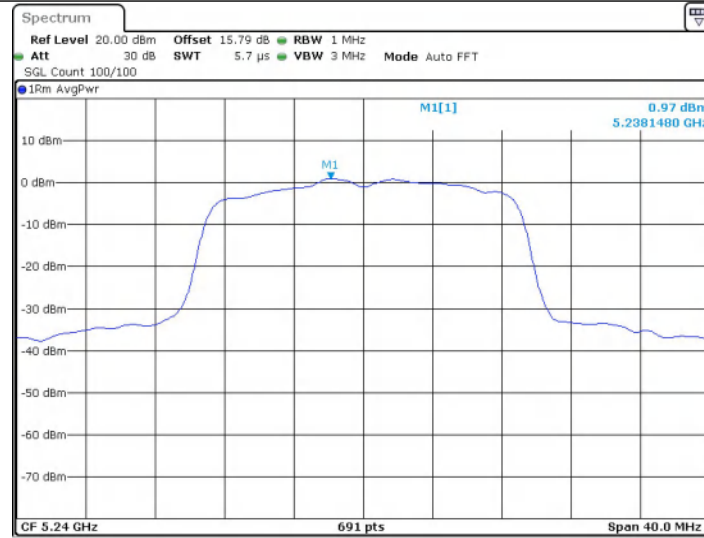
11AX20SISO_Ant1_5180



11AX20SISO_Ant1_5200

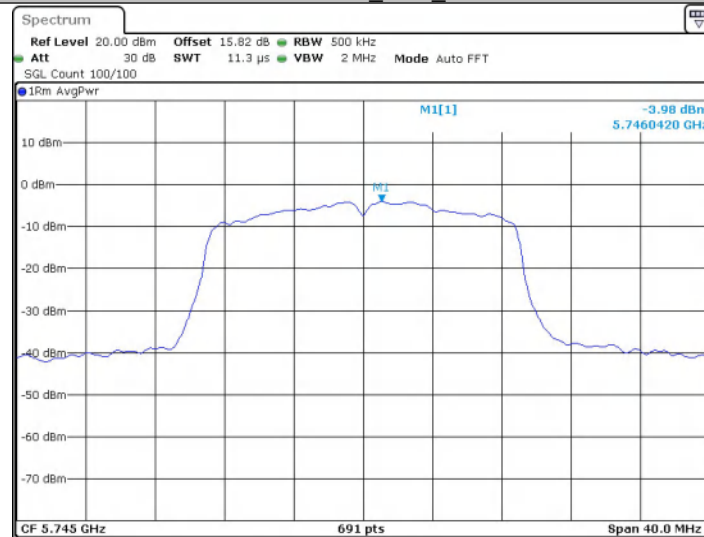


11AX20SISO_Ant1_5240



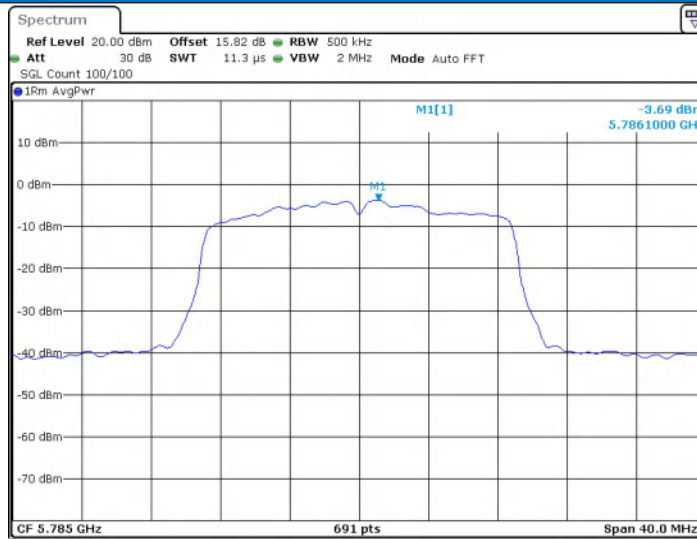
Date: 24 DEC 2025 17:44:17

11AX20SISO_Ant1_5745



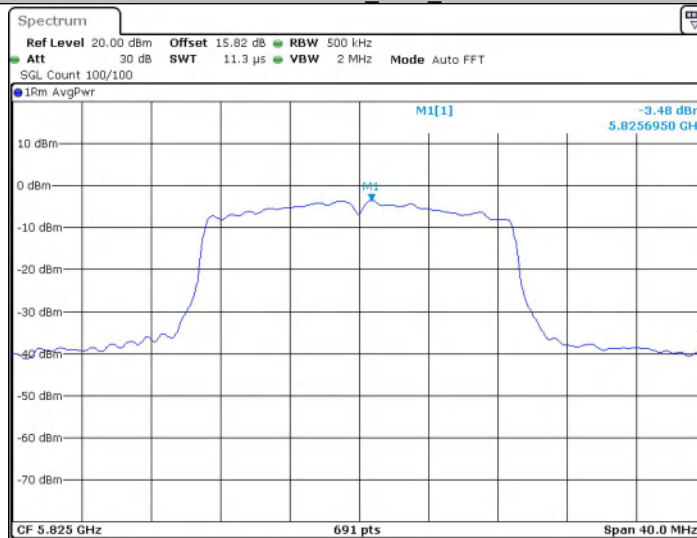
Date: 24 DEC 2025 17:49:20

11AX20SISO_Ant1_5785



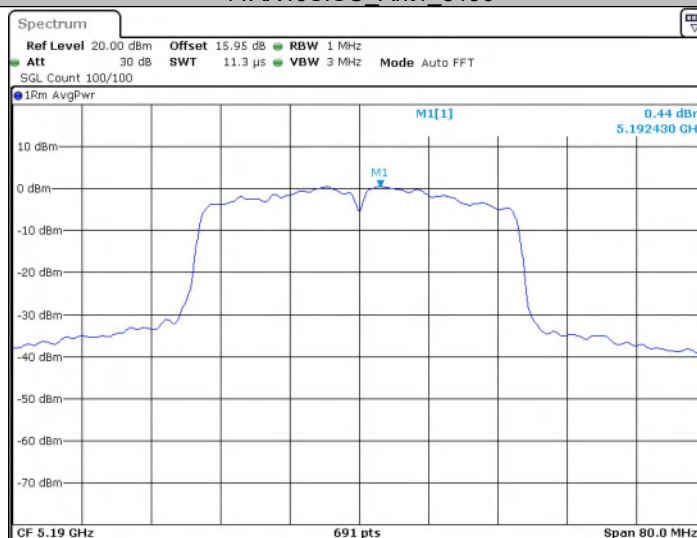
Date: 24 DEC 2025 17:50:59

11AX20SISO_Ant1_5825



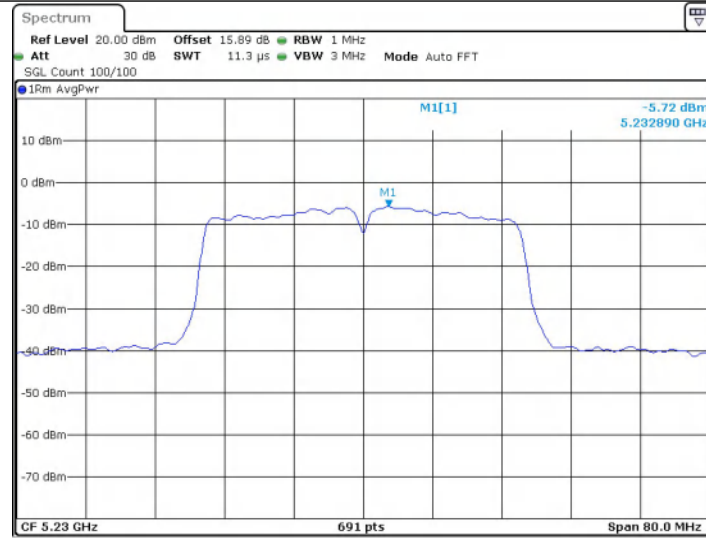
Date: 24 DEC 2025 17:52:09

11AX40SISO_Ant1_5190



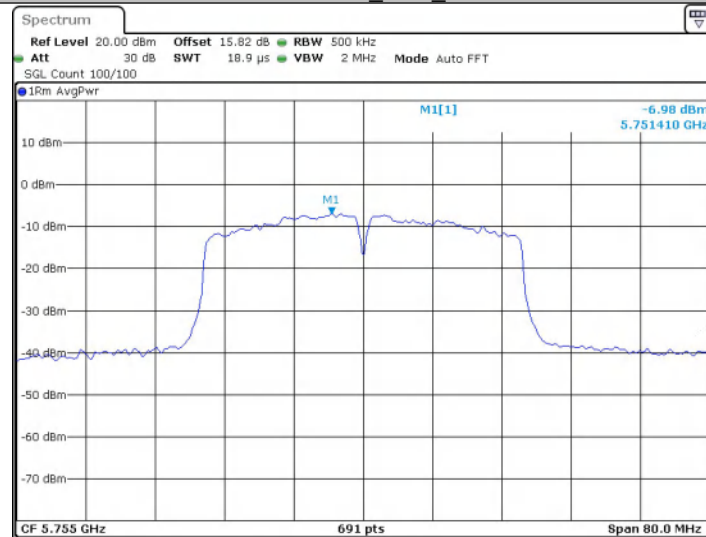
Date: 24 DEC 2025 17:54:25

11AX40SISO_Ant1_5230



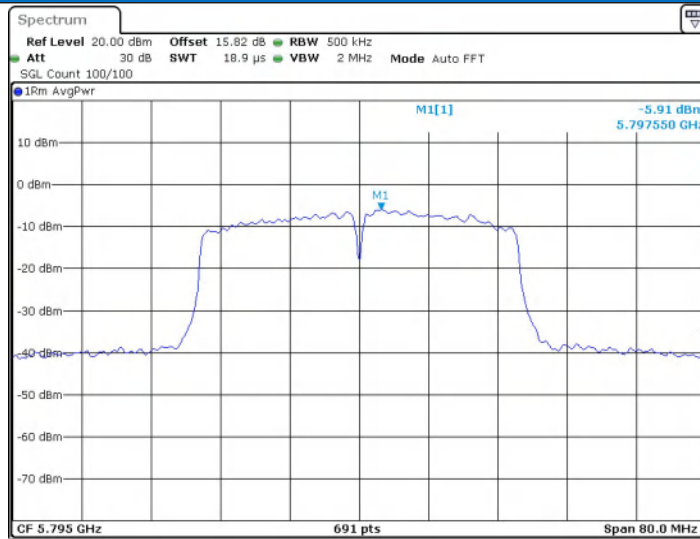
Date: 25 DEC 2025 11:53:13

11AX40SISO_Ant1_5755



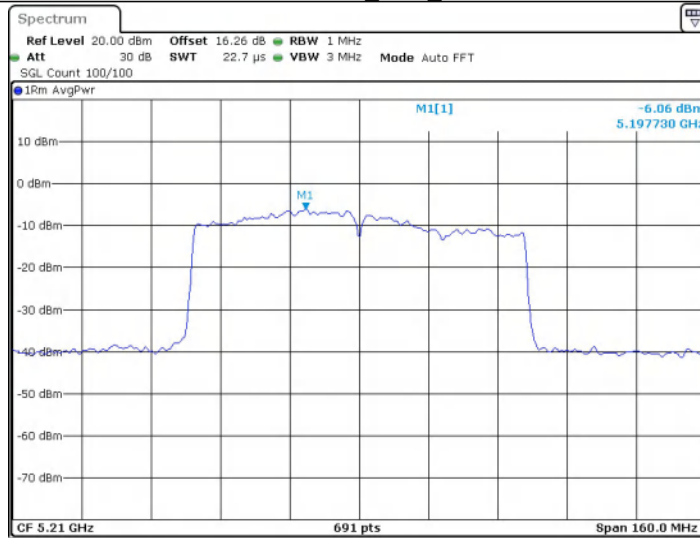
Date: 24 DEC 2025 18:47:47

11AX40SISO_Ant1_5795



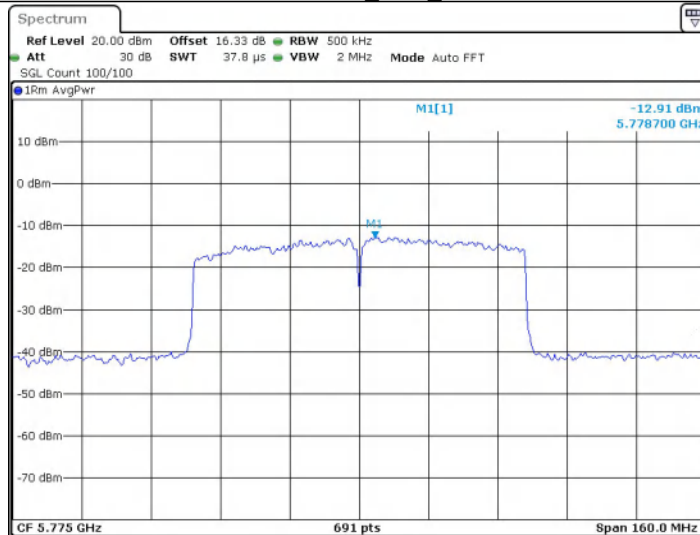
Date: 24 DEC 2025 18:50:32

11AX80SISO_Ant1_5210



Date: 25 DEC 2025 11:57:14

11AX80SISO_Ant1_5775



Date: 25 DEC 2025 12:01:46

ANT2:

TestMode	Freq(MHz)	Result [dBm/MHz]	Limit[dBm/MHz]	Verdict
11A	5180	3.69	≤11.00	PASS
	5200	2.69	≤11.00	PASS
	5240	0.61	≤11.00	PASS
	5745	-3.35	≤30.00	PASS
	5785	-3.66	≤30.00	PASS
	5825	-3.33	≤30.00	PASS
11N20SISO	5180	4.12	≤11.00	PASS
	5200	3.14	≤11.00	PASS
	5240	0.76	≤11.00	PASS
	5745	-4.07	≤30.00	PASS
	5785	-4.07	≤30.00	PASS
	5825	-4.05	≤30.00	PASS
11N40SISO	5190	1.08	≤11.00	PASS
	5230	-5.49	≤11.00	PASS
	5755	-6.68	≤30.00	PASS
	5795	-5.62	≤30.00	PASS
11AC20SISO	5180	3.72	≤11.00	PASS
	5200	3.47	≤11.00	PASS
	5240	1.56	≤11.00	PASS
	5745	-3.74	≤30.00	PASS
	5785	-4.38	≤30.00	PASS
	5825	-4.46	≤30.00	PASS
11AC40SISO	5190	0.86	≤11.00	PASS
	5230	-1.93	≤11.00	PASS
	5755	-7.37	≤30.00	PASS
	5795	-6.28	≤30.00	PASS
11AC80SISO	5210	-2.88	≤11.00	PASS
	5775	-8.83	≤30.00	PASS
11AX20SISO	5180	4.55	≤11.00	PASS
	5200	3.69	≤11.00	PASS
	5240	0.35	≤11.00	PASS
	5745	-3.56	≤30.00	PASS
	5785	-3.29	≤30.00	PASS
	5825	-2.82	≤30.00	PASS
11AX40SISO	5190	0.84	≤11.00	PASS

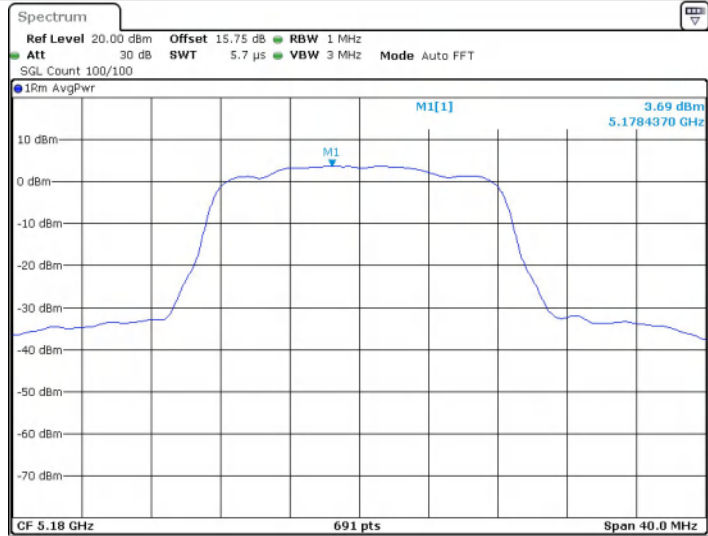
	5230	-3.16	≤ 11.00	PASS
	5755	-6.13	≤ 30.00	PASS
	5795	-5.35	≤ 30.00	PASS
11AX80SISO	5210	-3.26	≤ 11.00	PASS
	5775	-9.15	≤ 30.00	PASS

Remark:

PSD = Meas PSD + Duty Cycle Factor

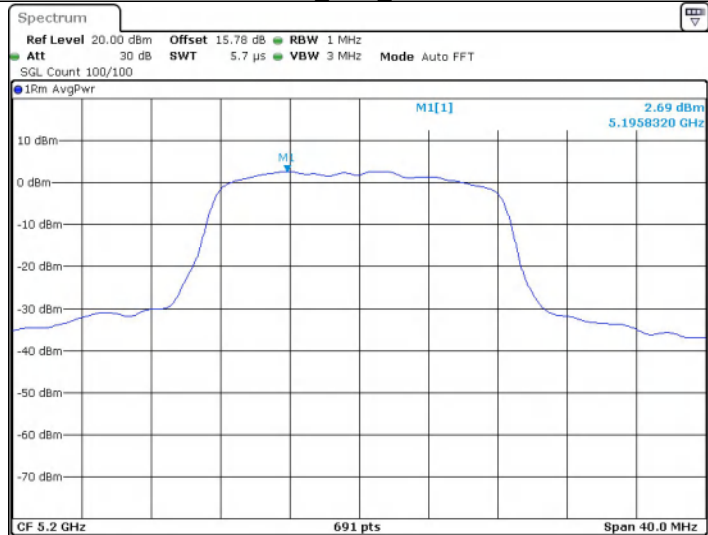
Transmitting in full-bandwidth single-user mode (Full RU) with all kinds of modulations, and at the lowest, middle, and highest data rates across the channel.

11A_Ant2_5180



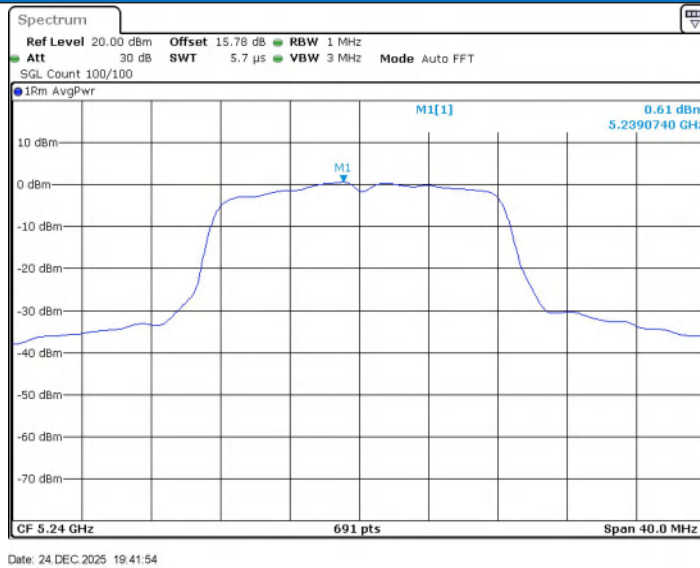
Date: 24 DEC 2025 19:37:34

11A_Ant2_5200

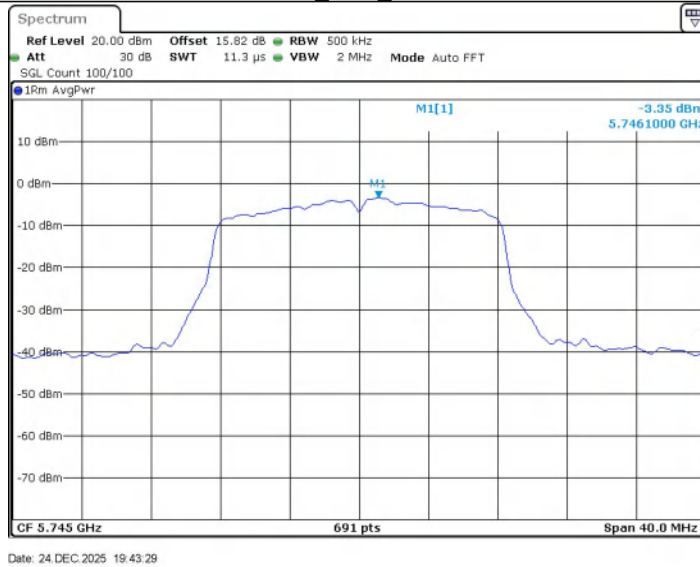


Date: 24 DEC 2025 19:40:53

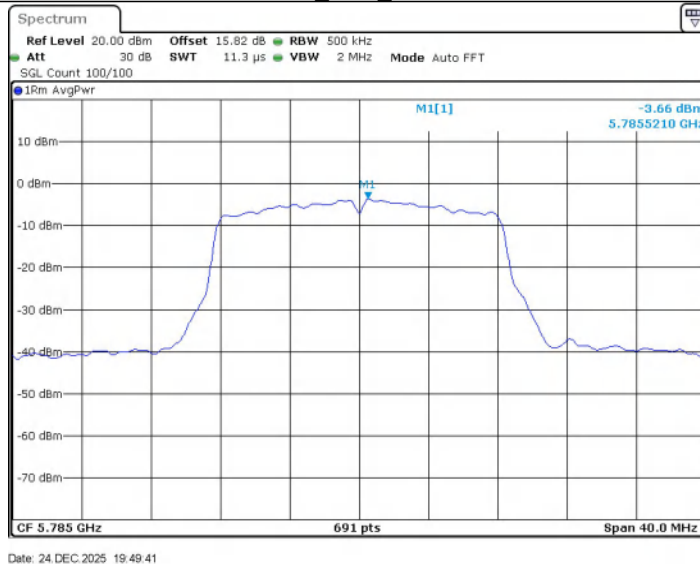
11A_Ant2_5240



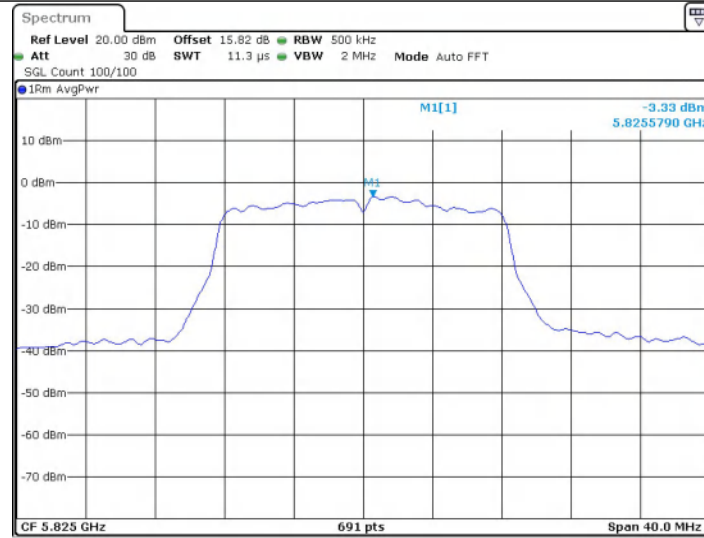
11A_Ant2_5745



11A_Ant2_5785

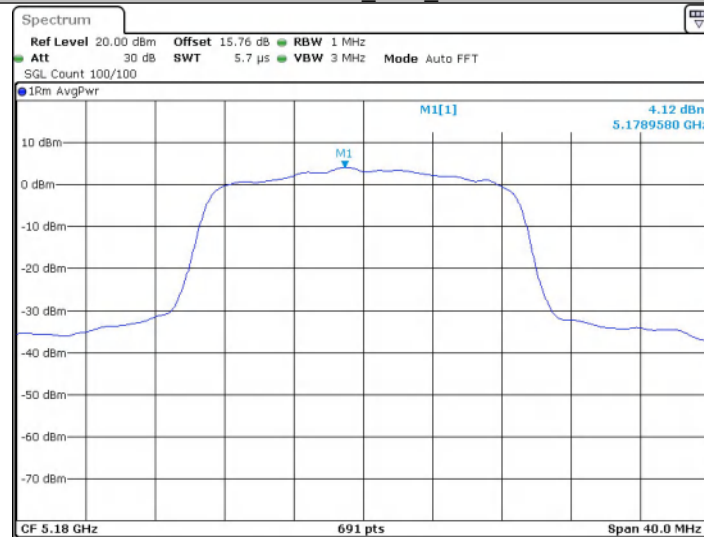


11A_Ant2_5825



Date: 24 DEC 2025 19:51:39

11N20SISO_Ant2_5180



Date: 24 DEC 2025 19:53:12

11N20SISO_Ant2_5200