Intel® Wi-Fi 6 AX201 (Harrison Peak 2) and Wi-Fi 6 AX101 (Harrison Peak 1)

External Product Specification (EPS)

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Revision History

Revision	Description	Date
0.5	Initial release	August 2017
0.6	Added Jasper Lake platform and other miscellaneous changes	November 2017
0.7	Added PCH-N/Quasar-V and SUSCLK/P_32k changes	November 2017
0.71	Added fixes and updates from the first round of stakeholder reviews: • 32kHz clock: External clock can be used (the default is internal) • RGI_RSP and BRI_RSP do not have PD on them (updated in all relevant tables) • Added internal-USB port# for CNVi usage	December 2017
0.72	Updated PU/PD information with more detailed explanations Added chapters for power-up flows and product IDs and an appendix for BIOS settings	January 2018
0.73	Internal changes; updated PDG section	January 2018
0.8	Small update to HrP SKUs table Added clarification to the Peak Current consumption table Added KPIs – Notice those are early estimated numbers Updated and added clarification to the PU/PD section Updated the Power-On/Init Signals flow example Added a section for Product IDs and Values Added a GPIO Mapping section Renumbered some sections	February 2018
0.81	Fixed typos Added alignment to new platform programs Updated SKU table Updated product architecture CNVio characteristic impedance changed to 85ohm Updated SUSCLK accuracy Updated BRI/RGI Rise, Fall Time change to 7ns 30%-70% Added Wi-Fi channels Added Power KPIs Added explanation as to why a power control switch is not recommended Updated ICL GPIOs RF_RESET, MODEM_CLKREQ	July 2018
0.9	Changed product name to Intel® Wi-Fi 6 AX201 Updated KPIs Updated M.2 Pin List (adding Platform side and Spec definitions) Clarified TDP and Thermal test conditions	Oct 2018
0.91	Updated Section 9 to align with TGL CNVi PDG	Nov 2018

Revision	Description	Date
0.92	Added name WiFi Product changes reference Aligned with Cyclone Peak for the shared interfaces (LED-RF-Kill…) and set the same format Updated KPI formats (from PRD) Fixed typo in vPro version (13.0) Updated BIOS CNV as appendix	Nov 2018
0.93	Updated BT-Quasar-USB mapping table (taken from PCH/BIOS settings) Updated KPIs Typo and clarification fixes (throughout) Updated Power supply section (adding Vbat case)	Jan 2019
0.94	Fixed typo in pin description #32 in Table 3–1: BRI changed to RGI Added Figure 9–3 as part of design guidelines	January 28, 2019
0.95	Added Table 9–2 – RF Companion module 2230 pin list Updated design guidelines Updated throughput KPIs Updated the 32KHz slow clock description Deleted CPU utilization from Section 6 Deleted previous Section 10.4, "Product name change" Updated power-up sequence Updated WiFi Tx power per MCS table Updated WiFi Rx Sensitivity Updated BT Tx and RX KPIs Added Tx regulatory limits Removed the "optional" comments from HW-RF-Kill /Wireless disable signals	April 18, 2019
0.96	Updated Tx per MCS tables with correct SRD data Updated CNVio clock rate "up to 2500Mbps per lane" in Section 9.13.1 Corrected pin numbers in the Power supply de-coupling section, 9.17	May 2, 2019
0.97	Adding Regulatory Tx Power limit table (in Regulatory section Removing the "optional" coments from HW-RF-Kill /Wireless disable signals Updated/aligned PDG section Fixed typo of "Intel LTE 7362" changed to Intel LTE 7360" Added scan capabilities table 7-2	June 13, 2019
1.0	Updated titles in PDG sections to identify sections relevant to CNVi solutions, Discrete solutions, or both.	June 25, 2019
1.1	Fixed typo in Section 7.2.1 (OTP + 1 dB -> OTP + 0.5 dB)	July 15, 2019
1.2	Updated Tx power per MCS with MIMO info in Table 6-1, Table 6-2, and Table 6-3	July 16, 2019
1.21	Added accuracy for Wi-Fi Rx KPIs	July 22, 2019

Revision History

Revision	Description	Date
1.3	Added/merged HrP1 EPS module info into this document Added NV SKU to SKU list Fixed typo mW → mA in power consumption Updated BT Rx KPIs Updated regulatory Tx power for ch13 Fixed Tx power tables for ch13 Updated BT Tx KPI table format in Section 6.2.4, and included the entry for BLE(LR-125k)	September 25, 2019
1.4	Fixed Rise/Fall time definition for 1.8v-based signals used as inputs (and not used as outputs) in Table 3-3.	October 31, 2019
1.41	Fixed typo in introduction	November 6, 2019
1.42	Added Section 7.5, "SAR Tx power limits" with Table 7–15, "SAR Tx power limits dependency on distance"	November 20, 2019
1.43	Fixed typo, returned accuracy +/– 1dB designation to Tx per MCS tables	December 23, 2019
1.44	Renamed Section 6.2.4 and Table 6-7 to "Bluetooth® sensitivity"; updated the Bluetooth Rx sensitivity values per the latest test results.	January 14, 2019
1.5	Removed previous Table 5-3, Thermal operating conditions	March 12, 2020

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Abbreviations

Term	Description
ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
AMP	Generic Alternate MAC/PHY
AMT	Active Management Technology
AP	Access Point
API	Application Programmer's Interface
BB	Base Band – the DSP/Phy layer in the MAC-BB chip
BCS	Best Channel Selection
BQE	Bluetooth Qualification Expert
BRI	Bluetooth Radio interface, between JfP and Pulsar
BSS	Basic service Set
BT	Bluetooth®
CA	Concept Approval – first approval meeting in a product's lifecycle
CCA	Clear Channel Assessment: Logical function in the physical layer (PHY) that Determines the current state of use of the wireless medium
CCB	Change Control Board
CCX	Cisco Client Extensions
CLINK	Control Link
CMP	Core Multiprocessing
CNV	Connectivity
CNVi	Integrated connectivity solution
CNVio	High speed data interface for CNVi
Coex	Coexistence
COS	Capability OS (EIT related)
CRF	Companion RF Chip/Module of the CNVi
DAC	Digital to Analog Converter
DC	Direct Current
DCR	Design Change Requirement
DIA	Development Investment Approval – meeting where the organization funds product planning
Doze Mode	In Power Save Mode
DPHY	Differential PHY (high-speed serial bus) – Old Internal Name for the CNVio – it is a misleading name, Please do not use anymore – replace with "CNVio"

Term	Description
E2E	End to End – work with Cisco or other AP vendor for full feature solution that requires end-to-end coordination (both client and AP), e.g., VOIP, also known as BCWS (Business Class Wireless System/Solution)
EAP	Extensible Authentication Protocol
EIB	Extended Ingredient Brand
EIRP	Equivalent isotropically radiated power
EoU	Ease of Use
GPIO	General Purpose Input/Output
HCI	Host Controller Interface
HLD	High-Level Design – design documents that guide product implementation
HrP	CNVi Companion RF Chip/Module – Harrison Peak (Second Gen)
I/O	Input/Output
I2C	Inter-Integrated Circuit bus
IBSS	Independent Basic Services Set (AKA Ad Hoc)
IEEE	Institute of Electrical and Electronics Engineers, the standards body for setting Ethernet standards
IHV	Independent Hardware Vendor
IOSF	Intel On-chip System Fabric
IPA	Implementation Plan Approval – a meeting where the organization approves the program Plan of Record and commits resources to develop the product
IPD/GID	Intel Product Dealer/Genuine Intel Dealer – a channel reseller authorized to sell Intel products
ISH	Integrated Sensor Hub
ISV	Independent Software Vendor
JfP	CNVi Companion RF Chip/Module – Jefferson Peak (First Gen)
LAN	Local Area Network
LCD	Liquid Crystal Display
LDO	Low-Dropout Regulator
LLD	Low-Level Design – specifis implementation details so the product can be sustained
LNA	Low Noise Amplifier
LOS	Line of sight
LTE	Long-term evolution (a mobile phone standard)
MAC	Media Access Controller
MIB	Management Information Base
MIPI	Mobile Industry Processor Interface
MPG	Mobile Platform Group
MRD	Marketing Requirements Document – provides the business case, marketing definition, target market, requested timeline and functional requirements for the product to be successful in the marketplace
NDIS	Network Driver Interface Specification

Term	Description
NIC	Network Interface Card
NLOS	Non Line Of Sight
NMA	Network Management Application (renamed to NMS)
NMS	Network Management Software
NOS	Network Operating System
OEM	Original Equipment Manufacturer
OTP	One Time Programmable non-volatile memory
PAN	Personal Area Network
PCH	Platform Control Hub
PCPL	PC Product Line (Division in WCS)
PHY	Physical (layer)
PLBP	Product Line Business Plan (Division-level stratetic plan)
PLC	Product Life Cycle
PMP	Program Management Plan – describes how program activities will be managed.
POP	Product Overview Proposal – describes the product vision, market, and business opportunity
PQM	Platform Quality Methods, a group within CQN. See http://pqm.intel.com
PRD	Product Requirement Document – describes requirements to enable product planning and development; completes requirements begun in the POP
PSK	Pre Shared Key
Pulsar/Quasar	The integrated IP part of the CNVi (First Gen/Second Gen)
QoS	Quality of Service
RF	Radio Frequency
RGI	Radio Generic interface, between JfP and Pulsar
ROS	Recovery OS (EIT related)
RTC	Real-Time Clock
SDK	Software Developer's Kit – helps third-party developers incorporate an Intel product into their own
SLRP	Strategic Long Range Plan – Intel's corporate strategic plan
SoC	System on Chip
SOS	Service OS (EIT related)
SOW	Statement of Work – defines product customizations required for a specific customer
TDK	Test Drive Kit – a version of a product that a customer can try out before buying
TDP	Thermal Design Power
TPC	Transmit Power Control
TPS	Technical Product Specification – what a direct Intel customer needs to understand the product
UART	Universal Asynchronous Serial Bus

Term	Description
UI	User interface
USB	Universal Serial Bus
WCS	Wireless Connectivity Solution (organization in iCDG, Intel)
WFA	Wi-Fi Alliance
Wi-Fi	Wireless LAN

§

1 Introduction

There are two kinds of Harrison Peak modules: the main "Intel® Wi-Fi 6 AX201" module (HrP 2x2), and its derived Low Cost product, based on a 1x1 Wi-Fi module, named "Intel® Wi-Fi 6 AX101" (HrP 1x1).

These products share the same M.2 interfaces and electrical signal behaviors; the only real difference is the 1x1 Wi-Fi behavior, and as so, only 1x1 subset KPIs are relevant to the HrP1 case.

Intel® Wi-Fi 6 AX201

The Intel® Wi-Fi 6 AX201 module, code named Harrison Peak 2 or HrP2, is an M.2 connectivity RF companion module for notebooks, tablets, and PCs.

When combined with the Intel System on Chip (SoC) that supports Connectivity Integration (CNVi), it supports the following radio technologies:

- 802.11abgn+acR2+ax MIMO 2x2
- Bluetooth® 5.0x

Intel® Wi-Fi 6 AX101

The Intel® Wi-Fi 6 AX101 module, code named Harrison Peak 1 or HrP1, is an M.2 connectivity RF companion module for notebooks, tablets, and PCs.

When combined with the Intel SoC that supports Connectivity Integration (CNVi), it supports the following radio technologies:

- 802.11abgn+acR2+axwith 1 antenna and 1 special stream (1x1 for the Wi-Fi)
- Bluetooth® 5.0x

The products provide a highly-integrated solution; the silicon design is based on the 28 nm process. It is a second generation for the new SoC-integrated architecture, which splits the Wi-Fi and Bluetooth* radio blocks into an integrated MAC block, residing in the Intel SoC, and the PHY/RF block, residing in the RF companion module. In addition, it implements the new Wi-Fi-6 spec (based on IEEE802.11ax). The increased performance and efficient operation of Wi-Fi 6 makes it an ideal complement to cellular standards and an integral part of 5G. This solution provides a higher level of integration with Intel platforms, combined with an improved low-power solution and a set of advanced capabilities. The Harrison Peak module uses a Wi-Fi-2x2 (HrP2) or 1x1 (HrP1) chip, has two RF chains for Wi-Fi in the HrP2 case and one RF chain for Wi-Fi in HrP1 case, and in parallel, one of the chains shares an antenna with the Bluetooth Chain.

The products are designed to be part of the Intel® Ice Lake, Comet Lake, and even Rocket/Tiger/Jasper Lake platforms, supporting Microsoft* Windows* as well as the Google* Chrome* OS and Linux*.

1.1 Reference documents/records

Table 1–1 lists companion documents for additional reference.

Table 1-1 Reference documents

	Document #	Title
Ref 1	573525	*Intel® Wireless-AC 9461 and 9462 Jefferson Peak 1 External Product Specification*
Ref 2	573970	*Using a Load Switch for Intel CNVi Designs White Paper*
Ref 3	574625	*Ice Lake Platform Controller Hub PCH BIOS Specification*
Ref 4	571119	*Gemini Lake Platform Intel Architecture Firmware Specification Volume 2 of 2 BIOS Specification*
Ref 5	559910	*Intel Connectivity Platforms BIOS Guidelines*

1.2 Key features

Table 1-2 Key features (when connected to the MAC part residing in the SoC)

Feature	Harrison Peak 2
Platform	Lead platform: Ice Lake Y, U, H, DT It shall also be integrated into: Comet Lake, Rocket Lake, Jasper Lake, and Tiger Lake Connected standby and traditional platform types
Form Factor and SKUs	– M.2 2230 – M.2 1216-soldered down module With 2x2 version (2 antennas, 1 of them is a shared BT/Wi-Fi antenna) • And in the next platforms wave adding also 1x1 SKU
Wi-Fi	High performance low power dual band Pre-Standard-802.11ax 2x2 (HrP2) or 1x1 (HrP1) with 160MHz channel support (in the HrP2 case)
Bluetooth®	Bluetooth® 5.0 (5.1[2])
Host Interfaces	Wi-Fi: PCIe based (Internal to the SoC) BT: USB based (Internal to the SoC), optional UART/I2S (Internal to the SoC) AMT: CLINK (Internal to the SoC, HrP2 only)
Interfaces to the SoC	Wi-Fi: CNVio Gen2 (Intel proprietary bus inspired by the DPHY low power interface) BT: BRI asynchronous serial bus (Intel proprietary) Control: RGI asynchronous serial bus (Intel proprietary) Notice – No shared clk (as was in previous product generation) (These interfaces connect the RF companion module to the MAC part which is integrated into the Intel SoC)
Wi-Fi Alliance certifications	802.11a/b/g/n/ac/ax(Pre-Standard) , WPA/2 Personal and enterprise, WPS2, PMF, WMM, WMM-PS, WFD, Miracast, Passpoint R2, Voice Personal
Wi-Fi-Bluetooth Coex	MIMO TX/TX and Rx/Rx Concurrency
LTE Coex	Real-Time and Non Real-Time, LTE filter (supported by one specific HrP2 SKU)

Feature	Harrison Peak 2
Power	Lower Active Power based on improved process technology
Performance (Wi-Fi)	TX Burst, TCP packet reordering, MSIx for reduced multi-core CPU load upto MCS11
vPro	AMT 13.0 (in the HrP2 case)
Smart SKU	Dynamic Regulatory SKU enabling automatic channel map and output power changes depending on the regulations of the country where it is operating
CNVi/Discrete auto-detect	Supports auto-detection by the SoC and by BIOS
Operating System	Windows 10*, Linux*, Chrome*

NOTE:

1. This module must be used with an Intel ICL SoC that supports integrated connectivity (ICL CNVi).
2. Additional future platform support is expected.
3. Real-time and Non-real-time LTE coexistence supported with Intel LTE 7360-7660.
4. The HrP module uses a Wi-Fi-2x2 chip and has two RF chains for Wi-Fi. For a 1x1 based solution, see **Ref 1**.

Figure 1–1 Harrison Peak 2 module block diagram

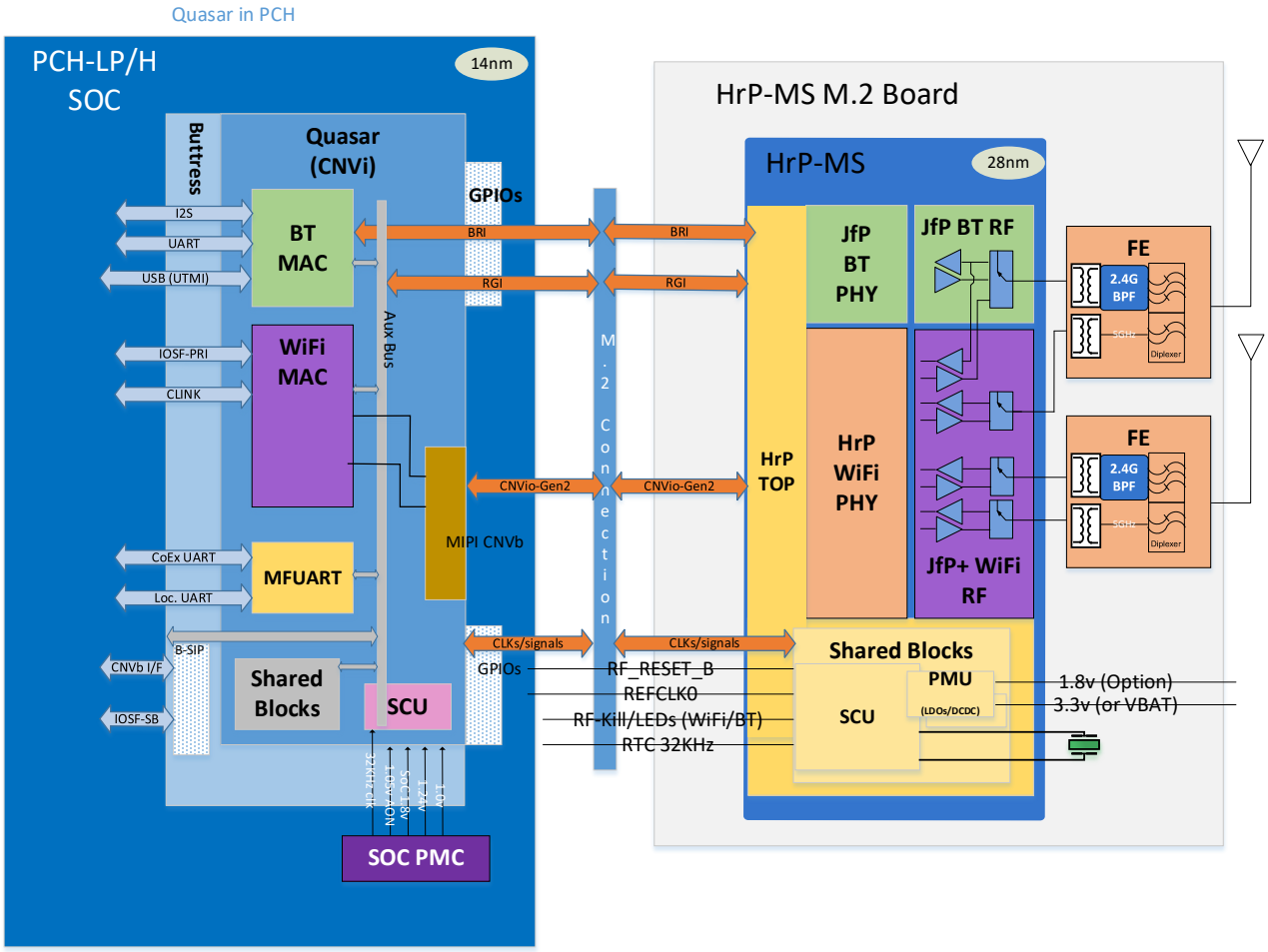
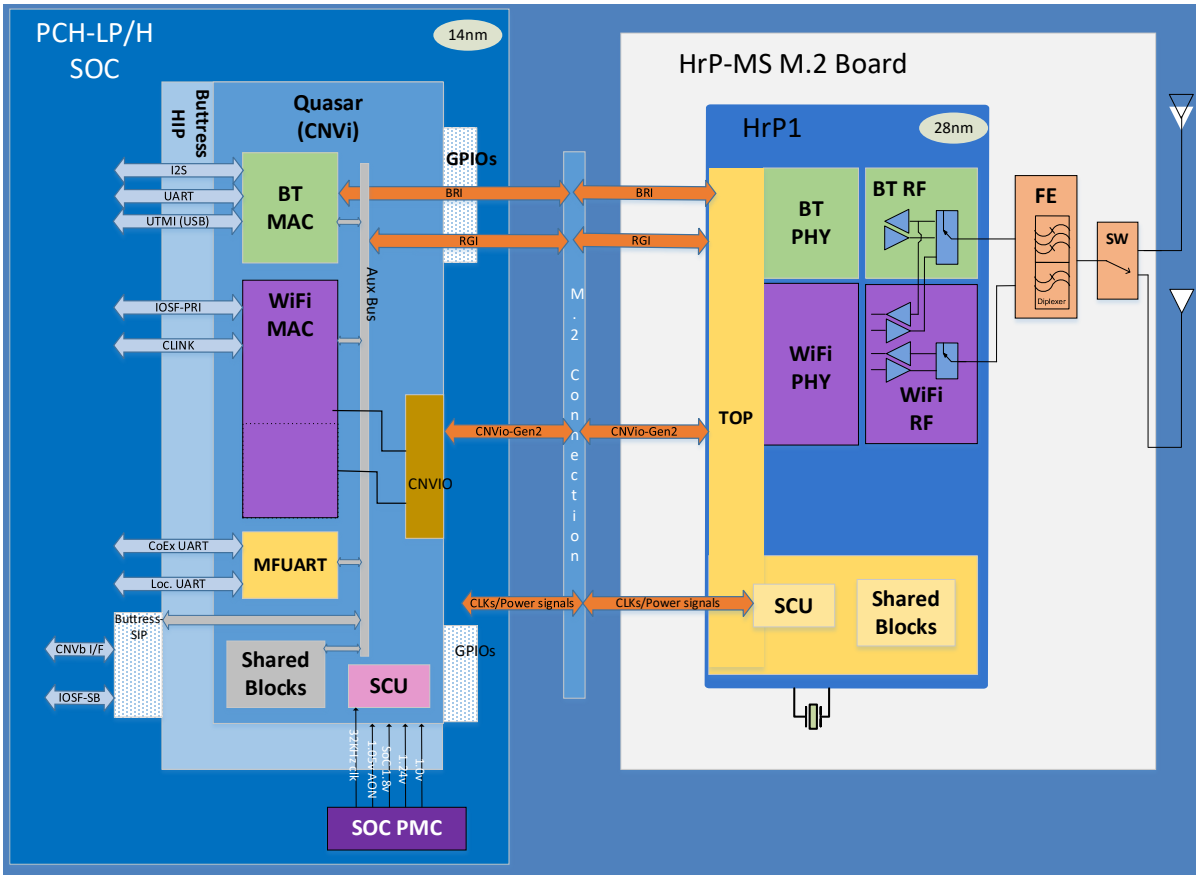


Figure 1–2 Harrison Peak 1 module block diagram



Note: 2.4Ghz band pass filters (BAW) are not supported by all SKUs.

1.3 Cross Platforms wireless module SKUs

The following are the modules/SKUs that shall be supported with Ice-Lake-based platforms.

The Harrison Peak module supports the hardware SKUs listed in Table 1–3.

Table 1-3 Harrison Peak-related module SKUs

SKU name	Form Factor	Interfaces	Front End
HrP2 mainstream (Intel® Wi-Fi 6 AX201)	2230 Hybrid keyE S3	CNVio-Gen2, BRI, RGI, Ref clock, controls	2x2, Integrated RF front end and balanced-diplexer, no LTE coex filter
HrP2-MS soldered down (Intel® Wi-Fi 6 AX201)	1216 S3	CNVio-Gen2, BRI, RGI, Ref clock, controls	2x2, Integrated RF front end and balanced-diplexer, no LTE coex filter
HrP2-MS LTE-CoEx (Intel® Wi-Fi 6 AX201)	1216 S3	CNVio-Gen2, BRI, RGI, Ref clock, controls	2x2, Integrated RF front end and balanced-diplexer, with LTE coex filter

SKU name	Form Factor	Interfaces	Front End
HrP1 Diversity (Intel® Wi-Fi 6 AX101)	2230 Hybrid keyE S3	CNVio-Gen2, BRI, RGI, Ref clock, controls	1x1 (2 antennas), Integrated RF front end and balanced-diplexer, no LTE coex filter
HrP1 Diversity soldered down (Intel® Wi-Fi 6 AX101)	1216 S3	CNVio-Gen2, BRI, RGI, Ref clock, controls	1x1 (2 antennas), Integrated RF front end and balanced-diplexer, no LTE coex filter
CcP Main (Intel® Wi-Fi 6 AX200)	2230 Hybrid key E S3	PCIe Gen2, USB	2x2, Integrated RF front end and balanced-diplexer, no LTE coex filter
CcP SD LTE (Intel® Wi-Fi 6 AX200)	1216 S3	PCIe Gen2, USB	2x2, Integrated RF front end and balanced-diplexer, with LTE coex filter
CcP SD (Intel® Wi-Fi 6 AX200)	1216 S3	PCIe Gen2, USB	2x2, Integrated RF front end and balanced-diplexer, no LTE coex filter

Additional WCS modules/SKUs that shall be available in Ice-Lake are listed in Table 1–4.

Table 1-4 Legacy Wireless supporting products

* The following are also supported with all Platform that integrate Quasar CNVi in them

SKU name	Form Factor	Interfaces	Front End
JfP 2x2	2230 Hybrid key E S3	CNVio-Gen1, BRI, RGI, Ref clock, controls	Integrated RF front end, no LTE coex filter
JfP 2x2 soldered down	1216 S3	CNVio-Gen1, BRI, RGI, Ref clock, controls	Integrated RF front end, no LTE coex filter
JfP 2x2 soldered down+LTE	1216 S3	CNVio-Gen1, BRI, RGI, Ref clock, controls	Integrated RF front end, with LTE coex filter (BAW)
JfP 1x1	2230 Hybrid key E S3	CNVio-Gen1, BRI, RGI, Ref clock, controls	Integrated RF front end, no LTE coex filter
JfP 1x1 soldered down	1216 S3	CNVio-Gen1, BRI, RGI, Ref clock, controls	Integrated RF front end, no LTE coex filter
JfP 1x1 Diversity	2230 Hybrid key E S3	CNVio-Gen1, BRI, RGI, Ref clock, controls	Integrated RF front end, no LTE coex filter, Antenna Diversity switch
JfP 1x1 soldered down Diversity	1216 S3	CNVio-Gen1, BRI, RGI, Ref clock, controls	Integrated RF front end, no LTE coex filter, Antenna Diversity switch
TnP 2x2	2230 Hybrid key E S3	PCIe Gen2, USB	Integrated RF front end, no LTE coex filter

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2 Product Architecture

2.1 Integrated connectivity concept

Quasar and Harrison Peak are the second generation of the CNVi product line, aligned with the 2018/19 platform based on the Ice Lake and Comet/Rocket/Tiger Lake Platform family. The first CNVi generation was based on Pulsar and Jefferson Peak, which were aligned with Cannon Lake-based platforms (and also Coffee Lake and Gemini Lake).

2.1.1 MAC-PHY split

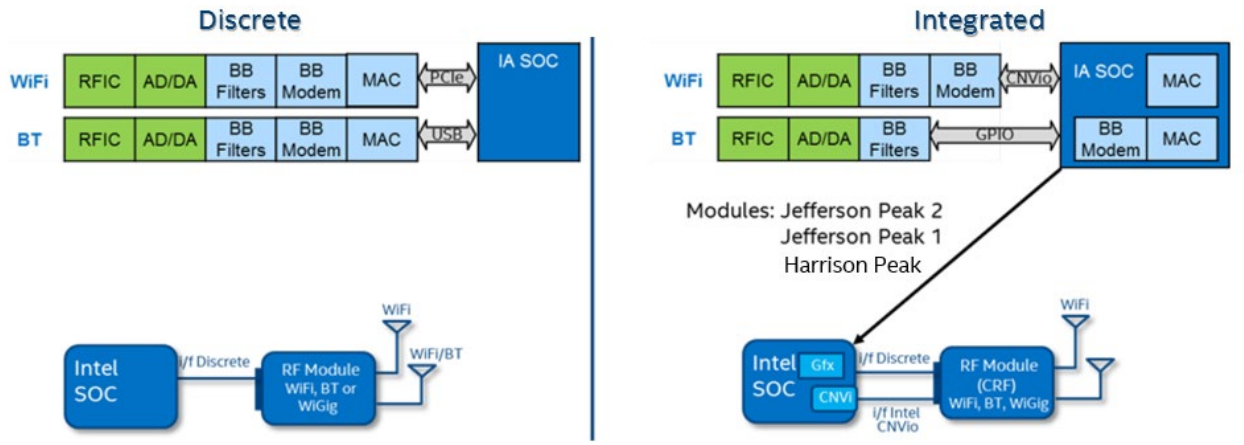
Integrated Connectivity (CNVi) is a new architecture for wireless connectivity devices. The concept of CNVi is to move a large part of the functional content of the connectivity chip from the radio chip into the SoC. As a result, a large portion of the chip logic and memory resources is moved out of the radio chip, reducing platform bill of material (BOM) size and cost, and improving accessibility to SoC resources (audio, memory, etc.).

In the CNVi architecture, the MACs of the Wi-Fi and Bluetooth®, including processors, logic and memory are relocated from the radio chip into the SoC chip. Signal processing, Analog and RF functions stay in the radio chip, which is called a Companion RF chip (CRF) in CNVi terminology.

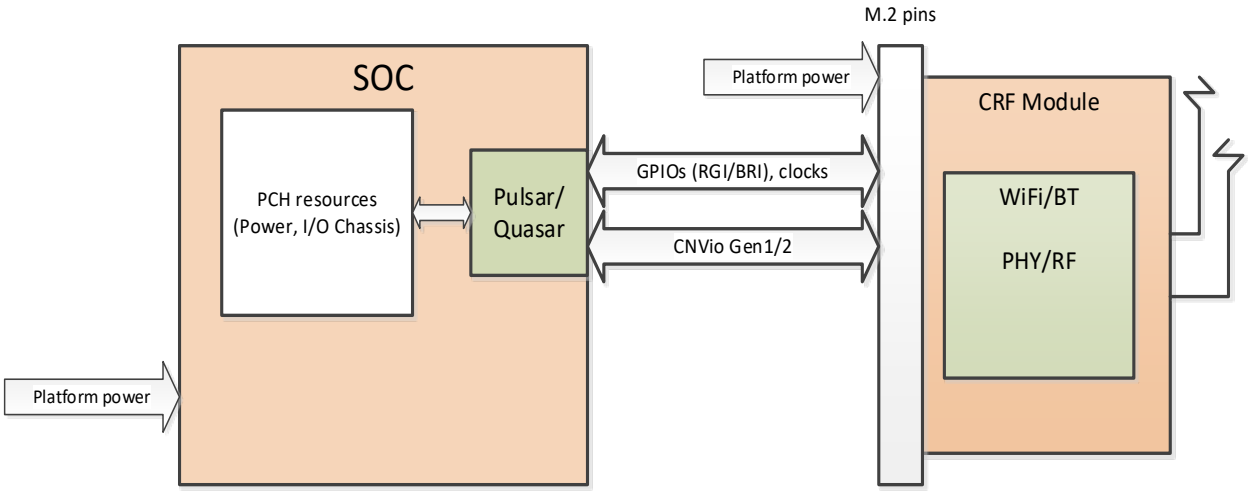
The part of the connectivity IP which is ported into the SoC is called Pulsar/Quasar (CNVi is the general name). The Pulsar/Quasar interfaces with the rest of the SoC functions through SoC-internal interfaces and buses, and does not require any host interfaces at the platform level. On the other hand, interfacing the Pulsar/Quasar and the Companion RF (CRF) chip does require platform signals to be routed between the SoC and the Companion RF chip (Intel-proprietary interfaces, based on existing M.2 signals).

The Integrated Connectivity architecture has the MAC part of the Wi-Fi and BT cores located inside the SoC. As a result, the Host interfaces of Wi-Fi and BT are no longer part of the M.2 module, which is an RF companion module. These Host Interfaces reside in the SoC and are not exposed to the platform.

Figure 2–1 CNVi architecture



e.g.,



2.1.2 SoC and Companion RF compatibility

To use the integrated connectivity architecture, the platform needs to include both a SoC and a connectivity device that supports CNVi. This means that the SoC needs to have the Pulsar/Quasar block inside, and a Companion RF module should be used in the design.

The Jefferson Peak Companion RF module can support the following SoC devices, which include Pulsar:

- Cannon Lake PCH-LP/H
- Coffee Lake and its refresh platforms
- Gemini Lake
- JfP SKUs can also work with the Quasar-based PCHs as listed below for Harrison Peak.

The Harrison Peak Companion RF module can support the following SoC devices, which include Quasar:

- Ice Lake PCH-LP / H
- Comet Lake
- Tiger Lake
- Rocket Lake
- Jasper Lake

2.1.3 Swappable Companion RF/Discrete

Companion RF (CRF) M.2 modules are swappable with the discrete connectivity M.2 module.

The meaning of swappable, in this context, is that the design of the M.2 socket on the platform can allow using the same M.2 socket for both CNVi and discrete connectivity, without the need to change the hardware configuration. When designing the platform to support swappable CRF/discrete, a CRF module can be changed to a discrete module, and vice versa, by simply removing one M.2 card type from the socket and swapping it with a new card type. Note that M.2 does not support hot-swapping and therefore the platform power should be turned off before doing this operation. The swappable concept is also applicable to 1216 soldered-down versions of the CRF, which also allow the same board space to be used for a single footprint, supporting either a 1216-SD JfP/HrP CRF or a standard M.2 discrete module. Obviously in the soldered-down case, swapping modules will require detaching the soldered module from the board.

The described products are M.2 with standard PCIe- and USB-based modules:

- Thunder Peak (2017-based products, based on Pulsar+JfP designs)
- Cyclone Peak (2018-based products, based on Quasar+HrP designs)

To design the platform to support both discrete and CNVi, and have the swappable feature, the platform needs to be designed properly. The specific guidelines for this type of design are in Section 9.

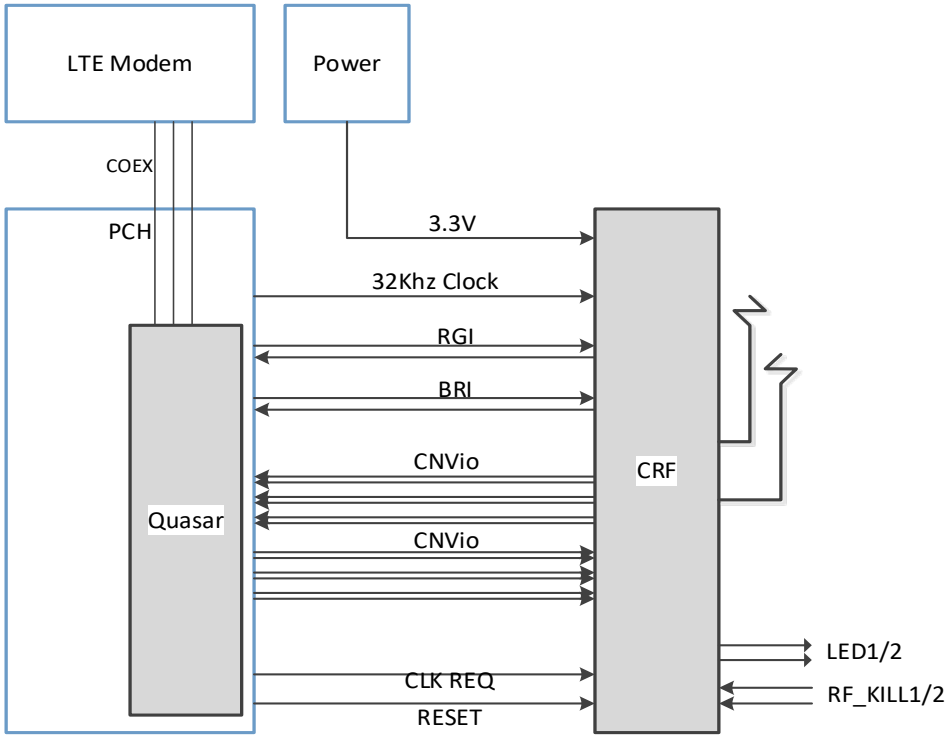
2.2 Harrison Peak interfaces

In general, Harrison Peak maintains the Jefferson Peak interfaces. The only changes are

1) CNVio generation is improved for HrP.
2) Shared clk/xTal exists in JfP, and *does **not*** exist in HrP, and *does **not*** exist in Quasar-based PCHs (even with JfP as CRF).

The Jefferson/Harrison Peak M.2 module connects the platform and the SoC through a proprietary interface for CNVio (Gen1 in the JfP case, and Gen2 in the HrP case) that connects the CRF module and the SoC/platform. A high-level description of the interface is shown in Figure 2–2.

Figure 2–2 Harrison Peak interfaces



2.2.1 Power supply

The Jefferson/Harrison Peak modules are powered by a 3.3V supply, connected to the dedicated power pins on the M.2 module connector, with proper decoupling capacitors placed close to the module/socket pins.

To avoid confusion, the main Power supply high value is 3.3v +/– 0.16v, and the low value is 0v (or in some transaction cases can be at least < 0.5v).

For the case where the platform may use Vbat (COB, Battery or 1S Batteries – ranged 2.5–5V) the product can handle the following:

1. Functional range 2.5V–5V (meaning: may have violations that are out of spec, but can maintain functionality and be able to recover)
2. Full operational range: 2.7V–4.8V

3. Restrictions still exist on specific signal/cases:
    a. The M.2 USB signals also have a USB Power entry which MUST be powered, and MUST NOT be >3.6v (it can be either 3.3 +/– 10% or 1.8v +/- 10%; in all cases the USB is not really used, e.g., in HrP or CcP-UART cases).
    b. For the WLAN_EN and BT_EN signals, VIHmax=1.8V +/– 10%.

       This means that for Vbat-based platforms, WLAN_EN and BT_EN should be externally driven by a 1.8V signal driver, and not connect to the resistor divider from Vbat as is done today in the M.2.

2.2.2 32-KHz slow clock

This signal is optional. It comes from the platform 32kHz RTC clock. The product module can use either an internal 32kHz clock or this external 32KHz clock. Using an external 32KHz clock has power saving benefits compared to using an internal clock.

In order to enable the option to use the external 32KHz clock, this clock must be driven by the platform at any time. In addition, a BIOS/ACPI-based indication is needed to indicate to the product that it can rely on the external 32KHz clock. (See Intel document number 559910, *Intel Connectivity Platforms BIOS Guidelines*).

The external 32kHz clock can come from a PCH pin or from a different source on the platform, depending on the platform used.

Note that the external 32kHz accuracy is assumed to be 20ppm.

If the BIOS does not indicate that the external 32KHz clock is valid, the product will use its internal 32KHz clock.

In HrP this signal is 1.8v based and is tolerant to 3.3v

2.2.3 BRI/RGI

These are two serial, asynchronous busses used for BT traffic (BRI) and for control data (RGI). Each bus has one signal per direction. The BRI and RGI busses do not require any clock to be sent with the data lines, as the clock at the receiving end of the bus is extracted from the data itself. The BRI and RGI toggle at 78.2Mbouds each (full duplex). The signals are standard 1.8V logic level.

In the CRF, we have a pull-up on the RGI/BRI_DT.

2.2.4 CNVio

The CNVio signals connect the JfP/HrP module and the SoC. They are used as the main data bus for Wi-Fi, to transfer data between the Pulsar/Quasar and the RF companion chip. The CNVio signals are physically similar to the MIPI DPHY standard, but have a different (and Intel proprietary) protocol.

The CNVio bus has two data lanes and one clock for each direction. Both data and clock signals are differential, 85-ohm signals. The total number of signals for the interface is 12 (6 pairs, 3 per direction). These signals should be routed as differential, controlled impedance traces. Due to the sensitivity of the CNVio bus to signal impairments, RF layout techniques and good length matching shall be used. Section 1 contains specific design guidelines for the CNVio routing.

JfP and Pulsar uses two lanes of Gen1 of the CNVio.

HrP and Quasar uses two lanes of Gen2 of CNVio (double the bus rate).

Note: Quasar CNVio Gen2 can work with JfP with its Gen1 CNVio.

Note: There is a Quasar-V (value/low-end variant of Quasar for PCH-N) that has only one lane of CNVio-Gen2, and which can work with both HrP and JfP, but with some max performance TPT impact.

For this one lane, using Clk and Lane0 only, Lane1 is not in use; based on pins 73, 71, 67, 65 and 23, 21, 17, 15.

2.2.5 Reference clock (38.4MHz) – REFCLK0

In JfP/Pulsar combination only

This section is relevant **only** in the Pulsar+JfP case, and is **not relevant** to ICL/TGL/JPL or any other Quasar-based systems.

This is the main clock used for both Pulsar (the MAC part of which is inside the SoC) and Jefferson Peak. The clock is driven by JfP output clock buffer at voltage levels of 1V (pk-pk). This clock shall be routed from JfP to the SoC with special care to minimize clock jitter. Section 9.13.3 contains specific design guidelines for the reference clock routing.

Not supported with Harrison Peak, which uses a 60MHz crystal (and not supported in Ice Lake-based platforms).

Note: There was a theoretical option for using a shared clock for the Quasar combined with JfP; this option was platform-dependent. This option does not exist in Ice Lake, or any current existing platform, so it is NOT part of the POR!

2.2.6 Reset and Clock request

The Reset and Clock request signals are automatically driven by the SoC to control the operation of the Companion RF and minimize system power consumption. The SoC uses the Reset only at initial power-up. The Clock request signal is used to change the Jefferson/Harrison Peak power modes between high-power clock and low-power clock (per the system power states).

The SUSCLK signal (for 32kHz indication) has an internal pull-down in the CRF.

2.2.7 LEDs

Jefferson/Harrison Peak M.2 modules support driving two LEDs to indicate wireless activity. These pins have open-drain buffers that sink current (to logical zero) when the LED is turned on.

The product has two LED signals: a Bluetooth LED, and a Wi-Fi LED.

The Bluetooth LED functionality is as follows:

1. LED is OFF when the Bluetooth is in HW or SW RF kill (SW RF kill also means driver disable, etc.).
2. LED is ON otherwise.

The Wi-Fi LED functionality is as follows:

1. LED is OFF when the Wi-Fi is not powered or in RF kill.
2. LED is ON otherwise.

Note: Chrome* OS doesn't support or require the LED for communications. Hence the LED signals should remain disconnected in Chrome platforms.

2.2.8 Wireless disable (RF-KILL)

Jefferson/Harrison Peak M.2 modules support receiving a wireless disable (RF-KILL) command through the two RF-KILL pins for turning off Wi-Fi and BT, respectively. These pins can be connected to a platform switch or to SoC GPIOs (If possible, it is recommended to not use GPIOs that have platform impact as "bootstraps" during platform initialization.)

The RF-KILL signals (Wireless disable*) are mandatory, and have an internal pull-up on the Harrison Peak side. (These are "Active Low" signals.)

2.2.8.1 Wi-Fi wireless disable

W_DISABLE1# (pin 56 in M.2 2230 pinout) serves as HW RF kill for the Wi-Fi radio.

Table 2-1 W_DISABLE1# characteristics

Characteristic	Description
Internal pull-up resistor	min 100 kOhm, max 200kOhm
VIL for asserting	min 0V, max 0.6V
VIH for de-asserting	min 1.26V, max 3.3V or float (not connected)

2.2.8.1.1 Wi-Fi SW RF kill

The product supports Wi-Fi SW RF kill through relevant OS API. When in RF kill state all RF activities are terminated, and device goes into low power mode.

Chrome OS doesn't use HW RF-Kill and does not support SW RF kill. Airplane mode for Chrome OS is achieved by detaching the driver from the WPA Supplicant.

Notice that this signal is also used for "BT RESET" functionality.

2.2.8.2 Bluetooth® wireless disable

The BT radio will be active only if both HW RF kill pin and SW RF kill mechanisms are in enable state.

Chrome OS doesn't support (ability for user to change) HW RF kill or SW RF kill.

Notice that this signal is also used for "BT RESET" functionality.

2.2.8.2.1 M.2 Bluetooth® HW RF kill

W_DISABLE2# (pin 54 in M.2 2230 pinout) serves as HW RF kill for the Bluetooth radio.

Asserting W_DISABLE#_2 signal will result in a complete shutdown of the Bluetooth part. The result from the user perspective is similar to removing the Bluetooth device from the laptop.

Table 2-2 W_DISABLE2# characteristics

Characteristic	Description
Internal pull-up resistor	min 100 kOhm, max 200kOhm
VIL for asserting	min 0V, max 0.6V
VIH for de-asserting	min 1.26V, max 3.3V or float (not connected)

2.2.8.2.2 Bluetooth SW RF kill

The product supports Bluetooth SW RF kill. The behavior of the SW RF kill is similar to the HW RF kill: all RF activities are terminated, and device goes into low power mode.

2.2.9 RF-RESET-B

This is an Intel-proprietary signal, used as an internal RESET indication from the SoC to the CRF during the init flow of the CNVi-based modules.

This signal has an internal pull-down on the Harrison Peak side.

2.2.10 ClkReq0 (Pin14 in M.2-2230, A43 in 1216)

This is an Intel-proprietary signal, used as a Clock request indication from the SoC to the CRF to supply clk from the CRF to the SoC; this is used by JfP but IS NOT USED by Harrison Peak.

In both CRFs, this signal is also used during the init flow of the CNVi-based modules (so is still a required signal).

This signal has an internal pull-down on the Harrison Peak side.

This signal is shared with an optional PCM interface that can be used with the Discrete Module solution (on CRF).

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3 Harrison Peak Electrical Specifications

This section provides information about the electrical specifications for the product module. The specification covers the module hardware interface signals.

3.1 2230 and 1216 form factor pinouts

There are two pinout lists, one for the platform side, and one for the module side. Note that some signals are crossed (for example, UART Rx on the platform side is connected to Tx on the module side).

Note: The 2230 module pinout is based on the Hybrid Key-E scheme. Hybrid Key-E is an Intel proprietary scheme based on the mechanical and electrical specifications of the P*CIe_M.2_Electromechanical_Spec*, modified with changes to the pinout in order to support Intel's Integrated Connectivity (CNVi).

3.1.1 2230 form factor and pinouts

This form factor module is based on the Hybrid Key-E approach, where it is determined at the platform level when CNVi should be supported and when swappable CNVi/discrete should be supported.

Table 3-1 Hybrid Key-E 2230-platform module pinout

Pin #	Pin Name Platform Pinout	Pin Name Spec (Product side) Pinout	Pin Name Module Pinout	Direction w/respect to JfP Module	JfP/HrP Voltage on Module Side	Connection on Platform/Usage
1	GND	GND	GND			
2	3.3 V	3.3 V	3.3 V		3.3 V	3.3 V Supply
3	USB_D+	USB_D+	NC	IO	3.3 V	Not used by Harrison Peak Shall be connected to USB for Discrete support
4	3.3 V	3.3 V	3.3 V		3.3 V	3.3 V Supply
5	USB_D-	USB_D-	NC	IO	3.3 V	Not used by Harrison Peak Shall be connected to USB for Discrete support
6	LED1#	LED1#	LED1#	O	OD	LED 1 (Main, Wi-Fi)
7	GND	GND	GND			
8	PCM_CLK/I2S SCK	PCM_CLK/I2S SCK	NC	IO	1.8 V	Not used by Harrison Peak Optional PCM interface when used with Discrete

Pin #	Pin Name Platform Pinout	Pin Name Spec (Product side) Pinout	Pin Name Module Pinout	Direction w/respect to JfP Module	JfP/HrP Voltage on Module Side	Connection on Platform/Usage
9	WGR_D1N	SDIO_CLK/SYSCLK	WGR_D1N	O	CNVio PHY	CNVio bus RX lane 1
10	PCM_SYNC/I2S WS/RF_RESET_B	PCM_SYNC/I2S WS	RF_RESET_B	I	1.8 V	The PCM functionality is not used by HrP, but using this signal as Harrison peak RF reset indication (active low, PD) Optional PCM interface when used with Discrete
11	WGR_D1P	SDIO_CMD	WGR_D1P	O	CNVio PHY	CNVio bus RX lane 1
12	PCM_IN/I2S SD_IN	PCM_IN/I2S SD_IN	NC	O	1.8 V	Not used by Harrison Peak Optional PCM interface when used with Discrete
13	GND	SDIO_DATA0	GND			
14	PCM_OUT/I2S SD_OUT/CLKREQ0	PCM_OUT/I2S SD_OUT	CLKREQ0	I	1.8 V	Has a role in the CRF init sequence. Also an optional Clock request for the 38.4M clock (CNVi reference clock; requires a specific SKU; used by JfP; not supported/used by HrP); has a PD in the CRF Optional PCM interface when used with Discrete
15	WGR_D0N	SDIO_DATA1	WGR_D0N	O	CNVio PHY	CNVio bus RX lane 0
16	LED2#	LED2#	LED2#	O	OD	LED secondery (BT)
17	WGR_D0P	SDIO_DATA2	WGR_D0P	O	CNVio PHY	CNVio bus RX lane 0
18	GND	GND	LNA_EN			A special-purpose test pin of the HrP module; should be connected to Ground on the platform
19	GND	GND/SDIO DATA3	GND			

Pin #	Pin Name Platform Pinout	Pin Name Spec (Product side) Pinout	Pin Name Module Pinout	Direction w/respect to JfP Module	JfP/HrP Voltage on Module Side	Connection on Platform/Usage
20	UART WAKE#	UART WAKE#	NC	O	3.3 V	Not used by Harrison Peak Optional UART interface when used with Discrete
21	WGR_CLKN	SDIO_WAKE#	WGR_ CLKN	O	CNVio PHY	CNVio bus RX clock
22	UART TXD/BRI_RSP	UART TXD	BRI_RSP	O	1.8 V	BRI bus RX Optional PCM interface when used with Discrete
23	WGR_CLKP	SDIO_RESET#	WGR_ CLKP	O	CNVio PHY	CNVio bus RX clock
24	Connector Key	Connector Key	Module Key			
25	Connector Key	Connector Key	Module Key			
26	Connector Key	Connector Key	Module Key			
27	Connector Key	Connector Key	Module Key			
28	Connector Key	Connector Key	Module Key			
29	Connector Key	Connector Key	Module Key			
30	Connector Key	Connector Key	Module Key			
31	Connector Key	Connector Key	Module Key			
32	UART TXD/RGI_DT	UART RXD	RGI_DT	I	1.8 V	RGI bus TX, 1.8v-PU in CRF Optional PCM interface when used with Discrete
33	GND	GND	GND			
34	UART CTS/RGI_RSP	UART RTS	RGI_RSP	O	1.8 V	RGI bus RX Optional PCM interface when used with Discrete

Pin #	Pin Name Platform Pinout	Pin Name Spec (Product side) Pinout	Pin Name Module Pinout	Direction w/respect to JfP Module	JfP/HrP Voltage on Module Side	Connection on Platform/Usage
35	PETp0	PERp0	NC		PCIe PHY	Not used by Harrison Peak Shall be connected to PCIe for Discrete support PCIe PHY signals
36	UART RTS/BRI_DT	UART CTS	BRI_DT	I	1.8 V	BRI bus TX
37	PETn0	PERn0	NC		PCIe PHY	Not used by Harrison Peak Shall be connected to PCIe for Discrete support PCIe PHY signals
38	CLINK RESET	<Vendor Defined> CLINK RESET	NC			Not used by Harrison Peak Optional CLINK interface when used with Discrete
39	GND	GND	GND			
40	CLINK DATA	<Vendor Defined> CLINK DATA	NC			Not used by Harrison Peak Optional CLINK interface when used with Discrete
41	PERp0	PETp0	NC		PCIe PHY	Not used by Harrison Peak Shall be connected to PCIe for Discrete support PCIe PHY signals
42	CLINK CLK	<Vendor Defined> CLINK CLK	NC			Not used by Harrison Peak Optional CLINK interface when used with Discrete
43	PERn0	PETn0	NC		PCIe PHY	Not used by Harrison Peak Shall be connected to PCIe for Discrete support PCIe PHY signals

Pin #	Pin Name Platform Pinout	Pin Name Spec (Product side) Pinout	Pin Name Module Pinout	Direction w/respect to JfP Module	JfP/HrP Voltage on Module Side	Connection on Platform/Usage
44	COEX3 (I/O)	COEX3 (I/O)	COEX3	(I/0)		Not used by Harrison Peak Optional Coex interface with LTE modem when used with Discrete
45	GND	GND	GND			
46	COEX2	COEX2	COEX2	(I/0)		Not used by Harrison Peak Optional Coex interface with LTE modem when used with Discrete
47	REFCLKP0	REFCLKP0	NC		PCIe PHY	Not used by Harrison Peak Shall be connected to PCIe for Discrete support PCIe PHY signals
48	COEX1	COEX1	COEX1	(I/0)		Not used by Harrison Peak Optional Coex interface with LTE modem when used with Discrete
49	REFCLKN0	REFCLKN0	NC		PCIe PHY	Not used by Harrison Peak Shall be connected to PCIe for Discrete support PCIe PHY signals
50	SUSCLK (32 kHz)	SUSCLK (32 kHz)	C_P32K (32 kHz)	I	3.3 V	HrP also supports 1.8 V electrical levels on this signal; PD in CRF
51	GND	GND	GND			
52	PERST0#	PERST0#	NC		3.3 V	Not used by Harrison Peak Shall be connected to PCIe for Discrete support
53	CLKREQ0#	CLKREQ0#	NC		3.3 V	PCIe clock request; not used by Harrison Peak Shall be connected to PCIe for Discrete support

Pin #	Pin Name Platform Pinout	Pin Name Spec (Product side) Pinout	Pin Name Module Pinout	Direction w/respect to JfP Module	JfP/HrP Voltage on Module Side	Connection on Platform/Usage
54	W_DISABLE 2#	W_DISABLE2#	W_DISABLE2#	I	3.3 V	HrP also supports 1.8 V electrical levels on this signal, 1.8v-PU in CRF
55	PEWAKE0#	PEWAKE0#	NC		3.3 V	Not used by Harrison Peak Shall be connected to PCIe for Discrete support
56	W_DISABLE 1#	W_DISABLE1#	W_DISABLE1#	I	3.3 V	HrP also supports 1.8 V electrical levels on this signal; 1.8v-PU in CRF
57	GND	GND	GND			
58	I2C DATA/ A4WP_I2C_ DATA	I2C DATA/ UART_TX	NC		1.8 V	Not used by Harrison Peak
59	WT_D1N	WT_D1N <PERp1>	WT_D1N	I	CNVio PHY	CNVio bus TX lane 1
60	I2C CLK/ A4WP_I2C_ CLK	I2C CLK/ UART_RX	NC		1.8 V	Not used by Harrison Peak
61	WT_D1P	WT_D1P <PER1n1>	WT_D1P	I	CNVio PHY	CNVio bus TX lane 1
62	ALERT#/ A4WP_IRQ# <GND>	ALERT#/ UART_RTS	NC		1.8 V	Not used by Harrison Peak
63	GND	GND	GND			
64	REFCLK0	REFCLK0/UART_ CTS <Reserve>	REFCLK0	O	1 V	38.4Mhz clock not supported by HrP (supported by JfP CRF) Disconnected and floting in HrP case
65	WT_D0N	WT_D0N <PET1p1>	WT_D0N	I	CNVio PHY	CNVio bus TX lane 0
66	PERST1#	PERST1#	NC			Not used by Harrison Peak
67	WT_D0P	WT_D0P <PET1n1>	WT_D0P	I	CNVio PHY	CNVio bus TX lane 0
68	CLKREQ1#	CLKREQ1#	NC			Not used by Harrison Peak
69	GND	GND	GND			

Pin #	Pin Name Platform Pinout	Pin Name Spec (Product side) Pinout	Pin Name Module Pinout	Direction w/respect to JfP Module	JfP/HrP Voltage on Module Side	Connection on Platform/Usage
70	UIM_POWER_ SRC/GPIO1/ PEWAKE1#	UIM_POWER_ SRC/GPIO1/ PEWAKE1#	NA			Not used by Harrison Peak
71	WT_CLKN	WT_CLKN <REFCLKP1>	WT_ CLKN	I	CNVio PHY	CNVio bus TX clock
72	3.3 V	3.3 V	3.3 V			3.3 V Supply
73	WT_ CLKP	WT_ CLKP <REFCLKN1>	WT_ CLKP	I	CNVio PHY	CNVio bus TX clock
74	3.3 V	3.3 V	3.3 V			3.3 V Supply
75	GND	GND	GND			

*PU – pull-up

*PD – pull-down

Table 3-2 1216-platform module pinout

Pin #	Pin Name platform pinout	Direction w/respect to Wireless client Module	Function When CNVi Is Used	Function When Standard (Discrete) M.2 Is Used	Comments
1	UIM_POWER_SRC/GPIO1		Not used	UIM_POWER_SRC/GPIO1	
2	UIM_POWER_SNK		Not used	UIM_POWER_SNK	
3	UIM_SWP		Not used	UIM_SWP	
4	3.3V		3.3V	3.3V	
5	3.3V		3.3V	3.3V	
6	GND		GND	GND	
7	RESERVED		Not used	RESERVED	
8	ALERT#		Not used	ALERT#	
9	I2C_CLK		Not used	I2C_CLK	
10	I2C_DATA		Not used	I2C_DATA	
11	COEX_TXD		Not used	COEX_TXD	
12	COEX_RXD		Not used	COEX_RXD	
13	COEX3		Not used	COEX3	
14	SYSCLK/GNSS0		Not used	SYSCLK/GNSS0	

Pin #	Pin Name platform pinout	Direction w/respect to Wireless client Module	Function When CNVi Is Used	Function When Standard (Discrete) M.2 Is Used	Comments
15	TX_BLANKING/GNSS1		Not used	TX_BLANKING/GNSS1	
16	RESERVED		Not used	RESERVED	
17	GND		GND	GND	
18	RESERVED		Not used	Not used	
19	RESERVED		Not used	Not used	
20	GND		GND	GND	
21	RESERVED		Not used	Not used	
22	RESERVED		Not used	Not used	
23	GND		GND	GND	
24	RESERVED		Not used	Not used	
25	RESERVED		Not used	Not used	
26	GND		GND	GND	
27	SUSCLK(32 kHz)(3.3V)		32Khz clock (3.3V)	SUSCLK(32kHz)(3.3V)	20ppm accuracy In HrP this signal is 1.8v based and is tolerant to 3.3v
28	W_DISABLE1#	I	W_DISABLE1#	W_DISABLE1#	
29	PEWAKE#		Not used	PEWAKE#	
30	CLKREQ#		Not used	CLKREQ#	
31	PERST#		Not used	PERST#	
32	GND		GND	GND	
33	REFCLKN0		Not used	REFCLKN0	
34	REFCLKP0		Not used	REFCLKP0	
35	GND		GND	GND	
36	PERn0		Not used	PERn0	
37	PERp0		Not used	PERp0	
38	GND		GND	GND	
39	PETn0		Not used	PETn0	
40	PETp0		Not used	PETp0	
41	GND		GND	GND	
42	CLink_CLK		Not used	CLink_CLK	
43	CLink_DATA		Not used	CLink_DATA	
44	CLink_RESET		Not used	CLink_RESET	

Pin #	Pin Name platform pinout	Direction w/respect to Wireless client Module	Function When CNVi Is Used	Function When Standard (Discrete) M.2 Is Used	Comments
45	SDIO_RESET#		Not used	Not used	SDIO is not supported
46	SDIO_WAKE#		Not used	Not used	SDIO is not supported
47	SDIO_DATA3		Not used	Not used	SDIO is not supported
48	SDIO_DATA2		Not used	Not used	SDIO is not supported
49	SDIO_DATA1		Not used	Not used	SDIO is not supported
50	SDIO_DATA0		Not used	Not used	SDIO is not supported
51	SDIO_CMD		Not used	Not used	SDIO is not supported
52	SDIO_CLK		Not used	Not used	SDIO is not supported
53	UART_WAKE# (3.3V)		Not used	UART_WAKE# (3.3V)	
54	LPSS_UART_RTS/bri_dt		Not used	LPSS_UART_RTS/bri_dt	Connected to A38 on the motherboard
55	LPSS_UART_RXD/bri_rsp		Not used	LPSS_UART_RXD/bri_rsp	Connected to A39 on the motherboard
56	LPSS_UART_TXD/rgi_dt		Not used	LPSS_UART_TXD/rgi_dt	Connected to A40 on the motherboard
57	LPSS_UART_CTS/rgi_rsp		Not used	LPSS_UART_CTS/rgi_rsp	Connected to A41 on the motherboard
58	PCM_SYNC/I2S_WS		Not used	PCM_SYNC/I2S_WS	Connected to A42 on the motherboard
59	PCM_OUT/I2S_SD_OUT		Not used	PCM_OUT/I2S_SD_OUT	Connected to A43 on the motherboard
60	PCM_IN/I2S_SD_IN		Not used	PCM_IN/I2S_SD_IN	
61	PCM_CLK/I2S_SCK		Not used	PCM_CLK/I2S_SCK	
62	GND		GND	GND	
63	W_DISABLE2#	I	W_DISABLE2#	W_DISABLE2#	
64	LED2#	O	LED2#	LED2#	
65	LED1#	O	LED1#	LED1#	

Pin #	Pin Name platform pinout	Direction w/respect to Wireless client Module	Function When CNVi Is Used	Function When Standard (Discrete) M.2 Is Used	Comments
66	RESERVED		Not used	RESERVED	
67	RESERVED		Not used	RESERVED	
68	GND		GND	GND	
69	USB_D-		Not used	USB_D-	
70	USB_D+		Not used	USB_D+	
71	GND		GND	GND	
72	3.3V		3.3V	3.3V	Connected to A48 on the motherboard
73	3.3V		3.3V	3.3V	Connected to A49 on the motherboard
74	GND		GND	GND	Connected to A50 on the motherboard
75	GND		GND	GND	
76	GND		GND	GND	
77	GND		GND	GND	
78	GND		GND	GND	
79	GND		GND	GND	
80	GND		GND	GND	
81	GND		GND	GND	
82	GND		GND	GND	
83	GND		GND	GND	
84	GND		GND	GND	
85	GND		GND	GND	
86	GND		GND	GND	
87	GND		GND	GND	
88	GND		GND	GND	
89	GND		GND	GND	
90	GND		GND	GND	
91	GND		GND	GND	
92	GND		GND	GND	
93	GND		GND	GND	
94	GND		GND	GND	
95	GND		GND	GND	
96	GND		GND	GND	
G1	GND		GND	GND	

Pin #	Pin Name platform pinout	Direction w/respect to Wireless client Module	Function When CNVi Is Used	Function When Standard (Discrete) M.2 Is Used	Comments
G2	GND		GND	GND	
G3	GND		GND	GND	
G4	GND		GND	GND	
G5	GND		GND	GND	Thermal pad
G6	GND		GND	GND	Thermal pad
G7	GND		GND	GND	Thermal pad
G8	GND		GND	GND	Thermal pad
G9	GND		GND	GND	Thermal pad
G10	GND		GND	GND	Thermal pad
G11	GND		GND	GND	Thermal pad
G12	GND		GND	GND	Thermal pad
All below are vendor-specific pinouts					
A07	GND		GND	Not Applicable	
A08	A4WP_IRQ#		NC	Not Applicable	Not connected
A09	A4WP_CLK		NC	Not Applicable	Not connected
A10	A4WP_DATA		NC	Not Applicable	Not connected
A11	RESERVED		RESERVED	Not Applicable	Not connected
A12	RESERVED		RESERVED	Not Applicable	Not connected
A13	RESERVED		RESERVED	Not Applicable	Not connected
A14	RESERVED		RESERVED	Not Applicable	Not connected
A15	LNA_EN		GND	Not Applicable	Connect to GND
A16	RESERVED		RESERVED	Not Applicable	Not connected
A17	RESERVED		RESERVED	Not Applicable	Not connected
A18	RESERVED		RESERVED	Not Applicable	Not connected
A19	WT_CLKP	I	WT_CLKP	Not Applicable	
A20	WT_CLKN	I	WT_CLKN	Not Applicable	
A21	WT_D0P	I	WT_D0P	Not Applicable	
A22	WT_D0N	I	WT_D0N	Not Applicable	
A23	WT_D1P	I	WT_D1P	Not Applicable	
A24	WT_D1N	I	WT_D1N	Not Applicable	
A25	C_P32K	I	C_P32K	Not Applicable	Connected to 27 on the motherboard
A26	GND		GND	Not Applicable	

Pin #	Pin Name platform pinout	Direction w/respect to Wireless client Module	Function When CNVi Is Used	Function When Standard (Discrete) M.2 Is Used	Comments
A27	RESERVED		RESERVED	Not Applicable	Not connected
A28	RESERVED		RESERVED	Not Applicable	Not connected
A29	RESERVED		RESERVED	Not Applicable	Not connected
A30	RESERVED		RESERVED	Not Applicable	Not connected
A31	GND		GND	Not Applicable	
A32	WGR_CLKP	O	WGR_CLKP	Not Applicable	
A33	WGR_CLKN	O	WGR_CLKN	Not Applicable	
A34	WGR_D0P	O	WGR_D0P	Not Applicable	
A35	WGR_D0N	O	WGR_D0N	Not Applicable	
A36	WGR_D1P	O	WGR_D1P	Not Applicable	
A37	WGR_D1N	O	WGR_D1N	Not Applicable	
A38	BRI_DT	I	BRI_DT	Not Applicable	
A39	BRI_RSP	O	BRI_RSP	Not Applicable	
A40	RGI_DT	I	RGI_DT	Not Applicable	
A41	RGI_RSP	O	RGI_RSP	Not Applicable	
A42	RF_RESET_B	I	RF_RESET_B	Not Applicable	
A43	CLKREQ0	I	CLKREQ0	Not Applicable	
A44	REFCLK0		REFCLK0	Not Applicable	Disconnected/floating on M.2 side
A45	NO CONNECT		NO CONNECT	Not Applicable	Pin must be left floating
A46	RESERVED		RESERVED	Not Applicable	Not connected
A47	RESERVED		RESERVED	Not Applicable	Not connected
A48	3.3V		3.3V	Not Applicable	
A49	3.3V		3.3V	Not Applicable	
A50	GND		GND	Not Applicable	

3.2 Input/output electrical specifications

Table 3-3 Input/output electrical specifications

I/O type	Symbol	Parameter	Min	Max	Unit	Notes
1.8V I/O RF_RESET_B	V_{IH}	Input High Voltage	1.26	2.1	V	
	V_{IL}	Input Low Voltage	-0.3	0.54	V	
	$R_{PU/PD}$	Weak Pull-Up or Pull-Down	70	150	Kohm	
	I_{IN}	Input Leakage Current		10	uA	No Pull Up/Down
	V_{OH}	Output High Voltage	1.62	1.8	V	When used as Input the following is less relevant Io = 2mA Load = 20pF
	V_{OL}	Output Low Voltage	0	0.18		
	T_R, T_F	Rise, Fall Time		6	ns	
	C_{IO}	IO Pin Capacitance		2	pF	
1.8V FS I/O ~~A4WP_IRQ#~~ ~~A4WP_I2C_CLK~~ ~~A4WP_I2C_CLK~~ (Note 1, A4WP placeholder; no longer in use)	V_{IH}	Input High Voltage	1.26	2.1	V	
	V_{IL}	Input Low Voltage	-0.3	0.54	V	
	$R_{PU/PD}$	Weak Pull-Up or Pull-Down	100	180	Kohm	
	I_{IN}	Input Leakage Current		10	uA	No Pulls
	V_{OL} Push-Pull	Output Low Voltage Push-pull	0	0.36		Io = 2mA Load = 50pF
	V_{OH} Push-Pull	Output Low Voltage Push-pull	1.62	1.8		Io = 2mA Load = 50pF
	T_R, T_F Push-Pull	Rise, Fall Time Push-pull		18.5	ns	Load = 50pF
	V_{OL} Open Drain	Output Low Voltage	0	0.36		Io = 2mA Load = 64pF RPU = 1Kohm
	C_{IO}	IO Pin Capacitance		2	pF	
1.8V FS_CR CLKREQ0 (Note 2)	V_{IH}	Input High Voltage	1.26	2.1	V	
	V_{IL}	Input Low Voltage	-0.3	0.54	V	
	$R_{PU/PD}$	Weak Pull-Up or Pull-Down	100	180	Kohm	
	I_{IN}	Input Leakage Current		10	uA	No Pulls
	V_{OH}	Output High Voltage	1.62	1.8	V	
	V_{OL}	Output Low Voltage	0	0.18		

I/O type	Symbol	Parameter	Min	Max	Unit	Notes
	T_R, T_F	Rise, Fall Time		18.5ns (out-put) to 10 uSec (input)	ns	When used as input, the following is less relevant: Io = 2mA Load = 20pF Actual Rise/Fall Time as input can be up-to 10uSec
	C_{IO}	IO Pin Capacitance		2	pF	
1.8V FS_3VT C_P32K (Note 3)	V_{IH}	Input High Voltage	1.26	2.1	V	
	V_{IL}	Input Low Voltage	-0.3	0.54	V	
	$R_{PU/PD}$	Weak Pull-Up or Pull-Down	150 (typical)		Kohm	
	I_{IN}	Input Leakage Current		10	uA	No Pulls
	V_{OH}	Output High Voltage	1.62	1.8	V	Io = 1mA Load = 30pF
	V_{OL}	Output Low Voltage	0	0.18		Io = 1mA Load = 30pF
	T_R, T_F	Rise, Fall Time		20	ns	Load = 30pF
	C_{IO}	IO Pin Capacitance		2	pF	
BRI and RGI 1.8V I/O BRI_DT BRI_RSP RGI_DT RGI_RSP (Note 4)	V_{IH}	Input High Voltage	1.26	2.1	V	
	V_{IL}	Input Low Voltage	-0.3	0.54	V	
	$R_{PU/PD}$					
	I_{IN}					
	V_{OH}	Output High Voltage	1.62	1.8	V	50ohm driver impedance Load = 35pF T_R, T_F 30%-70%
	V_{OL}	Output Low Voltage	0	0.18		
	T_R, T_F	Rise, Fall Time		7	ns	
	C_{IO}	IO Pin Capacitance		2	pF	
CNVio (Note 5)	Signal parameters follow the MIPI D-PHY Specifications, Rev 2.					

NOTE:

1. I2C is not in use in the HrP case, but for any other combination (JfP/CcP), I2C max speed will be 1MHz (Fast plus mode). I2C SDA and SCL I/Os must comply with 120ns max rise/fall time. I/O are protected against back-bias up to 1.8V and can withstand I/O voltage when the power supply is off.
2. I/O are protected against back-bias up to 1.98V and can withstand I/O voltage when the power supply is off.
3. Input is 3.6V tolerant. I/O are protected against back-bias up to 3.6V and can withstand I/O voltage when the power supply is off.
4. I/O is protected against back-bias up to 1.98V and can withstand I/O voltage when the power supply is off. See more on those signals and directives in the Platform design Guide line section.
5. The CNVio (D-PHY) I/O pins must comply with the DC electrical specifications in *MIPI Alliance Specification for D-PHY Rev1.1*. Specifically, the CNVio HrP transmitter (HrP to Quasar) DC characteristics are found in Section 9.1, Table 16. The CNVio HrP receiver (Quasar to HrP) DC characteristics are found in Section 9.2, Table 20.

3.3 Peak current consumption

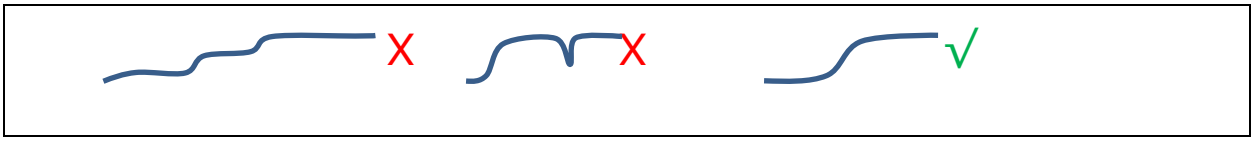
Table 3-4 Peak current consumption

Name	Description	Value [mA]	Notes
Peak current	Peak current from 3.3 V supply (over 100uSec)	Total theoretical M.2 spec worst case: 2000mA Actual Peak for any TDP/thermal or Current calculations: 800mA	Theoretical for general M.2 Cards 4*500mA per Vcc pin, assuming peak of Max Current over average at 100uSec Note that for HrP, the power consumption peak will be up to **800mA**

3.4 M.2 power and ripple limits

The supply voltage rise should be continuous and with a max rise time of 10 mSec (0 V to 3.3 V). It should not have any glitches or steps. Figure 3–1 shows examples of wrongful power-ups and of the correct rise flow.

Figure 3–1 Power supply rise flow



3.4.1 Power supply ripples

There must not be any glitches on the power supply that dip more 0.3 V. Any glitch that is higher than 0.3 V may be interpreted by the module as a *power-on reset*, which will cause the module to lose stored data and reboot.

During platform low-power modes, glitches during power state transitions such as S0->S3 (stand-by state) may lead to connection failure.

In addition, when using the CNVi architecture (CNVi part integrated into the PCH and Companion RF module added on the platform), the CRF module must have constant power, 3.3V, supplied and maintained prior to or together with the init flow of the PCH (and the CNVi IP inside it), or else the CRF may not be identified correctly. It is highly recommended to not have any power switch on the wireless card that can case race with the power-on of the CRF-SoC.

3.4.2 Platform state transitions

Platform designers should carefully design the transition from platform *on* state to platform *stand-by* state and vice versa, so that the power supply will remain stable and have no glitches.

Table 3-5 M.2 power supply and ripple limits

Platform Power Rail Requirements	
Power supply voltage range	3.3 V +/– 0.165 V (and for low value: <0.5v–0v)
Power on rise time	<10 msec
Maximum ripple	200 mVPP, frequency 10–500 kHz
Allowed power rail noise	300 mVpp

3.5 M.2 ground (GND)

All ground pins are connected on the M.2 module to a common ground plane. The platform designer should connect all M.2 GND pins to the platform system GND.

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4 Mechanical Specifications

Note: The module's mechanical specifications adhere to the *PCIe M.2 Electromechanical Spec*.

4.1 Weight

Table 4-1 Weight

Product SKU	Size (mm × mm)	Weight (g)
JfP/HrP 2230	22x30	2.33 +/– 0.3 g
JfP/HrP 1216	12x16	0.61 +/– 0.1 g

4.2 M.2 2230 mechanical specification

This section describes the mechanical specification of Jefferson/Harrison Peak 2230 modules. Figure 4–1 shows the dimensions for type 2230. Antenna connector configuration and functionality for this form factor is listed in Table 4–2 and shown in Figure 4–2.

Note: When testing a card or interacting with a card on a platform, it is a MUST to have the retention screw tightened and not leave the card non-retained

Figure 4–1 JfP/HrP M.2 2230 SKU dimensions

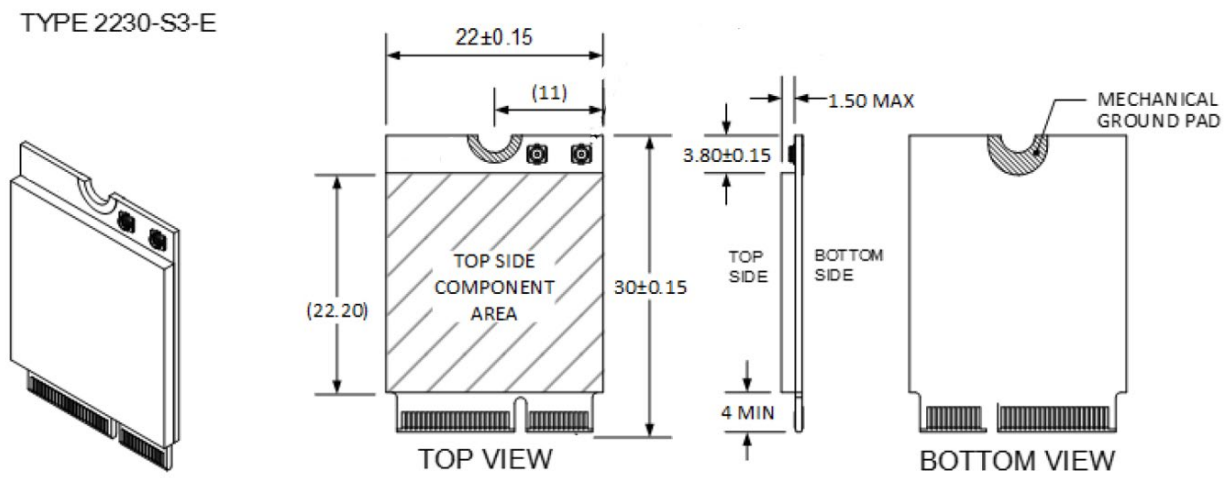
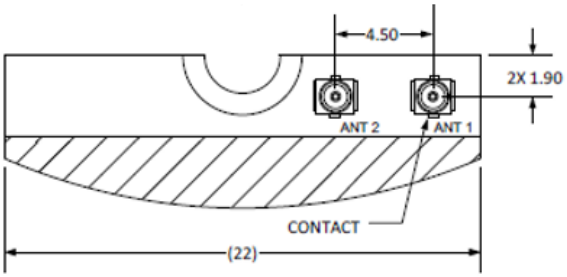


Table 4-2 Type 2230 antenna connector functionality

Antenna connector functionality	
Wi-Fi (chain A)+ BT	ANT1
Wi-Fi (chain B)	ANT2

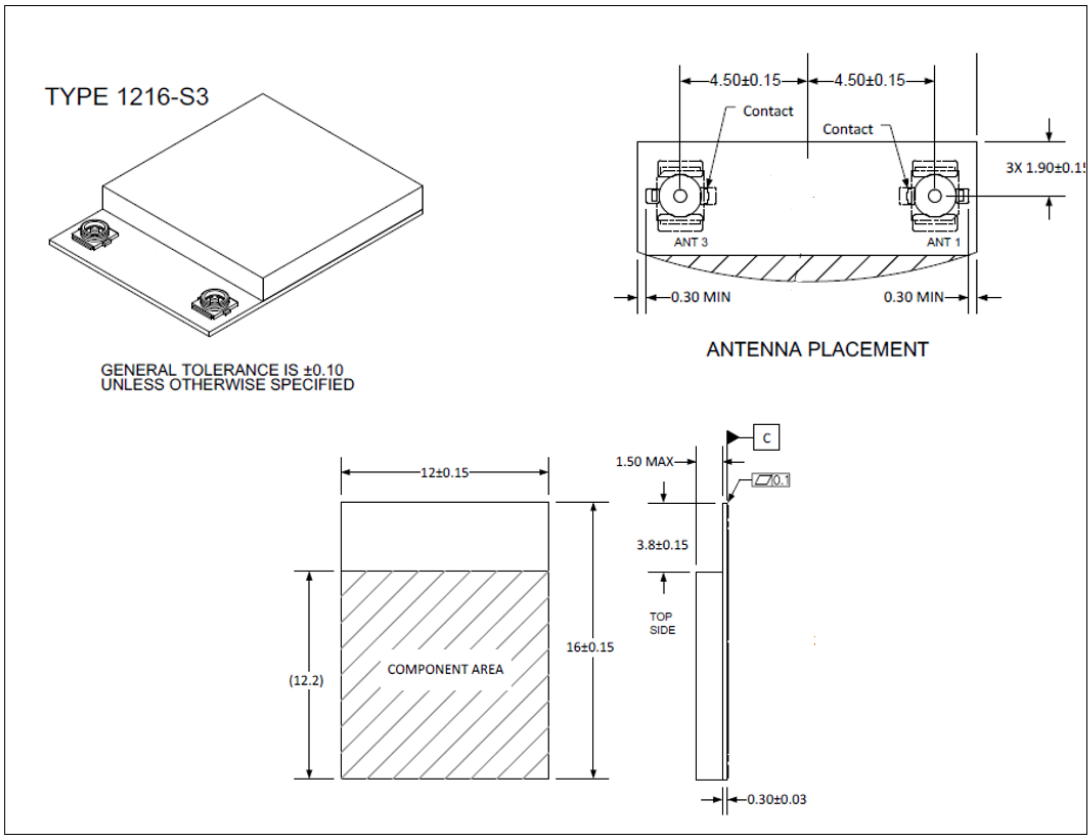
Figure 4–2 JfP/HrP M.2 2230 SKU antenna configuration



4.3 M.2 1216 mechanical specification

This section describes the mechanical specification of the JfP/HrP 1216 modules. Figure 4–3 shows the dimensions for type 1216. The antenna connector configuration and functionality for this form factor is listed in Table 4–3 and shown in Figure 4–3.

Figure 4–3 JfP/HrP M.2 1216 SKU dimensions



Antenna connector functional allocation for this form factor is defined in Table 4–3 (note the functionality is vendor-defined according to the M.2 spec).

Note: In JfP/HrP 1216, antenna ANT2 is not present.

Table 4-3 Type 1216 antenna connector functionality

Antenna connector functionality	
Wi-Fi (chain A) + BT	ANT1
Wi-Fi (Chain B)	ANT3

4.4 HrP 1216 Z height

HrP supports S3 Z height module 1.65+/-0.05 mm from module bottom surface to the top of the shield.

4.5 M.2 antenna retention

4.5.1 Recommended method for retention of M.2 cable

- It is recommended to restrain the antenna cables of M.2 products within the first 25 mm or less of cable length leaving the RF connectors on the module.
- It is recommended to use a robust tape or adhesive to secure the cables so they do not move or pull on the RF connector during shock and vibration of the system, as shown in Figure 4–4.

Figure 4–4 Retention of M.2 cables

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5 Thermal Specifications

Note: The numbers in this section are not final, and are subject to change.

5.1 Thermal dissipation

Maximum thermal dissipation is based on the assumption that both Wi–Fi and Bluetooth® communication are active. Table 5–1 describes the thermal dissipation and targets per operated mode.

Table 5-1 Thermal dissipation

Use Case		PC (mW)	
Wi–Fi	**BT**	**Wi–Fi**	**BT**
Worst case TDP: Based on average power consumption measurement over five minutes with max TCP/IP throughput activity.	**Worst case TDP** Based on average power consumption measurement over five minutes A2DP throughput activity	2300	100
Peak TDP (40MHz MCS0 2x2 HB 19.5dBm)	**Peak TDP** (TX 10dBm)	2500	240

Note: Total Peak gets to 2740mW that is translated to ~800mA (791mW) of peak Current consumption (assuming worst case Voltage of 3.3+5%=3.465v)

Note: Not applicable for scenarios that may only be exercised using lab or OEM support software tools.

5.2 Thermal specifications

Table 5-2 Thermals management

Name	Description
Thermal shield performance targets	Full performance at 50 ºC ambient (or at shield temperatures up to 80 ºC Functional operation is shield temperatures up to 85 ºC) For Oven-based testing conditions: **High temperture limit:** ~50 ºC (ambient) under controlled environment (oven), with no air flow (inside a box, in the oven) for Full perfromance. (And 55 ºC for Functional operation.) **Low temperture limit:** 0 ºC (starting point) under controlled environment (oven), with no air flow (inside a box).
Thermal silicon protection (CT–Kill)	Thermal silicon protection will not be activated below 85 ºC T-Shield temperature

NOTE:

1. Temperature values listed are as measured on the product shield; if measured as ambient Oven temperature it should be: T-Oven = T-Shield-30 c.

5.3 Thermal management

The device thermal management cuts off RF operation once a maximum temperature threshold (Critical Temperature termination CT–Kill) has been exceeded. After the cutoff point is reached, the RF remains at the off state until it cools down to the thermal activation threshold. During this time, the host cannot set the RF back to on.

When the product is heating up and nearing CT Kill, it will start decreasing the Wi-Fi activity in order to prevent the unit from heating further and reaching critical temperature. In such case, connectivity will be maintained but performance might be degraded gradually.

5.4 Module placement recommendations

The module disperses excess heat through the RF shield and the screws that ground the module to the chassis.

Correct module placement will ensure optimal thermal performance:

- The module orientation should be shield up.
- The module connection to chassis should be with a single metal screw.

5.5 Nonoperational module thermal storage

Table 5-3 Storage conditions

Environment	Limits
Storage Temperature (Non–Operational)	–40 ºC to 70 ºC (external direct temperture)
Humidity (Non–Operational)	50% to 90% non–condensing (at temperatures of 25 ºC to 35 ºC)

§

6 Performance KPIs

6.1 Wi-Fi channels

6.1.1 2.4GHz band channels

The supported channels are from 2.4GHz to 2.483GHZ, with channels 1-13 (for 20MHz channels).

Potentially supported channel-widths in this range are: 2-4-8-10-20-40 MHz channel width.

Figure 6–1 2.4GHz band channels

Frequency [GHz]	2.402	2.407	2.412	2.417	2.422	2.427	2.432	2.437	2.442	2.447	2.452	2.457	2.462	2.467	2.472	2.477	2.482
20MHz channel #			1	2	3	4	5	6	7	8	9	10	11	12	13		
20MHz																	
40MHz																	

6.1.2 5GHz band channels

The supported channels are from 5.170GHz to 5.33GHZ, 5.49GHz to 5.73GHz, and 5.735 to 5.835GHz, with channels 36-64, 100-144, 149-165 (for 20MHz channels).

Supported channel widths in this range are: 2-4-8 10-20-40-80-160 MHz channel width.

Figure 6–2 5GHz band channels

Domain	UNII-1				UNII-2					UNII-2 Extended													UNII-3				
DFS	NonDFS				DFS					DFS													NonDFS				
Frequency [GHz]	5.18 / 5.17	5.2	5.22	5.24	5.26	5.28	5.3	5.32		5.5 / 5.49	5.52	5.54	5.56	5.58	5.6	5.62	5.64	5.66	5.68	5.7	5.72		5.745 / 5.735	5.765	5.785	5.805	5.825
20MHz channel #	36	40	44	48	52	56	60	64		100	104	108	112	116	120	124	128	132	136	140	144		149	153	157	161	165
20MHz																											
40MHz																											
80MHz																											
160MHz																											

* 160MHz channels are supported in HrP2 case, and not in HrP1 case.

6.2 RF KPIs

6.2.1 Wi-Fi TX KPIs

All values below reflect the potential Tx Power of the product, and may not be used in the actual, specific product in a specific platform, Depending on the regulation limits selected per platform, see in the next regulatory section for the per regulation specific Tx Limits of the product.

All the following KPIs are the POR for the HrP2 case (as the more generic product). In the case of HrP1, the final values are not yet formalized; for now they shall be =(Min(ChainA, ChainB)-1) from the HrP2 tables.

Table 6-1 HrP 2x2 2230 TX Power per MCS

HrP 2x2 2230 TX Power per MCS														
Accuracy +/– 1dB														
						ETSI (EU) [dBm]			FCC (US) [dBm]			Default [dBm]		
Modulation	Band	BW	Channel	Channel Index	MCS	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB
.11b	LB	20MHz	2412	1	CCK11	15.5	15.5		19	19		15.5	15.5	
.11b	LB	20MHz	2417	2	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2422	3	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2427	4	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2432	5	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2437	6	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2442	7	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2447	8	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2452	9	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2457	10	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2462	11	CCK11	15.5	15.5		19	19		15.5	15.5	
.11b	LB	20MHz	2467	12	CCK11	15.5	15.5		18	18		15.5	15.5	
.11b	LB	20MHz	2472	13	CCK11	15.5	15.5		18	18		15.5	15.5	
.11g	LB	20MHz	2412	1	Rate6	16	16	13	16.25	16.5	13.5	15	15	11
.11g	LB	20MHz	2412	1	54	16	16	13	16.25	16.5	13.5	15	15	11
.11g	LB	20MHz	2417	2	Rate6	16	16	13	18	18	16	16	16	13
.11g	LB	20MHz	2417	2	54	16	16	13	17.25	17.25	16	16	16	13
.11g	LB	20MHz	2422	3	Rate6	16	16	13	19.25	19.25	17	16	16	13
.11g	LB	20MHz	2422	3	54	16	16	13	17.25	17.25	17	16	16	13

HrP 2x2 2230 TX Power per MCS														
Accuracy +/– 1dB														
						ETSI (EU) [dBm]			FCC (US) [dBm]			Default [dBm]		
Modulation	Band	BW	Channel	Channel Index	MCS	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB
.11g	LB	20MHz	2427	4	Rate6	16	16	13	19.25	19.25	17	16	16	13
.11g	LB	20MHz	2427	4	54	16	16	13	17.25	17.25	17	16	16	13
.11g	LB	20MHz	2432	5	Rate6	16	16	13	19.25	19.25	17	16	16	13
.11g	LB	20MHz	2432	5	54	16	16	13	17.25	17.25	17	16	16	13
.11g	LB	20MHz	2437	6	Rate6	16	16	13	19.25	19.25	17	16	16	13
.11g	LB	20MHz	2437	6	54	16	16	13	17.25	17.25	17	16	16	13
.11g	LB	20MHz	2442	7	Rate6	16	16	13	19.25	19.25	16.5	16	16	13
.11g	LB	20MHz	2442	7	54	16	16	13	17.25	17.25	16.5	16	16	13
.11g	LB	20MHz	2447	8	Rate6	16	16	13	19.25	19.25	16.5	16	16	13
.11g	LB	20MHz	2447	8	54	16	16	13	17.25	17.25	16.5	16	16	13
.11g	LB	20MHz	2452	9	Rate6	16	16	13	19.25	19.25	16.5	16	16	13
.11g	LB	20MHz	2452	9	54	16	16	13	17.25	17.25	16.5	16	16	13
.11g	LB	20MHz	2457	10	Rate6	16	16	13	18.25	18.25	16	16	16	13
.11g	LB	20MHz	2457	10	54	16	16	13	17.25	17.25	16	16	16	13
.11g	LB	20MHz	2462	11	Rate6	16	16	13	16	15.75	13.25	16	15.75	13
.11g	LB	20MHz	2462	11	54	16	16	13	16	15.75	13.25	16	15.75	13
.11g	LB	20MHz	2467	12	Rate6	16	16	13	14.5	14.5	12	14.5	14.5	12
.11g	LB	20MHz	2467	12	54	16	16	13	14.5	14.5	12	14.5	14.5	12
.11g	LB	20MHz	2472	13	Rate6	16	16	13	11.5	10	8.75	11.5	10	8.75
.11g	LB	20MHz	2472	13	54	16	16	13	11.5	10	8.75	11.5	10	8.75
.11n	LB	20MHz	2412	1	7	16	16	13	16.25	16.5	13.5	15	15	11
.11n	LB	20MHz	2417	2	7	16	16	13	17.25	17.25	16	16	16	13
.11n	LB	20MHz	2422	3	7	16	16	13	17.25	17.25	17	16	16	13
.11n	LB	20MHz	2427	4	7	16	16	13	17.25	17.25	17	16	16	13
.11n	LB	20MHz	2432	5	7	16	16	13	17.25	17.25	17	16	16	13
.11n	LB	20MHz	2437	6	7	16	16	13	17.25	17.25	17	16	16	13
.11n	LB	20MHz	2442	7	7	16	16	13	17.25	17.25	16.5	16	16	13
.11n	LB	20MHz	2447	8	7	16	16	13	17.25	17.25	16.5	16	16	13
.11n	LB	20MHz	2452	9	7	16	16	13	17.25	17.25	16.5	16	16	13

HrP 2x2 2230 TX Power per MCS														
Accuracy +/– 1dB														
						ETSI (EU) [dBm]			FCC (US) [dBm]			Default [dBm]		
Modulation	Band	BW	Channel	Channel Index	MCS	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB
.11n	LB	20MHz	2457	10	7	16	16	13	17.25	17.25	16	16	16	13
.11n	LB	20MHz	2462	11	7	16	16	13	16	15.75	13.25	16	15.75	13
.11n	LB	20MHz	2467	12	7	16	16	13	14.5	14.5	12	14.5	14.5	12
.11n	LB	20MHz	2472	13	7	16	16	13	11.5	10	8.75	11.5	10	8.75
.11ax	LB	20MHz	2412	1	11	15	15	13	15	15	13.5	15	15	11
.11ax	LB	20MHz	2437	6	11	15	15	13	15	15	15	15	15	13
.11ax	LB	20MHz	2462	11	11	15	15	13	15	15	13.25	15	15	13
.11ax	LB	20MHz	2467	12	11	15	15	13	14.5	14.5	12	14.5	14.5	12
.11ax	LB	20MHz	2472	13	11	15	15	13	11.5	10	8.75	11.5	10	8.75
.11a	HB	20MHz	5180	36	Rate6	16	16	13	18	18	16	16	16	13
.11a	HB	20MHz	5180	36	54	16	16	13	17.75	17	16	16	16	13
.11a	HB	20MHz	5200	40	Rate6	16	16	13	20	20	18	16	16	13
.11a	HB	20MHz	5200	40	54	16	16	13	17.75	17	17	16	16	13
.11a	HB	20MHz	5220	44	Rate6	16	16	13	20	20	18	16	16	13
.11a	HB	20MHz	5220	44	54	16	16	13	17.75	17	17	16	16	13
.11a	HB	20MHz	5240	48	Rate6	16	16	13	20	20	18	15	14.5	11.5
.11a	HB	20MHz	5240	48	54	16	16	13	17.75	17	17	15	14.5	11.5
.11a	HB	20MHz	5260	52	Rate6	16	16	13	20	20	17.75	15	14.75	11.75
.11a	HB	20MHz	5260	52	54	16	16	13	17.75	17	17	15	14.75	11.75
.11a	HB	20MHz	5280	56	Rate6	16	16	13	20	20	17.5	16	16	13
.11a	HB	20MHz	5280	56	54	16	16	13	17.75	17	17	16	16	13
.11a	HB	20MHz	5300	60	Rate6	16	16	13	19	19	16	16	16	13
.11a	HB	20MHz	5300	60	54	16	16	13	17.75	17	16	16	16	13
.11a	HB	20MHz	5320	64	Rate6	16	16	13	16.75	16.75	15.25	16	16	13
.11a	HB	20MHz	5320	64	54	16	16	13	16.75	16.75	15.25	16	16	13
.11a	HB	20MHz	5500	100	Rate6	16	16	13	17	17.25	15.75	16	16	13
.11a	HB	20MHz	5500	100	54	16	16	13	17	17.25	15.75	16	16	13
.11a	HB	20MHz	5520	104	Rate6	16	16	13	20	20	18	16	16	13
.11a	HB	20MHz	5520	104	54	16	16	13	17.75	17.5	17.5	16	16	13

HrP 2x2 2230 TX Power per MCS														
Accuracy +/– 1dB														
						ETSI (EU) [dBm]			FCC (US) [dBm]			Default [dBm]		
Modulation	Band	BW	Channel	Channel Index	MCS	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB
.11a	HB	20MHz	5785	157	Rate6	16	16	13	20	20	17.5	8	8	5
.11a	HB	20MHz	5785	157	54	16	16	13	17.75	17.5	17.5	8	8	5
.11a	HB	20MHz	5805	161	Rate6	16	16	13	20	20	17.5	8	8	5
.11a	HB	20MHz	5805	161	54	16	16	13	17.75	17.5	17.5	8	8	5
.11a	HB	20MHz	5825	165	Rate6	16	16	13	20	20	17.5	8	8	5
.11a	HB	20MHz	5825	165	54	16	16	13	17.75	17.5	17.5	8	8	5
.11n	HB	20MHz	5180	36	7	16	16	13	17.75	17	16	16	16	13
.11n	HB	20MHz	5200	40	7	16	16	13	17.75	17	17	16	16	13
.11n	HB	20MHz	5500	100	7	16	16	13	17	17.25	15.75	16	16	13
.11n	HB	20MHz	5580	116	7	16	16	13	17.75	17.5	17.5	16	16	13
.11n	HB	20MHz	5825	165	7	16	16	13	17.75	17.5	17.5	8	8	5
.11ac	HB	20MHz	5200	40	8	16	16	13	16.75	16.75	16.75	16	16	13
.11ac	HB	20MHz	5500	100	8	16	16	13	17	17	15.75	16	16	13
.11ac	HB	20MHz	5805	161	8	16	16	13	17	17	17	8	8	5
.11ax	HB	20MHz	5180	36	11	14	14	13	14	14	14	14	14	13
.11ax	HB	20MHz	5320	64	11	14	14	13	14	14	14	14	14	13
.11ax	HB	20MHz	5745	149	11	13.5	13.5	13	13.5	13.5	13.5	8	8	5
.11n	HB	40MHz	5190	38	7	17	17	14	17.5	17.5	15.25	16.5	16.5	13.5
.11n	HB	40MHz	5230	46	7	17	17	14	17.5	17.5	17.5	16.5	16.5	13.5
.11n	HB	40MHz	5510	102	7	17	17	14	17	17	15.75	17	17	14
.11n	HB	40MHz	5795	159	7	17	17	14	17.75	17.75	17.75	8	8	5
.11ac	HB	40MHz	5230	46	9	16	16	14	16	16	16	16	16	13.5
.11ac	HB	40MHz	5510	102	9	16	16	14	16	16	15.75	16	16	14
.11ac	HB	40MHz	5795	159	9	15.75	16	14	15.75	16	15.75	8	8	5
.11ax	HB	40MHz	5190	38	11	14	14	14	14	14	14	14	14	13.5
.11ax	HB	40MHz	5510	102	11	14	14	14	14	14	14	14	14	14
.11ax	HB	40MHz	5755	151	11	13.5	13.5	13.5	13.5	13.5	13.5	8	8	5
.11ac	HB	80MHz	5210	42	9	16.5	16.5	14	16.5	16.5	15	16.5	16.5	13.5
.11ac	HB	80MHz	5530	106	9	16.5	16.5	14	16.5	16.5	15	16.5	16.5	14

HrP 2x2 2230 TX Power per MCS														
Accuracy +/– 1dB														
						ETSI (EU) [dBm]			FCC (US) [dBm]			Default [dBm]		
Modulation	Band	BW	Channel	Channel Index	MCS	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB
.11ac	HB	80MHz	5775	155	9	15.5	15.75	14	15.5	15.75	15.5	8	8	5
.11ax	HB	80MHz	5210	42	11	14.5	14.5	14	14.5	14.5	14.5	14.5	14.5	13.5
.11ax	HB	80MHz	5290	58	11	14.5	14.5	14	14.5	14.5	13.5	14.5	14.5	13.5
.11ax	HB	80MHz	5530	106	11	14.5	14.5	14	14.5	14.5	14.5	14.5	14.5	14
.11ax	HB	80MHz	5610	122	11	14.5	14.5	14	14.5	14.5	14.5	14.5	14.5	14
.11ax	HB	80MHz	5690	138	11	14.5	14.5	14	14.5	14.5	14.5	14.5	14.5	14
.11ax	HB	80MHz	5775	155	11	14.5	14.5	14	14.5	14.5	14.5	8	8	5
.11ac	HB	160MHz	5250	50	9	13.75	13.75	13.75	13.75	13.75	11.5	13.75	13.75	11.5
.11ac	HB	160MHz	5570	114	9	13.5	13.5	13.5	13.5	13.5	13	13.5	13.5	13
.11ax	HB	160MHz	5250	50	11	11.25	11.25	11.25	11.25	11.25	11.25	11.25	11.25	11.25
.11ax	HB	160MHz	5570	114	11	11.25	11.25	11.25	11.25	11.25	11.25	11.25	11.25	11.25

Table 6-2 HrP 2x2 1216 TX Power per MCS

HrP 2x2 1216 TX Power per MCS														
Accuracy +/– 1dB														
						ETSI (EU) [dBm]			FCC (US) [dBm]			Default [dBm]		
Modulation	Band	BW	Channel	Channel Index	MCS	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB
.11b	LB	20MHz	2412	1	CCK11	15.5	15.5		19	18.75		15.5	15.5	
.11b	LB	20MHz	2417	2	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2422	3	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2427	4	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2432	5	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2437	6	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2442	7	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2447	8	CCK11	15.5	15.5		20	20		15.5	15.5	

HrP 2x2 1216 TX Power per MCS														
Accuracy +/– 1dB														
						ETSI (EU) [dBm]			FCC (US) [dBm]			Default [dBm]		
Modulation	Band	BW	Channel	Channel Index	MCS	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB
.11b	LB	20MHz	2452	9	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2457	10	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2462	11	CCK11	15.5	15.5		19	19		15.5	15.5	
.11b	LB	20MHz	2467	12	CCK11	15.5	15.5		18	18		15.5	15.5	
.11b	LB	20MHz	2472	13	CCK11	15.5	15.5		18.5	18.5		15.5	15.5	
.11g	LB	20MHz	2412	1	Rate6	16	16	13	16.25	16.5	13.5	15	15	11.5
.11g	LB	20MHz	2412	1	54	16	16	13	16.25	16.5	13.5	15	15	11.5
.11g	LB	20MHz	2417	2	Rate6	16	16	13	18	18	16	16	16	13
.11g	LB	20MHz	2417	2	54	16	16	13	17	17	16	16	16	13
.11g	LB	20MHz	2422	3	Rate6	16	16	13	19.5	19.5	17	16	16	13
.11g	LB	20MHz	2422	3	54	16	16	13	17	17	17	16	16	13
.11g	LB	20MHz	2427	4	Rate6	16	16	13	19.5	19.5	17	16	16	13
.11g	LB	20MHz	2427	4	54	16	16	13	17	17	17	16	16	13
.11g	LB	20MHz	2432	5	Rate6	16	16	13	19.5	19.5	17	16	16	13
.11g	LB	20MHz	2432	5	54	16	16	13	17	17	17	16	16	13
.11g	LB	20MHz	2437	6	Rate6	16	16	13	19.5	19.5	17	16	16	13
.11g	LB	20MHz	2437	6	54	16	16	13	17	17	17	16	16	13
.11g	LB	20MHz	2442	7	Rate6	16	16	13	19.5	19.5	16.5	16	16	13
.11g	LB	20MHz	2442	7	54	16	16	13	17	17	16.5	16	16	13
.11g	LB	20MHz	2447	8	Rate6	16	16	13	19.5	19.5	16.5	16	16	13
.11g	LB	20MHz	2447	8	54	16	16	13	17	17	16.5	16	16	13
.11g	LB	20MHz	2452	9	Rate6	16	16	13	19.5	19.5	16.5	16	16	13
.11g	LB	20MHz	2452	9	54	16	16	13	17	17	16.5	16	16	13
.11g	LB	20MHz	2457	10	Rate6	16	16	13	18.25	18.25	16	16	16	13
.11g	LB	20MHz	2457	10	54	16	16	13	17	17	16	16	16	13
.11g	LB	20MHz	2462	11	Rate6	16	16	13	15	14.5	13	15	14.5	13
.11g	LB	20MHz	2462	11	54	16	16	13	15	14.5	13	15	14.5	13
.11g	LB	20MHz	2467	12	Rate6	16	16	13	14.5	14.5	12.5	14.5	14.5	12.5
.11g	LB	20MHz	2467	12	54	16	16	13	14.5	14.5	12.5	14.5	14.5	12.5

HrP 2x2 1216 TX Power per MCS														
Accuracy +/– 1dB														
						ETSI (EU) [dBm]			FCC (US) [dBm]			Default [dBm]		
Modulation	Band	BW	Channel	Channel Index	MCS	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB
.11g	LB	20MHz	2472	13	Rate6	16	16	13	12.25	12	10	12.25	12	10
.11g	LB	20MHz	2472	13	54	16	16	13	12.25	12	10	12.25	12	10
.11n	LB	20MHz	2412	1	7	16	16	13	16.25	16.5	13.5	15	15	11.5
.11n	LB	20MHz	2417	2	7	16	16	13	17	17	16	16	16	13
.11n	LB	20MHz	2422	3	7	16	16	13	17	17	17	16	16	13
.11n	LB	20MHz	2427	4	7	16	16	13	17	17	17	16	16	13
.11n	LB	20MHz	2432	5	7	16	16	13	17	17	17	16	16	13
.11n	LB	20MHz	2437	6	7	16	16	13	17	17	17	16	16	13
.11n	LB	20MHz	2442	7	7	16	16	13	17	17	16.5	16	16	13
.11n	LB	20MHz	2447	8	7	16	16	13	17	17	16.5	16	16	13
.11n	LB	20MHz	2452	9	7	16	16	13	17	17	16.5	16	16	13
.11n	LB	20MHz	2457	10	7	16	16	13	17	17	16	16	16	13
.11n	LB	20MHz	2462	11	7	16	16	13	15	14.5	13	15	14.5	13
.11n	LB	20MHz	2467	12	7	16	16	13	14.5	14.5	12.5	14.5	14.5	12.5
.11n	LB	20MHz	2472	13	7	16	16	13	12.25	12	10	12.25	12	10
.11ax	LB	20MHz	2412	1	11	15	15	13	15	15	13.5	15	15	11.5
.11ax	LB	20MHz	2437	6	11	15	15	13	15	15	15	15	15	13
.11ax	LB	20MHz	2462	11	11	15	15	13	15	14.5	13	15	14.5	13
.11ax	LB	20MHz	2467	12	11	15	15	13	14.5	14.5	12.5	14.5	14.5	12.5
.11ax	LB	20MHz	2472	13	11	15	15	13	12.25	12	10	12.25	12	10
.11a	HB	20MHz	5180	36	Rate6	16	16	13	18	18	15.25	15.75	15.75	13
.11a	HB	20MHz	5180	36	54	16	16	13	18	18	15.25	15.75	15.75	13
.11a	HB	20MHz	5200	40	Rate6	16	16	13	19	19.5	17.5	15.75	15.75	13
.11a	HB	20MHz	5200	40	54	16	16	13	18	18	17.5	15.75	15.75	13
.11a	HB	20MHz	5220	44	Rate6	16	16	13	20	20	18	15.75	15.75	13
.11a	HB	20MHz	5220	44	54	16	16	13	18	18	18	15.75	15.75	13
.11a	HB	20MHz	5240	48	Rate6	16	16	13	20	20	18	15	15	12
.11a	HB	20MHz	5240	48	54	16	16	13	18	18	18	15	15	12
.11a	HB	20MHz	5260	52	Rate6	16	16	13	20	20	18	15	15	12

HrP 2x2 1216 TX Power per MCS

Accuracy +/– 1dB

						ETSI (EU) [dBm]			FCC (US) [dBm]			Default [dBm]		
Modulation	Band	BW	Channel	Channel Index	MCS	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB
.11a	HB	20MHz	5260	52	54	16	16	13	18	18	18	15	15	12
.11a	HB	20MHz	5280	56	Rate6	16	16	13	20	20	18	16	16	13
.11a	HB	20MHz	5280	56	54	16	16	13	18	18	18	16	16	13
.11a	HB	20MHz	5300	60	Rate6	16	16	13	20	20	17.5	16	16	13
.11a	HB	20MHz	5300	60	54	16	16	13	18	18	17.5	16	16	13
.11a	HB	20MHz	5320	64	Rate6	16	16	13	17.5	17.75	15.5	16	16	13
.11a	HB	20MHz	5320	64	54	16	16	13	17.5	17.75	15.5	16	16	13
.11a	HB	20MHz	5500	100	Rate6	16	16	13	18.5	18.5	15.25	16	16	13
.11a	HB	20MHz	5500	100	54	16	16	13	18	18	15.25	16	16	13
.11a	HB	20MHz	5520	104	Rate6	16	16	13	20	20	18.25	16	16	13
.11a	HB	20MHz	5520	104	54	16	16	13	18	18	18	16	16	13
.11a	HB	20MHz	5785	157	Rate6	16	16	13	20	20	17.5	8	8	5
.11a	HB	20MHz	5785	157	54	16	16	13	18	18	17.5	8	8	5
.11a	HB	20MHz	5805	161	Rate6	16	16	13	20	20	17.5	8	8	5
.11a	HB	20MHz	5805	161	54	16	16	13	18	18	17.5	8	8	5
.11a	HB	20MHz	5825	165	Rate6	16	16	13	20	20	17.5	8	8	5
.11a	HB	20MHz	5825	165	54	16	16	13	18	18	17.5	8	8	5
.11n	HB	20MHz	5180	36	7	16	16	13	18	18	15.25	15.75	15.75	13
.11n	HB	20MHz	5200	40	7	16	16	13	18	18	17.5	15.75	15.75	13
.11n	HB	20MHz	5500	100	7	16	16	13	18	18	15.25	16	16	13
.11n	HB	20MHz	5580	116	7	16	16	13	18.25	18.25	18.25	16	16	13
.11n	HB	20MHz	5825	165	7	16	16	13	18	18	17.5	8	8	5
.11ac	HB	20MHz	5200	40	8	16	16	13	17.5	17.5	17.5	15.75	15.75	13
.11ac	HB	20MHz	5500	100	8	16	16	13	17.5	17.5	15.25	16	16	13
.11ac	HB	20MHz	5805	161	8	16	16	13	17.5	17.5	17.5	8	8	5
.11ax	HB	20MHz	5180	36	11	14	14	13	14	14	14	14	14	13
.11ax	HB	20MHz	5320	64	11	14	14	13	14	14	14	14	14	13
.11ax	HB	20MHz	5745	149	11	14	14	13	14	14	14	8	8	5
.11n	HB	40MHz	5190	38	7	17	17	14	18	18	15.25	16.75	16.75	14

HrP 2x2 1216 TX Power per MCS														
Accuracy +/– 1dB														
						ETSI (EU) [dBm]			FCC (US) [dBm]			Default [dBm]		
Modulation	Band	BW	Channel	Channel Index	MCS	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB
.11n	HB	40MHz	5230	46	7	17	17	14	18.25	18	18	16.75	17	14
.11n	HB	40MHz	5510	102	7	17	17	14	17.75	17.75	15.75	17	17	14
.11n	HB	40MHz	5795	159	7	17	17	14	18.25	18.25	18	8	8	5
.11ac	HB	40MHz	5230	46	9	16.5	16.5	14	16.5	16.5	16.5	16.5	16.5	14
.11ac	HB	40MHz	5510	102	9	16.5	16.5	14	16.5	16.5	15.75	16.5	16.5	14
.11ac	HB	40MHz	5795	159	9	16.5	16.5	14	16.5	16.5	16.5	8	8	5
.11ax	HB	40MHz	5190	38	11	14.25	14.25	14	14.25	14.25	14.25	14.25	14.25	14
.11ax	HB	40MHz	5510	102	11	14.25	14.25	14	14.25	14.25	14.25	14.25	14.25	14
.11ax	HB	40MHz	5755	151	11	14.25	14.25	14	14.25	14.25	14.25	8	8	5
.11ac	HB	80MHz	5210	42	9	16.5	16.25	14	16.5	16.25	15.5	16.5	16.25	13.5
.11ac	HB	80MHz	5530	106	9	16	16	14	16	16	15.5	16	16	14
.11ac	HB	80MHz	5775	155	9	16.5	16.5	14	16.5	16.5	16	8	8	5
.11ax	HB	80MHz	5210	42	11	14.25	14.25	14	14.25	14.25	14.25	14.25	14.25	13.5
.11ax	HB	80MHz	5290	58	11	14.25	14.25	14	14.25	14.25	14	14.25	14.25	13.5
.11ax	HB	80MHz	5530	106	11	14.25	14.25	14	14.25	14.25	14.25	14.25	14.25	14
.11ax	HB	80MHz	5610	122	11	14.25	14.25	14	14.25	14.25	14.25	14.25	14.25	14
.11ax	HB	80MHz	5690	138	11	14.25	14.25	14	14.25	14.25	14.25	14.25	14.25	14
.11ax	HB	80MHz	5775	155	11	14.25	14.25	14	14.25	14.25	14.25	8	8	5
.11ac	HB	160MHz	5250	50	9	14	14	14	14	14	12.25	14	14	12
.11ac	HB	160MHz	5570	114	9	13.75	13.75	13.75	13.75	13.75	12.75	13.75	13.75	12.75
.11ax	HB	160MHz	5250	50	11	11.5	11.5	11.5	11.5	11.5	11.5	11.5	11.5	11.5
.11ax	HB	160MHz	5570	114	11	11.5	11.5	11.5	11.5	11.5	11.5	11.5	11.5	11.5

Table 6-3 HrP 2x2 1216LTE TX Power per MCS

HrP 2x2 1216LTE TX Power per MCS														
Accuracy +/– 1dB														
						ETSI (EU) [dBm]			FCC (US) [dBm]			Default [dBm]		
Modulation	Band	BW	Channel	Channel Index	MCS	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB
.11b	LB	20MHz	2412	1	CCK11	15.5	15.5		19	19		15.5	15.5	
.11b	LB	20MHz	2417	2	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2422	3	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2427	4	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2432	5	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2437	6	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2442	7	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2447	8	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2452	9	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2457	10	CCK11	15.5	15.5		20	20		15.5	15.5	
.11b	LB	20MHz	2462	11	CCK11	15.5	15.5		19	19		15.5	15.5	
.11b	LB	20MHz	2467	12	CCK11	15.5	15.5		18	17.5		15.5	15.5	
.11b	LB	20MHz	2472	13	CCK11	15.5	15.5		17.5	17.75		15.5	15.5	
.11g	LB	20MHz	2412	1	Rate6	16	16	13	17.75	17	14	15	15	11.5
.11g	LB	20MHz	2412	1	54	16	16	13	17.25	17	14	15	15	11.5
.11g	LB	20MHz	2417	2	Rate6	16	16	13	18	18	16	16	16	13
.11g	LB	20MHz	2417	2	54	16	16	13	17.25	17.25	16	16	16	13
.11g	LB	20MHz	2422	3	Rate6	16	16	13	19.5	19.5	17	16	16	13
.11g	LB	20MHz	2422	3	54	16	16	13	17.25	17.25	17	16	16	13
.11g	LB	20MHz	2427	4	Rate6	16	16	13	19.5	19.5	17	16	16	13
.11g	LB	20MHz	2427	4	54	16	16	13	17.25	17.25	17	16	16	13
.11g	LB	20MHz	2432	5	Rate6	16	16	13	19.5	19.5	17	16	16	13
.11g	LB	20MHz	2432	5	54	16	16	13	17.25	17.25	17	16	16	13
.11g	LB	20MHz	2437	6	Rate6	16	16	13	19.5	19.5	17	16	16	13
.11g	LB	20MHz	2437	6	54	16	16	13	17.25	17.25	17	16	16	13
.11g	LB	20MHz	2442	7	Rate6	16	16	13	19.5	19.5	16.75	16	16	13
.11g	LB	20MHz	2442	7	54	16	16	13	17.25	17.25	16.75	16	16	13
.11g	LB	20MHz	2447	8	Rate6	16	16	13	19.5	19.5	16.75	16	16	13

HrP 2x2 1216LTE TX Power per MCS														
Accuracy +/– 1dB														
						ETSI (EU) [dBm]			FCC (US) [dBm]			Default [dBm]		
Modulation	Band	BW	Channel	Channel Index	MCS	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB
.11g	LB	20MHz	2447	8	54	16	16	13	17.25	17.25	16.75	16	16	13
.11g	LB	20MHz	2452	9	Rate6	16	16	13	19.5	19.5	16.75	16	16	13
.11g	LB	20MHz	2452	9	54	16	16	13	17.25	17.25	16.75	16	16	13
.11g	LB	20MHz	2457	10	Rate6	16	16	13	18.25	18.25	15.25	16	16	13
.11g	LB	20MHz	2457	10	54	16	16	13	17.25	17.25	15.25	16	16	13
.11g	LB	20MHz	2462	11	Rate6	16	16	13	16.5	16	13.5	16	16	13
.11g	LB	20MHz	2462	11	54	16	16	13	16.5	16	13.5	16	16	13
.11g	LB	20MHz	2467	12	Rate6	16	16	13	14.5	14.5	11.5	14.5	14.5	11.5
.11g	LB	20MHz	2467	12	54	16	16	13	14.5	14.5	11.5	14.5	14.5	11.5
.11g	LB	20MHz	2472	13	Rate6	16	16	13	12	11.5	9	12	11.5	9
.11g	LB	20MHz	2472	13	54	16	16	13	12	11.5	9	12	11.5	9
.11n	LB	20MHz	2412	1	7	16	16	13	17.25	17	14	15	15	11.5
.11n	LB	20MHz	2417	2	7	16	16	13	17.25	17.25	16	16	16	13
.11n	LB	20MHz	2422	3	7	16	16	13	17.25	17.25	17	16	16	13
.11n	LB	20MHz	2427	4	7	16	16	13	17.25	17.25	17	16	16	13
.11n	LB	20MHz	2432	5	7	16	16	13	17.25	17.25	17	16	16	13
.11n	LB	20MHz	2437	6	7	16	16	13	17.25	17.25	17	16	16	13
.11n	LB	20MHz	2442	7	7	16	16	13	17.25	17.25	16.75	16	16	13
.11n	LB	20MHz	2447	8	7	16	16	13	17.25	17.25	16.75	16	16	13
.11n	LB	20MHz	2452	9	7	16	16	13	17.25	17.25	16.75	16	16	13
.11n	LB	20MHz	2457	10	7	16	16	13	17.25	17.25	15.25	16	16	13
.11n	LB	20MHz	2462	11	7	16	16	13	16.5	16	13.5	16	16	13
.11n	LB	20MHz	2467	12	7	16	16	13	14.5	14.5	11.5	14.5	14.5	11.5
.11n	LB	20MHz	2472	13	7	16	16	13	12	11.5	9	12	11.5	9
.11ax	LB	20MHz	2412	1	11	15	15	13	15	15	14	15	15	11.5
.11ax	LB	20MHz	2437	6	11	15	15	13	15	15	15	15	15	13
.11ax	LB	20MHz	2462	11	11	15	15	13	15	15	13.5	15	15	13
.11ax	LB	20MHz	2467	12	11	15	15	13	14.5	14.5	11.5	14.5	14.5	11.5
.11ax	LB	20MHz	2472	13	11	15	15	13	12	11.5	9	12	11.5	9

HrP 2x2 1216LTE TX Power per MCS														
Accuracy +/– 1dB														
						ETSI (EU) [dBm]			FCC (US) [dBm]			Default [dBm]		
Modulation	Band	BW	Channel	Channel Index	MCS	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB
.11a	HB	20MHz	5180	36	Rate6	16	16	13	18.5	18.5	15.5	16	16	13
.11a	HB	20MHz	5180	36	54	16	16	13	18	18	15.5	16	16	13
.11a	HB	20MHz	5200	40	Rate6	16	16	13	19.25	19.25	18	16	16	13
.11a	HB	20MHz	5200	40	54	16	16	13	18	18	18	16	16	13
.11a	HB	20MHz	5220	44	Rate6	16	16	13	20	20	18	16	16	13
.11a	HB	20MHz	5220	44	54	16	16	13	18	18	18	16	16	13
.11a	HB	20MHz	5240	48	Rate6	16	16	13	20	20	18	15.75	15.75	12.5
.11a	HB	20MHz	5240	48	54	16	16	13	18	18	18	15.75	15.75	12.5
.11a	HB	20MHz	5260	52	Rate6	16	16	13	20	20	18	15	15	12
.11a	HB	20MHz	5260	52	54	16	16	13	18	18	18	15	15	12
.11a	HB	20MHz	5280	56	Rate6	16	16	13	20	20	18	16	16	13
.11a	HB	20MHz	5280	56	54	16	16	13	18	18	18	16	16	13
.11a	HB	20MHz	5300	60	Rate6	16	16	13	20	20	18	16	16	13
.11a	HB	20MHz	5300	60	54	16	16	13	18	18	18	16	16	13
.11a	HB	20MHz	5320	64	Rate6	16	16	13	18	17.5	16	16	16	13
.11a	HB	20MHz	5320	64	54	16	16	13	18	17.5	16	16	16	13
.11a	HB	20MHz	5500	100	Rate6	16	16	13	18.75	18.75	16	16	16	13
.11a	HB	20MHz	5500	100	54	16	16	13	18.75	18.75	16	16	16	13
.11a	HB	20MHz	5520	104	Rate6	16	16	13	20	20	18.25	16	16	13
.11a	HB	20MHz	5520	104	54	16	16	13	18.75	18.75	18.25	16	16	13
.11a	HB	20MHz	5785	157	Rate6	16	16	13	20	20	18	7.5	7.5	4.5
.11a	HB	20MHz	5785	157	54	16	16	13	18	17.75	17.75	7.5	7.5	4.5
.11a	HB	20MHz	5805	161	Rate6	16	16	13	20	20	18	7.5	7.5	4.5
.11a	HB	20MHz	5805	161	54	16	16	13	18	17.75	17.75	7.5	7.5	4.5
.11a	HB	20MHz	5825	165	Rate6	16	16	13	20	20	18	7.5	7.5	4.5
.11a	HB	20MHz	5825	165	54	16	16	13	18	17.75	17.75	7.5	7.5	4.5
.11n	HB	20MHz	5180	36	7	16	16	13	18	18	15.5	16	16	13
.11n	HB	20MHz	5200	40	7	16	16	13	18	18	18	16	16	13
.11n	HB	20MHz	5500	100	7	16	16	13	18.75	18.75	16	16	16	13

HrP 2x2 1216LTE TX Power per MCS														
Accuracy +/– 1dB														
						ETSI (EU) [dBm]			FCC (US) [dBm]			Default [dBm]		
Modulation	Band	BW	Channel	Channel Index	MCS	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB
.11n	HB	20MHz	5580	116	7	16	16	13	18.25	18.25	18.25	16	16	13
.11n	HB	20MHz	5825	165	7	16	16	13	18	17.75	17.75	7.5	7.5	4.5
.11ac	HB	20MHz	5200	40	8	16	16	13	17.25	17.25	17.25	16	16	13
.11ac	HB	20MHz	5500	100	8	16	16	13	17.5	17.25	16	16	16	13
.11ac	HB	20MHz	5805	161	8	16	16	13	17.25	17.25	17.25	7.5	7.5	4.5
.11ax	HB	20MHz	5180	36	11	14.25	14.25	13	14.25	14.25	14.25	14.25	14.25	13
.11ax	HB	20MHz	5320	64	11	14.25	14.25	13	14.25	14.25	14.25	14.25	14.25	13
.11ax	HB	20MHz	5745	149	11	14	14	13	14	14	14	7.5	7.5	4.5
.11n	HB	40MHz	5190	38	7	17	17	14	18.25	18.25	15.5	16.5	16.5	14
.11n	HB	40MHz	5230	46	7	17	17	14	18.75	18.75	18	16.5	16.5	14
.11n	HB	40MHz	5510	102	7	17	17	14	17.75	17.75	16	17	17	14
.11n	HB	40MHz	5795	159	7	17	17	14	18.75	18.75	18	7.5	7.5	4.5
.11ac	HB	40MHz	5230	46	9	17	17	14	17.25	17.25	17.25	16.5	16.5	14
.11ac	HB	40MHz	5510	102	9	17	17	14	17.25	17.25	16	17	17	14
.11ac	HB	40MHz	5795	159	9	17	17	14	17.25	17.25	17.25	7.5	7.5	4.5
.11ax	HB	40MHz	5190	38	11	14.5	14.5	14	14.5	14.5	14.5	14.5	14.5	14
.11ax	HB	40MHz	5510	102	11	14.5	14.5	14	14.5	14.5	14.5	14.5	14.5	14
.11ax	HB	40MHz	5755	151	11	14.25	14.25	14	14.25	14.25	14.25	7.5	7.5	4.5
.11ac	HB	80MHz	5210	42	9	16.75	16.75	14	16.75	16.75	15	16.5	16.75	13.5
.11ac	HB	80MHz	5530	106	9	16.75	16	14	16.75	16	15.25	16.75	16	14
.11ac	HB	80MHz	5775	155	9	16.75	16.75	14	16.75	16.75	16.5	7.5	7.5	4.5
.11ax	HB	80MHz	5210	42	11	14.25	14.25	14	14.25	14.25	14.25	14.25	14.25	13.5
.11ax	HB	80MHz	5290	58	11	14.25	14.25	14	14.25	14.25	14.25	14.25	14.25	13.5
.11ax	HB	80MHz	5530	106	11	14.25	14.25	14	14.25	14.25	14.25	14.25	14.25	14
.11ax	HB	80MHz	5610	122	11	14.25	14.25	14	14.25	14.25	14.25	14.25	14.25	14
.11ax	HB	80MHz	5690	138	11	14.25	14.25	14	14.25	14.25	14.25	14.25	14.25	14
.11ax	HB	80MHz	5775	155	11	14.25	14.25	14	14.25	14.25	14.25	7.5	7.5	4.5
.11ac	HB	160MHz	5250	50	9	14.75	14.5	14	14.75	14.5	12.5	14.75	14.5	12
.11ac	HB	160MHz	5570	114	9	14.25	14	14	14	14	11.5	14	14	11.5

HrP 2x2 1216LTE TX Power per MCS														
Accuracy +/– 1dB														
						ETSI (EU) [dBm]			FCC (US) [dBm]			Default [dBm]		
Modulation	Band	BW	Channel	Channel Index	MCS	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB	SISO A	SISO B	MIMO AB
.11ax	HB	160MHz	5250	50	11	12.25	12.25	12.25	12.25	12.25	12.25	12.25	12.25	12
.11ax	HB	160MHz	5570	114	11	12	12	12	12	12	11.5	12	12	11.5

6.2.2 Wi-Fi RX KPIs

All the following KPIs are the POR for the HrP2 case (as the more generic product). In the case of HrP1, the final values are not yet formalized; for now they shall be =(Max(ChainA, ChainB)+1) from the HrP2 tables.

Table 6-4 HrP 2x2 2230 Rx sensitivity

					HrP 2230					
Mode	BW [MHz]	Conditions			Chain A [dBm, acc +/- 0.5 dB]			Chain B [dBm, acc +/- 0.5 dB]		
					LB/LHB	MHB	HHB	LB/LHB	MHB	HHB
11b	20	CCK, 1Mbps			-96.75			-96.75		
	20	CCK, 2Mbps			-93.25			-93.25		
	20	CCK, 5.5Mbps			-92			-91.75		
	20	CCK, 11 Mbps			-89.25			-89		
11g	20	Rate 6Mbps			-93.5			-93.25		
	20	Rate 9Mbps			-92			-91.75		
	20	Rate 12Mbps			-91			-90.75		
	20	Rate 18Mbps			-88.75			-88.5		
	20	Rate 24Mbps			-85.5			-85.25		
	20	Rate 36Mbps			-82.25			-82		
	20	Rate 48Mbps			-78			-77.75		
	20	Rate 54Mbps			-76.5			-76.25		
11n LDPC	20	MCS0			-93.75			-93.75		
	20	MCS1			-92.25			-92		
	20	MCS2			-90			-89.5		
	20	MCS3			-87.25			-87		
	20	MCS4			-83.75			-83.5		

Mode	BW [MHz]	Conditions			HrP 2230					
					Chain A [dBm, acc +/- 0.5 dB]			Chain B [dBm, acc +/- 0.5 dB]		
					LB/LHB	MHB	HHB	LB/LHB	MHB	HHB
	20	MCS5			-79.5			-79.25		
	20	MCS6			-78.5			-78		
	20	MCS7			-76.25			-76		
11n LDPC	40	MCS0			-91.25			-91		
	40	MCS1			-89.5			-89.25		
	40	MCS2			-87			-86.75		
	40	MCS3			-84.25			-84		
	40	MCS4			-80.5			-80.25		
	40	MCS5			-76.5			-76.25		
	40	MCS6			-75.25			-75		
	40	MCS7			-73.25			-72.75		
11ax LDPC	20	MCS0			-93.5			-93.25		
	20	MCS1			-91.75			-91.25		
	20	MCS2			-89			-88.75		
	20	MCS3			-86.5			-86		
	20	MCS4			-83			-82.5		
	20	MCS5			-79			-78.75		
	20	MCS6			-77.5			-77		
	20	MCS7			-75.75			-75.5		
	20	MCS8			-72			-71.5		
	20	MCS9			-70			-69.5		
	20	MCS10			-66.5			-65.75		
	20	MCS11			-64			-63.25		
11ax LDPC	40	MCS0			-91			-90.75		
	40	MCS1			-88.25			-87.75		
	40	MCS2			-86.25			-86		
	40	MCS3			-83.75			-83.25		
	40	MCS4			-80			-79.5		
	40	MCS5			-76.25			-75.75		
	40	MCS6			-74.5			-74.25		
	40	MCS7			-72.75			-72.5		
	40	MCS8			-69			-68.5		
	40	MCS9			-67			-66.5		
	40	MCS10			-63.5			-62.75		

Mode	BW [MHz]	Conditions	HrP 2230					
			Chain A [dBm, acc +/- 0.5 dB]			Chain B [dBm, acc +/- 0.5 dB]		
			LB/LHB	MHB	HHB	LB/LHB	MHB	HHB
	40	MCS11	-61			-60.25		
11a	20	Rate 6Mbps	-94.25	-94.5	-94	-94.5	-94.25	-94
	20	Rate 9Mbps	-92.75	-92.75	-92.5	-93	-92.75	-92.5
	20	Rate 12Mbps	-91.75	-92	-91.5	-92	-91.75	-91.5
	20	Rate 18Mbps	-89.5	-89.75	-89.5	-89.75	-89.5	-89.25
	20	Rate 24Mbps	-86.5	-86.75	-86.25	-86.5	-86.25	-86
	20	Rate 36Mbps	-83.25	-83.5	-83	-83.25	-83	-82.75
	20	Rate 48Mbps	-78.75	-79	-78.75	-79	-78.75	-78.5
	20	Rate 54Mbps	-77.5	-77.75	-77.25	-77.5	-77.25	-77
11n LDPC	20	MCS0	-94.75	-95	-94.75	-95	-94.75	-94.5
	20	MCS1	-93.25	-93.25	-93	-93.25	-93	-92.75
	20	MCS2	-90.75	-91	-90.75	-91	-90.75	-90.5
	20	MCS3	-88.25	-88.5	-88	-88.5	-88.25	-87.75
	20	MCS4	-84.5	-84.75	-84.5	-84.75	-84.5	-84.5
	20	MCS5	-80.5	-80.5	-80.25	-80.5	-80.25	-80
	20	MCS6	-79	-79.25	-79	-79.25	-79	-78.75
	20	MCS7	-77.25	-77.5	-77	-77.5	-77.25	-77
11n LDPC	40	MCS0	-92.5	-93	-92.25	-92.5	-92.25	-92.5
	40	MCS1	-90.5	-91.25	-90.25	-90.5	-90.25	-90
	40	MCS2	-88	-88.5	-87.75	-88	-87.75	-87.5
	40	MCS3	-85.25	-86	-85	-85.5	-85.25	-85
	40	MCS4	-81.5	-82.5	-81.25	-81.5	-81.5	-81.25
	40	MCS5	-77.75	-78	-77.25	-77.75	-77.5	-77.25
	40	MCS6	-76.25	-77	-76	-76.25	-76.25	-75.75
	40	MCS7	-74	-74.5	-73.75	-74	-74	-73.5
11ac LDPC	20	MCS0	-94.75	-95	-94.75	-95	-94.75	-94.5
	20	MCS1	-93	-93.25	-93	-93.25	-93	-92.75
	20	MCS2	-90.75	-91	-90.75	-90.75	-90.75	-90.5
	20	MCS3	-88.25	-88.5	-88	-88.5	-88.25	-87.75
	20	MCS4	-84.75	-84.75	-84.5	-84.75	-84.5	-84.5
	20	MCS5	-81	-81.25	-80.75	-81	-80.75	-80.5
	20	MCS6	-79	-79.25	-79	-79	-79	-78.75

Mode	BW [MHz]	Conditions	HrP 2230					
			Chain A [dBm, acc +/- 0.5 dB]			Chain B [dBm, acc +/- 0.5 dB]		
			LB/LHB	MHB	HHB	LB/LHB	MHB	HHB
	20	MCS7	-77.5	-77.75	-77.5	-77.75	-77.5	-77.25
	20	MCS8	-73.5	-73.75	-73.25	-73.5	-73.25	-73
11ac LDPC	40	MCS0	-92.5	-93	-92.25	-92.75	-92.25	-92.5
	40	MCS1	-90.5	-91	-90.25	-90.5	-90.5	-90
	40	MCS2	-88	-88.5	-87.75	-88	-87.75	-87.5
	40	MCS3	-85.25	-85.75	-85	-85.5	-85.25	-85
	40	MCS4	-81.75	-82.5	-81.5	-82	-81.75	-81.5
	40	MCS5	-77.75	-78.25	-77.5	-78	-77.5	-77.25
	40	MCS6	-76.5	-76.75	-76	-76.5	-76.25	-76
	40	MCS7	-74.5	-75	-74.25	-74.75	-74.25	-74.25
	40	MCS8	-70.75	-71.25	-70.5	-70.5	-70.5	-70.25
	40	MCS9	-69.25	-69.75	-69	-69.25	-69	-68.75
11ac LDPC	80	MCS0	-89.5	-89.5	-89.5	-89.75	-89.5	-89.25
	80	MCS1	-87	-87	-87	-87	-87	-86.5
	80	MCS2	-84.5	-84.75	-84.5	-84.75	-84.5	-84.25
	80	MCS3	-82	-82.25	-82	-82	-82	-81.5
	80	MCS4	-78.25	-78.5	-78.25	-78.5	-78.25	-77.75
	80	MCS5	-74.25	-74.5	-74	-74.5	-74	-73.75
	80	MCS6	-72.75	-72.75	-72.5	-72.75	-72.5	-72.25
	80	MCS7	-71.75	-72	-71.5	-71.75	-71.75	-71.25
	80	MCS8	-67.25	-67.5	-67.25	-67.25	-67.25	-66.75
	80	MCS9	-65.25	-65.5	-65.25	-65.25	-65.25	-64.75
11ac LDPC	160	MCS0	-86.25	-86.5		-86.75	-86.75	
	160	MCS1	-83.75	-84		-84	-83.75	
	160	MCS2	-81.5	-81.5		-81.75	-81.75	
	160	MCS3	-79	-79		-79	-79	
	160	MCS4	-75.25	-75.5		-75.5	-75.5	
	160	MCS5	-71	-71.25		-71.5	-71.5	
	160	MCS6	-69.75	-70		-70.25	-70	
	160	MCS7	-68	-68.25		-68.25	-68.25	
	160	MCS8	-63.75	-63.75		-64	-64	
	160	MCS9	-61.75	-61.75		-62.25	-62	

Mode	BW [MHz]	Conditions	HrP 2230					
			Chain A [dBm, acc +/- 0.5 dB]			Chain B [dBm, acc +/- 0.5 dB]		
			LB/LHB	MHB	HHB	LB/LHB	MHB	HHB
11ax LDPC	20	MCS0	-94.25	-94.5	-94.25	-94.75	-94.5	-94.25
	20	MCS1	-92.25	-92.5	-92	-92.5	-92.25	-92
	20	MCS2	-90	-90	-89.75	-90	-89.75	-89.5
	20	MCS3	-87.5	-87.5	-87.25	-87.5	-87.25	-87
	20	MCS4	-83.75	-84	-83.75	-84	-83.75	-83.5
	20	MCS5	-80	-80.25	-79.75	-80	-79.75	-79.75
	20	MCS6	-78.25	-78.5	-78.25	-78.5	-78.25	-78
	20	MCS7	-76.75	-77	-76.5	-76.75	-76.5	-76.25
	20	MCS8	-73	-73	-72.75	-73	-72.75	-72.5
	20	MCS9	-71	-71.25	-70.75	-71	-70.75	-70.5
	20	MCS10	-67.5	-67.75	-67.25	-67.25	-67.25	-67
	20	MCS11	-65	-65	-64.5	-64.75	-64.5	-64.25
11ax LDPC	40	MCS0	-92.25	-92.75	-92	-92.25	-92	-92
	40	MCS1	-89.25	-90	-89	-89.5	-89.25	-89
	40	MCS2	-87.25	-88	-87	-87.25	-87	-87
	40	MCS3	-84.75	-85.25	-84.5	-84.75	-84.5	-84.25
	40	MCS4	-81	-81.5	-80.75	-81	-80.75	-80.5
	40	MCS5	-77.25	-77.75	-77	-77.25	-77	-76.75
	40	MCS6	-75.5	-76.25	-75.25	-75.5	-75.5	-75.25
	40	MCS7	-73.75	-74.5	-73.5	-73.75	-73.75	-73.5
	40	MCS8	-70	-70.75	-70	-70.25	-70	-69.75
	40	MCS9	-68	-68.75	-67.75	-68	-68	-67.75
	40	MCS10	-64.25	-65	-64	-64.25	-64.25	-64
	40	MCS11	-62	-62.5	-61.75	-62	-61.75	-61.5
11ax LDPC	80	MCS0	-89	-89.25	-89	-89.25	-89.25	-88.75
	80	MCS1	-86	-86.25	-85.75	-86.25	-86	-85.5
	80	MCS2	-83.75	-84	-83.75	-84	-83.75	-83.25
	80	MCS3	-81.25	-81.5	-81.25	-81.5	-81.25	-80.75
	80	MCS4	-77.5	-77.75	-77.5	-77.75	-77.5	-77.25
	80	MCS5	-73.75	-73.75	-73.5	-73.75	-73.5	-73.25
	80	MCS6	-72.25	-72.25	-72	-72.25	-72	-71.75
	80	MCS7	-70.5	-70.75	-70.25	-70.5	-70.25	-70
	80	MCS8	-66.75	-67	-66.75	-66.75	-66.75	-66.5

Mode	BW [MHz]	Conditions	HrP 2230					
			Chain A [dBm, acc +/- 0.5 dB]			Chain B [dBm, acc +/- 0.5 dB]		
			LB/LHB	MHB	HHB	LB/LHB	MHB	HHB
	80	MCS9	-64.75	-65	-64.75	-65	-64.75	-64.5
	80	MCS10	-61.25	-61.25	-61	-61.25	-61	-60.75
	80	MCS11	-58.75	-59	-58.5	-59	-58.75	-58.25
11ax LDPC	160	MCS0	-86	-86.25		-86.25	-86.5	
	160	MCS1	-82.75	-82.5		-83	-82.75	
	160	MCS2	-81	-81		-81.25	-81	
	160	MCS3	-78.5	-78.25		-78.75	-78.5	
	160	MCS4	-74.75	-75		-75.25	-75	
	160	MCS5	-71	-71.25		-71.25	-71.25	
	160	MCS6	-69.5	-69.75		-69.75	-69.75	
	160	MCS7	-67.75	-67.75		-68	-68	
	160	MCS8	-64	-64.25		-64.5	-64.25	
	160	MCS9	-62	-62		-62.5	-62.25	
	160	MCS10	-58	-58.25		-58.5	-58.25	
	160	MCS11	-55.75	-55.75		-56.25	-56	

Table 6-5 HrP 2x2 1216 Rx sensitivity

Mode	BW [MHz]	Conditions	HrP 1216					
			Chain A [dBm, acc +/- 0.5 dB]			Chain B [dBm, acc +/- 0.5 dB]		
			LB/LHB	MHB	HHB	LB/LHB	MHB	HHB
11b	20	CCK, 1Mbps	-97			-97.25		
	20	CCK, 2Mbps	-93.5			-93.75		
	20	CCK, 5.5Mbps	-92			-92.25		
	20	CCK, 11 Mbps	-89.25			-89.5		
11g	20	Rate 6Mbps	-93.5			-93.75		
	20	Rate 9Mbps	-92			-92.25		
	20	Rate 12Mbps	-91			-91.25		
	20	Rate 18Mbps	-88.75			-89		
	20	Rate 24Mbps	-85.75			-85.75		
	20	Rate 36Mbps	-82.5			-82.5		
	20	Rate 48Mbps	-78			-78.25		
	20	Rate 54Mbps	-76.75			-77		

Mode	BW [MHz]	Conditions			HrP 1216					
					Chain A [dBm, acc +/- 0.5 dB]			Chain B [dBm, acc +/- 0.5 dB]		
					LB/LHB	MHB	HHB	LB/LHB	MHB	HHB
11n LDPC	20	MCS0			-94			-94		
	20	MCS1			-92.5			-92.5		
	20	MCS2			-90			-90.25		
	20	MCS3			-87.5			-87.5		
	20	MCS4			-83.75			-84		
	20	MCS5			-80			-80		
	20	MCS6			-78.5			-78.5		
	20	MCS7			-76.5			-76.75		
11n LDPC	40	MCS0			-91.5			-91.5		
	40	MCS1			-89.75			-89.75		
	40	MCS2			-87.25			-87.25		
	40	MCS3			-84.5			-84.5		
	40	MCS4			-80.75			-80.75		
	40	MCS5			-76.75			-76.75		
	40	MCS6			-75.5			-75.5		
	40	MCS7			-73.5			-73.25		
11ax LDPC	20	MCS0			-93.5			-93.75		
	20	MCS1			-91.75			-91.75		
	20	MCS2			-89.25			-89.25		
	20	MCS3			-86.5			-86.5		
	20	MCS4			-83			-83		
	20	MCS5			-79.25			-79.25		
	20	MCS6			-77.5			-77.75		
	20	MCS7			-75.75			-76		
	20	MCS8			-72			-72.25		
	20	MCS9			-70.25			-70.25		
	20	MCS10			-66.5			-66.5		
	20	MCS11			-64			-64		
11ax LDPC	40	MCS0			-91.25			-91		
	40	MCS1			-88.5			-88.5		
	40	MCS2			-86.5			-86.5		
	40	MCS3			-83.75			-83.75		
	40	MCS4			-80			-80.25		
	40	MCS5			-76.25			-76.25		

Mode	BW [MHz]	Conditions	HrP 1216					
			Chain A [dBm, acc +/- 0.5 dB]			Chain B [dBm, acc +/- 0.5 dB]		
			LB/LHB	MHB	HHB	LB/LHB	MHB	HHB
	40	MCS6	-74.75			-74.75		
	40	MCS7	-73			-73		
	40	MCS8	-69.25			-69.25		
	40	MCS9	-67.25			-67.25		
	40	MCS10	-63.75			-63.5		
	40	MCS11	-61.25			-61.25		
11a	20	Rate 6Mbps	-94.25	-94.5	-94	-94.5	-95	-94.75
	20	Rate 9Mbps	-92.75	-93	-92.5	-93.25	-93.5	-93.25
	20	Rate 12Mbps	-92	-92	-91.75	-92.25	-92.5	-92.25
	20	Rate 18Mbps	-89.5	-89.75	-89.5	-90	-90.25	-90
	20	Rate 24Mbps	-86.5	-86.75	-86.5	-86.75	-87	-86.75
	20	Rate 36Mbps	-83.25	-83.5	-83	-83.5	-83.75	-83.5
	20	Rate 48Mbps	-79	-79.25	-78.75	-79.25	-79.5	-79.25
	20	Rate 54Mbps	-77.5	-77.75	-77.5	-78	-78.25	-78
11n LDPC	20	MCS0	-94.5	-94.75	-94.5	-95	-95.25	-95
	20	MCS1	-93.25	-93.25	-93	-93.5	-93.75	-93.5
	20	MCS2	-90.75	-91.25	-90.75	-91.25	-91.5	-91.25
	20	MCS3	-88.25	-88.5	-88.25	-88.5	-89	-88.5
	20	MCS4	-84.75	-85	-84.5	-85	-85	-85
	20	MCS5	-80.5	-80.75	-80.5	-80.75	-81.25	-80.75
	20	MCS6	-79.25	-79.5	-79	-79.5	-79.75	-79.5
	20	MCS7	-77.5	-77.5	-77.25	-77.75	-78	-77.75
11n LDPC	40	MCS0	-92.5	-93	-92.5	-92.75	-93	-93.25
	40	MCS1	-90.5	-91.25	-90.25	-90.75	-91	-91
	40	MCS2	-88	-88.5	-87.75	-88.25	-88.5	-88.5
	40	MCS3	-85.5	-86	-85.25	-85.5	-86	-85.75
	40	MCS4	-81.75	-82.5	-81.5	-82	-82.25	-82
	40	MCS5	-77.75	-78.25	-77.5	-78	-78	-78
	40	MCS6	-76.5	-77	-76.25	-76.5	-76.75	-76.5
	40	MCS7	-74.25	-74.75	-73.75	-74.25	-74.5	-74.5
11ac LDPC	20	MCS0	-94.5	-94.75	-94.5	-95	-95.25	-95
	20	MCS1	-93.25	-93.25	-93	-93.5	-93.75	-93.5

Mode	BW [MHz]	Conditions	HrP 1216					
			Chain A [dBm, acc +/- 0.5 dB]			Chain B [dBm, acc +/- 0.5 dB]		
			LB/LHB	MHB	HHB	LB/LHB	MHB	HHB
	20	MCS2	-90.75	-91.25	-90.75	-91.25	-91.5	-91.25
	20	MCS3	-88.5	-88.5	-88.25	-88.5	-89	-88.5
	20	MCS4	-84.75	-85	-84.5	-85	-85.25	-85
	20	MCS5	-81	-81.25	-80.75	-81.25	-81.5	-81.5
	20	MCS6	-79.25	-79.5	-79	-79.5	-79.75	-79.5
	20	MCS7	-77.75	-78	-77.5	-78	-78.25	-78.25
	20	MCS8	-73.5	-73.75	-73.25	-73.75	-74	-74
11ac LDPC	40	MCS0	-92.5	-93	-92.5	-92.75	-93	-93.25
	40	MCS1	-90.5	-91	-90.25	-90.75	-91	-90.75
	40	MCS2	-88	-88.5	-87.75	-88.25	-88.5	-88.5
	40	MCS3	-85.5	-85.75	-85.25	-85.5	-86	-85.75
	40	MCS4	-82	-82.5	-81.75	-82	-82.5	-82.25
	40	MCS5	-78	-78.25	-77.75	-78	-78	-78
	40	MCS6	-76.5	-77	-76.25	-76.5	-76.75	-76.5
	40	MCS7	-74.75	-75.25	-74.5	-75	-75	-75
	40	MCS8	-70.75	-71.25	-70.5	-71	-71	-71
	40	MCS9	-69.25	-69.75	-69	-69.5	-69.75	-69.5
11ac LDPC	80	MCS0	-89.5	-89.75	-89.75	-89.75	-90.25	-90
	80	MCS1	-87	-87.25	-87	-87.25	-87.75	-87.5
	80	MCS2	-84.5	-84.75	-84.5	-85	-85.25	-85
	80	MCS3	-82	-82.25	-82	-82.25	-82.75	-82.5
	80	MCS4	-78.25	-78.75	-78.25	-78.75	-79	-78.75
	80	MCS5	-74.5	-74.5	-74.25	-74.5	-75	-74.5
	80	MCS6	-72.75	-73	-72.75	-73	-73.5	-73
	80	MCS7	-71.75	-72	-71.75	-72	-72.25	-72
	80	MCS8	-67.25	-67.5	-67.25	-67.5	-68	-67.5
	80	MCS9	-65.25	-65.5	-65.25	-65.5	-66	-65.75
11ac LDPC	160	MCS0	-86.5	-86.75		-87	-87.25	
	160	MCS1	-83.75	-84		-84.25	-84.5	
	160	MCS2	-81.5	-81.5		-82	-82.5	
	160	MCS3	-79	-79		-79.5	-79.75	
	160	MCS4	-75.5	-75.5		-75.75	-76.25	
	160	MCS5	-71.25	-71.25		-72	-72.25	

Mode	BW [MHz]	Conditions	HrP 1216					
			Chain A [dBm, acc +/- 0.5 dB]			Chain B [dBm, acc +/- 0.5 dB]		
			LB/LHB	MHB	HHB	LB/LHB	MHB	HHB
	160	MCS6	-69.75	-70		-70.75	-70.75	
	160	MCS7	-68.25	-68.25		-68.75	-69.25	
	160	MCS8	-63.75	-64		-64.75	-64.75	
	160	MCS9	-62	-62		-62.5	-62.75	
11ax LDPC	20	MCS0	-94.25	-94.5	-94.25	-94.75	-95	-94.75
	20	MCS1	-92.25	-92.25	-92	-92.5	-92.75	-92.5
	20	MCS2	-90	-90	-89.75	-90	-90.25	-90
	20	MCS3	-87.25	-87.5	-87.25	-87.5	-87.75	-87.5
	20	MCS4	-83.75	-84	-83.75	-84	-84.25	-84
	20	MCS5	-80	-80.25	-79.75	-80.25	-80.5	-80.25
	20	MCS6	-78.5	-78.5	-78.25	-78.5	-78.75	-78.5
	20	MCS7	-76.75	-77	-76.5	-77	-77.25	-77
	20	MCS8	-73	-73	-72.75	-73.25	-73.5	-73.25
	20	MCS9	-71	-71.25	-70.75	-71	-71.5	-71.25
	20	MCS10	-67.5	-67.75	-67.25	-67.75	-68	-67.75
	20	MCS11	-65	-65	-64.75	-65	-65.5	-65
11ax LDPC	40	MCS0	-92.25	-92.5	-92	-92.25	-92.5	-92.75
	40	MCS1	-89.5	-89.75	-89	-89.5	-89.75	-89.5
	40	MCS2	-87.25	-87.75	-87	-87.5	-87.75	-87.5
	40	MCS3	-84.75	-85.25	-84.5	-85	-85.25	-85
	40	MCS4	-81	-81.5	-80.75	-81.25	-81.5	-81.25
	40	MCS5	-77.25	-78	-77	-77.5	-77.75	-77.5
	40	MCS6	-75.75	-76.25	-75.5	-75.75	-76	-76
	40	MCS7	-74	-74.5	-73.75	-74	-74.5	-74.25
	40	MCS8	-70.25	-70.75	-70	-70.25	-70.5	-70.5
	40	MCS9	-68.25	-68.75	-68	-68.25	-68.5	-68.5
	40	MCS10	-64.5	-65	-64.25	-64.75	-65	-64.75
	40	MCS11	-62	-62.5	-61.75	-62.25	-62.5	-62.5
11ax LDPC	80	MCS0	-89.25	-89.5	-89.25	-89.5	-89.75	-89.5
	80	MCS1	-86	-86.25	-86.25	-86.5	-86.75	-86.5
	80	MCS2	-83.75	-84	-83.75	-84.25	-84.5	-84.25
	80	MCS3	-81.25	-81.5	-81.5	-81.5	-82	-81.75
	80	MCS4	-77.5	-77.75	-77.75	-78	-78.25	-78

Mode	BW [MHz]	Conditions			HrP 1216					
					Chain A [dBm, acc +/- 0.5 dB]			Chain B [dBm, acc +/- 0.5 dB]		
					LB/LHB	MHB	HHB	LB/LHB	MHB	HHB
	80	MCS5			-73.75	-74	-73.75	-74	-74.25	-74
	80	MCS6			-72.25	-72.5	-72.25	-72.5	-72.75	-72.5
	80	MCS7			-70.5	-70.5	-70.5	-70.75	-71	-70.75
	80	MCS8			-66.75	-67	-66.75	-67.25	-67.5	-67.25
	80	MCS9			-65	-65	-64.75	-65.25	-65.5	-65.25
	80	MCS10			-61.25	-61.25	-61	-61.5	-62	-61.5
	80	MCS11			-58.75	-59	-58.75	-59.25	-59.5	-59.25
11ax LDPC	160	MCS0			-86	-86.25		-86.5	-87	
	160	MCS1			-83	-83.25		-83.25	-83.5	
	160	MCS2			-81	-81.25		-81.5	-81.75	
	160	MCS3			-78.5	-78.75		-79	-79	
	160	MCS4			-75	-75		-75.5	-75.75	
	160	MCS5			-71	-71.25		-71.5	-71.75	
	160	MCS6			-69.5	-69.75		-70	-70.25	
	160	MCS7			-68	-68		-68.5	-68.75	
	160	MCS8			-64.25	-64.25		-64.75	-65	
	160	MCS9			-62.25	-62.25		-62.75	-63	
	160	MCS10			-58.25	-58.25		-58.75	-59	
	160	MCS11			-55.75	-56		-56.5	-56.75	

6.2.3 BT Tx KPIs

Table 6-6 BT Tx KPIs

BT Tx Power	Tx Power HrP 2230	Tx PowerHrP 1216	Tx PowerHrP 1216 LTE
BR	9.3 dBm	9.5 dBm	9.5 dBm
EDR2	5.5 dBm	5.5 dBm	5.5 dBm
EDR3	5.5 dBm	5.5 dBm	5.5 dBm
BLE(LR-125k)	5.5 dBm	5.5 dBm	5.5 dBm
BLE(1M)	5.5 dBm	5.5 dBm	5.5 dBm
BLE(2M)	5.5 dBm	5.5 dBm	5.5 dBm

Notes:

1. Accuracy is +/-1.5dB
2. Typical values (25c, typical Si process, Typical HW module
3. Values are averaged across Bluetooth channels
4. Measured at antenna port

6.2.4 Bluetooth® sensitivity

Table 6-7 Bluetooth® sensitivity

	HrP* 2230	HrP* 1216	HrP 1216 LTE
RX - DH5	-95dBm	-95dBm	-95 dBm
RX - 2DH5	-94 dBm	-94 dBm	-94 dBm
RX - 3DH5	-87 dBm	-87 dBm	-87 dBm
RX[1] – BLE 1M	-97 dBm	-97 dBm	-97 dBm
RX[1] – BLE 2M	-91.5 dBm	-91.5 dBm	-91.5 dBm
RX[1] – BLE LR S=2	-100 dBm	-100 dBm	-100 dBm
RX[1] – BLE LR S=8	-103.5 dBm	-103.5 dBm	-103.5 dBm

Notes:

1. Accuracy is +/-1.5dBm
2. Typical values (25c, typical Si process, Typical HW module)
3. Values are averaged across Bluetooth* channels
4. Measured at antenna port

6.3 Throughput KPIs

6.3.1 Max throughput

Table 6-8 HrP2 Max throughput

Scenario	Min	Target
Conductive Best Attenuation 11b LB RX TCP	5.4	5.5
Conductive Best Attenuation 11g LB RX TCP	21.6	22.4
Conductive Best Attenuation 11a HB RX TCP	22.0	22.8
Conductive Best Attenuation 11b LB TX TCP	5.4	5.5
Conductive Best Attenuation 11g LB TX TCP	20.0	22.4
Conductive Best Attenuation 11a HB TX TCP	20.0	22.8
Conductive Best Attenuation 11n LB 20 MHz RX UDP	123	127
Conductive Best Attenuation 11n HB 40 MHz RX UDP	255	264
Conductive Best Attenuation 11ac HB 80 MHz RX UDP	729	800
Conductive Best Attenuation 11ac HB 160 MHz RX UDP	1382	1557
Conductive Best Attenuation 11n LB 20 MHz TX UDP	120	124
Conductive Best Attenuation 11n HB 40 MHz TX UDP	235	243
Conductive Best Attenuation 11ac HB 80 MHz TX UDP	751	792
Conductive Best Attenuation 11ac HB 160 MHz TX UDP	1422	1528
Conductive Best Attenuation 11n LB 20 MHz RX TCP	119	123
Conductive Best Attenuation 11n HB 40 MHz RX TCP	243	252
Conductive Best Attenuation 11ac HB 80 MHz RX TCP	650	750
Conductive Best Attenuation 11ac HB 160 MHz RX TCP	1231	1375
Conductive Best Attenuation 11n LB 20 MHz TX TCP	114	118
Conductive Best Attenuation 11n HB 40 MHz TX TCP	213	221
Conductive Best Attenuation 11ac HB 80 MHz TX TCP	692	745
Conductive Best Attenuation 11ac HB 160 MHz TX TCP	1265	1391
Conductive Best Attenuation 11n HB 20 MHz RX UDP	126	131
Conductive Best Attenuation 11n LB 40 MHz RX UDP	245	255
Conductive Best Attenuation 11n HB 20 MHz TX UDP	122	127
Conductive Best Attenuation 11n LB 40 MHz TX UDP	231	239
Conductive Best Attenuation 11ac HB 20 MHz RX UDP	152	157
Conductive Best Attenuation 11ac HB 40 MHz RX UDP	338	350
Conductive Best Attenuation 11ac HB 20 MHz TX UDP	149	154
Conductive Best Attenuation 11ac HB 40 MHz TX UDP	345	358
Conductive Best Attenuation 11n HB 20 MHz RX TCP	122	126
Conductive Best Attenuation 11n LB 40 MHz RX TCP	234	245
Conductive Best Attenuation 11n HB 20 MHz TX TCP	116	120
Conductive Best Attenuation 11n LB 40 MHz TX TCP	210	218

Scenario	Min	Target
Conductive Best Attenuation 11ac HB 20 MHz RX TCP	146	152
Conductive Best Attenuation 11ac HB 40 MHz RX TCP	321	334
Conductive Best Attenuation 11ac HB 20 MHz TX TCP	139	145
Conductive Best Attenuation 11ac HB 40 MHz TX TCP	318	330
Conductive Best Attenuation 11ax LB 20 MHz TX TCP	223	232
Conductive Best Attenuation 11ax LB 20 MHz RX TCP	228	239
Conductive Best Attenuation 11ax LB 20 MHz TX UDP	238	247
Conductive Best Attenuation 11ax LB 20 MHz RX UDP	239	251
Conductive Best Attenuation 11ax LB 40 MHz TX TCP	430	469
Conductive Best Attenuation 11ax LB 40 MHz RX TCP	420	469
Conductive Best Attenuation 11ax LB 40 MHz TX UDP	477	494
Conductive Best Attenuation 11ax LB 40 MHz RX UDP	472	489
Conductive Best Attenuation 11ax HB 20 MHz TX TCP	220	239
Conductive Best Attenuation 11ax HB 20 MHz RX TCP	234	246
Conductive Best Attenuation 11ax HB 20 MHz TX UDP	245	254
Conductive Best Attenuation 11ax HB 20 MHz RX UDP	246	259
Conductive Best Attenuation 11ax HB 40 MHz TX TCP	464	482
Conductive Best Attenuation 11ax HB 40 MHz RX TCP	466	482
Conductive Best Attenuation 11ax HB 40 MHz TX UDP	491	508
Conductive Best Attenuation 11ax HB 40 MHz RX UDP	485	502
Conductive Best Attenuation 11ax HB 80 MHz TX TCP	942	1025
Conductive Best Attenuation 11ax HB 80 MHz RX TCP	865	1050
Conductive Best Attenuation 11ax HB 80 MHz TX UDP	1009	1075
Conductive Best Attenuation 11ax HB 80 MHz RX UDP	946	1100
Conductive Best Attenuation 11ax HB 160 MHz TX TCP	1646	1869
Conductive Best Attenuation 11ax HB 160 MHz RX TCP	1428	1967
Conductive Best Attenuation 11ax HB 160 MHz TX UDP	1849	2025
Conductive Best Attenuation 11ax HB 160 MHz RX UDP	1649	2212

Table 6-9 HrP1 Max throughput (Draft- Pre-SRA)

Scenario	Min	Target
Conductive Best Attenuation 11a HB RX TCP	22.3	23.1
Conductive Best Attenuation 11a HB TX TCP	20	23.1
Conductive Best Attenuation 11b LB RX TCP	5.4	5.5
Conductive Best Attenuation 11b LB TX TCP	5.2	5.5
Conductive Best Attenuation 11g LB RX TCP	22	22.7
Conductive Best Attenuation 11g LB TX TCP	20	22.7
Conductive Best Attenuation 11n LB 20 MHz RX UDP	63	66

Scenario	Min	Target
Conductive Best Attenuation 11n LB 20 MHz TX UDP	63	65
Conductive Best Attenuation 11n HB 40 MHz RX UDP	131	136
Conductive Best Attenuation 11ac HB 80 MHz RX UDP	367	380
Conductive Best Attenuation 11n HB 40 MHz TX UDP	131	136
Conductive Best Attenuation 11n LB 20 MHz RX TCP	61	64
Conductive Best Attenuation 11n HB 40 MHz RX TCP	127	132
Conductive Best Attenuation 11ac HB 80 MHz RX TCP	344	357
Conductive Best Attenuation 11n LB 20 MHz TX TCP	55	59
Conductive Best Attenuation 11n HB 40 MHz TX TCP	111	115
Conductive Best Attenuation 11ac HB 80 MHz TX TCP	343	355
Conductive Best Attenuation 11n HB 20 MHz RX UDP	65	67
Conductive Best Attenuation 11n LB 40 MHz RX UDP	129	134
Conductive Best Attenuation 11n HB 20 MHz TX UDP	64	66
Conductive Best Attenuation 11n LB 40 MHz TX UDP	129	134
Conductive Best Attenuation 11ac HB 20 MHz RX UDP	76	79
Conductive Best Attenuation 11ac HB 40 MHz RX UDP	171	177
Conductive Best Attenuation 11ac HB 20 MHz TX UDP	76	79
Conductive Best Attenuation 11ac HB 40 MHz TX UDP	176	182
Conductive Best Attenuation 11n HB 20 MHz RX TCP	62	65
Conductive Best Attenuation 11n LB 40 MHz RX TCP	125	129
Conductive Best Attenuation 11n HB 20 MHz TX TCP	57	60
Conductive Best Attenuation 11n LB 40 MHz TX TCP	109	113
Conductive Best Attenuation 11ac HB 20 MHz RX TCP	73	76
Conductive Best Attenuation 11ac HB 40 MHz RX TCP	165	171
Conductive Best Attenuation 11ac HB 20 MHz TX TCP	65	67
Conductive Best Attenuation 11ac HB 40 MHz TX TCP	148	153
Conductive Best Attenuation 11ac HB 80 MHz TX UDP	383	397
Conductive Best Attenuation 11ax (unscheduled) HB 80 MHz TX TCP	397	418
Conductive Best Attenuation 11ax (unscheduled) HB 80 MHz RX TCP	314	333
Conductive Best Attenuation 11ax (unscheduled) HB 80 MHz TX UDP	530	548
Conductive Best Attenuation 11ax (unscheduled) HB 80 MHz RX UDP	342	359
Conductive Best Attenuation 11ax (unscheduled) LB 20 MHz TX TCP	111.4	116.1
Conductive Best Attenuation 11ax (unscheduled) LB 20 MHz RX TCP	113	120
Conductive Best Attenuation 11ax (unscheduled) LB 20 MHz TX UDP	119	123.4
Conductive Best Attenuation 11ax (unscheduled) LB 20 MHz RX UDP	119.5	125.7

6.4 Wi-Fi power KPIs

Note: All TX usages listed in Table 6–9 assume Tx Power at 0dBm (typical in testing environments). To estimate Power consumption at the Max Tx Power case, add 700mW.

Table 6-10 HrP2 Wi-Fi power KPIs

Name	Units	Target (Typical)	Max
*TX Average – 11ac 2x2 HB/160	mW	1034	1138
RX Average – 11ac 2x2 HB/160	mW	769	846
*TX Average – 11ax 2x2 HB/160	mW	1248	1373
RX Average – 11ax 2x2 HB/160	mW	848	933
*TX Average – 11n 2x2 LB/20	mW	861	947
RX Average – 11n 2x2 LB/20	mW	419	461
*TX Average – 11n 2x2 HB/40	mW	908	999
RX Average – 11n 2x2 HB/40	mW	532	585
*TX Average – 11ac 2x2 HB/80	mW	1152	1268
RX Average – 11ac 2x2 HB/80	mW	642	706
Core Power Down	mW	1.6	1.6
Unassociated average	mW	6.2	6.7
Idle associated 2.4GHz (consumer) OOB	mW	3.4	3.9
Idle associated 5.2GHz (enterprise) OOB	mW	3.7	4.2
Idle associated 2.4GHz (consumer) benchmark	mW	2.9	3.4
Idle associated 5.2GHz (enterprise) benchmark	mW	3	3.8
Device in Dx 2.4 GHz (armed for WAKE) – RW	mW	2.2	2.7
Device in Dx 5.2 Ghz (armed for WAKE) – RW	mW	2.2	2.7
Web browsing 2.4GHz (consumer)	mW	14	16
Web browsing 5.2GHz (enterprise)	mW	15.9	17.4
VOIP 2.4GHz (consumer)	mW	232	255
VOIP 5.2GHz (enterprise)	mW	274	302
Video Conference 2.4GHz (consumer)	mW	241	266
Video Conference 5.2GHz (enterprise)	mW	280	325
Video Streaming 2.4GHz (consumer)	mW	29	34
Video Streaming 5.2GHz (enterprise)	mW	35.9	41
WiDi SCM Local Content Streaming (BSS STA @ 2.4GHz, Miracast Source as P2P GO @ 2.4GHz)	mW	357.1	392.9
WiDi SCM Presentation (BSS STA @ 5.2GHz, Miracast Source as P2P GO @ 5.2GHz)	mW	318	350
WiDi DCM Local Content Streaming (BSS STA @ 2.4GHz, Miracast Source as P2P client @ 5.2GHz)	mW	229.6	252.6
WiDi DCM Presentation (BSS STA @ 5.2GHz, Miracast Source as P2P client @ 5.2GHz)	mW	80.9	89

Table 6-11 HrP1 Wi-Fi power KPIs (Draft- Pre-SRA)

Name	Units	Target (Typical)	Max
TX Average - 11n 1x1 LB/20	mW	560	616
RX Average - 11n 1x1 LB/20	mW	303	334
TX Average - 11n 1x1 HB/40	mW	593	652
RX Average - 11n 1x1 HB/40	mW	407	448
TX Average - 11ac 1x1 HB/80	mW	800	880
RX Average - 11ac 1x1 HB/80	mW	477	524
Core Power Down	mW	1.6	1.6
Unassociated average	mW	6.2	6.7
Idle associated 2.4GHz (consumer) OOB	mW	3.4	3.9
Idle associated 5.2GHz (enterprise) OOB	mW	3.7	4.2
Idle associated 2.4GHz (consumer) benchmark	mW	2.9	3.4
Idle associated 5.2GHz (enterprise) benchmark	mW	3	3.8
Device in Dx 2.4 GHz (armed for WAKE) - RW	mW	2.2	2.7
Device in Dx 5.2 Ghz (armed for WAKE) - RW	mW	2.2	2.7
Web browsing 2.4GHz (consumer)	mW	20.67	23.62
Web browsing 5.2GHz (enterprise)	mW	26.47	28.97
VOIP 2.4GHz (consumer)	mW	235.64	259
VOIP 5.2GHz (enterprise)	mW	279.19	307.72
Video Conference 2.4GHz (consumer)	mW	214.7	236.97
Video Conference 5.2GHz (enterprise)	mW	266.84	309.73
Video Streaming 2.4GHz (consumer)	mW	34.09	39.96
Video Streaming 5.2GHz (enterprise)	mW	47.02	53.7
WiDi SCM Local Content Streaming (BSS STA @ 2.4GHz, Miracast Source as P2P GO @ 2.4GHz)	mW	294.68	324.44
WiDi SCM Presentation (BSS STA @ 5.2GHz, Miracast Source as P2P GO @ 5.2GHz)	mW	276.92	305.36
WiDi DCM Local Content Streaming (BSS STA @ 2.4GHz, Miracast Source as P2P client @ 5.2GHz)	mW	158.28	173.74
WiDi DCM Presentation (BSS STA @ 5.2GHz, Miracast Source as P2P client @ 5.2GHz)	mW	57.13	62.65

6.4.1 BT power LPIs

Table 6-12 BT power LPIs

Name	Units	Target (Typical)	Max
Rx Peak	mW	111.02	127.4
Tx Peak 10dbm	mW	163.75	171.93
BT Disable (De-assertion of BT_EN signal)	mW	1.55	1.62
BT Idle or BT Disable (SW)	mW	1.55	1.62
Page Scan	mW	5.73	6.53
Page and Inquiry Scan	mW	7.84	9.04
BLE Passive Scan	mW	3.74	4.15
BLE Advertising	mW	2.04	2.14
HID BLE connected idle	mW	13.35	14.61
BR/EDR Sniff Mode	mW	6.1	6.93
HFP eSCO	mW	39.42	45.74
A2DP Playback (Tpoll configured by FW)	mW	40.7	47.34
FTP/OPP TX	mW	100.04	115.76
FTP/OPP Rx	mW	101.71	120.81

§

7 Regulatory

7.1 Regulatory channel support and output power

Jefferson/Harrison Peak provides regulatory compliance via statically-configured SKUs or Dynamic Regulatory Solution (DRS).

For further details on the DRS scheme, see Section 8, Dynamic Regulatory Solution.

7.2 Wi–Fi channel configuration

7.2.1 Channel configuration – RF output power

The values listed in the power table (OTP table) represent the target power for the calibration process without antennae gain. This value has been verified to ensure margin from the regulatory limit based on post OTP factory calibration measurements using a diagnostic tool that operates the WLAN card at a ~99% DC (Duty Cycle) taken on both the main and auxiliary antenna ports.

As part of the factory test process, Intel measures the output power of every card. Any cards that exceed the maximum limits (OTP + 0.5 dB) will not pass the factory test. While in operation the card adjusts TX power using a closed loop TX power calibration algorithm. To do so, a power detector and temperature sensor are used.

Intel uses the antennae gain values listed in Table 7–1 for product and country certification work.

Table 7-1 Reference antenna gain

Antenna Type	Antenna Peak gain 2.4GHz (dBi)	Antenna Peak gain 5.2GHz (dBi)	Antenna Peak gain 5.5GHz (dBi)	Antenna Peak gain 5.8GHz (dBi)
Design target	3	5	5	5
PIFA	3.24	3.73	4.77	4.97
Dipole	2.89	3.19	4.41	4.22

Intel also incorporates a lower limit to ensure that compliance of the WLAN card is maintained. The minimum limits are set by factory process.

7.2.2 Channel configuration – scan

Table 7-2 describes the channel configuration scan configuration.

Table 7-2 Scan policies per sub-band and country settings

Channel Profile (DIS/PAS/ACT)									
Country/Geo	Sub-Band 2G4-A	Sub-Band 2G4-B	Sub-Band 5G2	Sub-Band 5G3	Sub-Band 5G4	Sub-Band 5G5	Sub-Band 5G8-A	Sub-Band 5G8-B	Sub-Band 5G9
	[25:24]	[27:26]	[29:28]	[31:30]	[33:32]	[35:34]	[37:36]	[39:28]	[41:40]
Default	2	2	1	1	0	1	1	1	0
FCC	2	2	1	1	0	1	2	1	0
USA TW	2	2	2	1	0	1	2	2	0
Canada IC	2	2	1	1	0	1	2	2	0
ETSI + 5G8SRD	2	2	1	1	0	1	2	2	0
Japan	2	2	1	1	0	1	1	1	0
Brazil	2	2	1	1	0	1	2	2	0
Indonesia	2	2	0	0	0	0	2	0	0
South-Korea	2	2	2	1	0	1	2	2	0
Chile	2	2	1	1	0	1	2	1	0

7.2.3 Output power restrictions for main geographies

Table 7-3 Output power restrictions, main geographies

Output Power (dBm)							
Country/Geo	2.4 GHz	5.15 – 5.25 GHz	5.25 – 5.35 GHz	5.47 – 5.65 GHz	5.65 – 5.725 GHz	5.725 – 5.85 GHz	Unit
EU Countries EIRP	20	23	23	23[3]	23[3]	14 SRD	dBm
> EU Countries Cond.[1]	17	18	18	18	18	9 SRD	dBm
United States[2] Cond.	1000	250	250	250	250	1000	mW
> United States[2] Cond.	30	24	24	24	24	30	dBm
Canada[2] Cond.	1000	200 EIRP	250	250	250	1000	mW
Canada[2] Cond.	30	23 EIRP	24	24	24	30	dBm
India	30	23 EIRP	23 EIRP	N/A	N/A	23 EIRP	dBm
China Cond.		18	18	24	24	27	dBm

Output Power (dBm)							
Country/Geo	**2.4 GHz**	**5.15 – 5.25 GHz**	**5.25 – 5.35 GHz**	**5.47 – 5.65 GHz**	**5.65 – 5.725 GHz**	**5.725 – 5.85 GHz**	**Unit**
China EIRP	20	23	23	30	30	33	dBm
Worst Case Cond. mW[2]	100	50	200	250	250	100	mW
Worst Case Cond. dBm[1]	17	18	18	18	18	18	dBm

NOTES: Reference antenna gain: Max. Antenna Gain 3 dBi for 2.4 GHz and 5 dBi for 5 GHz

1. Assuming Max. Antenna Gain 3 dBi for 2.4 GHz and 5 dBi for 5 GHz
2. Allowance of up to a 6 dBi antenna allowed, if antenna is > 6 dBi output power must be reduced by 1 dB per dBi of antenna gain.
3. As DFS Slave Device (30 dBm for Master).

7.3 Regulatory and safety certification

The following regulatory and safety information is subject to change.

Table 7-4 Wi-Fi safety and regulatory USA

USA	Requirements	Criteria
	EMI	FCC Part 15, Subpart B, Class B (CISPR 22 limits at 10 m)
	RF	FCC Part 15, Subpart C (Sections 15.205, 15.207, 15.209, and 15.247) FCC Part 15, Subpart E (Section 15.407)
	Safety	UL 60950–1

Table 7-5 Wi-Fi safety and regulatory Europe

Europe	Requirements	Criteria
	EMC	EN301489–1, EN 301489–17
	RF	EN300 328, EN300 440 and EN301–893 as DFS slave terminal
	Safety	EN60950–1 via CB Report (IEC60950–1) R&TTE Health Requirement referring to the EN 50566–2013 and 62209–2:2010

Table 7-6 Wi-Fi safety and regulatory Japan

Japan	Requirements	Criteria
	EMI	VCCI Class B
	RF	STD T66, STD T71, ARIB W52, W53, W56
	Safety	EN60950–1 via CB Report (IEC60950–1) R&TTE Health Requirement referring to the EN 50566–2013 and 62209–2:2010

Table 7-7 Wi-Fi safety and regulatory Australia/New Zealand

Australia/ New Zealand	Requirements	Criteria
	EMC	EU test reports
	RF	Radio communications (EMR) Standard 2003; EU test reports + Delta AS–NZ4268
	Safety	CB Cert. and Report (IEC60950–1)

Table 7-8 Wi-Fi safety and regulatory other geographies

Other Geographies	Requirements	Criteria
	Priority 2 Countries	To be covered in MWG Regulatory WW Country Coverage
	Priority 3 Countries	To be covered in MWG Regulatory WW Country Coverage

Note: Regulatory pre-scans and certification are tested using a combo Bluetooth/Wi-Fi reference antenna.

7.4 Tx power regulatory limits

Note: The "EU" tables below do not include the SRD (Short Range Device) limits. In Operational mode, when an ETSI country is selected, the SRD limits will kick in and reduce the Tx power below the values mentioned in Table 7–9, Table 7–11, and Table 7–13. Specifically, channels 149-161 will be limited to 7.5dBm.

HrP Default Tx power limits are calculated in firmware as the minimum of FCC, ETSI, and ROW tables.

Table 7-9 HrP2 2230 FCC max Tx power

HrP 2230 2.4GHz – 20MHz FCC						
		20MHz CCK		20MHz OFDM		
Central Freq.	Control / Central Channel	CCK SISO A	CCK SISO B	OFDM SISO A	OFDM SISO B	OFDM MIMO
2412	1	**19**	**19**	**16.25**	**16.5**	**13.5**
2417	2	20	20	18	18	16
2422	3	20	20	19.25	19.25	17
2427	4	20	20	19.25	19.25	17
2432	5	20	20	19.25	19.25	17
2437	6	20	20	19.25	19.25	17
2442	7	**20**	**20**	**19.25**	**19.25**	**16.5**
2447	8	20	20	19.25	19.25	16.5
2452	9	20	20	19.25	19.25	16.5
2457	10	20	20	18.25	18.25	16
2462	11	**19**	**19**	**16**	**15.75**	**13.25**
2467	12	**18**	**18**	**14.5**	**14.5**	**12**
2472	13	**18**	**18**	**11.5**	**10**	**8.75**

Note: 40MHz CCK is not supported by this product.

HrP 2230 2.4GHz – 40MHz FCC						
		40MHz CCK		40MHz OFDM		
Central Freq.	Control / Central Channel	CCK SISO A	CCK SISO B	OFDM SISO A	OFDM SISO B	OFDM MIMO
2422	3	9.5	9.5	**16**	**16**	**13.25**
2427	4	15.5	15.5	17	17	15
2432	5	15.5	15.5	17	17	15
2437	6	15.5	15.5	17	17	15
2442	7	15.5	15.5	**15.75**	**15.75**	**13.75**
2447	8	15.5	15.5	15.75	15.75	13.5
2452	9	9.5	9.5	**15.75**	**15.5**	**13**
2457	10	9.5	9.5	**11.5**	**11.75**	**9.25**
2462	11	9.5	9.5	**12**	**12**	**10**

HrP 2230 5GHz – 20MHz FCC				
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5180	36	**18**	**18**	**16**
5200	40	**20**	**20**	**18**
5220	44	20	20	18
5240	48	**20**	**20**	**18**
5260	52	20	20	17.75
5280	56	20	20	17.5
5300	60	19	19	16
5320	64	16.75	16.75	15.25
5340	68	Not Supported		
5360	72			
5380	76			
5400	80			
5420	84			
5440	88			
5460	92			
5480	96			
5500	100	**17**	**17.25**	**15.75**
5520	104	20	20	18
5540	108	20	20	18
5560	112	20	20	18
5580	116	20	20	18
5600	120	**20**	**20**	**18**
5620	124	20	20	18
5640	128	20	20	18
5660	132	20	20	18
5680	136	20	20	18
5700	140	**17.25**	**17.25**	**16**
5720	144	**20**	**20**	**18**
5745	149	**20**	**20**	**17.5**
5765	153	20	20	17.5
5785	157	**20**	**20**	**17.5**
5805	161	20	20	17.5
5825	165	**20**	**20**	**17.5**
5845	169	Not Supported		
5865	173			

HrP 2230 5GHz – 20MHz FCC				
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5885	177	Not Supported		
5905	181			

HrP 2230 5GHz – 40MHz FCC				
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5190	38	**17.5**	**17.5**	**15.25**
5230	46	**20**	**19**	**17.5**
5270	54	**19.75**	**19.5**	**16.5**
5310	62	**16**	**16**	**14.5**
5350	70	Not Supported		
5390	78			
5430	86			
5470	94			
5510	102	**17**	**17.25**	**15.75**
5550	110	20	20	18
5590	118	**20**	**20**	**18**
5630	126	20	20	18
5670	134	**18.5**	**18.5**	**17.75**
5710	142	**20**	**20**	**18**
5755	151	**20**	**20**	**18**
5795	159	**20**	**20**	**18**
5835	167	Not Supported		
5875	175			

HrP 2230 5GHz – 80MHz FCC				
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5210	42	**18**	**17.5**	**15**
5290	58	**16.75**	**17**	**13.5**
5370	74	Not Supported		
5450	90			
5530	106	**17.25**	**17.25**	**15**
5610	122	**19**	**19**	**18**
5690	138	**20**	**20**	**18**

HrP 2230 5GHz – 80MHz FCC				
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5775	155	**18.5**	**18.5**	**17.25**
5855	171	Not Supported		

HrP 2230 5GHz – 160MHz FCC				
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5250	50	**14.5**	**14.25**	**11.5**
5410	82	Not Supported		
5570	114	**14**	**14**	**13**
5815	163	Not Supported		

Table 7-10 HrP2 2230 ETSI max Tx power

HtP 2230 2.4GHz – 20MHz ETSI						
		20MHz CCK		**20MHz OFDM**		
Central Freq.	Control / Central Channel	CCK SISO A	CCK SISO B	OFDM SISO A	OFDM SISO B	OFDM MIMO
2412	1	**15.5**	**15.5**	**16**	**16**	**13**
2417	2	15.5	15.5	16	16	13
2422	3	15.5	15.5	16	16	13
2427	4	15.5	15.5	16	16	13
2432	5	15.5	15.5	16	16	13
2437	6	15.5	15.5	16	16	13
2442	7	**15.5**	**15.5**	**16**	**16**	**13**
2447	8	15.5	15.5	16	16	13
2452	9	15.5	15.5	16	16	13
2457	10	15.5	15.5	16	16	13
2462	11	15.5	15.5	16	16	13
2467	12	15.5	15.5	16	16	13
2472	13	**15.5**	**15.5**	**16**	**16**	**13**

HrP 2230 2.4GHz – 40MHz ETSI						
		20MHz CCK		40MHz OFDM		
Central Freq.	Control / Central Channel	CCK SISO A	CCK SISO B	OFDM SISO A	OFDM SISO B	OFDM MIMO
2422	3	15.5	15.5	**16**	**16**	**13**
2427	4	15.5	15.5	16	16	13
2432	5	15.5	15.5	16	16	13
2437	6	15.5	15.5	16	16	13
2442	7	15.5	15.5	**16**	**16**	**13**
2447	8	15.5	15.5	16	16	13
2452	9	15.5	15.5	16	16	13
2457	10	15.5	15.5	16	16	13
2462	11	15.5	15.5	**16**	**16**	**13**

HrP 2230 5GHz – 20MHz ETSI				
		20MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	MIMO A
5180	36	**16**	**16**	**13**
5200	40	16	16	13
5220	44	16	16	13
5240	48	16	16	13
5260	52	16	16	13
5280	56	16	16	13
5300	60	16	16	13
5320	64	**16**	**16**	**13**
5340	68	Not Supported		
5360	72			
5380	76			
5400	80			
5420	84			
5440	88			
5460	92			
5480	96			
5500	100	**16**	**16**	**13**
5520	104	16	16	13
5540	108	16	16	13
5560	112	16	16	13

HrP 2230 5GHz – 20MHz ETSI				
		20MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	MIMO A
5580	116	16	16	13
5600	120	16	16	13
5620	124	16	16	13
5640	128	16	16	13
5660	132	16	16	13
5680	136	16	16	13
5700	140	**16**	**16**	**13**
5720	144	16	16	13
5745	149	16	16	13
5765	153	16	16	13
5785	157	16	16	13
5805	161	16	16	13
5825	165	16	16	13
5845	169	Not Supported		
5865	173			
5885	177			
5905	181			

HrP 2230 5GHz – 40MHz ETSI				
		40MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	MIMO
5190	38	**17**	**17**	**14**
5230	46	17	17	14
5270	54	17	17	14
5310	62	**17**	**17**	**14**
5350	70	Not Supported		
5390	78			
5430	86			
5470	94			
5510	102	**17**	**17**	**14**
5550	110	17	17	14
5590	118	17	17	14
5630	126	17	17	14

HrP 2230 5GHz – 40MHz ETSI				
		40MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	MIMO
5670	134	**17**	**17**	**14**
5710	142	17	17	14
5755	151	17	17	14
5795	159	17	17	14
5835	167	Not Supported		
5875	175			

HrP 2230 5GHz – 80MHz ETSI				
		80MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5210	42	**17**	**17**	**14**
5290	58	**17**	**17**	**14**
5370	74	Not Supported		
5450	90			
5530	106	**17**	**17**	**14**
5610	122	**17**	**17**	**14**
5690	138	17	17	14
5775	155	17	17	14
5855	171	Not Supported		

HrP 2230 5GHz – 160MHz ETSI				
		160MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5250	50	**17**	**17**	**14**
5410	82	Not Supported		
5570	114	**17**	**17**	**14**
5815	163	Not Supported		

Table 7-11 HrP2 1216 FCC max Tx power

HrP 1216 2.4GHz – 20MHz FCC						
		20MHz CCK		20MHz OFDM		
Central Freq.	Control / Central Channel	CCK SISO A	CCK SISO B	OFDM SISO A	OFDM SISO B	OFDM MIMO
2412	1	**19**	**18.75**	**16.25**	**16.5**	**13.5**
2417	2	20	20	18	18	16
2422	3	20	20	19.5	19.5	17
2427	4	20	20	19.5	19.5	17
2432	5	20	20	19.5	19.5	17
2437	6	20	20	19.5	19.5	17
2442	7	**20**	**20**	**19.5**	**19.5**	**16.5**
2447	8	20	20	19.5	19.5	16.5
2452	9	20	20	19.5	19.5	16.5
2457	10	20	20	18.25	18.25	16
2462	11	**19**	**19**	**15**	**14.5**	13
2467	12	**18**	**18**	**14.5**	**14.5**	12.5
2472	13	**18.5**	**18.5**	**12.25**	**12**	**10**

Note: 40MHz CCK is not supported by this product.

HrP 1216 2.4GHz – 40MHz FCC						
		40MHz CCK		40MHz OFDM		
Central Freq.	Control / Central Channel	CCK SISO A	CCK SISO B	OFDM SISO A	OFDM SISO B	OFDM MIMO
2422	3	9.5	9.5	**16**	**16**	**13.75**
2427	4	15.5	15.5	16	16	14
2432	5	15.5	15.5	17	17	15
2437	6	15.5	15.5	15.5	15.5	14
2442	7	15.5	15.5	**15**	**15**	**13.25**
2447	8	15.5	15.5	15	15	13.25
2452	9	9.5	9.5	**14**	**15**	**12.5**
2457	10	9.5	9.5	**12**	**12**	**9**
2462	11	9.5	9.5	**12.5**	**12.25**	**11**

HrP 1216 5GHz – 20MHz FCC				
		20MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5180	36	**18**	**18**	**15.25**
5200	40	**19**	**19.5**	**17.5**
5220	44	20	20	18
5240	48	**20**	**20**	**18**
5260	52	**20**	**20**	**18**
5280	56	**20**	**20**	**18**
5300	60	**20**	**20**	**17.5**
5320	64	**17.5**	**17.75**	**15.5**
5340	68	Not Supported		
5360	72			
5380	76			
5400	80			
5420	84			
5440	88			
5460	92			
5480	96			
5500	100	**18.5**	**18.5**	**15.25**
5520	104	20	20	18.25
5540	108	20	20	18.25
5560	112	20	20	18.25
5580	116	20	20	18.25
5600	120	**20**	**20**	**18.25**
5620	124	20	20	18.25
5640	128	20	20	18.25
5660	132	20	20	18.25
5680	136	20	20	18.25
5700	140	**17**	**17.5**	**14.5**
5720	144	**20**	**20**	**18**
5745	149	**20**	**20**	**17.5**
5765	153	20	20	17.5
5785	157	**20**	**20**	**17.5**
5805	161	20	20	17.5
5825	165	**20**	**20**	**17.5**
5845	169	Not Supported		
5865	173			

HrP 1216 5GHz – 20MHz FCC				
		20MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5885	177	Not Supported		
5905	181			

HrP 1216 5GHz – 40MHz FCC				
		40MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5190	38	**18**	**18**	**15.25**
5230	46	**20**	**20**	**18**
5270	54	**20**	**20**	**18**
5310	62	**16.75**	**16.75**	**14.25**
5350	70	Not Supported		
5390	78			
5430	86			
5470	94			
5510	102	**17.75**	**17.75**	**15.75**
5550	110	20	20	18
5590	118	**20**	**20**	**18**
5630	126	20	20	18
5670	134	**18.75**	**18.75**	**17.5**
5710	142	**20**	**20**	**19**
5755	151	**20**	**20**	**18**
5795	159	**20**	**20**	**18**
5835	167	Not Supported		
5875	175			

HrP 1216 5GHz – 80MHz FCC				
		80MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5210	42	**18**	**17.75**	**15.5**
5290	58	**17.25**	**17.25**	**14**
5370	74	Not Supported		
5450	90			

HrP 1216 5GHz – 80MHz FCC				
		80MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5530	106	**18.25**	**18.25**	**15.5**
5610	122	**19.25**	**19.25**	**17.75**
5690	138	**20**	**20**	**18.5**
5775	155	**18**	**18**	**16**
5855	171	Not Supported		

HrP 1216 5GHz – 160MHz FCC				
		160MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5250	50	**14.25**	**14.75**	**12.25**
5410	82	Not Supported		
5570	114	**13.75**	**14**	**12.75**
5815	163	Not Supported		

Table 7-12 HrP2 1216 ETSI max Tx power

HrP 1216 2.4GHz – 20MHz ETSI						
		20MHz CCK		20MHz OFDM		
Central Freq.	Control / Central Channel	CCK SISO A	CCK SISO B	OFDM SISO A	OFDM SISO B	OFDM MIMO
2412	1	**15.5**	**15.5**	**16**	**16**	**13**
2417	2	15.5	15.5	16	16	13
2422	3	15.5	15.5	16	16	13
2427	4	15.5	15.5	16	16	13
2432	5	15.5	15.5	16	16	13
2437	6	15.5	15.5	16	16	13
2442	7	**15.5**	**15.5**	**16**	**16**	**13**
2447	8	15.5	15.5	16	16	13
2452	9	15.5	15.5	16	16	13
2457	10	15.5	15.5	16	16	13
2462	11	15.5	15.5	16	16	13
2467	12	15.5	15.5	16	16	13
2472	13	**15.5**	**15.5**	**16**	**16**	**13**

Note: 40MHz CCK is not supported by this product.

HrP 1216 2.4GHz – 40MHz ETSI						
		40MHz CCK		**40MHz OFDM**		
Central Freq.	Control / Central Channel	CCK SISO A	CCK SISO B	OFDM SISO A	OFDM SISO B	OFDM MIMO
2422	3	15.5	15.5	**16**	**16**	**13**
2427	4	15.5	15.5	16	16	13
2432	5	15.5	15.5	16	16	13
2437	6	15.5	15.5	16	16	13
2442	7	15.5	15.5	**16**	**16**	**13**
2447	8	15.5	15.5	16	16	13
2452	9	15.5	15.5	16	16	13
2457	10	15.5	15.5	16	16	13
2462	11	15.5	15.5	**16**	**16**	**13**

HrP 1216 5GHz – 20MHz ETSI				
		20MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	MIMO
5180	36	**16**	**16**	**13**
5200	40	16	16	13
5220	44	16	16	13
5240	48	16	16	13
5260	52	16	16	13
5280	56	16	16	13
5300	60	16	16	13
5320	64	**16**	**16**	**13**
5340	68	Not Supported		
5360	72			
5380	76			
5400	80			
5420	84			
5440	88			
5460	92			
5480	96			
5500	100	**16**	**16**	**13**
5520	104	16	16	13
5540	108	16	16	13
5560	112	16	16	13

HrP 1216 5GHz – 20MHz ETSI				
		20MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	MIMO
5580	116	16	16	13
5600	120	16	16	13
5620	124	16	16	13
5640	128	16	16	13
5660	132	16	16	13
5680	136	16	16	13
5700	140	**16**	**16**	**13**
5720	144	16	16	13
5745	149	16	16	13
5765	153	16	16	13
5785	157	16	16	13
5805	161	16	16	13
5825	165	16	16	13
5845	169	Not Supported		
5865	173			
5885	177			
5905	181			

HrP 1216 5GHz – 40MHz ETSI				
		40MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	MIMO
5190	38	**17**	**17**	**14**
5230	46	17	17	14
5270	54	17	17	14
5310	62	**17**	**17**	**14**
5350	70	Not Supported		
5390	78			
5430	86			
5470	94			
5510	102	**17**	**17**	**14**
5550	110	17	17	14
5590	118	17	17	14
5630	126	17	17	14

HrP 1216 5GHz – 40MHz ETSI				
		40MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	MIMO
5670	134	**17**	**17**	**14**
5710	142	17	17	14
5755	151	17	17	14
5795	159	17	17	14
5835	167	Not Supported		
5875	175			

HrP 1216 5GHz – 80MHz ETSI				
		80MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5210	42	**17**	**17**	**14**
5290	58	**17**	**17**	**14**
5370	74	Not Supported		
5450	90			
5530	106	**17**	**17**	**14**
5610	122	**17**	**17**	**14**
5690	138	17	17	14
5775	155	17	17	14
5855	171	Not Supported		

HrP 1216 5GHz – 160MHz ETSI				
		160MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5250	50	**17**	**17**	**14**
5410	82	Not Supported		
5570	114	**17**	**17**	**14**
5815	163	Not Supported		

Table 7-13 HrP2 1216LTE FCC max Tx power

HrP 1216LTE 2.4GHz – 20MHz FCC						
		20MHz CCK		20MHz OFDM		
Central Freq.	Control / Central Channel	CCK SISO A	CCK SISO B	OFDM SISO A	OFDM SISO B	OFDM MIMO
2412	1	**19**	**19**	**17.75**	**17**	**14**
2417	2	20	20	18	18	16
2422	3	20	20	19.5	19.5	17
2427	4	20	20	19.5	19.5	17
2432	5	20	20	19.5	19.5	17
2437	6	20	20	19.5	19.5	17
2442	7	**20**	**20**	**19.5**	**19.5**	**16.75**
2447	8	20	20	19.5	19.5	16.75
2452	9	20	20	19.5	19.5	16.75
2457	10	20	20	18.25	18.25	15.25
2462	11	**19**	**19**	**16.5**	**16**	**13.5**
2467	12	**18**	**17.5**	**14.5**	**14.5**	**11.5**
2472	13	**17.5**	**17.75**	**12**	**11.5**	**9**

Note: 40MHz CCK is not supported by this product.

HrP 1216LTE 2.4GHz – 40MHz FCC						
		40MHz CCK		40MHz OFDM		
Central Freq.	Control / Central Channel	CCK SISO A	CCK SISO B	OFDM SISO A	OFDM SISO B	OFDM MIMO
2422	3	9.5	9.5	**16**	**15**	**12.25**
2427	4	15.5	15.5	16	16	14
2432	5	15.5	15.5	17	17	15
2437	6	15.5	15.5	17	17	15
2442	7	15.5	15.5	**16**	**16.5**	**14.25**
2447	8	15.5	15.5	15	15	13.75
2452	9	9.5	9.5	**14.5**	**14.25**	**13**
2457	10	9.5	9.5	**10**	**10.25**	**8**
2462	11	9.5	9.5	**12**	**13**	**11.75**

HrP 1216LTE 5GHz – 20MHz FCC				
		20MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5180	36	**18.5**	**18.5**	**15.5**

HrP 1216LTE 5GHz – 20MHz FCC				
		20MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5200	40	**19.25**	**19.25**	**18**
5220	44	20	20	18
5240	48	**20**	**20**	**18**
5260	52	**20**	**20**	**18**
5280	56	**20**	**20**	**18**
5300	60	20	20	18
5320	64	**18**	**17.5**	**16**
5340	68	Not Supported		
5360	72			
5380	76			
5400	80			
5420	84			
5440	88			
5460	92			
5480	96			
5500	100	**18.75**	**18.75**	**16**
5520	104	20	20	18.25
5540	108	20	20	18.25
5560	112	20	20	18.25
5580	116	20	20	18.25
5600	120	**20**	**20**	**18.25**
5620	124	20	20	18.25
5640	128	20	20	18.25
5660	132	20	20	18.25
5680	136	20	20	18.25
5700	140	**17**	**17.5**	**16**
5720	144	20	20	18
5745	149	**20**	**20**	**17.75**
5765	153	20	20	18
5785	157	**20**	**20**	**18**
5805	161	20	20	18
5825	165	**20**	**20**	**18**
5845	169	Not Supported		
5865	173			
5885	177			

HrP 1216LTE 5GHz – 20MHz FCC				
		20MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5905	181	Not Supported		

HrP 1216LTE 5GHz – 40MHz FCC				
		40MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5190	38	**18.25**	**18.25**	**15.5**
5230	46	**20**	**20**	**18**
5270	54	**20**	**20**	**17.75**
5310	62	**16.25**	**16.25**	**13.5**
5350	70	Not Supported		
5390	78			
5430	86			
5470	94			
5510	102	**17.75**	**17.75**	**16**
5550	110	20	20	18
5590	118	**20**	**20**	**18**
5630	126	20	20	18
5670	134	**18.75**	**18.75**	**17**
5710	142	20	20	18
5755	151	**20**	**20**	**18**
5795	159	**20**	**20**	**18**
5835	167	Not Supported		
5875	175			

HrP 1216LTE 5GHz – 80MHz FCC				
		80MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5210	42	**17.75**	**17.75**	**15**
5290	58	**17.25**	**17**	**14.25**
5370	74	Not Supported		
5450	90			
5530	106	**17.5**	**17.75**	**15.25**

HrP 1216LTE 5GHz – 80MHz FCC				
		80MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5610	122	**19**	**19**	**17.75**
5690	138	20	20	18
5775	155	**18.5**	**18.5**	**16.5**
5855	171	Not Supported		

HrP 1216LTE 5GHz – 160MHz FCC				
		160MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5250	50	**14.75**	**14.5**	**12.5**
5410	82	Not Supported		
5570	114	**14**	**14**	**11.5**
5815	163	Not Supported		

Table 7-14 HrP2 1216LTE ETSI max Tx power

HrP 1216LTE 2.4GHz – 20MHz ETSI						
		20MHz CCK		20MHz OFDM		
Central Freq.	Control / Central Channel	CCK SISO A	CCK SISO B	OFDM SISO A	OFDM SISO B	OFDM MIMO
2412	1	**15.5**	**15.5**	**16**	**16**	**13**
2417	2	15.5	15.5	16	16	13
2422	3	15.5	15.5	16	16	13
2427	4	15.5	15.5	16	16	13
2432	5	15.5	15.5	16	16	13
2437	6	15.5	15.5	16	16	13
2442	7	**15.5**	**15.5**	**16**	**16**	**13**
2447	8	15.5	15.5	16	16	13
2452	9	15.5	15.5	16	16	13
2457	10	15.5	15.5	16	16	13
2462	11	15.5	15.5	16	16	13
2467	12	15.5	15.5	16	16	13
2472	13	**15.5**	**15.5**	**16**	**16**	**13**

Note: 40MHz CCK is not supported by this product.

HrP 1216LTE 2.4GHz – 40MHz ETSI						
		40MHz CCK		**40MHz OFDM**		
Central Freq.	Control / Central Channel	CCK SISO A	CCK SISO B	OFDM SISO A	OFDM SISO B	OFDM MIMO
2422	3	15.5	15.5	**16**	**16**	**13**
2427	4	15.5	15.5	16	16	13
2432	5	15.5	15.5	16	16	13
2437	6	15.5	15.5	16	16	13
2442	7	15.5	15.5	**16**	**16**	**13**
2447	8	15.5	15.5	16	16	13
2452	9	15.5	15.5	16	16	13
2457	10	15.5	15.5	16	16	13
2462	11	15.5	15.5	**16**	**16**	**13**

HrP 1216LTE 5GHz – 20MHz ETSI				
		20MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	MIMO
5180	36	**16**	**16**	**13**
5200	40	16	16	13
5220	44	16	16	13
5240	48	16	16	13
5260	52	16	16	13
5280	56	16	16	13
5300	60	16	16	13
5320	64	**16**	**16**	**13**
5340	68	Not Supported		
5360	72			
5380	76			
5400	80			
5420	84			
5440	88			
5460	92			
5480	96			
5500	100	**16**	**16**	**13**
5520	104	16	16	13
5540	108	16	16	13
5560	112	16	16	13

HrP 1216LTE 5GHz – 20MHz ETSI				
		20MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	MIMO
5580	116	16	16	13
5600	120	16	16	13
5620	124	16	16	13
5640	128	16	16	13
5660	132	16	16	13
5680	136	16	16	13
5700	140	**16**	**16**	**13**
5720	144	16	16	13
5745	149	16	16	13
5765	153	16	16	13
5785	157	16	16	13
5805	161	16	16	13
5825	165	16	16	13
5845	169	Not Supported		
5865	173			
5885	177			
5905	181			

HrP 1216LTE 5GHz – 40MHz ETSI				
		40MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	MIMO
5190	38	**17**	**17**	**14**
5230	46	17	17	14
5270	54	17	17	14
5310	62	**17**	**17**	**14**
5350	70	Not Supported		
5390	78			
5430	86			
5470	94			
5510	102	**17**	**17**	**14**
5550	110	17	17	14
5590	118	17	17	14
5630	126	17	17	14

HrP 1216LTE 5GHz – 40MHz ETSI				
		40MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	MIMO
5670	134	**17**	**17**	**14**
5710	142	17	17	14
5755	151	17	17	14
5795	159	17	17	14
5835	167	Not Supported		
5875	175			

HrP 1216LTE 5GHz – 80MHz ETSI				
		80MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5210	42	**17**	**17**	**14**
5290	58	**17**	**17**	**14**
5370	74	Not Supported		
5450	90			
5530	106	**17**	**17**	**14**
5610	122	**17**	**17**	**14**
5690	138	17	17	14
5775	155	17	17	14
5855	171	Not Supported		

HrP 1216LTE 5GHz – 160MHz ETSI				
		160MHz OFDM		
Central Freq.	Control / Central Channel	OFDM SISO A	OFDM SISO B	OFDM MIMO
5250	50	**17**	**17**	**14**
5410	82	Not Supported		
5570	114	**17**	**17**	**14**
5815	163	Not Supported		

7.5 SAR Tx power limits

OEMs who implement SAR limitations on their platforms can use the values in Table 7–15 for Tx power limits based on antenna-to-human-body separation distance. Using these limits will enable OEMs to minimize their C1PC paperwork. In the case of shorter distances, specific platform tests and a C2PC approval process will be needed.

Table 7–15 SAR Tx power limits dependency on distance

d = Antenna to Human Body Separation [mm]	Value [dBm] for Both Chain A and B acc: +/- 0.5dB		Required OEM SAR Regulatory Process
	2.4GHz	5GHz	
HrP2 2230: d>= 17 HrP2 1216: d>= 12 HrP2 1216 LTE >= 15	No need for BIOS SAR limits		None
8 <= d < (17 for 2230, 12 for 1216 and 15 for LTE)	17.5	16	C1PC
5 <= d < 8	15	13.5	C1PC
<5	OEM to set specific BIOS SAR limits		C2PC

NOTES:
1. The values in the table are per chain. Both chains can transmit at the stated power simultaneously.
2. The C1PC process is allowed only if the same antenna "Type" has already been filed. If for any reason an OEM files for a new antenna "Type," the C2PC process is required, even if the TX power falls within the limits.

§

8 Dynamic Regulatory Solution

8.1 Overview

Beginning with the Intel® Dual Band Wireless 7265 module (Stone Peak 2/D), Intel® introduces a new Dynamic Regulatory Solution (DRS) which offers worldwide regulatory compliance on one hardware SKU, while offering optimizations to various country regulations based on geo–location discovery. These Wi–Fi optimizations bring the PC market up to capabilities offered in other segments, and include the following benefits:

- More robust regulatory compliance
- Consolidation to a single worldwide regulatory SKU
- Country–specific channel optimizations
- Minimized OEM effort on enablement, production, and inventory management
- Ability to meet changing regulations and field support with software updates
- Simpler worldwide procurement and distribution for enterprise customers

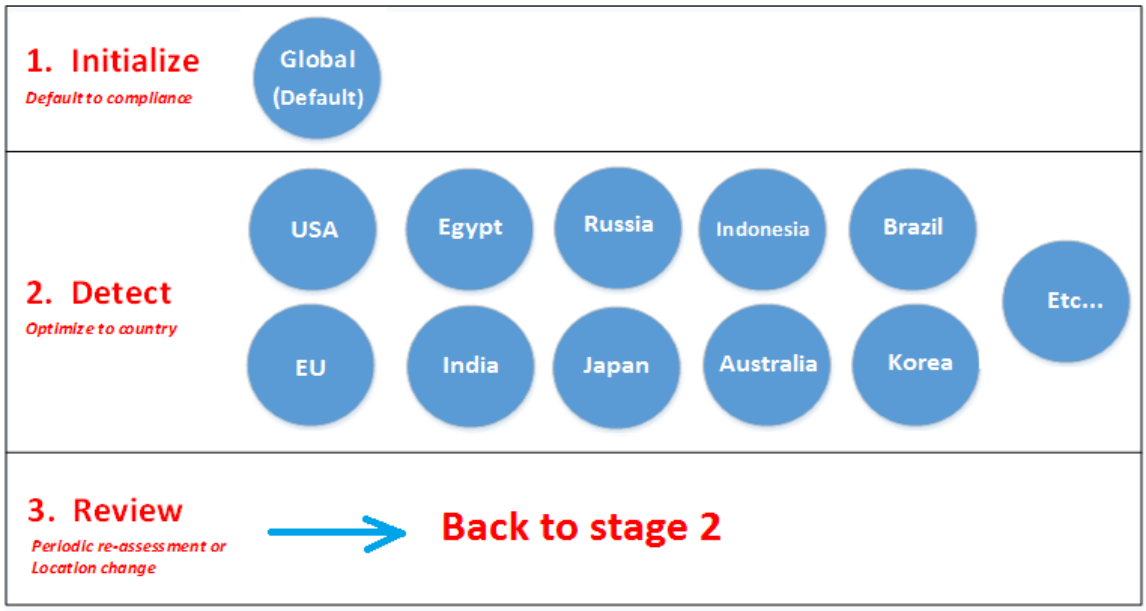
The new dynamic solution provides a significant improvement in compliance reliability by ensuring the compliance always aligns to the adapter's location. It also provides the ability to react more quickly to changing regulations, both in new product shipments as well as field upgrades. Changing regulations can be applied precisely to the relevant country or countries without impacting optimizations to any other country.

8.2 Operation

DRS uses a proprietary country detection mechanism that, through a combination of field surveys and theoretical analysis, demonstrated >99.9999% accuracy. DRS's basic operational flow consists of initializing the adapter to a most-of-world (MoW) or global configuration, detecting and optimizing to a specific country, and using a feedback loop to periodically review the location and change the configuration as necessary. This operational flow is designed to ensure an optimized environment of regulatory compliance and user experience:

1. **Initialize:** Configure the adapter to MoW compliance by using minimum channel configurations to meet both FCC and ETSI regulations. This MoW configuration is used to ensure a good user experience.
2. **Detect**: Utilizing the proprietary country detection mechanism, configure to an optimized channel map for the given country detected. In most cases, the adapter will optimize around FCC regulations *or* ETSI regulations. In exceptions, the adapter will disable channels (for example, Indonesia), channel widths for 802.11ac (such as Russia before its adoption in 2016), or bands (such as Tunisia). When no country is detected, the adapter will remain in the "Default" configuration. Country maps and channel configurations are detailed in the subsequent section.
3. **Review:** Periodically reassess the location to ensure the configuration is valid or determine that it should change. The reviews are triggered under any condition that indicates a user has changed location. Since Wi–Fi is a local–area networking technology, this can be achieved by using network connectivity changes (system power on/resume, profile change, airplane mode, etc.) to trigger the review. DRS also uses a one–hour timer to reassess the location and ensure continual monitoring.

Figure 8–1 DRS flow



In addition to the operational flow described, a regulatory exception exists where:

(1) There are significant channel restrictions from the MoW configuration, and

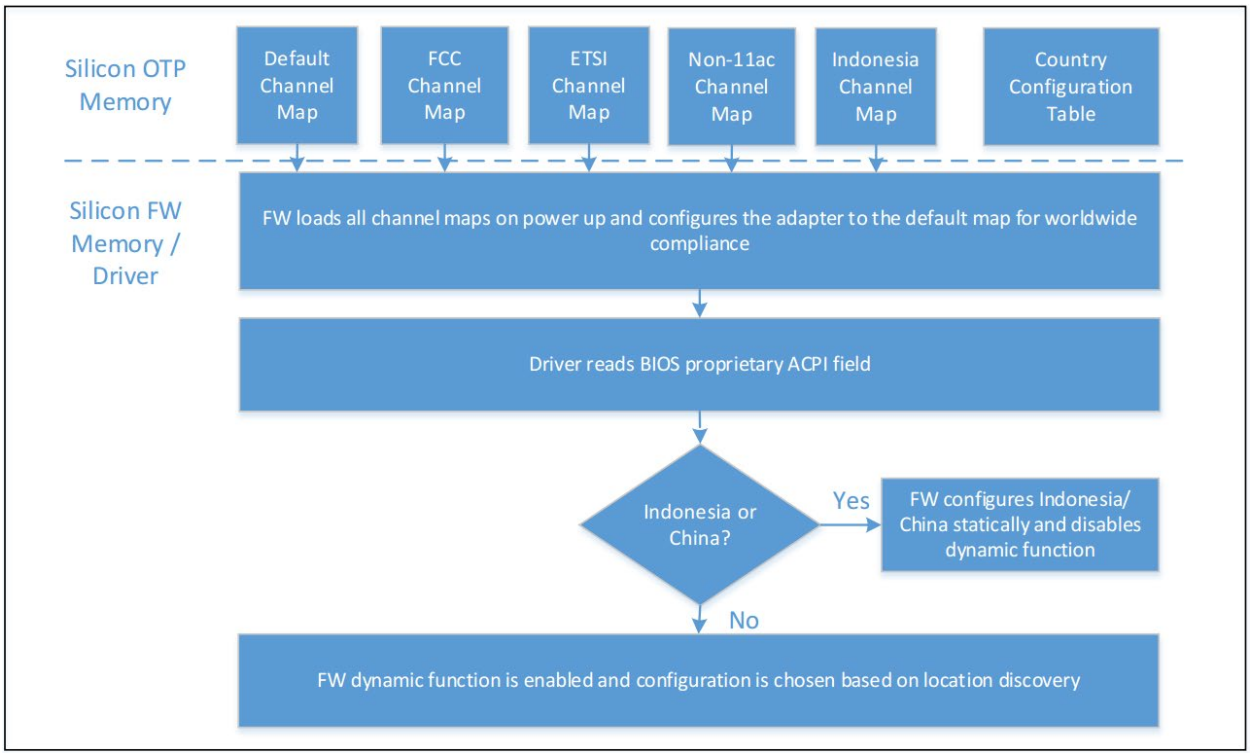
(2) System (platform) approvals are required that place the regulatory responsibility on OEMs.

In this case (and for any future scenarios that may require this capability), DRS provides the ability to configure the adapter at the system level to a static channel map that complies with the specific country restrictions (example is Indonesia restrictions). The system (platform) configuration is done by indication that specify the specific country target through a custom BIOS ACPI setting. Please refer to Section 8.6 for details on programming the BIOS. For example, when the BIOS is configured to Indonesia, the device driver is designed to read this setting, disable the dynamic location detection mechanism, and statically configure the adapter to the Indonesia channel map.

8.3 DRS architecture

The DRS architecture, including the optional BIOS configuration, is shown in Figure 8–2. DRS leverages multiple product components.

Figure 8–2 Dynamic regulatory architecture



8.3.1 Regulatory Tx values tables

The device contains four full Tx channel maps:

- Table 0 – Default table that is used before country location is confirmed. It represents the minimum values of the other tables.
- Table 1 – US FCC and alike
- Table 2 – ETSI Limits and alike
- Table 3 – Contains Other remaining Tx Power limitations

8.3.2 Country profiles

The device supports up to 31 country profiles. Each profile defines which Tx power table to use per sub-band.

8.3.3 Mapping country code to country profile

The device contains a table mapping country code (total of 129) to the relevant profile.

8.3.4 Determining the location

The Intel Wi-Fi driver and firmware execute a proprietary mechanism to determine the location. Based on the location found the FW chooses the country profile bases on the table mapping country code to profile.

if the platform BIOS is configured to regulatory static configuration, Driver and firmware set the location accordingly, and disables the location detection mechanism.

8.4 Validation of regulatory compliance

Intel owns the validation of the DRS feature. This includes validation of the location detection mechanism, choosing the correct country profile, and enabling/disabling allowed/not-allowed channels and bandwidth.

8.5 Performance testing

When the adapter cannot determine the regulatory domain, it will default to the global "Default" profile. This can result in lower TX performance than the maximum the adapter is capable of. If performance testing with other profiles is desired, customer is encouraged to:

1. Order a limited number of adapters hard coded to other domain profiles (such as FCC). Please contact your Wireless TAM for availability.
2. Use the ANT tool and force regulatory domain for testing performance. The ANT tool uses a command line function to set DRS's MCC (Mobile Country Code) to a specific country configuration. It runs over the standard driver to ensure the adapter's production configuration is tested. Details are included in the tool's user guide. Please note that this configuration is time-limited and the device will disconnect after the timer expires, to prevent bypassing the DRS mechanism.
3. For PHY parameters tests (Tx power, EVM), use the DRTU tool. The DRTU tool supports configuration to a specific country code.

8.6 BIOS configuration

The device supports BIOS configuration to support regulatory special cases, as follows:

1. Static regulatory setting – Set to a specific country and disable the dynamic regulatory scan.
2. Static SAR tables to configure the platform to have specific SAR limits (per antenna, per sub-band).
3. Dynamic SAR tables – Choose the SAR limits based on platform triggers (requires application that support this mode).

For additional information on updated BIOS configuration, please refer to the BIOS guidelines doc.

Figure 8–3 Regulatory domain (WRDD) object definition

```
Name (WRDD, Package()
{   // Field Name          Field Type
  Revision.                // DWordConst

  Package()                // Default Configuration
  {
    DomainType.            // WiFi = 0x7
    RegulatoryDomain.      // Country identifier as defined in ISO/IEC 3166-1
                           // Default(AP)=0x4150, Indonesia(ID) = 0x4944
  },
}) // End of WRDD object
```

Table 8-1 WRDD field descriptions

Field	Format	Description
Revision	DWordConst	Revision identifier for this structure. Set to 0 always.
DomainType	DWordConst	Identifies the domain this object is providing default configuration data for. The domain type identifies a bitmap-based value, so that default values for a combination of domains can be specified. Use 0x7 for Wi-Fi in this instance.
RegulatoryDomain	WordConst	Defines the regulatory domain to be used: **Default(AP) = 0x4150** // Device ignores and resumes dynamic operation **Indonesia(ID) = 0x4944** // Device configures statically to Indonesia

Additional details, including a sample configuration, can be found in the *BIOS Reference Spec*:

Platform Reference Code for 5th Generation Intel® Core™ Processor Platforms (codenamed Broadwell)

The WRDD object is referenced in the following locations within the spec:

BroadwellRcPkg\AcpiTables\Dsdt\GloblNvs.asl

BroadwellRcPkg\Cpu\SampleCode\Include\Protocol\GlobalNvsArea.h

BroadwellRcPkg\AcpiTables\SampleCode\AcpiPlatform\Dxe\AcpiPlatform.c

BroadwellRcPkg\AcpiTables\SampleCode\Library\PlatformAcpiLib\AcpiGnvsInitLib.c

Note: There are two instances of the WRDD object in the reference spec. Only the first instance needs to be created in this scenario.

§

9 Wireless Connectivity Integration (CNVi) Design Considerations

This section includes important platform design and implementation aspects that the OEM should take into consideration when implementing a platform that would accommodate this product.
Harrison Peak 2 is an integrated connectivity RF companion module, and has special platform design guidelines that are different from standard M.2 connectivity design features.

Besides having new interface requirements, integrated connectivity allows designing the platform so as to support both integrated and discrete connectivity M.2 modules using a single platform design. This allows the OEM to have one motherboard design accommodating either a Companion RF or a discrete M.2 card which can be "swappable" on the same M.2 socket.

This section focuses on the dual CNVi/Discrete design and therefore will include guidelines applicable to the Jefferson Peak M.2 card as well as to other discrete M.2 cards.

9.1 Wireless Connectivity Integration (CNVi)

Connectivity integration (CNVi) is a general term referring to a family of connectivity solutions which started with Pulsar family in CNL, and continues with Quasar family for ICL-CML-TGL-JPL. The common component of all these solutions is the Quasar IP, which is a hard macro embedded in various Intel SOC chips and is the updated Generation of the Pulsar IP that was used in CNL.

The CNVi solution also contains an external RF companion module (CRF) and RF antennas. This module can be implemented in the following variations:

- M.2 (2230)
- Soldered-down M.2 (1216)
- Chip-on board (COB)

9.2 Integrated connectivity concept (CNVi)

Figure below shows the Platform-level view of CNVi, including all related system components.

9.2.1 MAC-PHY split

Integrated Connectivity (CNVi) is a new architecture for wireless connectivity devices. The concept of CNVi is to move a large part of the functional content of the connectivity chip from the radio chip into the SoC. As a result, a large portion of the chip logic and memory resources is moved out of the radio chip, reducing platform bill of material (BOM) size and cost, and improving accessibility to SoC resources (audio, memory, etc.).

In the CNVi architecture, the MACs of the Wi-Fi and Bluetooth®, including processors, logic and memory are relocated from the radio chip into the SoC chip. Signal processing, Analog and RF functions stay in the radio chip, which is called a Companion RF chip (CRF) in CNVi terminology.

The part of the connectivity IP which is ported into the SoC is called Pulsar/Quasar (CNVi is the general name). The Pulsar/Quasar interfaces with the rest of the SoC functions through SoC-internal interfaces and buses, and does not require any host interfaces at the platform level. On the other hand, interfacing the Pulsar/Quasar and the Companion RF (CRF) chip does require platform signals to be routed between the SoC and the Companion RF chip (Intel-proprietary interfaces, based on existing M.2 signals).

The Integrated Connectivity architecture has the MAC part of the Wi-Fi and BT cores located inside the SoC. As a result, the Host interfaces of Wi-Fi and BT are no longer part of the M.2 module, which is an RF companion module. These Host Interfaces reside in the SoC and are not exposed to the platform.

Figure 9–1 CNV Discrete vs integrated architecture

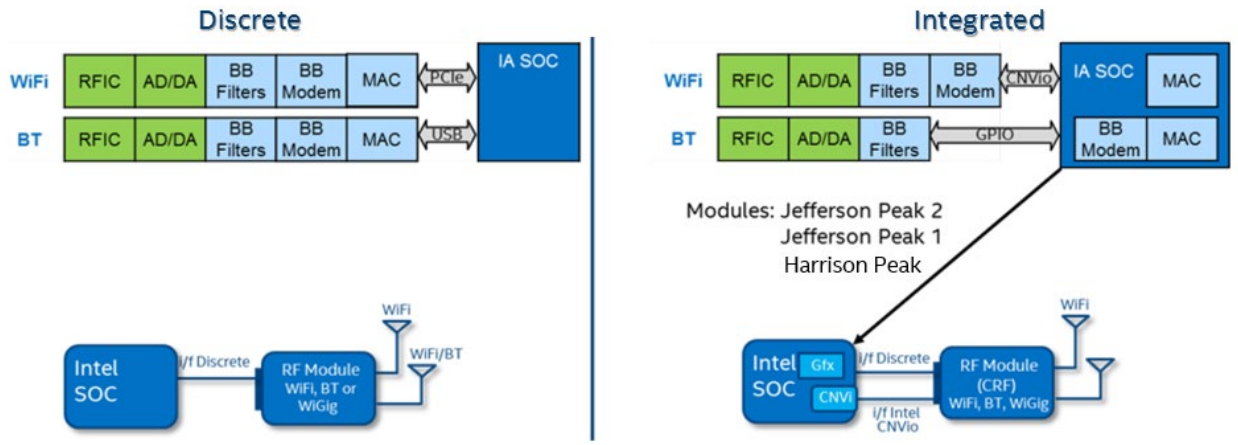


Figure 9–2 CNVi high-level block diagram

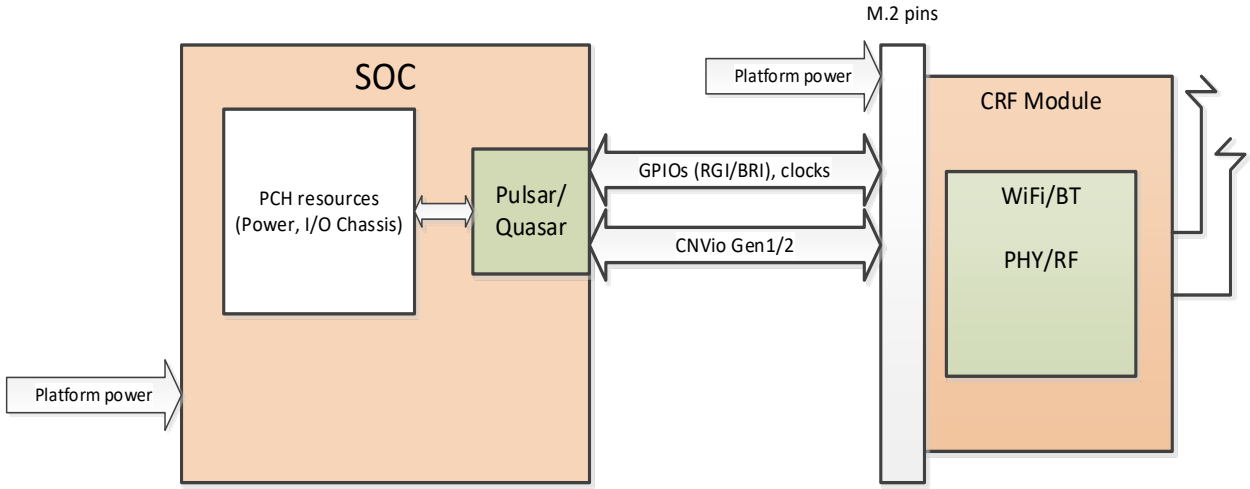
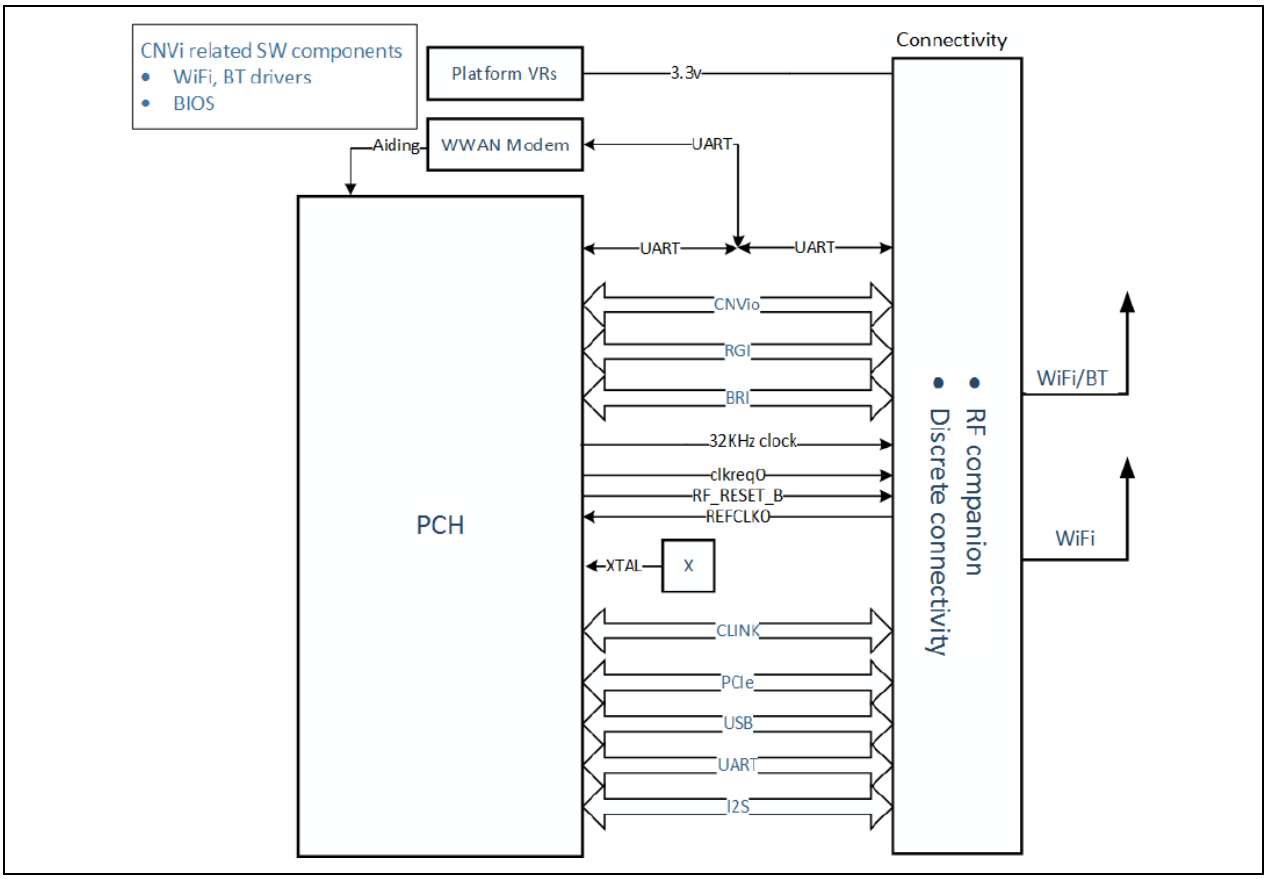


Figure 9–3 CNVi Platform block diagram



The CNVi platform system includes the following relevant blocks:

- System-on-Chip (SOC)
  - Pulsar/Quasar IP is integrated in the PCH (LP and H) part of Multi-chip module (MCM).
- Platform Crystal
  - In Quasar generation, The CRF and the platform have, each, its own crystal. There is NO shared clock between the Wireless CRF and the PCH/Platform.
  - In Pulsar generation, The CRF share its 38.4MHz clock with the Pulsar that is in the PCH.
  - The CRF (code name HrP – Harrison Peak) operate with 60 MHz Crystal. The SOC and the Quasar-IP uses the PCH Crystal, either 24MHz (e.g. CML) or 38.4MHz (e.g. ICL) one (depend on the Platform/PCH variant.
- WWAN Co-existence
  - This is a Cellular modem module, typically an M.2 card which provides cellular connectivity to the platform. The WWAN modem interacts with the CNVi through two different interfaces:
  - UART – A bus used to exchange Real Time co-existence data between Wi-Fi/BT and the cellular modem.
  - Aiding – Signals driven by the modem, which are used to assist in improving performance.

- Platform VRs
  - Provides a single 3.3V rail to the external connectivity circuitry.
- CNVi Related Straps
  - These are pin-straps used on SOC pins. These straps control SOC initialization functions related to CNVi implementation.
  - See "Power-up sequence" Sections for the signals and power-up flow
- Connectivity CRF/Discrete
  - The connectivity block can have different mechanical implementations depending on the form factor and functionality. Connectivity modules are characterized by the following properties:
    - Integration level: Intel RF companion chip (CRF) or Discrete (Intel or TPV)
    - Form factor: M.2 2230 (Connectorized module) or M.2 1216 or (Solder down module) Chip-on-board (COB)
    - Includes both Wi-Fi and BT Cores
    - Wi-Fi streams (depending on the used CRF):
      - New Generation CRF – 2x2 802.11ax (HrP2)
      - New Generation CRF – 1x1 802.11ax (CNVi Only, HrP1)
      - New Generation Discrete – 2x2 802.11ax (CcP)
      - Previous generation CRF - 1x1 or 2x2 802.11ac (JfP1/JfP2)
      - Previous generation Discrete – 2x2 802.11ac (ThP)
    - BT Stream is similar for both Previous generation (JfP) and New Generation (HrP)
- Connectivity Antennas
  - 2x2 Configuration includes:
    - Wi-Fi Main Antenna
    - Shared Wi-Fi/Bluetooth Antenna (combining Wi-Fi chain-1 and Bluetooth signals together)
  - 1x1 Configuration includes:
    - Wi-Fi/Bluetooth Antenna with Diversity option (can select one of the 2 available antennas).

Table 9-1 Antenna connector functionality

Functionality	Antenna Mark
Wi-Fi + BT	ANT1
Wi-Fi	ANT2 (M.2-2230) / ANT3 (M.2-1216)

9.3 CNVi form factors (CNVi/Discrete)

The following module variants are available:

- RF Companion M.2 (2230)
- RF Companion Solder-down M.2 (1216)
- RF Companion COB

9.4 RF Companion M.2 (2230) (CNVi/Discrete)

The RF Companion 2230 module has the same mechanical outline as the standard M.2 connectivity Type 2230-S3-E card.

The standard M.2 Key E connector pinout is modified to accommodate the proprietary RF companion signals, and is called "Hybrid Key-E". This unique design allows inserting the RF Companion module into a standard M.2 Key E socket.

This feature is possible only when the motherboard design follows specific guidelines described in this document.

The M.2 socket with the Hybrid Key-E scheme is intended to be used with a proprietary pinout. This scheme is called "Hybrid Key-E" due to the mechanical similarity to a Key-E connector and the ability to support both Companion RF and Discrete modules. When designing a motherboard with this scheme, it is possible to have the same M.2 socket supporting two different connectivity cards:

(1) CNVi Companion RF module (CRF)

(2) Standard M.2 discrete module (Discrete)

The ability to swap between these cards on the same M.2 socket, while using the same motherboard design, is an important feature desired by PC platform OEMs.

When designing the motherboard M.2 socket and routing according the Hybrid Key-E scheme, and subject to certain assumptions that will be defined later, the following basic properties are guaranteed:

- Inserting either of the optional cards (CRF, Discrete) to the M.2 socket will be safe (meaning no damage to the motherboard or card will occur).
- Both options can be used and will function as desired, subject to the following:
  1. For CNVi: CNVio/RGI/BRI and few of the CNVi-CRF signals are in place.
  2. For Discrete: All external interfaces (PCIe/USB/CLINK) are available and connected.

9.4.1 RF Companion module 2230 Hybrid Key-E pinout

The pinout for the Hybrid Key-E socket on the motherboard is shown in Figure 9–4. The inner columns show the Companion RF proprietary signals at their assigned pins. The Companion RF signals, listed with the prefix "/", signify that they are electrically MUX'd inside the PCH/SoC, and are shared. Due to this internal SoC sharing, these signals do not require any jumpers to select between the two functions. Note that there are six (6) such signals.

Figure 9–4 Hybrid Key-E socket pinout

Single Key Platform Slot Pinout

	PS - Bottom		CS - Top		
	Standard M.2 Key E	Next Gen iCNV Signals	Next Gen iCNV Signals	Standard M.2 Key E	
74	+V3P3A		GND		75
72	+V3P3A		WT_CLKP	REFCLKN1	73
70	PEWake1# (IO)(0/3.3V)		WT_CLKN	REFCLKP1	71
68	CLKREQ1# (IO)(0/3.3V)		GND		69
66	PERST1# (O)(0/3.3V)		WT_D0P	PERn1	67
64	RESERVED	REFCLK0 ~~(1V@38.4MHz)~~	WT_D0N	PERp1	65
62	ALERT# (I)(0/1.8)	~~A4WP_IRQ#~~ Not Used	GND		63
60	I2C_CLK (O)(0/1.8V)	~~A4WP_I2C_CLK~~ Not Used	WT_D1P	PETn1	61
58	I2C_DATA (IO)(0/1.8)	~~A4WP_I2C_DATA~~ Not Used	WT_D1N	PETp1	59
56	W_DISABLE1# (O)(0/3.3V)		GND		57
54	W_DISABLE2# (O)(0/3.3V)		PEWake0# (IO)(0/3.3V)		55
52	PERST0# (O)(0/3.3V)		CLKREQ0# (IO)(0/3.3V)		53
50	SUSCLK(32kHz) (O)(0/3.3V)	C_P32K (3.3V Tolerant)	GND		51
48	COEX_TXD (O)(0/1.8V)		REFCLKN0		49
46	COEX_RXD (O)(0/1.8V)		REFCLKP0		47
44	COEX3 (IO)(0/1.8V)		GND		45
42	CLink CLK		PERn0		43
40	CLink DATA		PERp0		41
38	CLink RESET (O)(0/3.3V)		GND		39
36	LPSS UART RTS (O)(0/1.8V)	/ BRI_DT (MUX'd in PCH/SoC)	PETn0		37
34	LPSS UART CTS (I)(0/1.8V)	/ RGI_RSP (MUX'd in PCH/SoC)	PETp0		35
32	LPSS UART Tx (O)(0/1.8V)	/ RGI_DT (MUX'd in PCH/SoC)	GND		33
E	Connector Key		Connector Key		E
	Connector Key		Connector Key		
	Connector Key		Connector Key		
	Connector Key		Connector Key		
22	LPSS UART Rx (I)(0/1.8V)	/ BRI_RSP (MUX'd in PCH/SoC)	WGR_CLKP	SDIO Reset#(O)(0/1.8V)	23
20	UART Wake# (I)(0/3.3V)		WGR_CLKN	SDIO Wake#(I)(0/1.8V)	21
18	GND	GND/LNA_EN (LcP Production)	GND	SDIO DAT3(IO)(0/1.8V)	19
16	LED2# (I)(OD)		WGR_D0P	SDIO DAT2(IO)(0/1.8V)	17
14	PCM_OUT (O)(0/1.8V)	/ CLKREQ0 (MUX'd in PCH/SoC)	WGR_D0N	SDIO DAT1(IO)(0/1.8V)	15
12	PCM_IN (I)(0/1.8V)		GND	SDIO DAT0(IO)(0/1.8V)	13
10	PCM_SYNC (OI)(0/1.8V)	/ RF_RESET_B (MUX'd in PCH/SoC)	WGR_D1P	SDIO CMD(IO)(0/1.8V)	11
8	PCM_CLK (OI)(0/1.8V)		WGR_D1N	SDIO CLK(O)(0/1.8V)	9
6	LED1# (I)(OD)		GND		7
4	+V3P3A		USB_D-		5
2	+V3P3A		USB_D+		3
			GND		1

9.4.2 RF Companion module 2230 pin list

The RF Companion 2230 module pin list is shown in Table 9–2.

Table 9-2 RF Companion module 2230 pin list

M.2 Pin#	Hybrid Key E M.2 2230 Pin Name	CNVi RF Companion Pin Description	Standard WLAN Solution Pin Description
1	GND	Connect all GND pins to Platform ground	Connect all GND pins to Platform ground
2	+V3P3A	Connect all +V3P3A pins to Platform 3.3V supply.	Connect all +V3P3A pins to Platform 3.3V supply.
3	USB D+	Unused	USB
4	+V3P3A	Connect all +V3P3A pins to Platform 3.3V supply.	Connect all +V3P3A pins to Platform 3.3V supply.
5	USB D-	Unused	USB
6	LED1#	Open-drain output capable of driving a platform LED. Optional to connect to Platform LED 1 (if needed).	Open-drain output capable of driving a platform LED. Optional to connect to Platform LED 1 (if needed).
7	GND	Connect all GND pins to Platform ground	Connect all GND pins to Platform ground
8	PCM_CLK	Unused	Optional Bluetooth I2S bus clock
9	WGR_D1N	CNVio lane 1 to Pulsar (Negative). Connect to SoC CNVio input D1- pin	Unused
10	PCM_SYNC/LCP_RSTN	RF companion reset signal, active low. Connect to SoC output.	Optional Bluetooth I2S bus sync
11	WGR_D1P	CNVio lane 1 to Pulsar (Positive) Connect to SoC CNVio input D1+ pin	Unused
12	PCM_IN	Unused	Optional Bluetooth I2S bus din
13	GND	Connect all GND pins to Platform ground	Connect all GND pins to Platform ground
14	PCM_OUT/CLKREQ0	Clock request signal. Used by the SoC to request the RF companion clock (38.4M Ref clock) for Pulsar and SoC.	Optional Bluetooth I2S bus dout
15	WGR_D0N	CNVio lane 0 to Pulsar (Negative) Connect to SoC CNVio input D0- pin	Unused
16	LED2#	Open-drain output capable of driving a platform LED. Optional to connect to Platform LED 2 (if needed).	Open-drain output capable of driving a platform LED. Optional to connect to Platform LED 1 (if needed).
17	WGR_D0P	CNVio lane 0 to Pulsar (Positive) Connect to SoC CNVio input D0+ pin	Unused
18	GND	Connect all GND pins to Platform ground	Connect all GND pins to Platform ground
19	GND	Connect all GND pins to Platform ground	Connect all GND pins to Platform ground
20	UART_WAKE#	Unused	Optional host wake for Bluetooth
21	WGR_CLKN	CNVio clock to Pulsar (Negative). Connect to SoC CNVio input CLK- pin	Unused
22	UART_RX/BRI_RSP	BRI bus output to SoC. Used for Bluetooth data and control between pulsar and the RF companion. Connect to SoC BRI input.	Optional Bluetooth UART bus rx

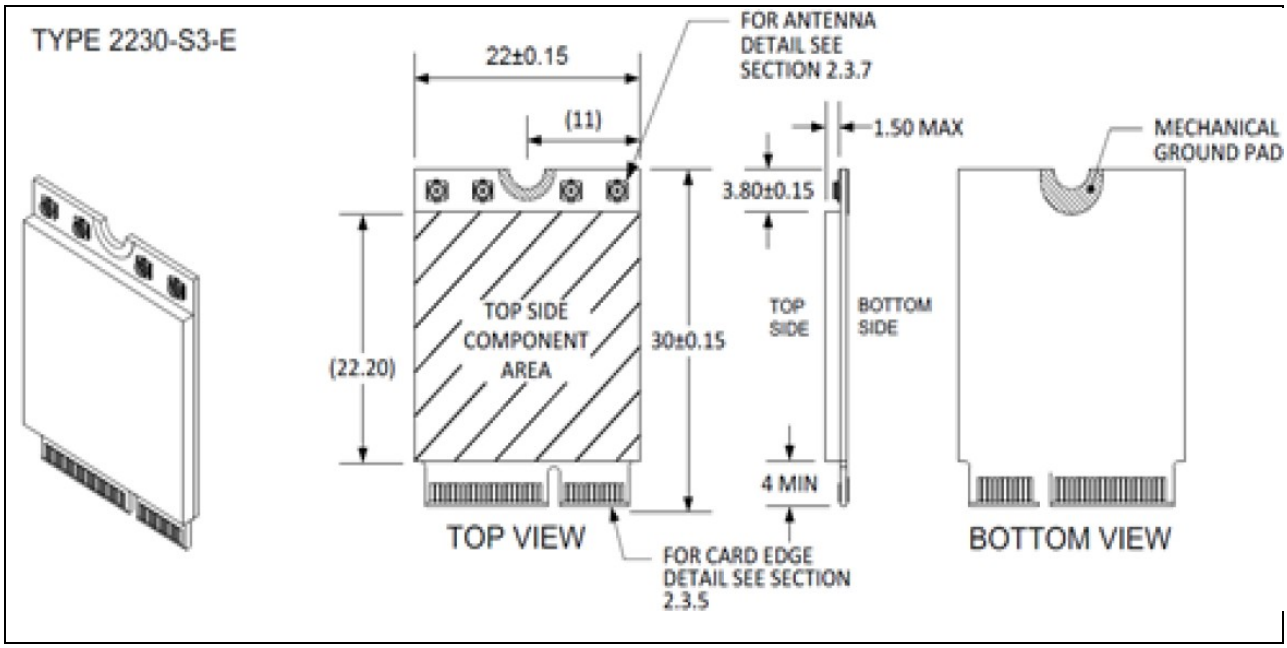
M.2 Pin#	Hybrid Key E M.2 2230 Pin Name	CNVi RF Companion Pin Description	Standard WLAN Solution Pin Description
23	WGR_CLKP	CNVio clock to Pulsar (Positive) Connect to SoC CNVio input CLK+ pin	Unused
32	UART_TX/RGI_DT	RGI bus input from SoC. Used for general control between pulsar and the RF companion. Connect to SoC RGI output	Optional Bluetooth UART bus tx
33	GND	Connect all GND pins to Platform ground	Connect all GND pins to Platform ground
34	UART_CTS/RGI_RSP	RGI bus output to SoC. Used for general control between pulsar and the RF companion. Connect to SoC RGI input	Optional Bluetooth UART bus cts
35	PETP0	Unused	Wi-Fi PCIe* tx lane 0
36	UART_RTS/BRI_DT	BRI bus input from SoC. Used for Bluetooth data and control between pulsar and the RF companion. Connect to SoC BRI output	Optional Bluetooth UART bus rts
37	PETN0	Unused	Wi-Fi PCIe* tx lane 0
38	CLINK_RESET	Unused	CLINK bus reset
39	GND	Connect all GND pins to Platform ground	Connect all GND pins to Platform ground
40	CLINK_DATA	Unused	CLINK bus data
41	PERP0	Unused	Wi-Fi PCIe* rx lane 0
42	CLINK_CLK	Unused	CLINK bus clock
43	PERN0	Unused	Wi-Fi PCIe* rx lane 0
44	COEX3	Unused	LTE coex standard pin
45	GND	Connect all GND pins to Platform ground	Connect all GND pins to Platform ground
46	COEX2	Unused	LTE coex UART rx
47	REFCLKP0	Unused	Wi-Fi PCIe* clock lane 0
48	COEX1	Unused	LTE coex UART tx
49	REFCLKN0	Unused	Wi-Fi PCIe* clock lane 0
50	SUSCLK	Slow clock input for low power logic. Connect to a 32Khz clock from the Platform or SoC.	Optional Slow clock input for low power logic. Connect to a 32Khz clock from the Platform or SoC. This clock may not be required- depending on the M.2 module specific requirements In HrP this signal is 1.8v based and is tolerant to 3.3v
51	GND	Connect all GND pins to Platform ground	Connect all GND pins to Platform ground
52	PERST0#	Unused	Wi-Fi PCIe* reset lane 0
53	CLKREQ0#	Unused	Wi-Fi PCIe* clock request lane 0
54	W_DISABLE2#	BT_KILL input. Connect to a Bluetooth KILL signal from the SoC or from the platform	BT_KILL input. a Bluetooth KILL signal from the SoC or from the platform(EC)
55	PEWAKE0#	Unused	Wi-Fi PCIe* host wake lane 0
56	W_DISABLE1#	WLAN_KILL input. Connect to a Wi-Fi* KILL signal from the SoC or from the platform	WLAN_KILL input. a Wi-Fi KILL signal from the SoC or from the platform(EC)

M.2 Pin#	Hybrid Key E M.2 2230 Pin Name	CNVi RF Companion Pin Description	Standard WLAN Solution Pin Description
57	GND	Connect all GND pins to Platform ground	Connect all GND pins to Platform ground
58	A4WP_I2C_DATA	Unused	Unused
59	WT_D1N	CNVio lane 1 from Pulsar (Negative). Connect to SoC CNVio output D1- pin	Unused
60	A4WP_I2C_CLK	Unused	Unused
61	WT_D1P	CNVio lane 1 from Pulsar (Positive) Connect to SoC CNVio output D1+ pin	Unused
62	A4WP_IRQ#	Unused	Unused
63	GND	Connect all GND pins to Platform ground	Connect all GND pins to Platform ground
64	REFCLK0	Clock signal. Used The 38.4M ref clock for Pulsar.	Unused
65	WT_D0N	CNVio lane 0 from Pulsar (Negative) Connect to SoC CNVio output D0- pin	Unused
66	PERST1#	Unused	Unused
67	WT_D0P	CNVio lane 0 from Pulsar (Positive) Connect to SoC CNVio output D0+ pin	Unused
68	CLKREQ1#	Unused	Unused
69	GND	Connect all GND pins to Platform ground	Connect all GND pins to Platform ground
70	PEWAKE1#	Unused	Unused
71	WT_CLKN	CNVio clock from Pulsar (Negative). Connect to SoC CNVio output CLK- pin	Unused
72	+V3P3A	Connect all +V3P3A pins to Platform 3.3V supply.	Connect all +V3P3A pins to Platform 3.3V supply.
73	WT_CLKP	CNVio clock from Pulsar (Positive) Connect to SoC CNVio output CLK+ pin	Unused
74	+V3P3A	Connect all +V3P3A pins to Platform 3.3V supply.	Connect all +V3P3A pins to Platform 3.3V supply.
75	GND	Connect all GND pins to Platform ground	Connect all GND pins to Platform ground

9.4.3 RF Companion module 2230 mechanical dimensions

The M.2 2230 CRF module mechanical diagram is shown in Figure 9–5.

Figure 9–5 Module mechanical diagram; source is PCI-SIG M.2



9.5 Special considerations for the Hybrid Key-E scheme (CNVi/Discrete)

The Hybrid Key-E scheme relies on assigning multiple functions to the M.2 connector pins and PCH pins. This causes a significant reduction of the amount of signals that needs to be routed between the SoC and the M.2 module, at the expense of additional dependency between modes, and the loss of some functionality. The dependencies between multiple function pins and M.2 card functionality is described in the following sections.

9.5.1 Shared M.2 socket pins

The M.2 pins described below are shared between different functions (CNVi/Discrete).

V3P3A, GND

These are the M.2 card power supply (3.3V) and Ground pins, respectively. Both have multiple pins on the connector. These pins have the same purpose in either Discrete or CNVi implementations, and therefore are not affected by the Hybrid Key-E scheme.

PCIe-1/CNVio

These are six pins that are assigned to the PCIe-1 bus in the M.2 standard pinout. This bus has three differential pairs, two for the PCIe data lanes (one per direction) and one for the PCIe clock. In the Hybrid Key-E scheme, these signals are used for the CNVio interface from Pulsar/Quasar (CNVi) to the RF companion chip. Due to this sharing, the Hybrid Key-E scheme does not support PCIe-1.

SDIO/CNVio

These are eight pins which are assigned to the SDIO bus in the M.2 standard pinout. This bus has eight signals, four bi-directional for the SDIO data, one be-directional command signal, one clock (SoC to M.2) and 2 control (Reset SoC to M.2, Wake M.2 to SoC). In the Hybrid Key-E scheme these signals are used for CNVio interface the RF companion chip to Pulsar (six for CNVio and two for ground). Due to this sharing, the Hybrid Key-E scheme does not support SDIO.

PCM/ClockReq and Reset

The standard M.2 defines four pins for a dedicated PCM audio serial bus. In the Hybrid Key-E scheme, two of these signals are used for CNVi Clock (from RF companion to SoC) and Reset (For SoC to RF companion). Since the PCM serial bus is connected to PCH GPIO pins, and the CNVi clock request and reset pins are also connected to PCH GPIO pins, it is possible to have support for both PCM bus and CNVi signals by changing the PCH GPIO muxing function select. Due to this sharing, the Hybrid Key-E scheme can still support PCM (for discrete connectivity with PCM support).

UART (BT) / BRI and RGI

The standard M.2 defines four pins for a dedicated UART serial bus for Bluetooth. In the Hybrid Key-E scheme, all of these signals are used for CNVi BRI (Bluetooth Radio Interface) and RGI (Radio Generic interface), each comprising of two signals (one per direction). Since the UART serial bus is connected to PCH GPIO pins, and the CNVi BRI and RGI are also connected to PCH GPIO pins, it is possible to have support for both UART bus and CNVi signals by changing the PCH GPIO muxing function select. Due to this sharing, the Hybrid Key-E scheme can still support BT UART (for discrete connectivity with BT-UART support).

SUSCLK/P_32k

These signals are both functionally similar. In the M.2 standard, this pin is optionally connected to a 32kHz RTC clock. In the Hybrid Key-E scheme for CNVi, it should be connected to a 32kHz clock. In the CRF, there is an option to use either an internal 32kHz clock or this external clock. The decision can be made by an auto-detect mechanism that checks whether the external 32kHz clock is indeed active (configurable option), and selects it if so, else it will choose the internal clock. The "price" is additional power consumption in low-power states. If an external clock is used, it MUST be driven by a valid 32kHz clock any time the RF companion module is powered on (no glitches are allowed), and a BIOS/ACPI based indication is needed as well (see **Ref 5** "*Intel Connectivity Platforms BIOS Guidelines*"). The 32kHz clock can come from a PCH pin or from a different source on the platform, depending on the platform used.

Note that the External 32kHz accuracy is assumed to be 20ppm.

GND/LNA_EN

This signal is used for different purposes in CNVi and discrete, but in both cases should be connected to ground. Therefore, it does not affect functionality.

NFC I/F, and A4WP+Ref clock

In the Hybrid Key-E scheme, only one of these four signals is used. The REFCLK0 (in JfP case) signal connects the reference clock (single ended, 1V p-p, 38.4 MHz) from the RF companion to the SoC. The remaining three signals are not used.

RF_RESET_B

This is an Intel proprietary signal between the SoC and the CRF, used as internal RESET indication from the SoC to the CRF used during the init flow of the CNVi based modules. This signal has an internal Pull-Down in HrP side.

ClkReq0 (Pin14 in M.2-2230, A43 in 1216)

This is an Intel proprietary signal between the SoC and the CRF , used as Clock request indication from the SoC to the CRF to supply Clk from the CRF to the SoC – this is used by JfP, but NOT used by HrP

In both CRFs, this signal is also used during the init flow of the CNVi based modules (so is still a required signal)

This signal has an internal Pull-Down in HrP side. It is also shared with Optional PCM interface that can be used with Discrete Module solution (Non CRF).

9.5.2 Non-shared M.2 socket pins

Some pins on the M.2 connector are not shared, meaning they are not used for any CNVi function. The functions of these pins can still be impacted by the Hybrid Key-E scheme as described below.

PEWake1#, CLKREQ1#, PERST1#

These are three control signals used by the PCIe-1 bus in standard M.2 cards. Although these signals are not shared with any other function, they have no usage in a Hybrid Key-E scheme design. This is because the PCIe-1 bus by itself is not usable. (See PCIe-1/ CNVio sharing, above.)

PCIe-0 Bus

This consists of six signals (three differential pairs) used for transmitting PCIe data to and from the SoC, and a single pair used for the PCIe bus clock. In a CNVi RF companion configuration, these signals are left unused. In standard discrete configurations, these signals are used as the Wi-Fi bus interface.

W_DISABLE1#, W_DISABLE2#.

These signals are used for Wi-Fi and BT RF-Kill control, respectively. (Asserting these signals shuts off the RF transmission or the relevant core.) The functions of these signals are the same for Hybrid Key-E and therefore they are not affected by this scheme.

Jefferson/Harrison Peak M.2 modules support receiving a wireless disable (RF-KILL) command through the two RF-KILL pins for turning off Wi-Fi and BT, respectively. These pins can be connected to a platform switch or to SoC GPIOs (Recommendation- if possible do not use GPIOs that have Platform impact as “bootstraps” during platform init).

The RF-Kill signals (Wireless disable*) have an internal pull-up in HrP side (they are “Active Low” signals).

PEWake0#, CLKREQ0#, PERST0#

These are three control signals used by the PCIe-0 bus in standard M.2 cards. They should be routed to SoC pins that are assigned to GPIOs in Discrete mode.

Coex UART interface

This interface consist of three signals (two UART bus signals and one GPIO). They are used for Wi-Fi/BT-LTE coexistence signaling in the M.2 standard definition. Since these pins are left unused in the RF companion configuration, they can still be used with a discrete M.2 card, even when designing with the Hybrid Key-E scheme. In platforms that are designed to support a WWAN modem and Hybrid Key-E, there should be three pins connected to each signal, to allow the modem to connect to the M.2 pin (in the Discrete connectivity case) or to the PCH (in the CNVi case).

CLINK interface

This I/F is relevant, and is a MUST for vPRO based platforms. This consists of 3 signals (clock, data and reset). This bus in an Intel proprietary bus. Since these pins are left unused in the RF companion,

they will still be used with a discrete M.2 card even when designing with the "Hybrid Key-E" scheme on vPRO based platforms.

LED1, LED2

These are optional pins that are assigned to drive LEDs on the platform in the standard M.2 cards. They are used for the same function when using CNVi, and therefore are not affected by the Hybrid Key-E scheme.

USB bus

The standard M.2 defines two pins for a differential USB bus. This has no usage in the RF companion configuration. When using a standard M.2 Discrete card, the pins will have the standard functionality and are not affected by the Hybrid Key-E scheme.

The different connectivity interfaces used by standard M.2 Intel connectivity (TPV), CNVi and RF companion, configurations are summarized in Table 9–3. The table also points to the different restrictions posed by the use of a Hybrid Key-E socket design on the motherboard.

Table 9-3 Hybrid Key-E interface mapping for different connectivity cards

M.2 interface	CNVi	Discrete
PCIe-1	M.2 pins are not connected to the CRF. Wi-Fi uses internal IOSF to interface the host.	Used for Wi-Fi host interface
PCIe-2	Not functional Pins are connected to CRF and Pulsar/Quasar CNVio and can't be used as PCIe.	Not functional Pins are connected to Pulsar/Quasar CNVio and can't be used as PCIe.
Wi-Fi SDIO	Not functional Pins are connected to CRF and Pulsar/Quasar CNVio and can't be used as SDIO.	Not functional Pins are connected to Pulsar/Quasar CNVio and can't be used as SDIO.
Wi-Fi CLINK	M.2 pins are not connected to the CRF. Wi-Fi uses internal CLINK to interface the ME.	Used for Wi-Fi CSME interface
Wi-Fi RF-Kill	Used (optional)	Used (optional)
BT USB	M.2 pins are not connected to the CRF. BT uses internal U2U to interface the host.	Used for BT USB interface
BT UART	M.2 pins are not connected to the CRF. BT uses internal UART to interface the host.	Used for BT UART interface
BT I2S (Audio)	M.2 pins are not connected to the CRF. BT uses internal I2S to interface the host.	Used for BT I2S interface
BT wake	M.2 pin is not connected to the CRF. BT uses internal vGPIO.	Used for BT wake signal
BT RF-Kill	Used (optional)	Used (optional)
NFC	Not functional Pins are connected to A4WP bus and to Refclock (38.4M system clock) and can't be used for NFC.	Not functional Pins are connected to A4WP bus and to Refclock (38.4M system clock) and can't be used for NFC.

M.2 interface	CNVi	Discrete
I2C bus to A4WP	Used for A4WP support to connect to platform WPR module.	Used for A4WP support to connect to platform WPR module.
3.3V Power supply pins	Used per M.2 standard	Used per M.2 standard
GND	Used per M.2 standard	Used per M.2 standard

Other General Recommendations

The Following Pins are not in use and, at least on the Intel ICL RVPs it is recommended to Not Connect or connect to test points:

- Pins 58,60,62,64, 68, 70 will be TP (or disconnected).

Pin 66 can be connected to the "platform reset" BUT notice that Intel Wireless Products will not respond to this specific signal and will ignore it.

9.6 RF Companion Soldered-down M.2 (1216) (CNVi/Discrete)

The RF Companion SD-1216 module has the same mechanical outline as the standard M.2 connectivity type 1216-S3. The standard M.2 land pattern is modified to accommodate the proprietary RF companion module signals. As opposed to the connectorized module, the SD-1216 module is not sharing the standard M.2 pads for the RF companion functions. Instead, it has an additional set of solder pads which don't overlap with the standard solder pads. This allows having a single motherboard design that can accommodate either a standard M.2 1216 card or an RF companion 1216 card. However, unlike in the connectorized case, swapping cards requires removing a soldered-down module and can't be done by a simple socket card exchange. Additionally, the assembly tooling and BOM should change between a Discrete and CNVi motherboard assembly.

9.6.1 RF Companion module 1216 pad-out

The special pad-out required for supporting CNVi and Discrete is shown in Figure 9–6 and Figure 9–7.

Figure 9–6 SD-1216 module pad-out for supporting CNVi and Discrete 1216 modules

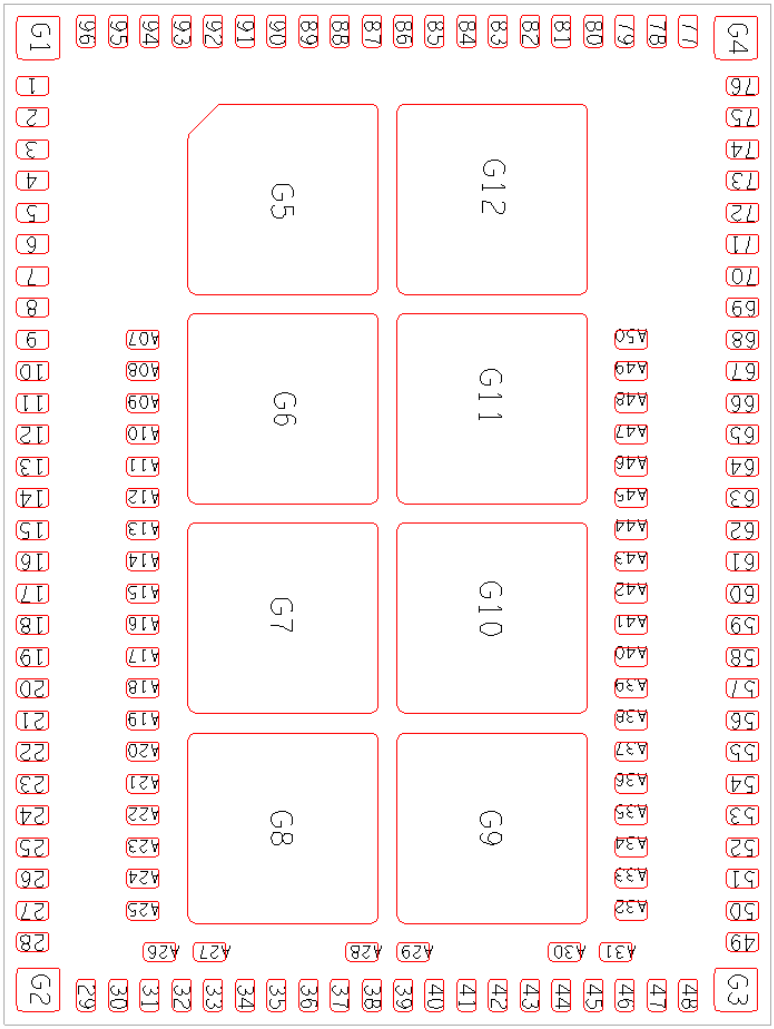
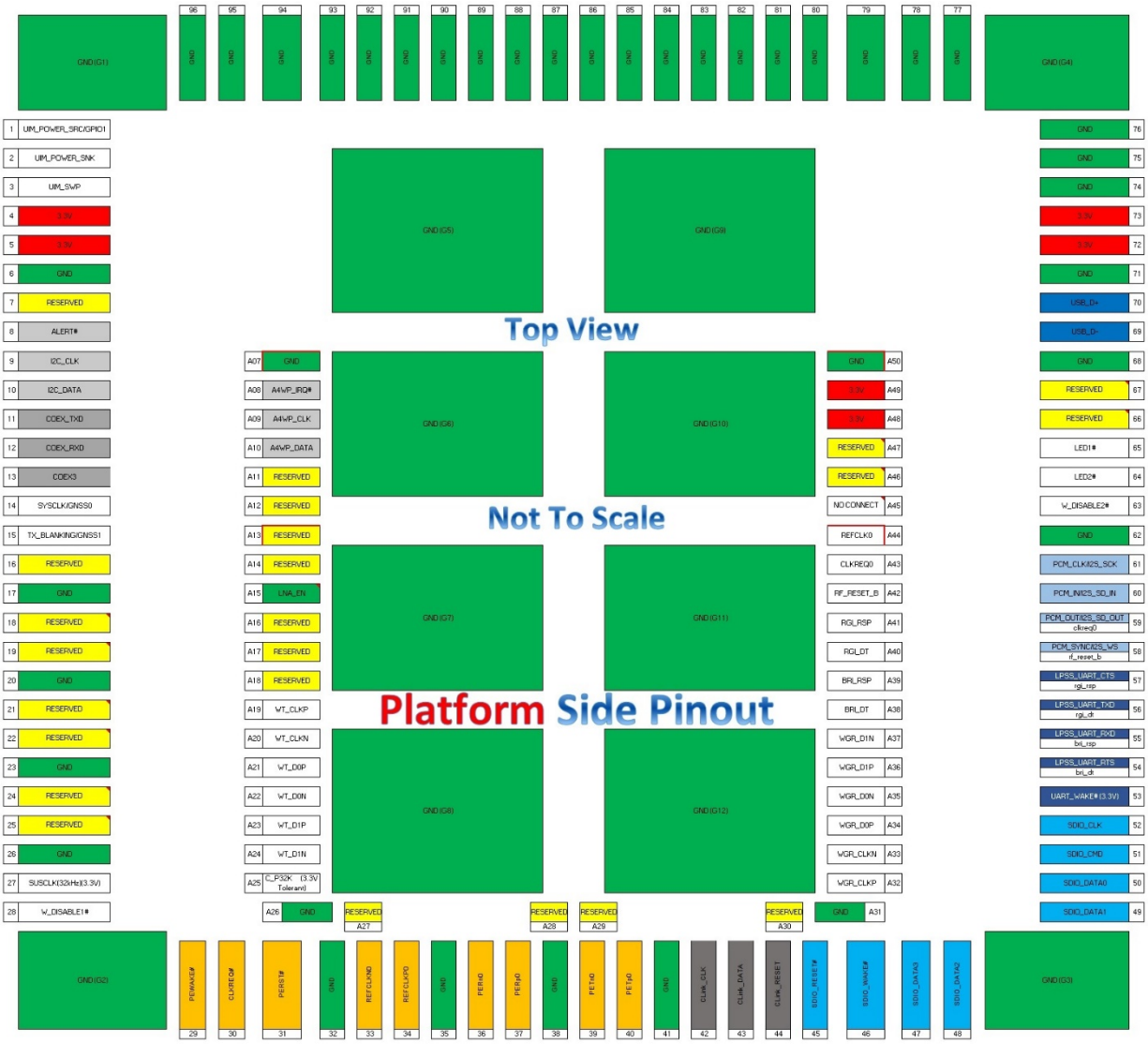


Figure 9–7 SD-1216 module pad-out for supporting CNVi and Discrete 1216 modules



9.6.2 RF Companion module 1216 pin list (CNVi only)

Table 9-4 RF Companion module 1216 pin list

Pin #	Pin Name	Function When CNVi is Used	Function When Standard M.2 is Used
1	UIM_POWER_SRC/GPIO1	Not used	UIM_POWER_SRC/GPIO1
2	UIM_POWER_SNK	Not used	UIM_POWER_SNK
3	UIM_SWP	Not used	UIM_SWP
4	3.3V	3.3V	3.3V
5	3.3V	3.3V	3.3V
6	GND	GND	GND

Pin #	Pin Name	Function When CNVi is Used	Function When Standard M.2 is Used
7	RESERVED	Not used	RESERVED
8	ALERT#	Not used	ALERT#
9	I2C_CLK	Not used	I2C_CLK
10	I2C_DATA	Not used	I2C_DATA
11	COEX_TXD	Not used	COEX_TXD
12	COEX_RXD	Not used	COEX_RXD
13	COEX3	Not used	COEX3
14	SYSCLK/GNSS0	Not used	SYSCLK/GNSS0
15	TX_BLANKING/GNSS1	Not used	TX_BLANKING/GNSS1
16	RESERVED	Not used	RESERVED
17	GND	GND	GND
18	RESERVED	Not used	Not used
19	RESERVED	Not used	Not used
20	GND	GND	GND
21	RESERVED	Not used	Not used
22	RESERVED	Not used	Not used
23	GND	GND	GND
24	RESERVED	Not used	Not used
25	RESERVED	Not used	Not used
26	GND	GND	GND
27	SUSCLK(32kHz)(3.3V)	Not used	SUSCLK(32kHz)(3.3V)
28	W_DISABLE1#	W_DISABLE1#	W_DISABLE1#
29	PEWAKE#	Not used	PEWAKE#
30	CLKREQ#	Not used	CLKREQ#
31	PERST#	Not used	PERST#
32	GND	GND	GND
33	REFCLKN0	Not used	REFCLKN0
34	REFCLKP0	Not used	REFCLKP0
35	GND	GND	GND
36	PERn0	Not used	PERn0
37	PERp0	Not used	PERp0
38	GND	GND	GND
39	PETn0	Not used	PETn0
40	PETp0	Not used	PETp0
41	GND	GND	GND
42	CLink_CLK	Not used	CLink_CLK
43	CLink_DATA	Not used	CLink_DATA
44	CLink_RESET	Not used	CLink_RESET

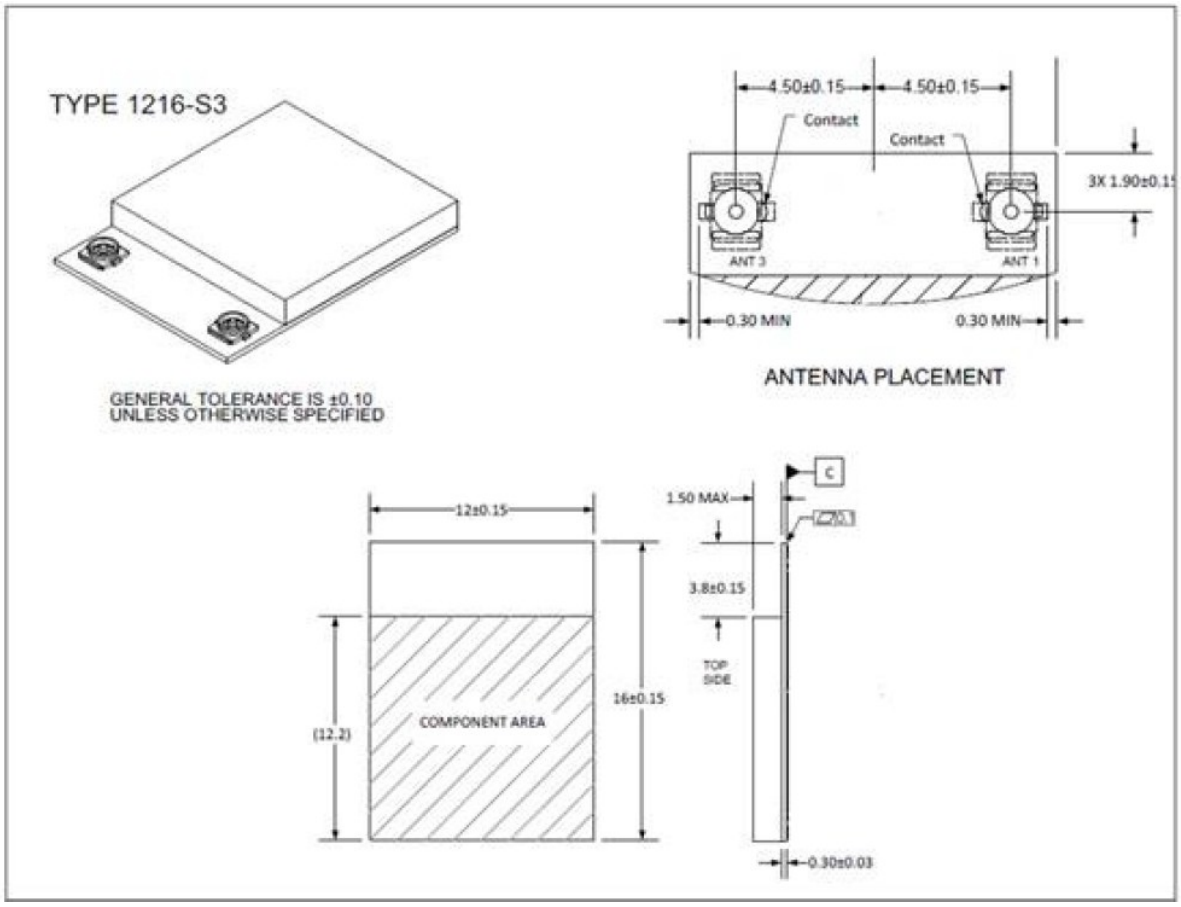
Pin #	Pin Name	Function When CNVi is Used	Function When Standard M.2 is Used
45	SDIO_RESET#	Not used	Not used
46	SDIO_WAKE#	Not used	Not used
47	SDIO_DATA3	Not used	Not used
48	SDIO_DATA2	Not used	Not used
49	SDIO_DATA1	Not used	Not used
50	SDIO_DATA0	Not used	Not used
51	SDIO_CMD	Not used	Not used
52	SDIO_CLK	Not used	Not used
53	UART_WAKE# (3.3V)	Not used	UART_WAKE# (3.3V)
54	LPSS_UART_RTS/bri_dt	Not used	LPSS_UART_RTS/bri_dt
55	LPSS_UART_RXD/bri_rsp	Not used	LPSS_UART_RXD/bri_rsp
56	LPSS_UART_TXD/rgi_dt	Not used	LPSS_UART_TXD/rgi_dt
57	LPSS_UART_CTS/rgi_rsp	Not used	LPSS_UART_CTS/rgi_rsp
58	PCM_SYNC/I2S_WS	Not used	PCM_SYNC/I2S_WS
59	PCM_OUT/I2S_SD_OUT	Not used	PCM_OUT/I2S_SD_OUT
60	PCM_IN/I2S_SD_IN	Not used	PCM_IN/I2S_SD_IN
61	PCM_CLK/I2S_SCK	Not used	PCM_CLK/I2S_SCK
62	GND	GND	GND
63	W_DISABLE2#	W_DISABLE2#	W_DISABLE2#
64	LED2#	LED2#	LED2#
65	LED1#	LED1#	LED1#
66	RESERVED	Not used	RESERVED
67	RESERVED	Not used	RESERVED
68	GND	GND	GND
69	USB_D-	Not used	USB_D-
70	USB_D+	Not used	USB_D+
71	GND	GND	GND
72	3.3V	3.3V	3.3V
73	3.3V	3.3V	3.3V
74	GND	GND	GND
75	GND	GND	GND
76	GND	GND	GND
77	GND	GND	GND
78	GND	GND	GND
79	GND	GND	GND
80	GND	GND	GND
81	GND	GND	GND
82	GND	GND	GND

Pin #	Pin Name	Function When CNVi is Used	Function When Standard M.2 is Used
83	GND	GND	GND
84	GND	GND	GND
85	GND	GND	GND
86	GND	GND	GND
87	GND	GND	GND
88	GND	GND	GND
89	GND	GND	GND
90	GND	GND	GND
91	GND	GND	GND
92	GND	GND	GND
93	GND	GND	GND
94	GND	GND	GND
95	GND	GND	GND
96	GND	GND	GND
G1	GND	GND	GND
G2	GND	GND	GND
G3	GND	GND	GND
G4	GND	GND	GND
G5	GND	GND	GND
G6	GND	GND	GND
G7	GND	GND	GND
G8	GND	GND	GND
G9	GND	GND	GND
G10	GND	GND	GND
G11	GND	GND	GND
G12	GND	GND	GND
A07	GND	GND	Not Applicable
A08	A4WP_IRQ#	A4WP_IRQ#	Not Applicable
A09	A4WP_CLK	A4WP_CLK	Not Applicable
A10	A4WP_DATA	A4WP_DATA	Not Applicable
A11	RESERVED	RESERVED	Not Applicable
A12	RESERVED	RESERVED	Not Applicable
A13	RESERVED	RESERVED	Not Applicable
A14	RESERVED	RESERVED	Not Applicable
A15	LNA_EN	GND	Not Applicable
A16	RESERVED	RESERVED	Not Applicable
A17	RESERVED	RESERVED	Not Applicable
A18	RESERVED	RESERVED	Not Applicable

Pin #	Pin Name	Function When CNVi is Used	Function When Standard M.2 is Used
A19	WT_CLKP	WT_CLKP	Not Applicable
A20	WT_CLKN	WT_CLKN	Not Applicable
A21	WT_D0P	WT_D0P	Not Applicable
A22	WT_D0N	WT_D0N	Not Applicable
A23	WT_D1P	WT_D1P	Not Applicable
A24	WT_D1N	WT_D1N	Not Applicable
A25	C_P32K	C_P32K	Not Applicable
A26	GND	GND	Not Applicable
A27	RESERVED	RESERVED	Not Applicable
A28	RESERVED	RESERVED	Not Applicable
A29	RESERVED	RESERVED	Not Applicable
A30	RESERVED	RESERVED	Not Applicable
A31	GND	GND	Not Applicable
A32	WGR_CLKP	WGR_CLKP	Not Applicable
A33	WGR_CLKN	WGR_CLKN	Not Applicable
A34	WGR_D0P	WGR_D0P	Not Applicable
A35	WGR_D0N	WGR_D0N	Not Applicable
A36	WGR_D1P	WGR_D1P	Not Applicable
A37	WGR_D1N	WGR_D1N	Not Applicable
A38	BRI_DT	BRI_DT	Not Applicable
A39	BRI_RSP	BRI_RSP	Not Applicable
A40	RGI_DT	RGI_DT	Not Applicable
A41	RGI_RSP	RGI_RSP	Not Applicable
A42	RF_RESET_B	RF_RESET_B	Not Applicable
A43	CLKREQ0	CLKREQ0	Not Applicable
A44	REFCLK0	REFCLK0	Not Applicable
A45	NO CONNECT	NO CONNECT	Not Applicable
A46	RESERVED	RESERVED	Not Applicable
A47	RESERVED	RESERVED	Not Applicable
A48	3.3V	3.3V	Not Applicable
A49	3.3V	3.3V	Not Applicable
A50	GND	GND	Not Applicable

9.6.3 RF Companion module 1216 mechanical dimensions

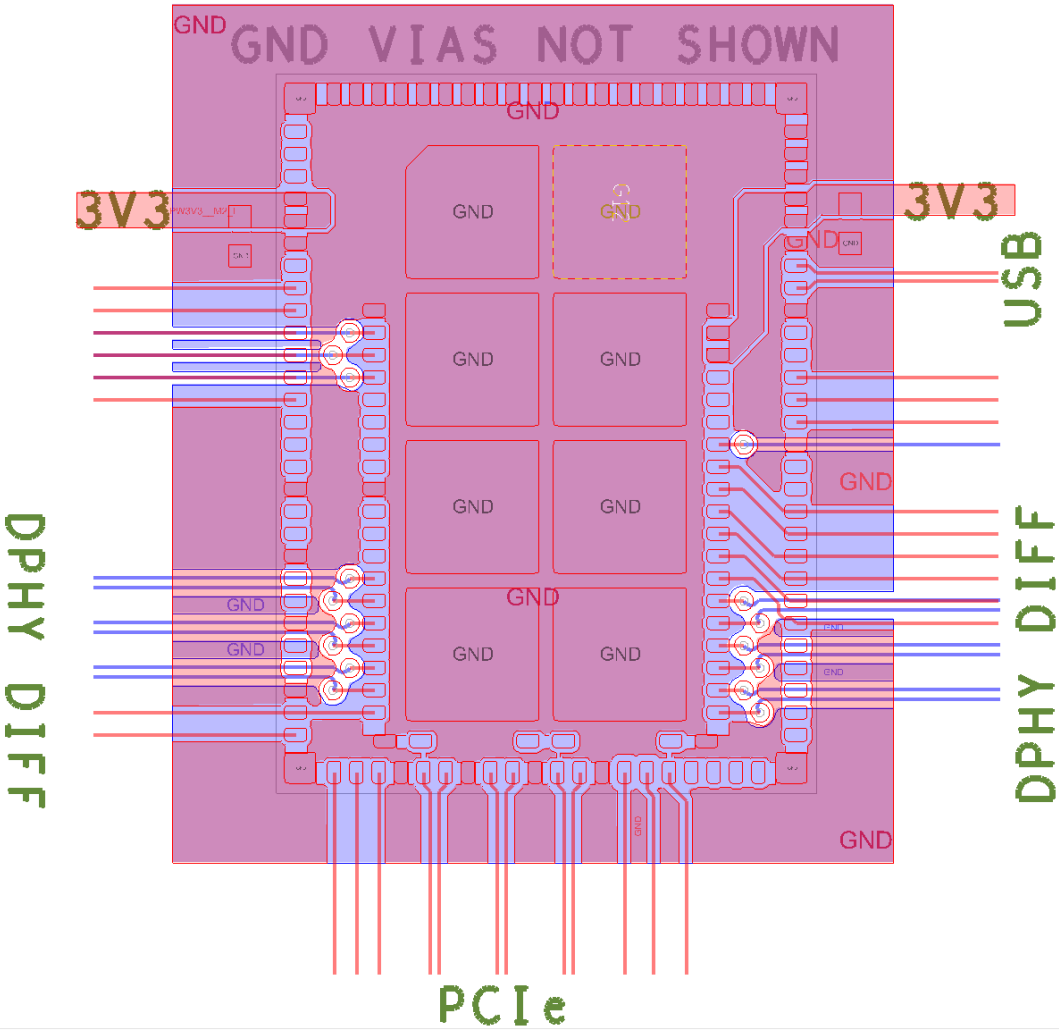
Figure 9–8 SD-1216 module mechanical diagram



9.7 Breakout example for JfP/HrP soldered-down module

The soldered-down JfP/HrP modules have a special pad shape which combines the standard M.2 pad ring on the outside with the new inner ring of the CNVi pads. It is recommended to consider all signal properties when designing the motherboard for dual discrete/CNVi design supporting this M.2 1216. An example for the breakout layout for a type-3 board (with no micro-via) is shown in Figure 9–9. Note that in order to keep the picture clear, this example shows only two signal layers (top layer and third layer), while the other layers are not shown. Also, there is an assumption that the second layer shall be ground.

Figure 9–9 Board layout example showing the breakout from JfP/HrP 1216 pads



9.8 Platform considerations (CNVi/Discrete)

9.8.1 Selecting a connectivity solution

The platform motherboard can be designed to support discrete connectivity (either Intel or TPV), integrated connectivity (CNVi).

Note: All CNVi 2230 SKUs can support a "Hybrid Key-E" routing with no jumpers. When considering a TPV module, one should only use a Key-E module if the motherboard design is "Hybrid Key-E." A Key-A module will not fit into this scheme.

Table 9-5 CNVi module SKUs

SKU	M.2 type	Wi-Fi chains	LTE coex (on-module BAW filter)	Comments
JfP1 2230	2230	1x1	No	Basic 1x1
JfP1 2230 diversity	2230	1x1	No	Basic 1x1 with diversity
JfP1-SD	1216	1x1	No	Solder-down 1x1
JfP1-SD diversity	1216	1x1	No	Solder-down 1x1 with diversity
JfP2 2230	2230	2x2	No	Basic 2x2
JfP2 2230 vPro	2230	2x2	No	vPro 2x2
JfP2 2230 vPro Coex	2230	2x2	Yes	vPro 2x2 with Coex
JfP2 SD	1216	2x2	No	Solder-down 2x2
JfP2 SD Coex	1216	2x2	Yes	Solder-down 2x2 with LTE Coex
JfP2 SD vPro	1216	2x2	No	Solder-down vPro 2x2
HrP1 2230	2230	1x1	No	.11ax 1x1
HrP1 SD Diversity	1216	1x1	No	.11ax Solder-down 1x1
HrP2 2230	2230	2x2	No	.11ax 2x2
HrP2 SD-1216	1216	2x2	No	.11ax Solder-down 2x2
HrP2 SD-1216 LTE	1216	2x2	Yes	.11ax Solder-down 2x2

Table 9-6 Discrete module SKUs

SKU	M.2 type	Wi-Fi chains	LTE coex (on-module BAW filter)	Comments
ThP2 2230	2230	2x2	No	Basic 2x2 module
ThP2 2230 vPro	2230	2x2	No	vPro 2x2 module
CcP 2230	2230	2x2	No	.11ax 2x2 module
CcP SD-1216	1216	2x2	No	.11ax 2x2 module
CcP SD-1216 LTE	1216	2x2	Yes	.11ax 2x2 module

9.9 Signal connection pitfalls (CNVi/Discrete)

The OEM should make sure to follow the M.2 definitions of signal names and directions (I/O, Tx/Rx, etc.) and avoid confusion between the platform side and device side.

Note that some lines are bidirectional, such as PCIe CLKREQ, PEWAKE.

9.10 Internal USB port used in the PCH part (CNVi)

The CNVi IP (Quasar-IP) that is embedded in the PCH uses an internal IOSF (PCIe like) bus for Wi-Fi and internal USB for BT.

The port used for this internal USB (for BT) can change between different PCH variants, as shown in Table 9–7.

Note: The ports are assigned zero-based numbers (e.g., the 10th port is #9).

Table 9-7 Example internal USB port assignments in PCH

PCH	PCH-LP (ICPLP, TGPLP, CMPLP, CNPLP, MCC)	PCH-H (ICPH, TGPH, CMPH, CNPH)	PCH-N (JPL)
USB Port Number (Zero-based) (When starting with "1", e.g., BIOS)[1]	Port 9 (#10)	Port 13 (#14)	Port 7 (#8)

[1] Can change between PCHs!

9.11 Pull-ups and pull-downs (CNVi/Discrete)

9.11.1 Internal/integrated PU/PD settings

The OEM should consider the pull-ups and pull-downs on the CRF card, as described in Table 9–8.

Table 9-8 Pull-ups and pull-downs

I/F	Signals	PU/PD in CNVr (CRF)	PU/PU in CNVi (SoC)	Comment
BRI/RGI (BT UART)	RGI_DT/BRI_DT	PU (~120-150Kohm), RGI_DT shall be applied with 1K pull down during power-on Init	-	Shared with BT UART Expected power wasted while active with 100K <32uW at each pin RGI_DT is used by the platform to strap the presence of the CRF, as such it is a strong pull-down by the CRF (1K) as long as RF_RESET_B = 0 BRI_RSP is used by the CNVi to strap the CRF type; i.e, when to apply PLL speed: when BRI_RSP = 0 – PLL at 1280M (JfP), when BRI_RSP =1 – PLL at 1320 (HrP and other future parts)
	RGI_RSP/BRI_RSP	none	PU = 20Kohm This can be set by the BIOS after boot-up; needs to be enabled ONLY if CNVi is not used in the platform	
W_Disable*#	Wi-Fi/BT RF Kill	PU (~110–130Kohm)	-	
Slow CLK	SUSCLK (32kHz)	PD (~100Kohm)	-	If avaliable on platform
Init Signals	RF_RESET_B	PD (~100Kohm)	-	Shared with PCM_SYNC
	CLKREQ0	PD (~200Kohm)	-	Shared with PCM_OUT

9.11.2 Platform PU/PD requirements

The OEM should apply pull-ups and pull-downs on the platform side according to Table 9–9.

Table 9-9 Platform pull-up and pull-down requirements

I/F	Signals	PU/PD in Platform	Comment
BRI/RGI BT UART	RGI_DT	PU (20kohm)	This pull is required so that the SOC will be able to reliably detect that the CRF is present at power-up. However, it is possible to increase the resistor to 50K or even to to 100K instead of 20K.
Init signals	RF_RESET_B	PD (75kohm)	It is highly encouraged to increase this resistor (or allow to switch it off when CNVi is active; not sure this is possible at the platform level). This resistor consumes power (43uW) all the time.

I/F	Signals	PU/PD in Platform	Comment
38.4 Ref clock	RefCLK	PD (10kohm) (for JfP)	Only if used (e.g. Pulsar based platform, a platform-level decision); **not supported and not connected by HrP**.
A4WP indication	A4WP_PRESENT (GPP_F_19 in ICL-PCH-LP)	PD (75kohm)	Although not used, it is Recommended to not use this GPIO for other neeeds, to not toggle it, and to add a PD at the platform level to avoid a floating signal (with a non-deterministic value)

The OEM must avoid using a specific PU/PD when not needed or when required to not be used. Unless this rule is followed, a back-bias condition will result, where the IO is getting voltage before the device side is ready for it.

9.12 IO connection scenarios and best practices (CNVi/Discrete)

The motherboard designer should address the following requirements for the sake of avoiding failsafe problems, reducing unneeded leakage and for following best practice design rules:

- Level-shifter back-bias prevention
  - Level shifter shall not set value in A side when not getting voltage in B side.
    - **Rationale:** Prevent back bias and wrong logic condition.
  - Level shifters shall be back-bias protected.
    - **Rationale:** The level shifter is often supplied with a different supply than the IO connected to it. During ramp up/down states there might be back-bias scenario.

9.13 I/F-specific guidelines (CNVi)

9.13.1 CNVio signals

The CNVio signals connect between the RF companion module and the SoC. They are used as the main data bus for Wi-Fi, to transfer data between the Pulsar and the RF companion chip. The CNVio signals are physically similar to those in the MiPi DPHY standard, but have a different (and Intel-proprietary) protocol.

Since the physical layer of the CNVio is similar to the MiPi DPHY standard, the user should follow the MiPi DPHY routing signal requirements. These are well documented in the MiPi DPHY standard specification. (See Chapter 7 of the MiPi DPHY standard: Interconnect and Lane Configuration.)

The CNVio bus is source-synchronous, getting up to 2500Mbps per lane. Each lane has data carried over a differential pair, and each direction may have multiple lanes and a single clock driven by the source.

Routing

The two traces of each lane must be routed together / same-length, as matched as possible (to reduce the signal propagation time difference). Moreover, since the CNVio uses one clock signal for multiple lanes in each direction, there should also be good delay matching between the two data lanes and the clock. There are no special delay matching requirements between lanes on opposite directions.

If needed, there is an option to add test points on those signals, but try to reduce such additional capacitance to a minimum. See the recommended parameters in Table 9–11.

Table 9-10 CNVio DATA vs. CLK imbalance budget

CNVIO Protocol	Protocol End2End	Intel Platform with 2230			Intel Platform with 1216		
		M.2 Board	Platform Board	End2End	M.2 Board	Platform Board	End2End
	[mil/mm]	[mil/mm]	[mil/mm]	[mil/mm]	[mil/mm]	[mil/mm]	[mil/mm]
CNVio Gen1 (JfP)	96/2.4	12/0.3	40/1	52/1.3	**81/2**	40/1	**121/3**
CNVio Gen2 (HrP)	240/6.1	12/0.3	80/2	92/2.3	81/2	80/2	161/4.1

Table 9-11 CNVio recommended parameters

Parameter	Value	Comment
Differential pair length matching	0.02UI For 1280M: <80 mil	This parameter may effect EMI and RFI
Characteristic impedance	85 ohm differential	50 ohm to ground for each trace
Maximum length	10 inch	9 inch from M.2 connector pins to SoC pins
Maximum resistance	5 ohm	50 ohm to ground for each trace
Shielding	Berried microstrip (Stripline)	Recommended for minimizing EMI/RFI
Delay matching between pairs of the same direction	Better than 80 mil	Including the two lanes and the clock in every direction
Vias	Minimize usage	Recommended to avoid Via connections as much as possible and follow differential
BER	1E-12	Standard PHY bit error rate for a CNVio lane

9.13.2 RGI and BRI signals

These are GPIO signals (1.8V) running between the SoC and the RF companion module. The BRI and RGI signals share the same traces as UART signals (for Discrete). Since the UART baud rate is expected to be lower than the BRI/RGI toggle rate, it can be assumed the BRI/RGI sets the requirements for this bus. BRI and RGI are two bi-directional busses. These signals have slew-rate controlled I/Os on both ends (SoC and RF companion), which should be optimized to minimize EMI/RFI while maintaining good signal waveform. No special control impedance is needed. The BRI and RGI packets are protected by error correction coding and with standard routing and signal integrity practices applied, no errors are expected to be noticed on the busses.

Note:

- The directions of the signals are set by the CNVi/SoC/PCH side.
- RGI/BRI_DT is the Tx side from the SoC to the CRF (so it is an Output signal on the SoC and Input signal on the CRF).
- RGI/BRI_RSP is the Rx side at the SoC from the CRF (so it is an Input signal on the SoC and Output signal on the CRF).

- It is recommended to not use the GPIOs that are mapped to these signals for any Boot-Stepping function without considering the electrical behavior of this signal. (See Section 1).
- The RGI-BRI bus frequency is double the xTal used on the CNVi side. So for current PCH cases, it uses a 38.4MHz xTal so operates in the frequency of 76.8MHz.
- Notice that the RGI/BRI signals are GPIOs from the PCH, as so they can be impacted by BIOS settings to the GPIOs (e.g. impact the Rise-Fall time of the signals) see the Product EPS for mode details.

9.13.3 38.4M reference clock signal (JfP+Pulsar only)

This section is relevant only in the Pulsar+JfP case ONLY , and is **not relevant** to ICL/TGL/JPL or any other Quasar-based systems.

One more comment – in CML Platform the CML-ES is planned to be out with Pulsar in it, as in WHL. This means that CML-ES will work with JfP only and the CML-ES Platform require to KEEP this shared clk line (M.2 Pin 64) in place. In CML-QS that will have Quasar in it this line is not needed anymore.

Ref Clock is a 38.4M clock signal which is generated by the RF companion module and sent to the SoC. This clock can be used as the SoC main clock (in clock sharing configuration) or as the Pulsar clock (in non-clock sharing configuration). When using the latter option, the SoC should have another clock for its operation, but Pulsar (within the SoC) will always get the 38.4M clock coming from the Companion RF.

The clock signal is a 1V nominal, 10Kohm typical resistive load with 35pF load capacitance.

It is recommended to route the clock with special care while maintaining clock routing practices, preferably as a microstrip, to minimize EMI/RFI and susceptibility to noise.

Quasar does not support such shared clk flows, and in HrP this signal was disconnected from the M.2 module.

The routing guideline should refer to 567247-glk-pdg Table 17-4. CNVi Clock Input Signal with M.2 Connector Routing Guideline.

9.13.4 Wi-Fi/BT/LTE coexistence signals

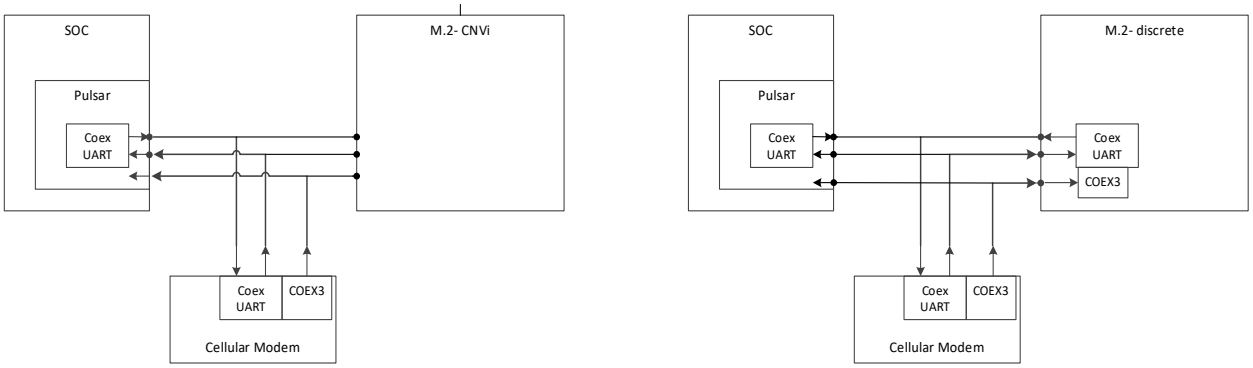
In order to allow a Hybrid Key-E scheme supporting both connectivity and a cellular modem, there is a need to connect the modem coexistence bus in a configuration that will allow the modem to connect to the connectivity coexistence control logic. In Intel connectivity modules, this logic may reside in the M.2 module or in the SoC, depending on whether the CNVi or discrete solutions are used:

- For CNVi, the logic which is connected to the coexistence bus resides in Pulsar, which is part of the SoC.
- For discrete M.2 cards, this logic resides in the module.

As a result, when a motherboard design contains a modem, and it is desired to be able to support CNVi and Discrete on the same M.2 socket, there is a need to have a 3-way connection of the board, as shown in Figure 9–10. In this diagram, the red lines represent lines that are unused in each connection scenario. One can simplify the routing by adding a jumper resistor to select between the two configurations; however, this will result in losing the option to swap between CNVi and Discrete on the board. Any such swapping will then require a board HW change for changing the jumper resistor position.

Note that when doing this 3-way connection between SoC, M.2, and the modem, there will always be an unused signal that is not optimally terminated for that connection. This signal is shown in red in the connection diagram. The effect of this signal is similar to a stub that adds undesired impedance change to the trace. The effect of this stub on the UART bus depends on several system parameters: distance between the different UART pins, UART bus speed, and the electrical characteristics of the UART drivers and receivers (referenced to the signal pins). This effect must be considered and analyzed through design practices or simulations to ensure that signal integrity is not compromised. For this analysis, the UART baud rate shall be assumed to be not higher than 4Mbaud.

Figure 9–10 Coexistence UART for connectivity/modem 3-way configuration



Notice this is hardware readiness infrastructure for such CoEx ability, still require future firmware implementation and integration in order to commit and operate it, and depends on potential Platform use case needs.

9.14 Connectivity module power control (CNVi/Discrete)

When designing the platform for CNVi, it is recommended to either not have this switch in the design, or to hard-wire it to be always-on by following the PCH (ON when the PCH is ON). This is because the operation of the RF companion module does not allow switching off its main power in any system state where the PCH is powered on, in order to maintain synchronization with the at all times.

Refer to **Ref 2** for information on the correct usage of Load Switch (573970 – *Using a Load Switch for Intel CNVi Designs White Paper*).

Note that the power supply to the M.2 module is connected directly to the platform V3.3A rail without having any controlled power switch on the line. This ensures that the CNVi will be powered early in the platform power-up process as required by the CNVi power up sequencing. Note that CNVi does not support wake-on-WLAN/BT during deep system sleep states (DSx). Connecting the CRF to 3.3V_DSW rail is not specifically recommended; since the PCH rails needed for CNVi will be powered off in the deep-system-sleep state, getting out of DSx requires the CNVi, in the PCH, to Boot, Cold-Boot, in any case, so there is no real value in having the CRF on 3.3V_DSW.

Note also that the CRF module was designed with low-leakage power, and so therefore does not require any external power control to be used during normal operation.

9.15 Wi-Fi wireless disable and RF-Kill (CNVi/Discrete)

W_DISABLE1# (pin 56 in M.2 2230 pinout, pin 28 in M.2 1216 SD pinout) serves as HW RF-Kill for the Wi-Fi radio. The pin is recommended to be left unconnected if, and only if, the HW RF-Kill signal is not required.

Asserting the W_DISABLE#_1 signal will result in a complete shutdown of the RF of the Wi-Fi part. The result from the user perspective is similar to that of disabling the Wi-Fi device from the laptop. Note that HW RF-Kill is part of the spec of the M.2 modules.

On some platforms this signal is also mapped as a PCH GPIO; if so, it is recommended to not use the GPIO that is mapped to this signal for any Boot-Stepping function without considering the electrical behavior of this signal. (See Section 9.11.)

9.16 M.2 Bluetooth® HW RF-Kill (CNVi/Discrete)

W_DISABLE2# (pin 54 in M.2 2230 pinout, pin 63 in M.2 1216 SD pinout) serves as HW RF-Kill for the Bluetooth radio.

Asserting W_DISABLE#_2 signal will result in a complete shutdown of the Bluetooth part. The result from the user perspective is similar to that of removing the Bluetooth device from the platform.

It is recommended to not use the GPIO that is mapped to this signal for any Boot-Stepping function without considering the electrical behavior of this signal. (See Section 9.11.)

9.17 Power supply de-coupling (CNVi/Discrete)

It is required to have decoupling caps on the power feeds in each end of the connector.

- 10uF+0.1uF+0.01uF at one end of socket in support of 3.3 V pins 2 and 4 (in 2230 modules) or pins 4 and 5 (in 1216 modules)
- 10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V pins 72 and 74 (in 2230 modules) or pin 72 and 73 (in 1216 modules)

9.18 A4WP issues (CNVi/Discrete)

Although A4WP is not supported in ICL/CML/TGL, and the dedicated signals between the PCH and the M.2 are not used, there are still platforms with this internal signal that gets into the PCH, and then to the CNVi IP (GPP_F_19/23 – A4WP_PRESENT), that indicates A4WP enablement. Apparently, this GPIO signal functionality was supposed to be fused, and disabled, but it was not. So, this signal might either be used by other means and/or be floating, and therefore sometimes get a value of "1," and thereby impact the BT in our module, keeping it ON.

For this we specifically recommend:

1) Not to use this GPIO – assuming starting from TGL it will be removed from the Platform level.
2) Add a PD on it at the Platform level for ICL- and CML-based platforms, and as needed in CNL/CFL.

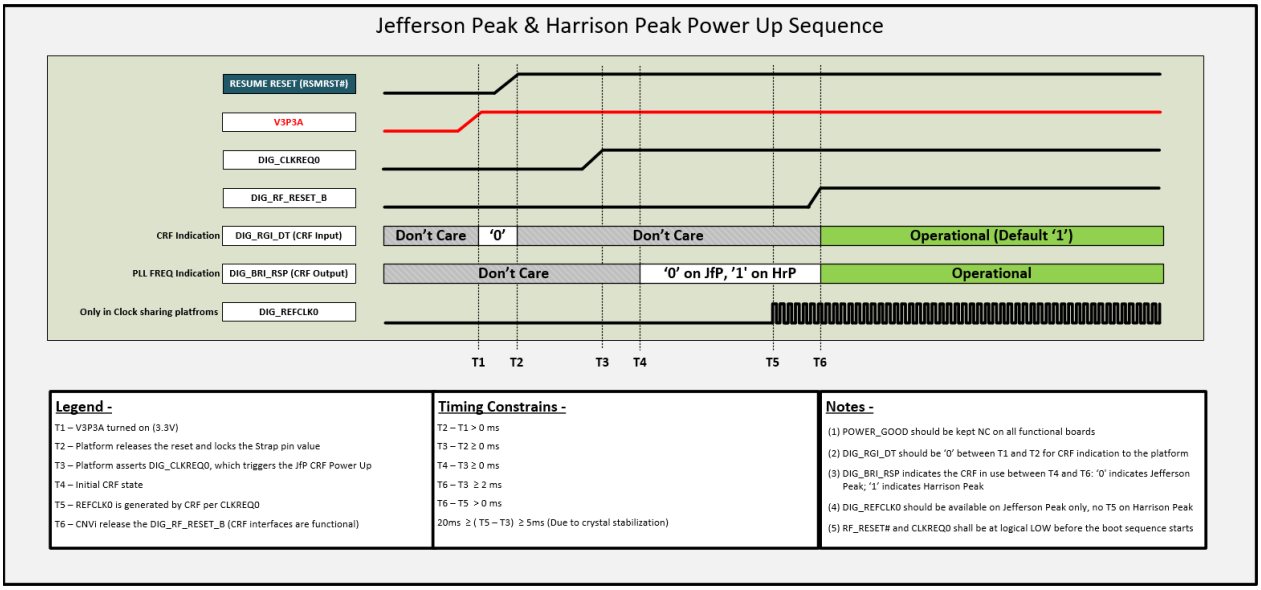
9.19 BIOS (CNVi/Discrete)

The CNVi modules (including Jefferson/Harrison Peak) require specific BIOS support. A full description of BIOS support needed for the Cannon Lake and Gemini Lake platforms can be found in the Connectivity BIOS Guide documents.

See the checklist in Section 12.

9.20 Power-up sequence (CNVi)

Figure 9–11 Power-up sequence



Note: One small clarification: BRI_RSP has a weak PU (on the CNVi side), so once the V3P3A is up, it will get to "1", which means that T4 will be hard to identify (and not really needed); this also means that prior to T4, the "Don't care" period of the BRI_RSP will be actually "1" – but is still "Don't care."

9.21 Discrete Module Platform design guidelines (Discrete)

This section includes several important implementation aspects the OEM should take into consideration when implementing a platform that would accommodate this product.

9.21.1 Socket 1 mechanical key options

Socket 1 has two options: Key E and Key A. Each key with different supported list of I/Fs as defined in the M.2 specification.

In general the different Keys should be used in the following cases:

- **Key E** – when UART/I2S for BT is required.

It is possible to have a single-motherboard design that supports either of these options, and select between them using resistor assembly options.

9.21.2 Signal connection pitfalls

- The OEM should make sure to follow the M.2 definitions of signal names and directions (I/O TX/Rx etc.) and avoid confusion between platform side and device side.
- Note that some lines are bidirectional, such as PCIe CLKREQ, PEWAKE.

9.21.3 Pullups and pulldowns

The OEM should apply pullups and pulldowns in the platform side according to Table 9–14.

Table 9-12 Socket 1 pullups and pulldowns

I/F	Signals	PU/PD Guideline	Rationale
W_Disable#		PU	May be required by M.2 cards; in Intel Wireless products there is already a PU at the silicon level
A4WP_PRESENT	A4WP_PRESENT	PD	Mapped as PCH-GPIO (GPP_F_19/23) depend on the platform/PCH
PCIe	PEWAKE#	PU	Open drain, required by M.2
	CLKREQ#	PU	Open drain, required by M.2
	PERST#	PD	Required by Intel platform design guidelines
	Other PCIe signals	None	PCIe spec

The OEM must avoid using PU/PD when not needed or when required not to be used. Unless this rule is followed, it would result in a back-bias condition, in which the IO is getting voltage before the device side is ready for it.

9.21.4 IO connection scenarios and best practices

The motherboard designer should address the following requirements for the sake of avoiding failsafe problems, reducing unneeded leakage and for following best practice design rules:

- Level-shifter back-bias prevention
  - Level shifter shall not set value in A side when not getting voltage in B side.
    - **Rationale:** Prevent back-bias and wrong logic condition.
  - Level shifters shall be back-bias protected.
    - **Rationale:** The level shifter is often supplied with a different supply than the IO connected to it. During ramp up/down states there might be back-bias scenario.

9.21.5 I/F specific guidelines

9.21.5.1 PCIe

- The product is using PCIe interface for Wi-Fi. Although each core is using a dedicated PCIe interface, in certain conditions some of the PCIe signals can be shared.
  - CLK_REQ# is required not to be shared, but is point-to-point.
    - This is because CLK_REQ# is being used for PCIe link management, which is done for each PCIe device independently.

- PESRT# and PEWAKE# are used for D3 flows.
  - PERST# cannot be shared in case there is a need to put only specific PCIe device in reset. But as explained below there is no such scenario.
  - PEWAKE# cannot be shared in case there is a need to identify the wake source from specific PCIe device.
  - Connected standby flows are using RTD3hot. RTD3hot is not using PERST#, and not using PEWAKE#
  - In this case the PEWAKE# can be shared. As example Wi-Fi PEWAKE# and WiGig PEWAKE# can be a single WAKE# signal
  - Also PERST# signal can be shared. As example Wi-Fi PERST# and WiGig PERST# can be a single PERST# signal.
  - Non-connected standby flows are using D3cold. D3cold is using PERST# and PEWAKE#.
- In S3-5 the platform puts all the devices to D3cold, and will assert PERST# to all of them, as a result PERST# can be shared.
- Wi-Fi core can still be kept active in D3, but in that case, since it is D3cold, Wi-Fi will ignore PERST# even if it puts Wi-Fi into PCIe reset.
- Wi-Fi core can wake the system using PEWAKE# and there is added value in non-CS platforms to have dedicated PEWAKE# signals, but it is not mandatory.
- To conclude, even in non-connected standby flows the signals can be shared.

9.21.6 Connectivity module power control

The platform designer has the following options for controlling the power rail of the connectivity module:

- Connect directly to the rail +3.3A ***(recommended option; applies to platform design for both CNVi/CNVd)***:
  - The device will be on as long as the rail provides power.
  - This option removes the need to use a power switch, and minimizes connectivity module power leakage in the relevant platform states.
- Connect to rail DSW or +3.3VA through a power switch and control the switch using SLP_WLAN controlling signal ***(applies to platform design for CNVd only)***:
  - The SLP_WLAN signal will keep the connectivity awake when needed, and turn it off when not needed.
  - For example, if ME in Sx is not used, and wake on WLAN in Sx is not used, then connectivity can be turned off.

9.21.7 Power feed

It is required to have decoupling caps on the power feeds in each end of the connector.

10uF+0.1uF+0.01uF at one end of socket in support of 3.3 V3V pins 2 and 4.

10uF+0.1uF+0.01uF at the other end of the socket in support of 3.3 V3V pins 72 and 74.

9.21.8 BIOS

The customer will need to apply the relevant CNV BIOS objects and methods, along with their appropriate settings, according to the device in use. Wrong values in the BIOS will result in unexpected behavior and degraded performance.

Specific details can be found in the *Platform CNV BIOS SAS*, provided as an external documentation.

9.22 PCIe host interface errata (Discrete)

This section includes several important implementation aspects about PCIe host interface. The platform designer should take these items into account as part of the platform design.

9.22.1 Squelch detect mechanism

The Squelch (SQ) detect mechanism may not consistently identify PCH wake signaling (TS1 symbols) as valid above SQ Max threshold of 175 mV, as defined in the PCIe spec.

It is important to follow proper platform design and layout guidelines as defined in the PCIe CEM specification to ensure PCH wake signaling (Electrical Idle Detect Threshold - *Vrx-idle-det-diff-p-p* parameter) in the range of:

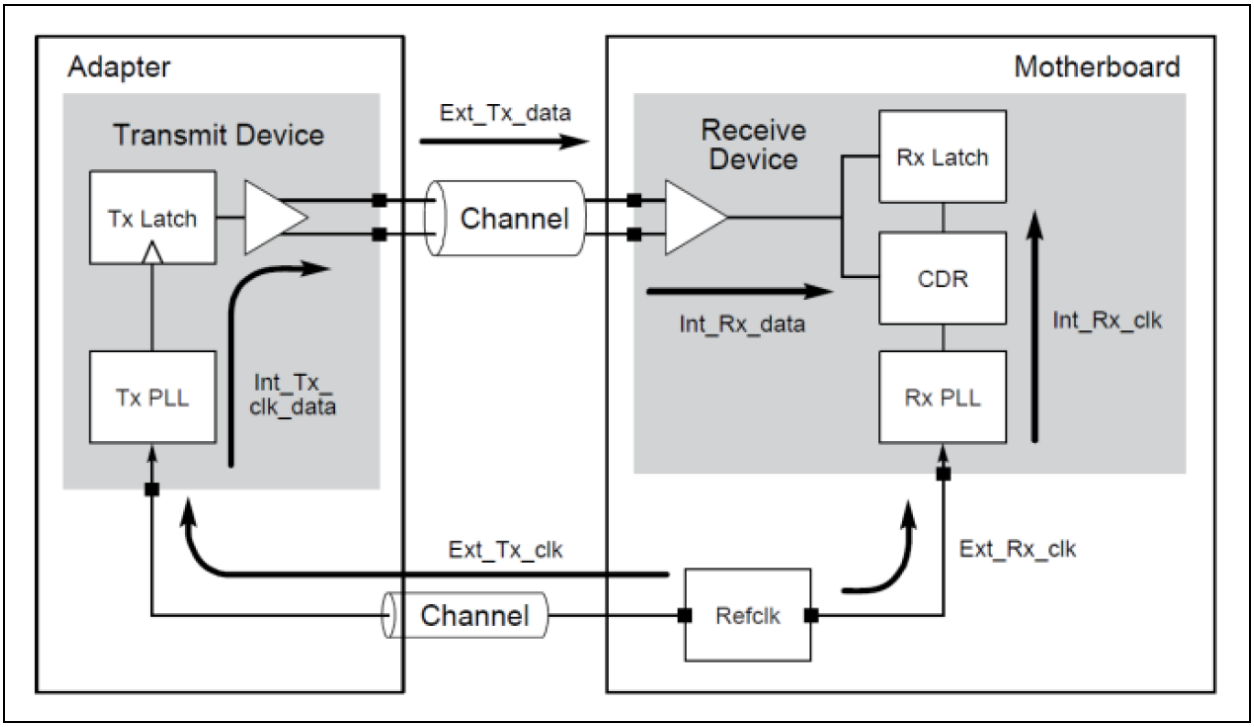
- 65 mV to 280 mV

Customers should design/plan appropriately for all adapters that may be used in a given platform.

9.22.2 Common clock configuration

PCIe on both the platform side (PCH) and WLAN side must operate using a common clock configuration. Both PCH and WLAN are configured for this by default (bit 6 is set in registers 0x50 and 0xF0). From a hardware perspective, the same reference clock (Refclk) must be used for both PCH and Wi-Fi card, as shown in Figure 9–12.

Figure 9–12 PCIe common clock configuration



Source: PCI Express Rev 2.0 specification (*PCI_Express_Base_Rev_2.0_20Dec06a*, Figure 4-50)

9.22.3 Enabling PCIe controllers with ASPM

ASPM defines the L states of the PCIe connections, L0, L0s, L1 and L2.

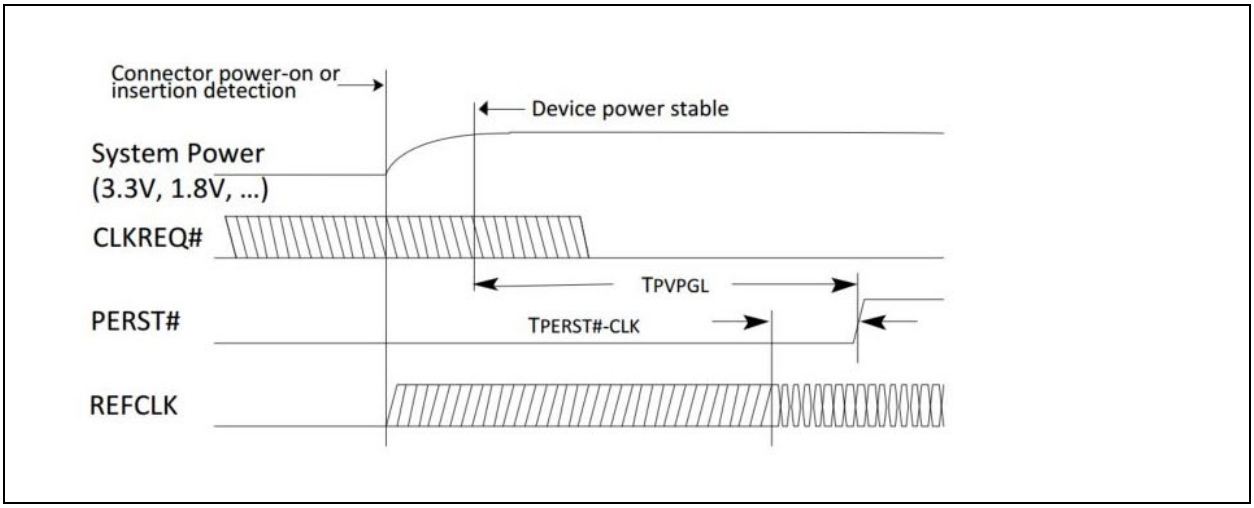
The device supports L1 state, and does not support L0s. This is in order to benefit from the power saving that is achieved with L1 state, while avoiding platform integration complexity which is involved with using L0s state.

The device supports ASPM optionality ECN, allowing support of L1 without L0s. Therefore, there is no need for special BIOS actions as with previous Intel's wireless products.

9.22.4 CLKREQ# timing

Latest PCIe M.2 spec do not specify a constraint on when PCIe device should assert CLKREQ# after *Power Valid* (which is the point where the V3.3 rail reached nominal level). See below timing diagram Figure 9–13 and timing tables Table 9–15 taken from PCI M.2 spec and as can be seen, CLKREQ# assertion timing is not defined.

Figure 9–13 PCIe CLKREQ# timing



Source: M.2 specification

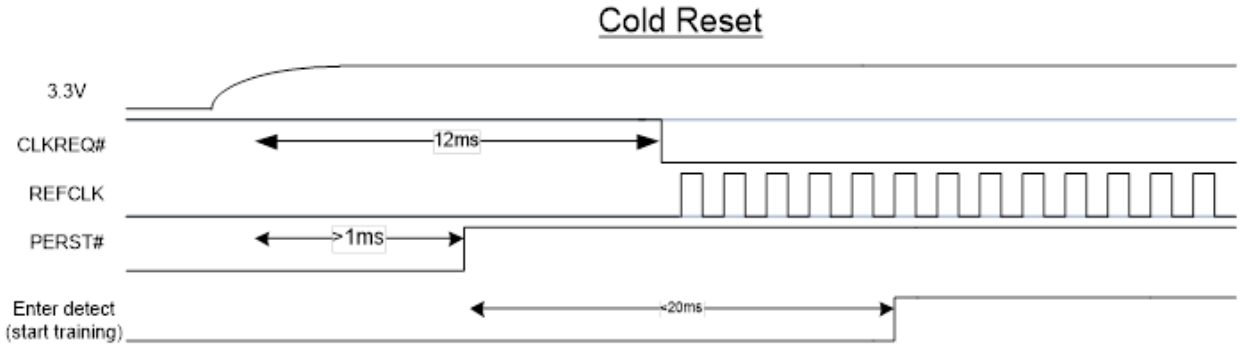
Table 9-13 Power-up CLKREQ# timing

Symbol	Parameter	Min	Max	Units
T_{PVPGL}	Power valid to PERST# Input active	Implementation specific; recommended 50mS		ms
$T_{PERST\#-CLK}$	REFCLK stable before PERST# inactive	100		µs

The timing of CLKREQ# is not defined, but iti s required that the device will enter DETECT state within 20ms of PERST# de-assertion.

Cyclone Peak asserts CLKREQ# within12ms from power valid as shown in Figure 9–14. Cyclone Peak complies with the requirement to enter DETECT within 20ms of PERST# de-assertion.

Figure 9–14 Cyclone Peak 2 PCIe CLKREQ# timing



9.22.5 PERST# rise-time timing

The PERST# signal rise time needs to meet the limitations listed in Table 9–16. This guarantees robust out-of-reset flow of the device and better immunity to noise that can be carried by this signal. In addition, it is required that this signal rise in a monotonic way and avoid a step-like rise.

Table 9-14 PERST# rise-time

PERST# Rise Time		
Parameter	**Intel® Wireless Devices**	
	Stone Peak **Sandy Peak**	**Snowfield Peak** **Windstorm Peak** **Thunder Peak** **Cyclone Peak**
PERST# Rise Time	< 20 nSec Monotonic rise	< 150 nSec Monotonic rise
PERST# Ripple/Glitch During Rise Time	< 50 mV glitch during the rise time phase	< 100 mV glitch during the rise time phase

9.22.6 PCI setting for Gen2 and De-emphasis

Some platforms experienced difficulties enumerating the Wi-Fi device after warm boot. The cause of this issue is the ability to choose the right PCI interface speed (Gen1/2). A workaround for this issue is to disable the PCI De-emphasis option in the BIOS and set speed to Gen2.

1. De-emphasis disabled.
2. Speed – AUTO (to allow Gen2 speed).

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10 Product IDs (CNVi/Discrete)

These IDs are the PCIe IDs and USB IDs.

10.1 Debug combinations

Table 10-1 Debug combinations

Product	Wi-Fi Model Number (Product Code)	Wi-Fi PCI Vendor ID	Quasar Type	Wi-Fi PCI Device ID	Wi-Fi PCI Sub Vendor ID	Wi-Fi PCI Subsystem ID	HW String in INF	BUS Vendor ID	BUS Product ID
Harrison Peak Wi-Fi+BT CRF 2230	22560.NGW – NO OTP	8086	QnJ	2720	8086	0000	PCI\VEN_8086&DEV_2720&SUBSYS_80860000	8087	0026
	22560.NGW	8086	QnJ	2720	8086	0070	PCI\VEN_8086&DEV_2720&SUBSYS_80860070	8087	0026
Harrison Peak Wi-Fi+BT CRF 2230 – CoB	22560.NGW – CoB	8086	QnJ	2720	8086	0070	PCI\VEN_8086&DEV_2720&SUBSYS_80860070	8087	0026
HrP 1216 LTE COEX	22560.D2W – LTE	8086	QnJ	2720	8086	0078	PCI\VEN_8086&DEV_2720&SUBSYS_80860078	8087	0026
HrP 1216 MS (No COEX)	22560.D2W	8086	QnJ	2720	8086	0070	PCI\VEN_8086&DEV_2720&SUBSYS_80860070	8087	0026

10.2 Platform combinations

Table 10-2 Platform combinations

Product	Wi-Fi Model Number (Product Code)	Wi-Fi PCI Vendor ID	Quasar Type/ Platform	Wi-Fi PCI Device ID	Wi-Fi PCI Sub Vendor ID	Wi-Fi PCI Sub system ID	HW String in INF (example with ICL-LP and TGL-LP)	BUS Vendor ID	BUS Product ID
Harison Peak Wi-Fi+BT CRF 2230 – CoB	201.NGW	8086	Ice Lake, Tiger Lake LP, CML LP, CML H	34F0,A0F0, 02F0, 06F0	8086	0070	PCI\VEN_8086&DEV_34F0,A0F0&SUBSYS_80860070	8087	0026
	201.NGW – CoB	8086	Ice Lake, Tiger Lake LP, CML LP, CML H	34F0,A0F0, 02F0, 06F0	8086	0070	PCI\VEN_8086&DEV_34F0,A0F0&SUBSYS_80860070	8087	0026
HrP 1216 LTE COEX	201D2W – LTE	8086	Ice Lake, Tiger Lake LP, CML LP, CML H	34F0,A0F0, 02F0, 06F0	8086	0078	PCI\VEN_8086&DEV_34F0,A0F0&SUBSYS_80860078	8087	0026
HrP 1216 MS (No COEX)	201.D2W	8086	Ice Lake, Tiger Lake LP, CML LP, CML H	34F0,A0F0, 02F0, 06F0	8086	0070	PCI\VEN_8086&DEV_34F0,A0F0&SUBSYS_80860070	8087	0026
	201.D2W .NV	8086	Ice Lake, Tiger Lake LP, CML LP, CML H	34F0,A0F0, 02F0, 06F0	8086	0074	PCI\VEN_8086&DEV_2720,34F0,A0F0,43F0,02F0,06F0&SUBSYS_80860074	8087	0026

NOTES:

- The Device ID values above assume the use of PCH-LP (:ICL-LP 34F0; TGL-LP A0F0, CML-LP 02F0).
- When using PCH-H the value will change to :ICL-H 3DF0; TGL-H 43F0; CML-H 06F0.
- For ICL-N (used in JPL), the value will be 38F0 (and may still be changed).

10.3 Silicon internal IDs (for debug needs)

Table 10-3 Silicon internal IDs

Chip Variant	Register	Address	Value	Comment
Harrison Peak	CNVR_AUX_MISC_CHIP_ID	0x0000b800	A0:0x00000504 B0: 0x01000504 B3: 0x01300504	Flavor[31..28];Step[27..24];Dash[23..20];reserved[19..12];type[11..0]
Harrison Peak	REG_SYS_RO_LGC_IDBUFFS_0 (WIFI RF IDBUFF)	A0:0x00ad04dc B3=B0:0x00ad04a0	A0: 0x0010A000 B3=B0: 0x0010A100	
QuasarB (ICP/ TGP-Z0)	CNVI_AUX_MISC_CHIP	0x000000b0	A0: 0x00000300 B0: 0x01000300 C0=D0: 0x02000300	Flavor[31..28];Step[27..24];Dash[23..20];reserved[19..12];type[11..0]
QuasarZ (CMP/TGP/ JPL-PCH	CNVI_AUX_MISC_CHIP	0x000000b0	0x20000302	Flavor[31..28];Step[27..24];Dash[23..20];reserved[19..12];type[11..0]
QnJ	CNVI_AUX_MISC_CHIP	0x000000b0	A0:0x00000506 A1:0x00100506	Flavor[31..28];Step[27..24];Dash[23..20];reserved[19..12];type[11..0]

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11 GPIO Signals Mapping (CNVi)

Table 11-1 GPIO signals mapping

ICL CNVI Control		Refer to Section 30.2, **Ref 3**

PCH-LP

Function	GPIO	BIOS Configuration
CNV_BRI_DT	GPP_F0	Native F1
CNV_BRI_RSP	GPP_F1	Native F1
CNV_RGI_DT	GPP_F2	Native F1
CNV_RGI_RSP	GPP_F3	Native F1
CNV_RF_RESET	GPP A8* / GPP_F4	Native F2 / F1
MODEM_CLKREQ	GPP_A9* / GPP_F5	Native F2 / F2

*Default

PCH-H-TBD

From Legacy platform (for reference needs), and for CML Platform:

Legacy CNL CNVI Control	Refer to Section 30.2, **Ref 3**

PCH-LP

Function	GPIO	BIOS Configuration
CNV_BRI_DT	GPP_F4	Native F1
CNV_BRI_RSP	GPP_F5	Native F1
CNV_RGI_DT	GPP_F6	Native F1
CNV_RGI_RSP	GPP_F7	Native F1
CNV_RF_RESET	GPP_H1	Native F3
MODEM_CLKREQ	GPP_H2	Native F3
Power	GPPH	1.8V

Legacy GML CNVI Control	Refer to Section 29.2, **Ref 4**

PCH-H

Function	GPIO	BIOS Configuration
CNV_BRI_DT	GPP_J4	Native F1
CNV_BRI_RSP	GPP_J5	Native F1
CNV_RGI_DT	GPP_J6	Native F1
CNV_RGI_RSP	GPP_J7	Native F1
CNV_RF_RESET	GPP_D5	Native F3
MODEM_CLKREQ	GPP_D6	Native F3
Power	GPPD	1.8V

SoC

Function	GPIO	BIOS Configuration
CNV_BRI_DT	GPIO_191	Native F1
CNV_BRI_RSP	GPIO_192	Native F1
CNV_RGI_DT	GPIO_193	Native F1
CNV_RGI_RSP	GPIO_194	Native F1
CNV_RF_RESET	GPIO_195	Native F1
MODEM_CLKREQ	GPIO_196	Native F1

JPL-N CNVI Control	Refer to Section 30.2,

PCH-LP

Function	GPIO
CNV_BRI_DT	GPPC_E_20
CNV_BRI_RSP	GPPC_E_21
CNV_RGI_DT	GPPC_E_22
CNV_RGI_RSP	GPPC_E_23
CNV_RF_RESET	GPP_F_4
MODEM_CLKREQ	GPPC_H_13

Additionally, there are more Dynamic GPIO settings per platform design.

For Intel's ICL RVP, the Signal-GPIO mapping is listed in Table 11–2.

Table 11-2 Virtual GPIOs

GPPC_H_19	O	UART_BT_WAKE output. Optional to connect to BT Wake on the Bluetooth® module. This is the recommended GPIO, but other GPIOs can be selected for this function. For Discrete mode, the GPPC_H19 is used for BT over UART wake. For integrated, it is Virtual GPIO: vGPIO_4 BUT this signal is actually not planned to be used.
GPPC_B_18	O	BT_KILL output. Optional to connect to a BT KILL pin on the Bluetooth module. This is the recommended GPIO but other GPIOs can be selected for this function. Optional to be used in both Discrete and integrated options. GPPC_B18 was assigned originally for BT RF KILL. It is recommended to not use the GPIO that is mapped to this signal for any Boot-Stepping function without considering the electrical behavior of this signal. (See Section 9.11).

GPPC_B_16	O	For CNVi: Unused Wi-Fi PCIe host wake output for standard CNV. Optional to connect to a WLAN PCIe host wake pin on the Wi-Fi module. This is the recommended GPIO but other GPIOs can be selected for this function. In the Intel ICL RVP with ICP-LP, it seems that the GPPC_B_16 is used for the PCIe Wake GPIO.
GPPC_B_15	O	WLAN_KILL output. Optional to connect to a WLAN KILL pin on the Wi-Fi module. This is the recommended GPIO but other GPIOs can be selected for this function. Optional to be used in both Discrete and integrated options. GPPC_B15 was assigned originally for Wi-Fi RF KILL in Intel ICL RVP with ICP-LP It is recommended to not use the GPIO that is mapped to this signal for any Boot-Stepping function without considering the electrical behavior of this signal. (See Section 9.11).

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12 BIOS-related Settings/Features Checklist (CNVi/Discrete)

12.1 Platform dependency

Table 12–1 provides a summary of the required BIOS capabilities relevant for each platform in the 2015–2017 portfolio, and indicates whether each capability is relevant to the discrete solution only, to the integrated solution only, or to both discrete and integrated solutions.

Table 12-1 Required BIOS capabilities

Feature/Core Specific	Feature/Capability	CNL/ CFL	GLK	ICL	Core Boot	UEFI Variable For CNL/CFL/ICL	Discrete/ Integrated/ Both
Thermal Management	Wi-Fi SPLC	✓	✓	✓	✓	✓	Both
	PSM- Power Sharing Manager	✓	×	✓	×	×	Both
Regulatory	WRDD – Domain settings	✓	✓	✓	✓	✓	Both
	WRDS – Static Wi-Fi SAR	✓	✓	✓	✓	✓	Both
	BRDS – Static BT SAR	✓	✓	✓	✓	✓	Both
	EWRD – Dynamic SAR	✓	✓	✓	×	✓ (no driver support)	Both
	WGDS – Geo awareness SAR	✓	✓	✓	×	✓	Both
Cross Cores	PCIe L1 Sub states	✓	✓	✓	✓	×	Discrete
	CNVi/Discrete Mode Selection	✓	✓	✓	✓	×	Both
	Native PCIe	✓	✓	✓	✓	×	Discrete
	PCIe ASPM Control	✓	✓	✓	✓	×	Discrete
	PME Wake Support	✓	✓	✓	✓	×	Both
	RTD3 Support	✓	✓	✓	✓	×	Discrete
	Conditional Sx Wake	×	✓	×	×	×	Integrated
	PEP Constraint	✓	✓	✓	✓	×	Both
	PCIe T-Power-On	✓	✓	✓	✓	×	Discrete
	SADS – Switched Antenna Diversity Selection	✓	✓	✓	×	✓	Both
	GPC- General Purpose Configuration	✓	×	✓	×	✓	Both
Wi-Fi Specific	WAND -Wireless Antenna Diversity	✓	✓	✓	×	×	Both
	Wlan Sleep (Wake on WLAN)	✓	✓	✓	✓	×	Both
	WLAN PLDR Support	✓	✓	✓	×	×	Both
BT Specific	BT Device Select	✓	✓	✓	✓	×	Both
	Bluetooth USB port	✓	✓	✓	✓	×	Both
	BT RTD3 Control	✓	✓	✓	✓	×	Both

Feature/Core Specific	Feature/Capability	CNL/ CFL	GLK	ICL	Core Boot	UEFI Variable For CNL/CFL/ICL	Discrete/ Integrated/ Both
	BT Power states	✓	✓	✓	✓	×	Both
	Audio Offload	×	×	✓	×	×	Integrated

Details on the remaining Wireless connectivity BIOS settings can be found in ***Ref 5***.

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