



HMT89 Series Open Hardware Design

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1 Introduction

The Open solution of the module enables it to function as the primary processor. The continuous advancements in communication technologies and evolving market demands further emphasize its advantages. This solution offers the following benefits:

- **Accelerate embedded application development:** Streamline the development process and significantly reduce the product R&D cycle.
- **Simplify circuit and hardware design:** Minimize complexity in design, leading to lower engineering costs.
- **Miniaturize product:** Achieve a more compact product design.
- **Reduce power consumption:** Enhance energy efficiency for longer battery life and lower operational costs.
- **Implement OTA (Over-the-Air) technology:** Facilitate seamless firmware updates and remote management.
- **Boost product competitiveness and cost-effectiveness:** Improve market positioning and overall value proposition.

The document defines the HMT89 series module itself in Open solution, its air interfaces and hardware interfaces which are connected to your applications. This document can help you quickly understand interface specifications, RF characteristics, electrical and mechanical details, as well as other information of the module.

1.1. Text Conventions

Table 1: Text Conventions

dev	Unless stated otherwise, the presence of the mark "dev" following a function, feature, interface, pin name, command, argument, etc., signifies that it is still in the development phase and not yet supported. Additionally, when "dev" appears after a model, it indicates that the model sample is currently unavailable.
NOTE	"NOTE" is used to identify important information. When you see "NOTE" in this document, please be aware that the information contained therein may be crucial for understanding, implementing, or operating related technologies or steps. We strongly recommend that you pay special attention to these "NOTE" sections while reading the document to ensure that you can use this technical documentation correctly and efficiently.
[...]	Brackets ([...]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO_DATA pins, SDIO_DATA0, SDIO_DATA1, SDIO_DATA2 and SDIO_DATA3.

2 Product Overview

The module is an SMD module with compact packaging, which is engineered to meet most of the demands of M2M applications.

HMT89 is a series of industrial-grade modules for industrial and commercial applications only.

[Table 2: Basic Information](#)

HMT89 Series	
Packaging type	LGA
Pin counts	570
Dimensions	(44.0 ±0.20) mm × (53.0 ±0.20) mm × (2.95 ±0.20) mm
Weight	HMT89-LD: approx.16.86 g HMT89-EPV: approx.16.82 g
Models	HMT89-LD, HMT89-EPV

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

	HMT89-LD	HMT89-EPV
5G NR SA	n2/n5/n7/n12/n13/n14/n25/ n26/n29/n30/n38/n41/n48/ n66/n70/n71/n77/n78	n1/n3/n5/n7/n8/n20/n28/n38/ n40/n41/n75/n76/n77/n78
5G NR NSA	n2/n5/n7/n12/n13/n14/n25/ n26/n29/n30/n38/n41/n48/ n66/n70/n71/n77/n78	n1/n3/n5/n7/n8/n20/n28/n38/ n40/n41/n75/n76/n77/n78
LTE-FDD	B2/B4/B5/B7/B12 (B17)/ B13/B14/B25/B26/B29/B30/ B66/B70/B71	B1/B3/B5/B7/B8/B20/B28/B32
LTE-TDD	B38/B41/B42/B43/B48/B46 (LAA)	B38/B40/B41/B42/B43
WCDMA	-	B1/B5/B8
GNSS	L1 + L5	L1 + L5 (optional)

2.2. Key Features

Table 4: Key Features

Category	Description
Supply Voltage	● 3.3–4.4 V ● Typ.: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: (U)SIM card by default
(U)SIM Interface	1.8 V and 3.0 V
Audio Features	Two digital audio interfaces: PCM
PCM Interface	● Two PCM interfaces ● Used for audio data transmission between the module and the external SLIC ● Long and short frame synchronization ● Master and slave modes (but must be in master mode for long frame synchronization)
SPI Interface	● Three SPI interfaces ● Master and slave modes ● 1.8 V voltage domain ● Clock rate: up to 52 MHz
I2C Interface	Four I2C interfaces
USXGMII Interface	● 100 Mbps, 1000 Mbps, 2500 Mbps, 5000 Mbps and 10000 Mbps Ethernet connection in full duplex mode ● IEEE 802.3x compliant ● Max. data rates: - DL: 10 Gbps - UL: 10 Gbps
USB Interface	● Complies with USB 3.2 Gen 2 specification ● Data rates: - USB 3.2 Gen 2: up to 10 Gbps - USB 2.0: up to 480 Mbps ● Use: AT command communication, data transmission, software debugging and firmware upgrade ● USB serial drivers for USB drivers under Windows 8.1/10/11
SDIO Interface	● Use: SD card application, Wi-Fi application and wireless connection ● Complies with SD 3.0 protocol
UART	Main UART: ● Use: AT command communication and data transmission ● Baud rate: 115200 bps ● RTS and CTS hardware flow control Debug UART: ● Use: Linux console and log output ● Baud rate: 921600 bps Bluetooth UART: ● Use: Bluetooth communication ● Baud rate: 115200 bps
PCIe Interface	● PCIe1: Complies with PCIe 4.0 specification, supports 2 lanes, 16 Gbps/lane ● PCIe2/3: Complies with PCIe 3.0 specification, supports 2 lanes, 8 Gbps/lane ● Only supports RC mode ● Use: connect to an external Wi-Fi IC and used for Wi-Fi communication by default

Network Indication	NET_MODE: ● Use: network registration status indication NET_STATUS: ● Use: network activity status indication
AT Commands	Compliant with 3GPP TS 27.007, 27.005 and NetPrisma enhanced AT commands
Rx-diversity	5G NR, LTE and WCDMA (HMT89-EPV only) Rx-diversity
Antenna Interfaces	● Cellular antenna interfaces (ANT0–7) ● GNSS antenna interface (ANT GNSS) ● 50 Ω characteristic impedance
Transmitting Power	HMT89-LD: ● 5G NR bands: Class 3 (23 dBm $\pm$2 dB) ● 5G NR HPUE ¹ bands (n38/n41/n77/n78): Class 2 (26 dBm +2/-3 dB) ● 5G NR HPUE ¹ bands (n41/n77/n78): Class 1.5 (29 dBm +2/-3 dB) ● LTE bands: Class 3 (23 dBm $\pm$2 dB) ● LTE HPUE ¹ bands (B38/B41): Class 2 (26 dBm +2/-3 dB) HMT89-EPV: ● 5G NR bands: Class 3 (23 dBm $\pm$2 dB) ● 5G NR HPUE ¹ bands (n41/n77/n78): Class 2 (26 dBm +2/-3 dB) ● 5G NR HPUE ¹ bands (n41/n77/n78): Class 1.5 (29 dBm +2/-3 dB) ● LTE bands: Class 3 (23 dBm $\pm$2 dB) ● LTE HPUE ¹ band (B41): Class 2 (26 dBm +2/-3 dB) ● WCDMA bands: Class 3 (23 dBm $\pm$2 dB)
5G NR Features	● The module complies with 3GPP Rel-16 specification ● DL modulations: QPSK, 16QAM, 64QAM and 256QAM ● UL modulations: $\pi/2$-BPSK, QPSK, 16QAM, 64QAM and 256QAM ● DL 4 $\times$ 4 MIMO: HMT89-LD: n2/n5/n7/n12/n13/n14/n25/n26/n30/n38/n41/n48/n66/n70/n71/n77/n78 HMT89-EPV: n1/n3/n5/n7/n8/n20/n28/n38/n40/n41/n77/n78 ● UL 2 $\times$ 2 MIMO: HMT89-LD: n2/n5/n25/n38/n41/n48/n66/n70/n71/n77/n78 HMT89-EPV: n38/n40/n41/n77/n78 ● SCS: – FDD: 15 kHz – TDD: 30 kHz NSA and SA: ● Option 3x, Option 3a, Option 3 and Option 2 ● NSA max. data rates – DL: 5.67 Gbps – UL: 1.46 Gbps ● SA max. data rates: – DL: 7.01 Gbps – UL: 2.5 Gbps SRS: HMT89-LD: – NSA: 1T4R (n38/n41/n48/n77/n78) – SA: 2T4R (n38/n41/n48/n77/n78) HMT89-EPV: – NSA: 1T4R (n38/n40/n41/n77/n78) – SA: 2T4R (n38/n40/n41/n77/n78)
LTE Features	● The module complies with 3GPP Rel-16 FDD and TDD ● Max. LTE category: – DL: Cat 19 – UL: Cat 18 ● 1.4 MHz, 3 MHz, 5 MHz, 10 MHz, 15 MHz and 20 MHz RF bandwidths ● DL modulations: QPSK, 16QAM, 64QAM and 256QAM ● UL modulations: QPSK, 16QAM, 64QAM and 256QAM ● DL 4 $\times$ 4 MIMO: HMT89-LD: B2/B4/B5/B7/B12 (B17)/B13/B14/B25/B26/B30/B38/B41/B42/B43/B48/B66/B70/B71 HMT89-EPV: B1/B3/B5/B7/B8/B20/B28/B38/B40/B41/B42/B43 ● LTE max. data rates:

¹ HPUE is only for single carrier.

	- DL: 1.6 Gbps - UL: 211 Mbps
UMTS Features	● The module complies with 3GPP Rel-8 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA ● DL Modulations: QPSK, 16QAM and 64QAM ● UL Modulations: QPSK, 16QAM ● DC-HSDPA max. data rate: 42.2 Mbps (DL) ● HSUPA max. data rate: 11.5 Mbps (UL) ● WCDMA max. data rates: - DL: 384 kbps - UL: 384 kbps
GNSS Features	● Supports GPS/BDS/GLONASS/Galileo/QZSS ● Dual-band GNSS: L1 and L5 ● The module complies with NMEA 0183 protocol ● The data update rate is 1 Hz by default and can support a max. value of 5 Hz ● Supports AGNSS. For more details, see document 2
Internet Protocol Features	● The module complies with TCP, UDP, PPP, NTP, NITZ, FTP, HTTP, PING, HTTPS, FTPS, SSL, SMTP, SMTPS protocols ● The module complies with PPP protocol's PAP and CHAP authentication
Temperature Ranges	● Normal operating temperature ²: -30 °C to +70 °C ● Extended operating temperature ³: -40 °C to +85 °C ● Storage temperature: -40 °C to +90 °C
Firmware Upgrade	● USB 2.0 interface ● FOTA
RoHS	All hardware components are fully complying with EU RoHS directive

2.3. Functional Diagram

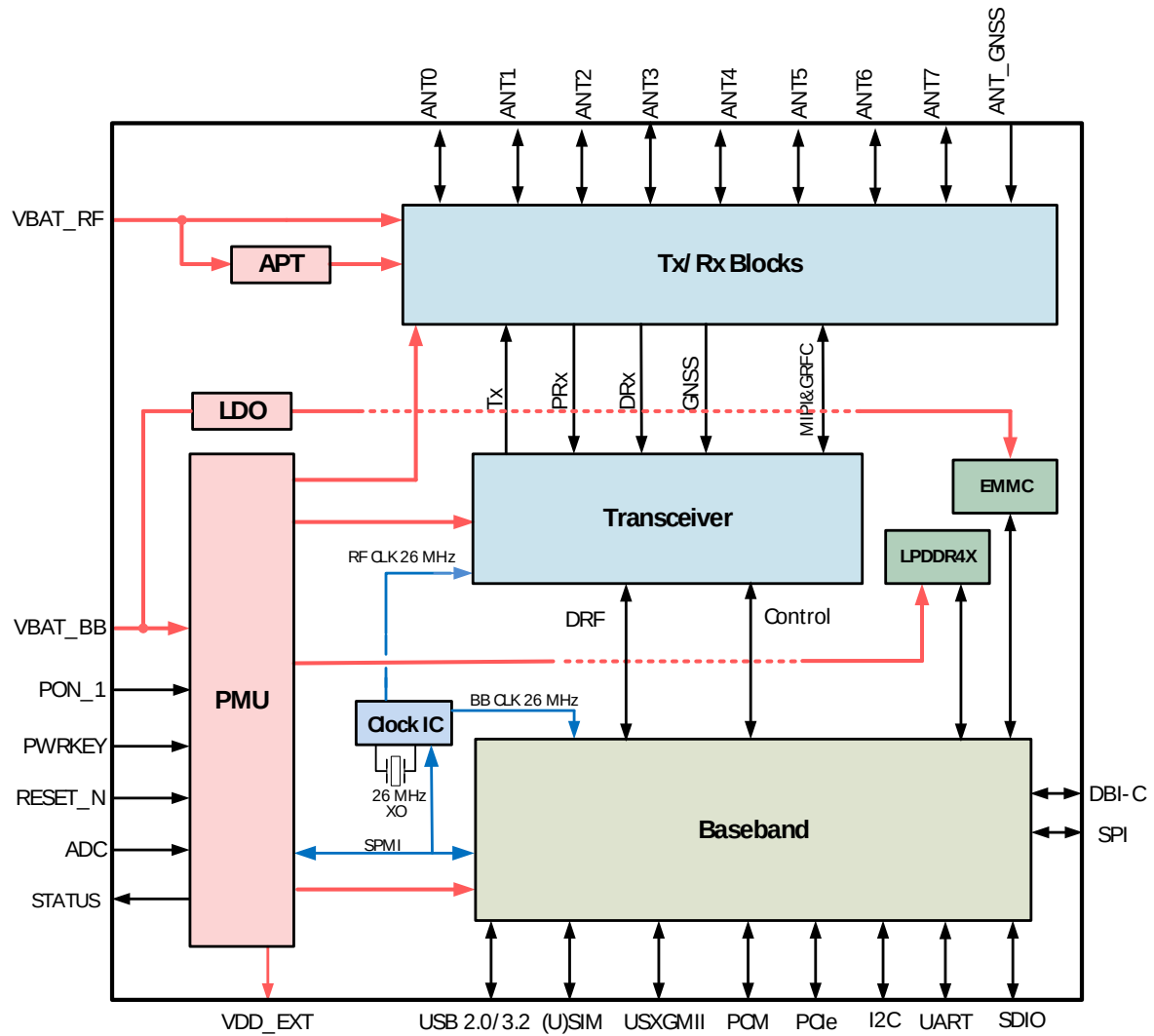
The functional diagram illustrates the following major functional parts:

- Power management
- Baseband part
- LPDDR4X + EMMC
- Radio frequency part
- Peripheral interfaces

Figure 1: Functional Diagram

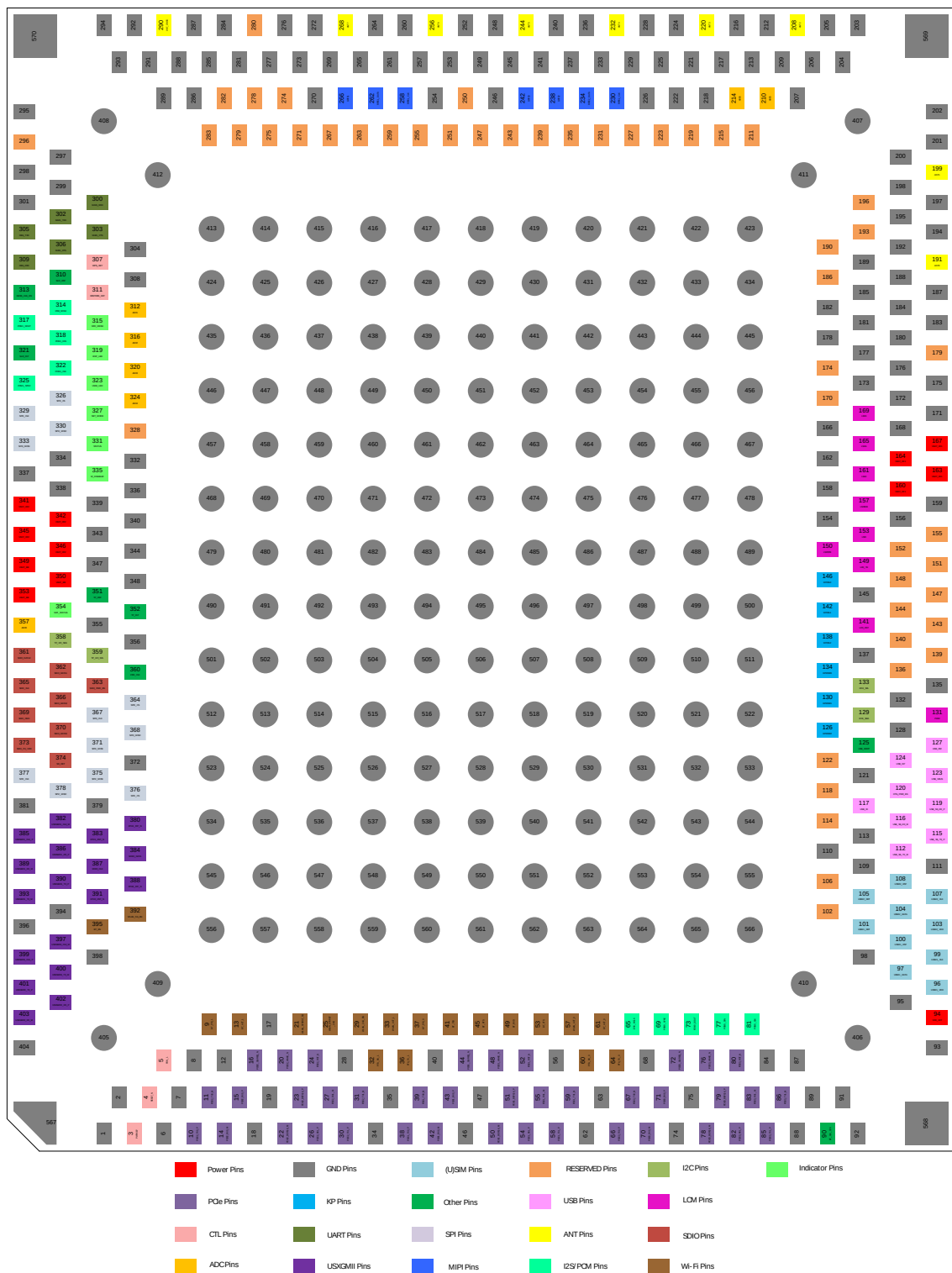
² To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

³ To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within the range of -40 to -30 °C or 70 to 85 °C, the module retains the ability to establish and maintain functions such as voice, SMS, and emergency call, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.



2.4. Pin Assignment

Figure 2: Pin Assignment (Top View)



NOTE

Keep all RESERVED pins unconnected.

2.5. Pin Description

Table 5: Parameter Definition

Parameter	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VBAT_BB	349, 350, 353	PI	Power supply for the module's baseband part	V _{max} = 4.4 V V _{min} = 3.3 V V _{nom} = 3.8 V	
VBAT_RF1	160, 163, 164, 167	PI	Power supply for the module's RF part	V _{max} = 4.4 V V _{min} = 3.3 V V _{nom} = 3.8 V	
VBAT_RF2	341, 342, 345, 346	PI	Power supply for the module's RF part	V _{max} = 4.4 V V _{min} = 3.3 V V _{nom} = 3.8 V	
VDD_EXT	94	PO	Provide 1.8 V for external circuit	V _{nom} = 1.8 V I _{omax} = 50 mA	Power supply for external GPIO's pull-up circuits. A test point is recommended to be reserved.
Turn On/Off & Other Control Signals					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	3	DI	Turn on/off the module	V _{IHmin} = 1.45 V V _{ILmax} = 0.3 V	Internally pulled up to 1.8 V. Active low.

RESET_N	4	DI	Reset the module	V _{IH} min = 1.45 V V _{IL} max = 0.3 V	Internally pulled up to 1.8 V. Active low. A test point is recommended to be reserved if unused.
PON_1	5	DI	Turn on/off the module	VBAT_BB	
RESTORE_KEY	311	DI	Restore the module	VDD_EXT	
WPS_KEY	307	DI	Wi-Fi protected setup		

Indication Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
STATUS	331	OD	Indicate the module's operation status	VDD_EXT	PMIC_ISINK3
W_DISABLE#	335	OD	Indicate the module's airplane mode		PMIC_ISINK1
NET_STATUS	354	OD	Indicate the module's network activity status		PMIC_ISINK2
NET_MODE	327	DO	Indicate the module's network registration mode		
WIFI_MESH ^{dev}	315	DO	Indicate the Wi-Fi mesh function status		
USIM_LED	323	DO	Indicate the (U)SIM card function status		
VOIP_LED ^{dev}	319	DO	Indicate the VoIP function status		

USB Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	123	AI	USB connection detect	$V_{max} = 15\text{ V}$ $V_{min} = 4.2\text{ V}$ $V_{nom} = 5.0\text{ V}$	Used for USB connection detection. Cannot be used for power supply. A test point must be reserved.
USB_DP	124	AIO	USB differential data (+)	VDD_EXT	Require differential impedance of 90 Ω . Test points must be reserved.
USB_DM	127	AIO	USB differential data (-)		
USB_SS_TX_P	115	AO	USB 3.2 SuperSpeed transmit (+)		Require differential impedance of 90 Ω . If unused, connect Rx to GND directly.
USB_SS_TX_M	112	AO	USB 3.2 SuperSpeed transmit (-)		
USB_SS_RX_P	119	AI	USB 3.2 SuperSpeed receive (+)		
USB_SS_RX_M	116	AI	USB 3.2 SuperSpeed receive (-)		
USB_ID	117	DI	USB ID detect		

OTG_PWR_EN	120	DO	OTG power control		
(U)SIM Interfaces					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USIM1_VDD	96	PO	(U)SIM1 card power supply	High-voltage: Vmax = 3.3 V Vnom = 3.0 V Vmin = 2.7 V Low-voltage: Vmax = 1.98 V Vnom = 1.8 V Vmin = 1.62 V	
USIM1_DATA	97	DIO	(U)SIM1 card data		
USIM1_CLK	99	DO	(U)SIM1 card clock	USIM1_VDD	
USIM1_RST	100	DO	(U)SIM1 card reset		
USIM1_DET	101	DI	(U)SIM1 card hot-plug detect	VDD_EXT	
USIM2_VDD	103	PO	(U)SIM2 card power supply	High-voltage: Vmax = 3.3 V Vnom = 3.0 V Vmin = 2.7 V Low-voltage: Vmax = 1.98 V Vnom = 1.8 V Vmin = 1.62 V	
USIM2_DATA	104	DIO	(U)SIM2 card data		
USIM2_CLK	107	DO	(U)SIM2 card clock	USIM2_VDD	
USIM2_RST	108	DO	(U)SIM2 card reset		
USIM2_DET	105	DI	(U)SIM2 card hot-plug detect	VDD_EXT	
SDIO Interface					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SDIO_CLK	365	DO	SDIO clock		
SDIO_CMD	369	DIO	SDIO command		
SDIO_DATA0	370	DIO	SDIO data bit 0	VDD_EXT	
SDIO_DATA1	362	DIO	SDIO data bit 1		
SDIO_DATA2	361	DIO	SDIO data bit 2		
SDIO_DATA3	366	DIO	SDIO data bit 3		
SD_DET	374	DI	SD card hot-plug detect		
SDIO_PWR_EN	363	DO	SDIO power supply enable		

SDIO_PU_VDD	373	PO	SD card IO pull-up power supply	High-voltage: Vnom = 3.0 V Iomax = 200 mA Low-voltage: Vnom = 1.8 V Iomax = 200 mA	
Main UART Interface					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
MAIN_CTS	303	DO	Clear to send signal from the module	VDD_EXT	Connect to the MCU's CTS.
MAIN_RTS	306	DI	Request to send signal to the module		Connect to the MCU's RTS.
MAIN_RXD	300	DI	Main UART receive		
MAIN_TXD	302	DO	Main UART transmit		
Bluetooth UART Interface					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
BT_TXD	41	DO	Bluetooth UART transmit	VDD_EXT	
BT_RXD	49	DI	Bluetooth UART receive		
BT_RTS	45	DI	Request to send signal to the module		Connect to the Wi-Fi&Bluetooth module's RTS.
BT_CTS	53	DO	Clear to send signal from the module		Connect to the Wi-Fi&Bluetooth module's CTS.
Debug UART Interface					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
DBG_RXD	309	DI	Debug UART receive	VDD_EXT	Test points must be reserved.
DBG_TXD	305	DO	Debug UART transmit		
I2C Interface					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
TP_I2C_SCL	359	OD	TP I2C clock	VDD_EXT	External pull-up resistor is required. 1.8 V only. If unused, keep it open.
TP_I2C_SDA	358	OD	TP I2C data		
I2C4_SCL	133	OD	I2C serial clock		
I2C4_SDA	129	OD	I2C serial data		
PCM Interfaces					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PCM0_SYNC	69	DIO	PCM data frame sync	VDD_EXT	In master mode, they are output signals. In

PCM0_CLK	81	DIO	PCM clock	VDD_EXT	slave mode, they are input signals. If unused, keep them open.
PCM0_DIN	77	DI	PCM data input		If unused, keep them open.
PCM0_DOUT	73	DO	PCM data output		
PCM1_SYNC	325	DIO	PCM data frame sync		In master mode, they are output signals. In slave mode, they are input signals. If unused, keep them open.
PCM1_CLK	322	DIO	PCM clock		
PCM1_DIN	318	DI	PCM data input		If unused, keep them open.
PCM1_DOUT	317	DO	PCM data output		
I2S0_MCLK	314	DO	I2S0 master clock		
I2S4_MCLK	65	DO	I2S4 master clock		

PCIe Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PCIE1_REFCLK_M	50	AO	PCIe1 reference clock (-)	VDD_EXT	The REFCLK requires differential impedance of 100 Ω . The Tx/Rx requires differential impedance of 85 Ω . PCIe Gen 4 compliant. If unused, connect Rx to GND directly.
PCIE1_REFCLK_P	51	AO	PCIe1 reference clock (+)		
PCIE1_RX0_M	42	AI	PCIe1 receive 0 (-)		
PCIE1_RX0_P	43	AI	PCIe1 receive 0 (+)		
PCIE1_TX0_M	39	AO	PCIe1 transmit 0 (-)		
PCIE1_TX0_P	38	AO	PCIe1 transmit 0 (+)		
PCIE1_RX1_M	55	AI	PCIe1 receive 1 (-)		
PCIE1_RX1_P	54	AI	PCIe1 receive 1 (+)		
PCIE1_TX1_M	59	AO	PCIe1 transmit 1 (-)		
PCIE1_TX1_P	58	AO	PCIe1 transmit 1 (+)		
PCIE1_RST_N	52	DO	PCIe1 reset		
PCIE1_WAKE_N	48	DI	PCIe1 wake up		
PCIE1_CLKREQ_N	44	DI	PCIe1 clock request		
PCIE2_REFCLK_M	22	AO	PCIe2 reference clock (-)		The REFCLK requires differential impedance of 100 Ω . The Tx/Rx requires differential impedance of 85 Ω . PCIe Gen 3 compliant.
PCIE2_REFCLK_P	23	AO	PCIe2 reference clock (+)		
PCIE2_RX0_M	14	AI	PCIe2 receive 0 (-)		
PCIE2_RX0_P	15	AI	PCIe2 receive 0 (+)		

PCIE2_TX0_M	11	AO	PCIe2 transmit 0 (-)		If unused, connect Rx to GND directly.
PCIE2_TX0_P	10	AO	PCIe2 transmit 0 (+)		
PCIE2_RX1_M	27	AI	PCIe2 receive 1 (-)		
PCIE2_RX1_P	26	AI	PCIe2 receive 1 (+)		
PCIE2_TX1_M	31	AO	PCIe2 transmit 1 (-)		
PCIE2_TX1_P	30	AO	PCIe2 transmit 1 (+)		
PCIE2_RST_N	24	DO	PCIe2 reset		
PCIE2_WAKE_N	20	DI	PCIe2 wake up	VDD_EXT	
PCIE2_CLKREQ_N	16	DI	PCIe2 clock request		
PCIE3_REFCLK_M	78	AO	PCIe3 reference clock (-)		The REFCLK requires differential impedance of 100 Ω. The Tx/Rx requires differential impedance of 85 Ω. PCIe Gen 3 compliant. If unused, connect Rx to GND directly.
PCIE3_REFCLK_P	79	AO	PCIe3 reference clock (+)		
PCIE3_RX0_M	70	AI	PCIe3 receive 0 (-)		
PCIE3_RX0_P	71	AI	PCIe3 receive 0 (+)		
PCIE3_TX0_M	67	AO	PCIe3 transmit 0 (-)		
PCIE3_TX0_P	66	AO	PCIe3 transmit 0 (+)		
PCIE3_RX1_M	83	AI	PCIe3 receive 1 (-)		
PCIE3_RX1_P	82	AI	PCIe3 receive 1 (+)		
PCIE3_TX1_M	86	AO	PCIe3 transmit 1 (-)		
PCIE3_TX1_P	85	AO	PCIe3 transmit 1 (+)		
PCIE3_RST_N	80	DO	PCIe3 reset		
PCIE3_WAKE_N	76	DI	PCIe3 wake up	VDD_EXT	
PCIE3_CLKREQ_N	72	DI	PCIe3 clock request		

LCM Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
LSDI	153	DI	SPI serial input data	VDD_EXT	Pins 150,153, 157, 161,165 and 169 are belong to DBI-C interface.
LSA0	161	DO	Indicate transmission of data or command		
LSCE0B	157	DO	SPI chip select		
LSRSTB	150	DO	SPI reset		
LSCK	169	DO	SPI serial clock		

LSDA	165	DO	SPI serial output data	
PWM	131	DO	PWM output	For LCD only.
LCD_TE	149	DI	LCM tearing effect	
LCD_RST	141	DO	LCM reset	

USXGMII Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
MDIO_DATA	384	DIO	MDIO data		
MDIO_CLK	387	DO	MDIO clock		
ETH0_INT_N	388	DI	Ethernet PHY 0 interrupt	VDD_EXT	
ETH0_RST_N	391	DO	Ethernet PHY 0 reset		
ETH1_INT_N	380	DI	Ethernet PHY 1 interrupt		
ETH1_RST_N	383	DO	Ethernet PHY 1 reset		
USXGMII0_CLK_M	397	AO	USXGMII0 clock (-)		
USXGMII0_CLK_P	399	AO	USXGMII0 clock (+)		
USXGMII0_TX_M	400	AO	USXGMII0 transmit (-)		
USXGMII0_TX_P	401	AO	USXGMII0 transmit (+)		
USXGMII0_RX_P	402	AI	USXGMII0 receive (+)		
USXGMII0_RX_M	403	AI	USXGMII0 receive (-)		
USXGMII1_CLK_M	382	AO	USXGMII1 clock (-)		Require differential impedance of 100 Ω. If unused, connect Rx to GND directly.
USXGMII1_CLK_P	385	AO	USXGMII1 clock (+)		
USXGMII1_RX_P	386	AI	USXGMII1 receive (+)		
USXGMII1_RX_M	389	AI	USXGMII1 receive (-)		
USXGMII1_TX_P	390	AO	USXGMII1 transmit (+)		
USXGMII1_TX_M	393	AO	USXGMII1 transmit (-)		

WWAN/WLAN Control Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
WLAN_SYSRST_5G	21	DO	WLAN 5 GHz system reset		
WLAN_2.4G_EN _{dev}	29	DO	WLAN 2.4 GHz function enable control	VDD_EXT	
WLAN_SYSRST_2.4G	25	DO	WLAN 2.4 GHz system reset		

WLAN_5G_EN ^{dev}	392	DO	WLAN 5 GHz function enable control	VDD_EXT	Used for WWAN/WLAN coexistence by default.
BT_ACT_0 ^{dev}	61	DO	Coexistence interface for WWAN and WLAN		
BT_PRI_0 ^{dev}	37	DO	Coexistence interface for WWAN and WLAN		
WLAN_ACT_0 ^{dev}	57	DI	Coexistence interface for WWAN and WLAN		
PTA_TX_0 ^{dev}	64	DO	Coexistence interface for WWAN and WLAN		
PTA_RX_0 ^{dev}	60	DO	Coexistence interface for WWAN and WLAN		
BT_ACT_1 ^{dev}	13	DO	Coexistence interface for WWAN and WLAN		
BT_PRI_1 ^{dev}	9	DO	Coexistence interface for WWAN and WLAN		
WLAN_ACT_1 ^{dev}	33	DI	Coexistence interface for WWAN and WLAN		
PTA_TX_1 ^{dev}	36	DO	Coexistence interface for WWAN and WLAN		
PTA_RX_1 ^{dev}	32	DO	Coexistence interface for WWAN and WLAN		

RF Antenna Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ANT0	191	AIO	Antenna 0 interface	VDD_EXT	50 Ω characteristic impedance.
ANT1	199	AIO	Antenna 1 interface		
ANT2	208	AIO	Antenna 2 interface		
ANT3	220	AIO	Antenna 3 interface		
ANT4	232	AIO	Antenna 4 interface		
ANT5	244	AIO	Antenna 5 interface		
ANT6	256	AIO	Antenna 6 interface		
ANT7	268	AIO	Antenna 7 interface		
ANT_GNSS	290	AI	GNSS antenna interface		

Antenna Tuner Control Interfaces^{dev}

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
GRFC1	266	DO	Generic RF Controller	VDD_EXT	
GRFC2	238	DO	Generic RF Controller		

GRFC3	242	DO	Generic RF Controller
RFFE1_DATA	262	DIO	Used for external MIPI IC control
RFFE1_CLK	258	DO	Used for external MIPI IC control
RFFE2_DATA	234	DIO	Used for external MIPI IC control
RFFE2_CLK	230	DO	Used for external MIPI IC control

SPI Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SPI0_CS	364	DO	SPI0 chip select	VDD_EXT	Recommended for SLIC IC communication.
SPI0_CLK	367	DO	SPI0 clock		
SPI0_MOSI	371	DO	SPI0 master-out slave-in		
SPI0_MISO	368	DI	SPI0 master-in slave-out		
SPI2_CS	376	DO	SPI2 chip select		
SPI2_CLK	377	DO	SPI2 clock		
SPI2_MOSI	375	DO	SPI2 master-out slave-in		
SPI2_MISO	378	DI	SPI2 master-in slave-out		
SPI3_CS	326	DO	SPI3 chip select		
SPI3_CLK	329	DO	SPI3 clock		
SPI3_MOSI	333	DO	SPI3 master-out slave-in		
SPI3_MISO	330	DI	SPI3 master-in slave-out		

ADC Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ADC0	357	AI	General-purpose ADC interface	0.04–1.78 V	If unused, connect it to GND directly.
ADC1	312	AI	General-purpose ADC interface		
ADC2	316	AI	General-purpose ADC interface		
ADC3	320	AI	General-purpose ADC interface		
ADC4	324	AI	General-purpose ADC interface		
ADC5	210	AI	General-purpose ADC interface		
ADC6	214	AI	General-purpose ADC interface		

Matrix Keypad Interface ^{dev}

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
KPCOL0	146	DIO	Matrix keypad column0	VDD_EXT	Do not pull it low before startup, otherwise it will force the module into download mode.
KPCOL1	142	DIO	Matrix keypad column1		
KPCOL2	138	DIO	Matrix keypad column2		
KPROW0	134	DIO	Matrix keypad row0		
KPROW1	130	DIO	Matrix keypad row1		
KPROW2	126	DIO	Matrix keypad row2		

Other Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_BOOT	125	DI	Force the module into download mode	VDD_EXT	A test point is recommended to be reserved.
SLIC_RST	310	DO	SLIC reset		
SLIC_INT	321	DI	SLIC interrupt		
TP_RST	351	DO	TP reset		
TP_INT	352	DI	TP interrupt		
BT_EN ^{dev}	395	DO	Bluetooth enable control		
GNSS_LNA_EN ^{dev}	313	DO	GNSS LNA enable control; 1PPS pulse output and frame synchronization	VDD_EXT	
BT_CLK_32K ^{dev}	90	DO	32 kHz clock for WLAN/Bluetooth		
26M_CLK	360	DO	26 MHz clock for others		

Reserved Pins

Pin Name	Pin No.	Comment
RESERVED	102, 106, 114, 118, 122, 136, 139, 140, 143, 144, 147, 148, 151, 152, 155, 170, 174, 179, 186, 190, 193, 196, 211, 215, 219, 223, 227, 231, 235, 239, 243, 247, 250, 251, 255, 259, 263, 267, 271, 274, 275, 278, 279, 280, 282, 283, 296, 328	Keep these pins open.

GND

Pin Name	Pin No.	Comment
GND	1, 2, 6–8, 12, 17–19, 28, 34, 35, 40, 46, 47, 56, 62, 63, 68, 74, 75, 84, 87–89, 91–93, 95, 98, 109–111, 113, 121, 128, 132, 135, 137, 145, 154, 156, 158, 159, 162, 166, 168, 171, 172, 173, 175–178, 180–185, 187–189, 192, 194, 195, 197, 198, 200–207, 209, 212, 213, 216, 217, 218, 221, 222, 224–226, 228, 229, 233, 236, 237, 240, 241, 245, 246, 248, 249, 252–254, 257, 260, 261,	Connect these pins to ground.

264, 265, 269, 270, 272, 273, 276, 277, 281, 284–289,
291–295, 297–299, 301, 304, 308, 332, 334, 336–340,
343, 344, 347, 348, 355, 356, 372, 379, 381, 394, 396,
398, 404–570

NOTE

To reduce the probability of module damage and extend module service life, do not power up and down frequently.

2.6. EVB Kit

NetPrisma supplies a 5G-SOC-EVB with accessories to develop and test the module. For more details, see **document 1**.

3 Operating Characteristics

3.1. Operating Modes

Table 7: Operating Modes Overview

Mode	Description
Full Functionality Mode	Idle The module remains registered on the network but has no data interaction with the network. Software is active.
	Voice/Data The module is connected to the network. Power consumption is decided by network settings and data rate.
Minimum Functionality Mode	AT+CFUN=0 can set the module to the minimum functionality mode without removing the power supply. In this mode, both the RF function and the (U)SIM card is invalid.
Airplane Mode	AT+CFUN=4 command can set the module to airplane mode. In this case, RF function is invalid.
Sleep Mode	In this mode, power consumption of the module will be reduced to an ultra-low level. In this mode, the module can still receive paging, SMS, voice call and TCP/UDP data from network.
Shutdown Mode	PMU shuts down the power supply. Software is inactive and UART are inaccessible. However, the voltage supply (for VBAT _{RF} and VBAT _{BB}) remains connected.

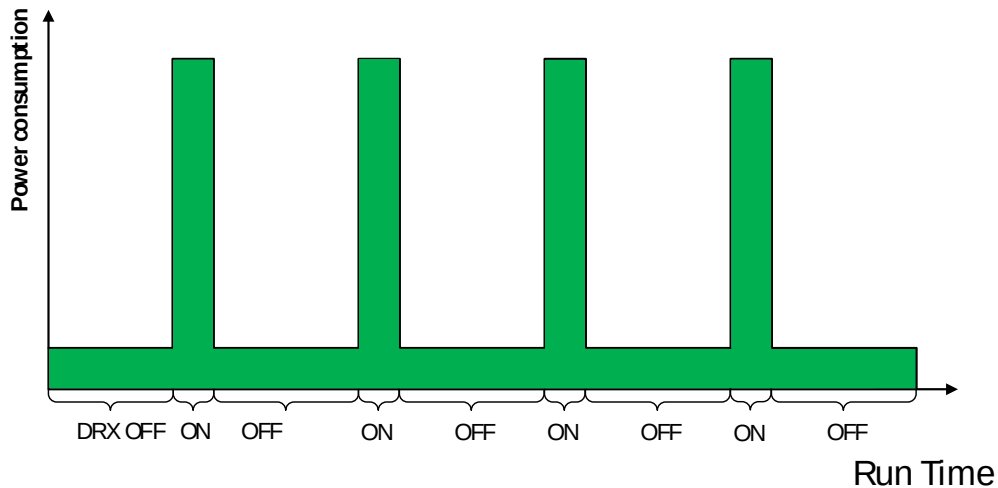
NOTE

For more details about **AT+CFUN**, see **Chapter 9.1**.

3.2. Sleep Mode

With DRX technology, power consumption of the module will be reduced to an ultra-low level.

Figure 3: Module Power Consumption in Sleep Mode



NOTE

DRX cycle values are transmitted over the wireless network.

3.2.1. UART Application Scenario

If the host communicates with the module via UART interface, the following precondition should be met to set the module into sleep mode:

- Execute **AT+QSCLK=1** command to enable sleep mode. For more details about **AT+QSCLK**, see **Chapter 9.2**.

3.2.2. USB Application Scenario

If the host communicates with the module via USB interface, the following precondition should be met to set the module into sleep mode:

- Execute **AT+QSCLK=1** command to enable sleep mode. For more details about **AT+QSCLK**, see **Chapter 9.2**.

3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via **AT+CFUN**.

AT+CFUN=<fun> command provides choices of the functionality level by setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0**: Minimum functionality (Disable RF function and (U)SIM function).
- **AT+CFUN=1**: Full functionality (Default).
- **AT+CFUN=4**: Airplane mode (Disable RF function).

NOTE

The execution of **AT+CFUN** command will not affect GNSS function. For more details about **AT+CFUN**, see **Chapter 9.1**.

3.4. Power Supply

3.4.1. Power Supply Interface

The module provides 11 VBAT pins dedicate to connecting with the external power supply:

Table 8: VBAT and GND Pins

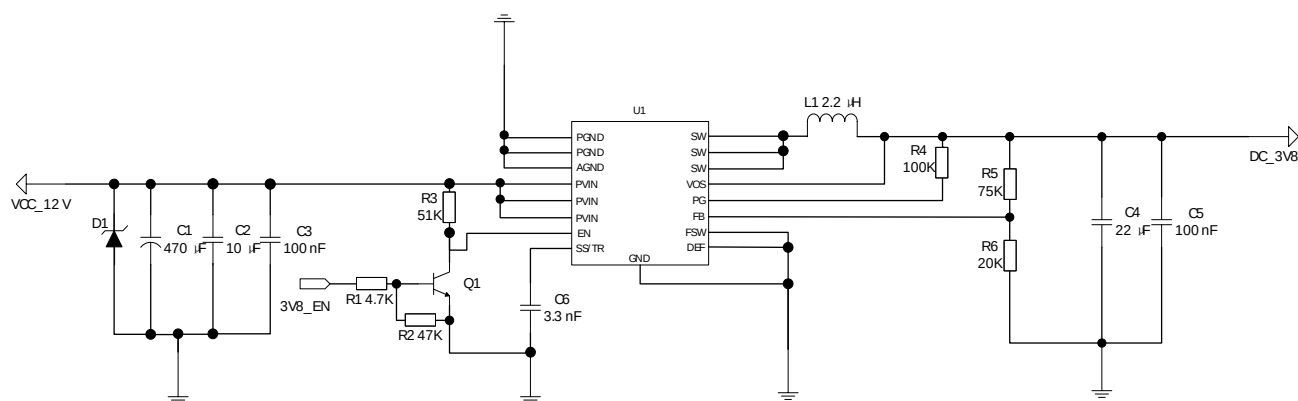
Pin Name	Pin No.	I/O	Description	Comment
VBAT_BB	349, 350, 353	PI	Power supply for the module's baseband part	
VBAT_RF1	160, 163, 164, 167	PI	Power supply for the module's RF part	
VBAT_RF2	341, 342, 345, 346	PI	Power supply for the module's RF part	
VDD_EXT	94	PO	Provide 1.8 V for external circuit	Power supply for external GPIO's pull-up circuits. A test point is recommended to be reserved.
GND	1, 2, 6–8, 12, 17–19, 28, 34, 35, 40, 46, 47, 56, 62, 63, 68, 74, 75, 84, 87–89, 91–93, 95, 98, 109–111, 113, 121, 128, 132, 135, 137, 145, 154, 156, 158, 159, 162, 166, 168, 171, 172, 173, 175–178, 180–185, 187–189, 192, 194, 195, 197, 198, 200–207, 209, 212, 213, 216, 217, 218, 221, 222, 224–226, 228, 229, 233, 236, 237, 240, 241, 245, 246, 248, 249, 252–254, 257, 260, 261, 264, 265, 269, 270, 272, 273, 276, 277, 281, 284–289, 291–295, 297–299, 301, 304, 308, 332, 334, 336–340, 343, 344, 347, 348, 355, 356, 372, 379, 381, 394, 396, 398, 404–570			

3.4.2. Reference Design for Power Supply

Power design for the module is essential. The power supply of the module should be able to provide sufficient current of 4.5 A at least. If the voltage difference between input voltage and the supply voltage is small, it is suggested to use an LDO; if the voltage difference is big, a buck converter is recommended.

The following figure shows a reference design for 12 V input power supply. The designed output of the power supply is about 3.8 V and the rated current is 4.5 A.

Figure 4: Reference Design of Power Input



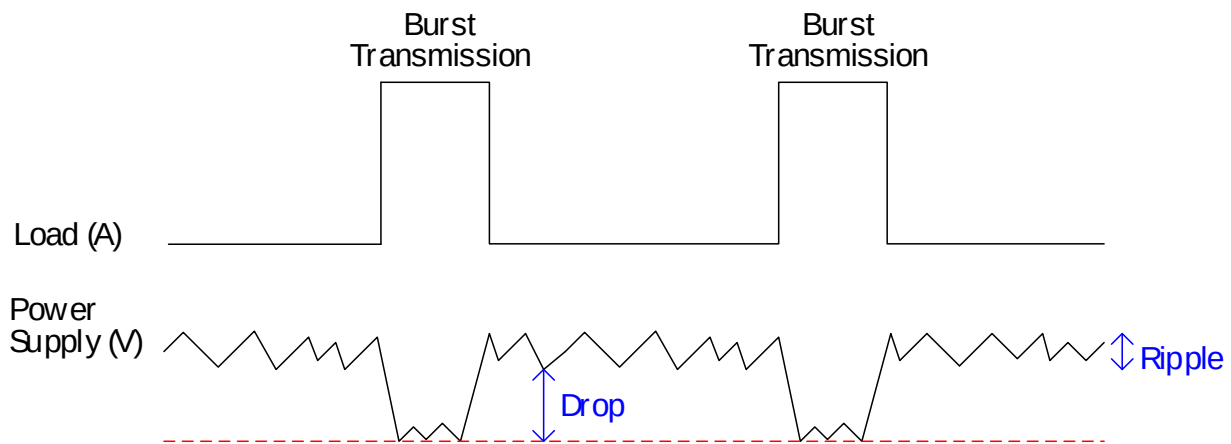
NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after turning off the module with PWRKEY can you cut off the power supply.

3.4.3. Requirements for Voltage Stability

The power supply range of the module is from 3.3 V to 4.4 V. Ensure the input voltage never drops below 3.3 V.

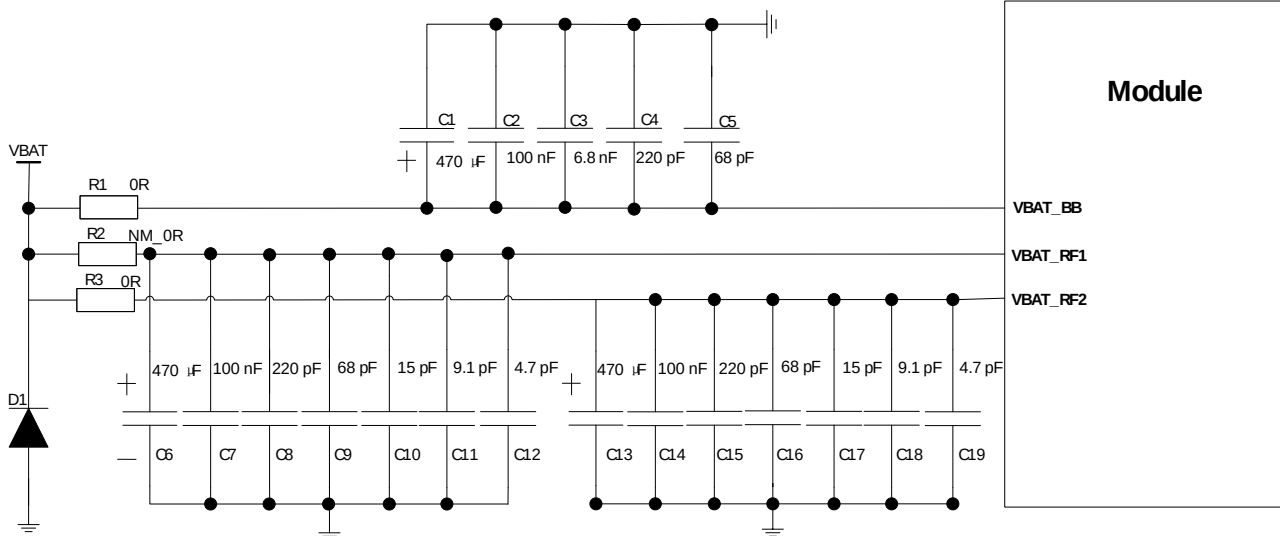
Figure 5: Power Supply Limits During Burst Transmission



To decrease the voltage drop, a bypass capacitor of about 470 μ F with low ESR ($ESR \leq 0.7 \Omega$) and a multi-layer ceramic chip (MLCC) capacitor array with ultra-low ESR should be used for VBAT_BB/RF. It is recommended to use 4 ceramic capacitors (100 nF, 6.8 nF, 220 pF, 68 pF) for composing the MLCC array for VABT_BB and 6 ceramic capacitors (100 nF, 220 pF, 68 pF, 15 pF, 9.1 pF, 4.7 pF) for composing the MLCC array for VABT_RF, and place these capacitors close to VBAT pins. The main power supply from an external application must be a single voltage source which can supply power along two sub paths with star topology. The width of VBAT_BB trace should be not less than 2 mm. The width of VBAT_RF trace should be not less than 2.5 mm. In principle, the longer the VBAT trace is, the wider it should be.

To avoid the ripple and surge and to ensure the stability of the power supply to the module, add a high-power rated TVS component at the front end of the power supply.

Figure 6: Reference Design of Power Supply



3.5. Turn-on

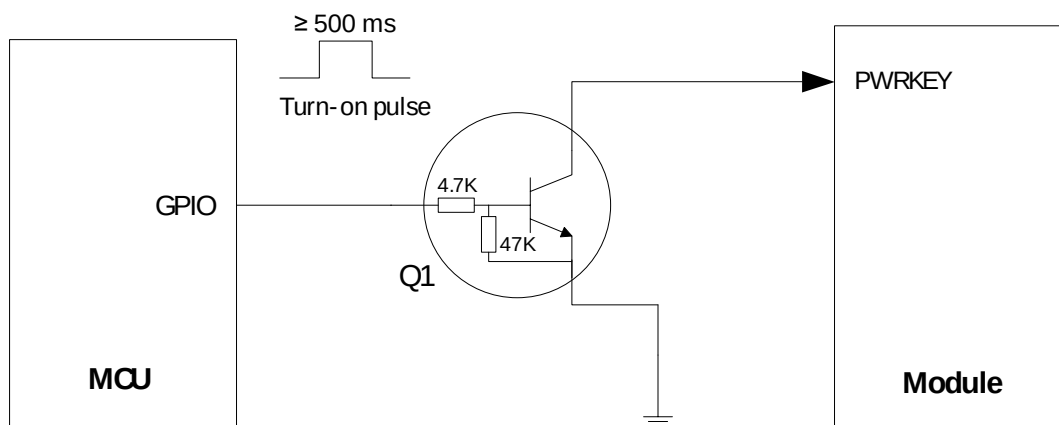
3.5.1. Turn-on with PWRKEY

Table 9: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	3	DI	Turn on/off the module	Internally pulled up to 1.8 V. Active low.

When the module is in turn-off state, it can be turned on by driving PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY.

Figure 7: Reference Design of Turn on with Driving Circuit



Another way to control the PWRKEY is using a button directly. When pressing the button, an electrostatic strike may be generated from finger. Therefore, you should place a TVS component near the button for ESD protection.

Figure 8: Reference Design of Turn on with Button

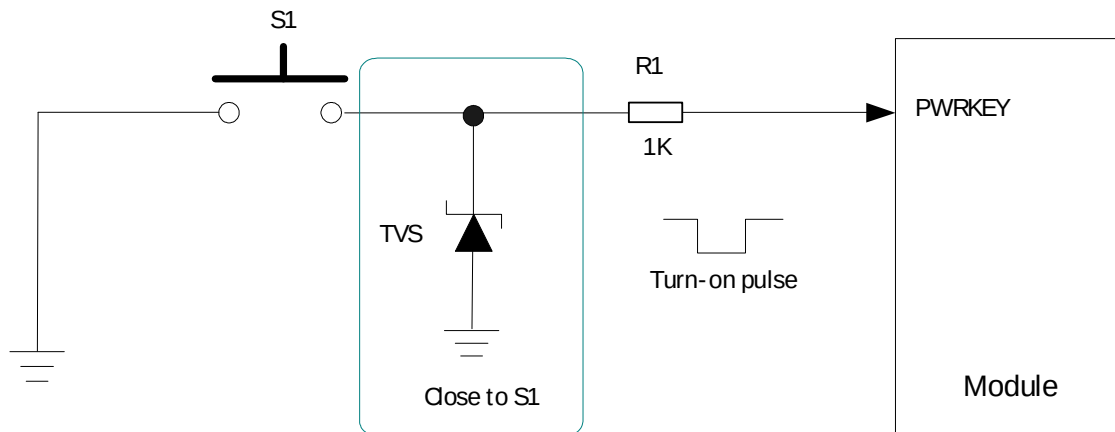
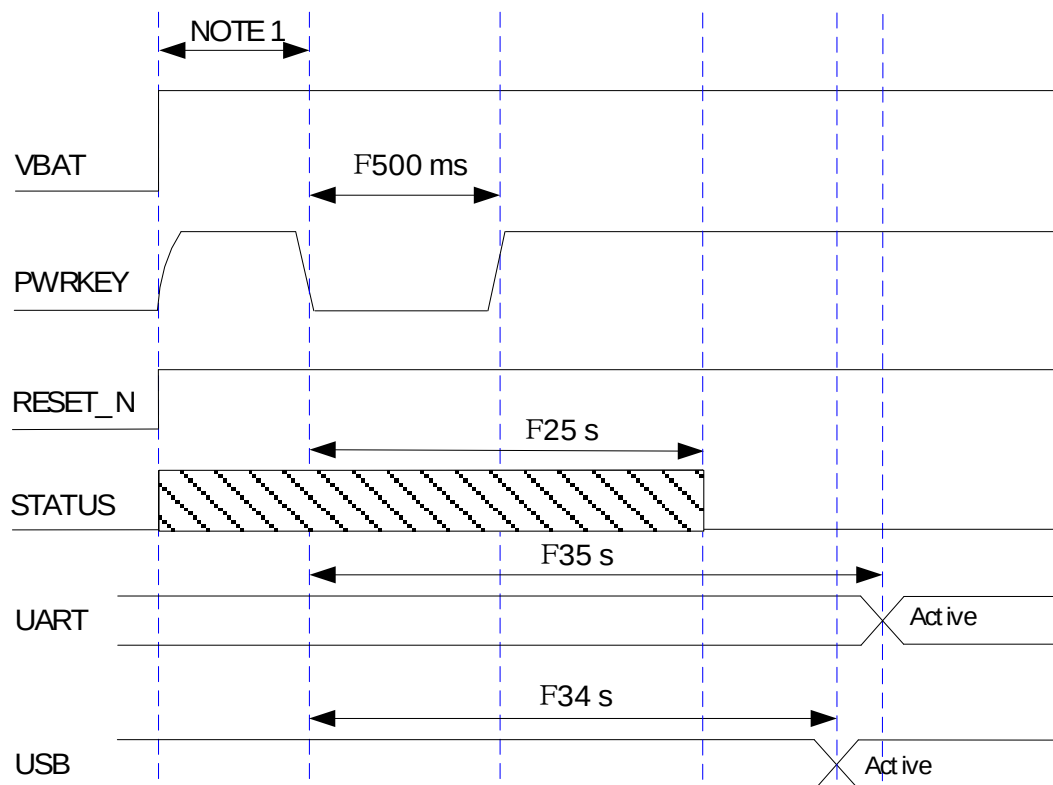


Figure 9: Timing of Turning on with PWRKEY



NOTE

1. Ensure the voltage of VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

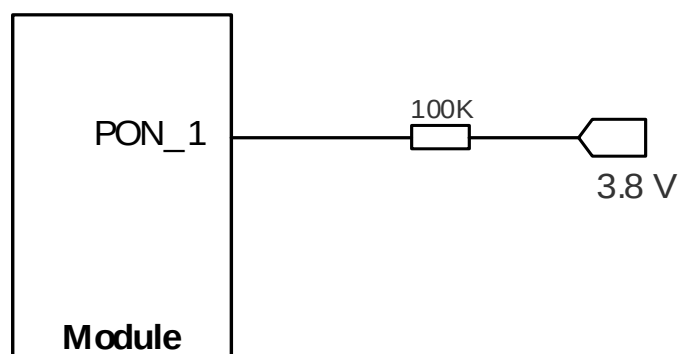
3.5.2. Turn-on with PON_1

Table 10: Pin Description of PON_1

Pin Name	Pin No.	I/O	Description	Comment
PON_1	5	DI	Turn on/off the module	

When the module is in turn-off state, it can be turned on by driving PON_1 high.

Figure 10: Reference Design of Turning on with PON_1

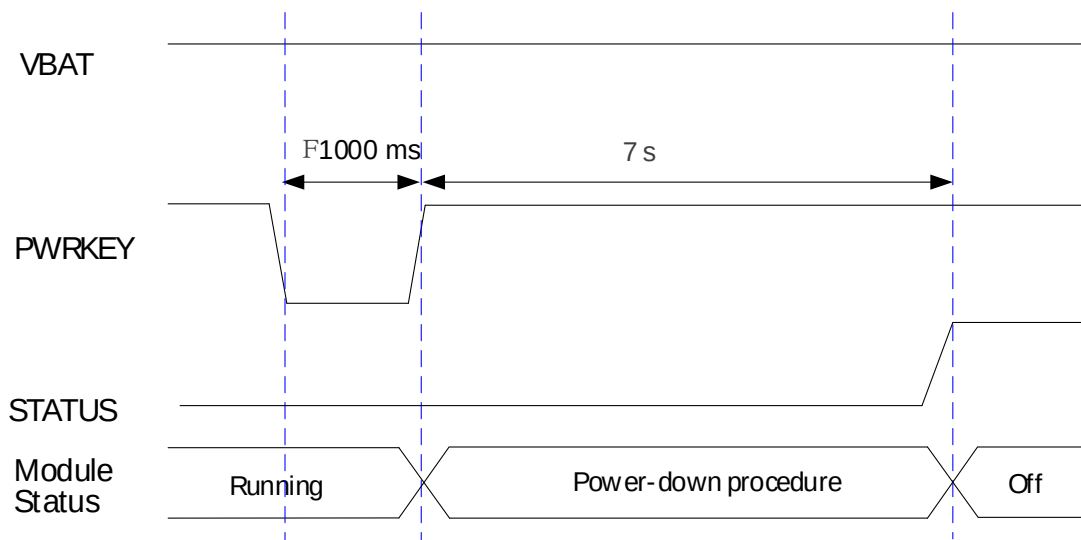


3.6. Turn-off

3.6.1. Turn-off with PWRKEY

Drive PWRKEY low for at least 1000 ms and then release it. Then, the module will execute turn-off procedure.

Figure 11: Timing of Turning off with PWRKEY



3.6.2. Turn-off with PON_1

You can turn off the module by driving PON_1 low.

NOTE

1. When turning off the module with PON_1, please keep PWRKEY at a high level after the execution of power-off. Otherwise, the module will be turned on again after power-off.
2. When USB_VBUS detects USB connection, the module always remains in the power-on state.
3. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY, can you cut off the power supply.

3.7. Reset

Driving RESET_N low for at least 1200 ms and then releasing it can reset the module. RESET_N signal is sensitive to interference, consequently it is recommended to route the trace as short as possible and surround it with ground.

Table 11: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	4	DI	Reset the module	Internally pulled up to 1.8 V. Active low. A test point is recommended to be reserved if unused.

The recommended circuit for reset function is similar to the PWRKEY control circuit. You can use an open drain/collector driver or a button to control RESET_N.

Figure 12: Reference Design of Resetting with Driving Circuit

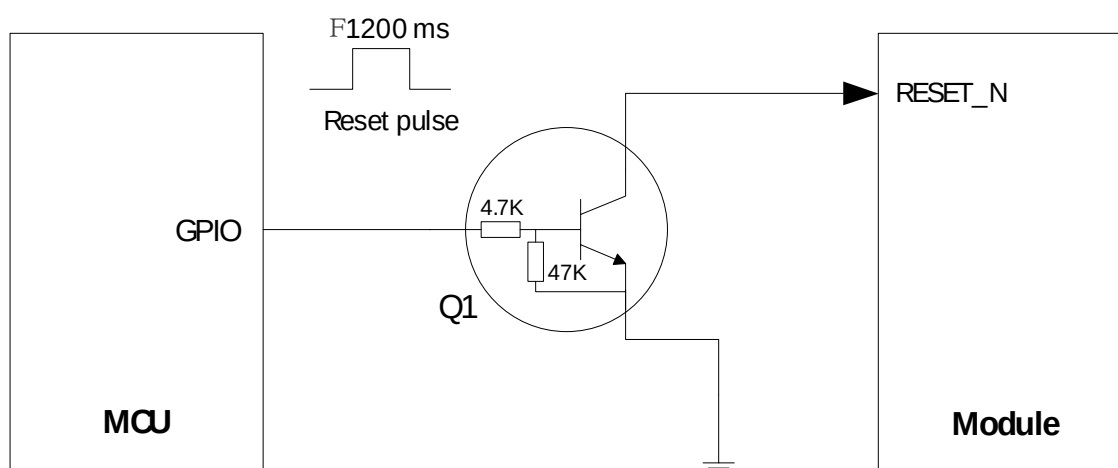


Figure 13: Reference Design of Resetting with Button

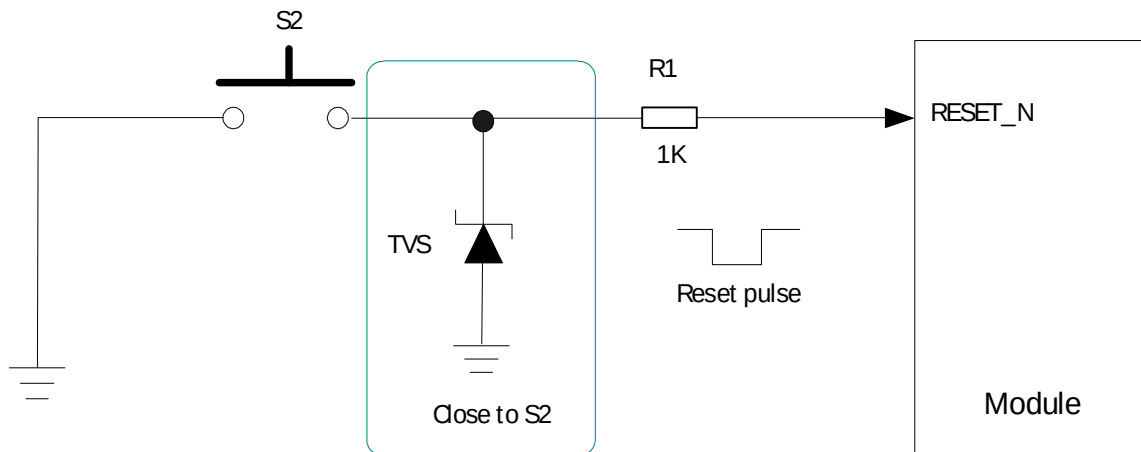
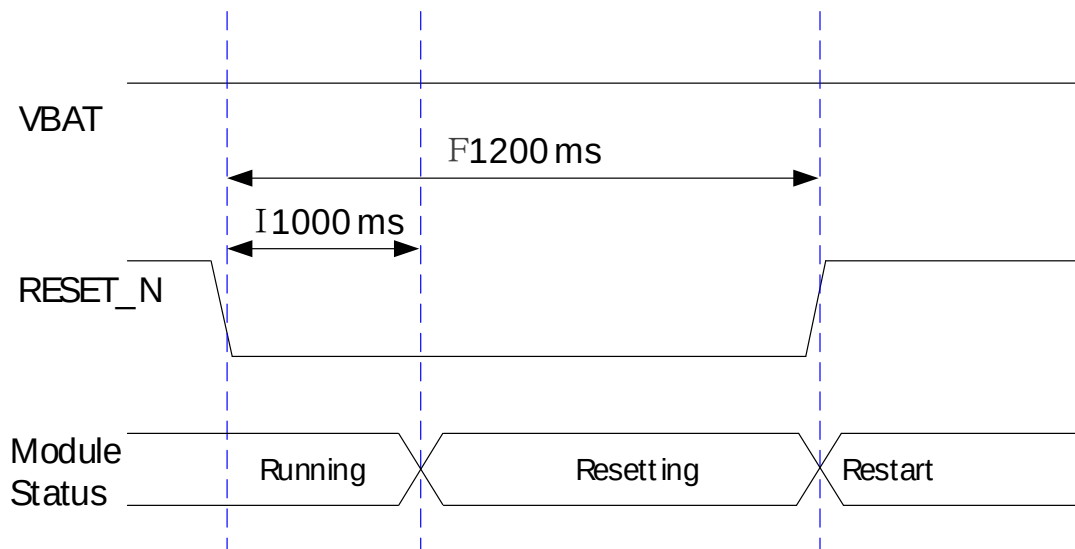


Figure 14: Timing of Resetting



NOTE

Ensure there is no large capacitance on PWRKEY and RESET_N.

4 Application Interfaces

4.1. USB Interface

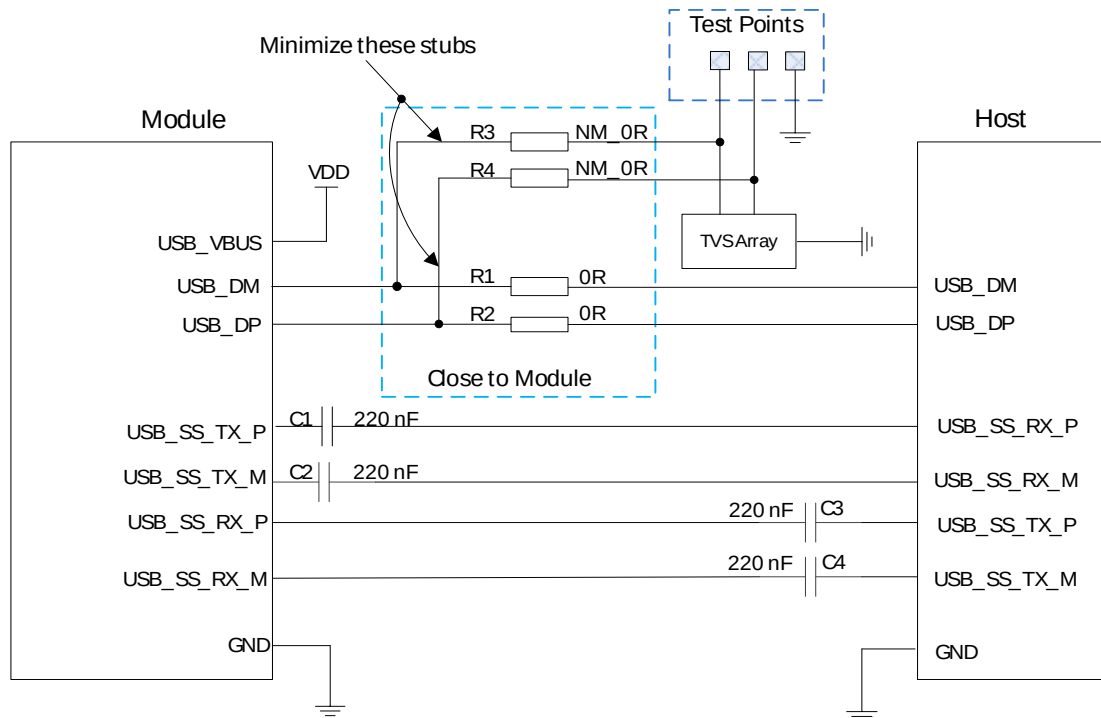
The module provides one USB interface which complies with the USB 3.2 Gen 2 and USB 2.0 specifications and supports SuperSpeed (10 Gbps) for USB 3.2 Gen 2, high-speed (480 Mbps) and full-speed (12 Mbps) for USB 2.0. The USB interface can be used for AT command communication, data transmission, software debugging and firmware upgrade.

Table 12: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	123	AI	USB connection detect	Used for USB connection detection. Cannot be used for power supply. A test point must be reserved.
USB_DP	124	AIO	USB differential data (+)	Require differential impedance of 90 Ω . Test points must be reserved.
USB_DM	127	AIO	USB differential data (-)	
USB_SS_TX_P	115	AO	USB 3.2 SuperSpeed transmit (+)	Require differential impedance of 90 Ω . If unused, connect Rx to GND directly.
USB_SS_TX_M	112	AO	USB 3.2 SuperSpeed transmit (-)	
USB_SS_RX_P	119	AI	USB 3.2 SuperSpeed receive (+)	
USB_SS_RX_M	116	AI	USB 3.2 SuperSpeed receive (-)	
USB_ID	117	DI	USB ID detect	
OTG_PWR_EN	120	DO	OTG power control	

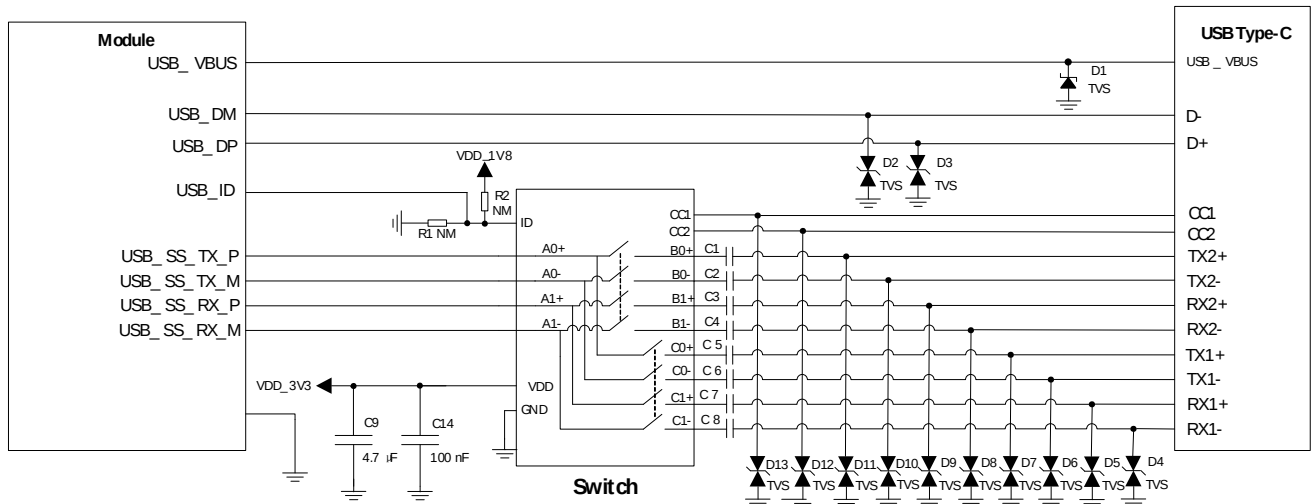
It is recommended to use USB 2.0 interface for firmware upgrading and reserve test points for debugging in your designs.

Figure 15: Reference Design of USB Interface



To ensure the signal integrity of USB data transmission, you should place C1 and C2 close to the module, place C3, C4 close to the host, and place resistors R1 to R4 close to each other. Moreover, keep extra stubs of trace as short as possible.

Figure 16: Reference Design of USB Type-C Interface



Type-C interface USB_VBUS can charge the battery through the external charging circuit, and can also be used for module's USB insertion detection. Input voltage of the USB_VBUS power supply ranges from 4.2 V to 15 V. The voltage should be adjusted for high-voltage charging through divider circuit and the recommended value is 5.0 V. The module supports charging management of a single Li-ion battery. Different charging parameters need to be set for batteries with different capacities. Meanwhile, the module also supports USB OTG mode. When USB_ID is held at high level by default, the module acts as USB slave device. When USB_ID is grounded, the module acts as USB master device. USB_VBUS pin of the charging IC is the OTG power output.

To ensure performance, you should follow the following principles when designing USB interface:

- Route USB signal traces as differential pairs with surrounded ground. The impedance of USB 2.0/3.2 differential trace is 90 Ω.

- For USB 3.2 Gen 2 signal traces, the trace length should be less than 80 mm, and the length matching of each differential data pair (Tx/Rx) should be less than 0.125 mm.
- For USB 2.0 signal traces, the trace length should be less than 150 mm, and the differential data pair matching (P/M) should be less than 0.5 mm.
- Route USB differential traces at the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. For signal traces, provide clearance from power supply traces, crystal-oscillators, magnetic devices, sensitive signals such as RF signals, analog signals, noisy signals generated by clock, and DC-DC.
- Pay attention to the impact caused by stray capacitance of the ESD protection component on USB data lines. Typically, the stray capacitance should be less than 3.0 pF for USB 2.0, and less than 0.5 pF for USB 3.2 Gen 2.
- If possible, reserve one 0 Ω resistor on USB_DP and USB_DM traces respectively.

For more details about the USB specifications, visit <http://www.usb.org/home>.

Table 13: USB Interface Trace Length Inside the Module (Unit: mm)

Pin Name.	Pin No.	Length	Length Mismatch
USB_DM	127	27.48	-0.05
USB_DP	124	27.53	
USB_SS_RX_M	116	26.31	-0.08
USB_SS_RX_P	119	26.39	
USB_SS_TX_M	112	25.12	0.11
USB_SS_TX_P	115	25.01	

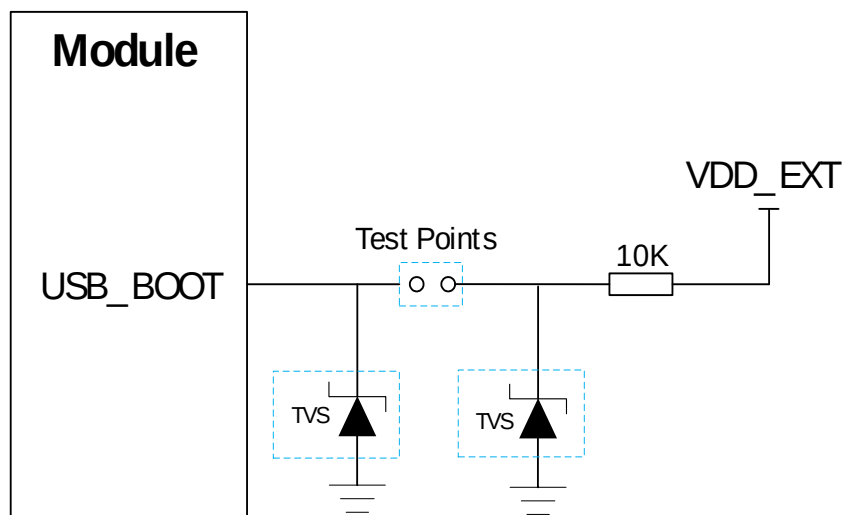
4.2. USB_BOOT

The module provides a USB_BOOT for forced download. Pulling up USB_BOOT to VDD_EXT before turning on the module, and then the module will enter forced download mode. In this mode, the module supports firmware upgrade over USB 2.0 interface.

Table 14: Pin Description of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	125	DI	Force the module into download mode	A test point is recommended to be reserved.

Figure 17: Reference Design of USB_BOOT



NOTE

It is not recommended to pull up USB_BOOT to 1.8 V before powering up VBAT. Directly connecting the test point as shown in the above figure can manually force the module to enter download mode.

4.3. (U)SIM Interfaces

The (U)SIM interfaces meet ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V (U)SIM card is supported, and Dual SIM Single Standby function is supported.

Table 15: Pin Description of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description
USIM1_VDD	96	PO	(U)SIM1 card power supply
USIM1_DATA	97	DIO	(U)SIM1 card data
USIM1_CLK	99	DO	(U)SIM1 card clock
USIM1_RST	100	DO	(U)SIM1 card reset
USIM1_DET	101	DI	(U)SIM1 card hot-plug detect
USIM2_VDD	103	PO	(U)SIM2 card power supply
USIM2_DATA	104	DIO	(U)SIM2 card data
USIM2_CLK	107	DO	(U)SIM2 card clock
USIM2_RST	108	DO	(U)SIM2 card reset

USIM2_DET

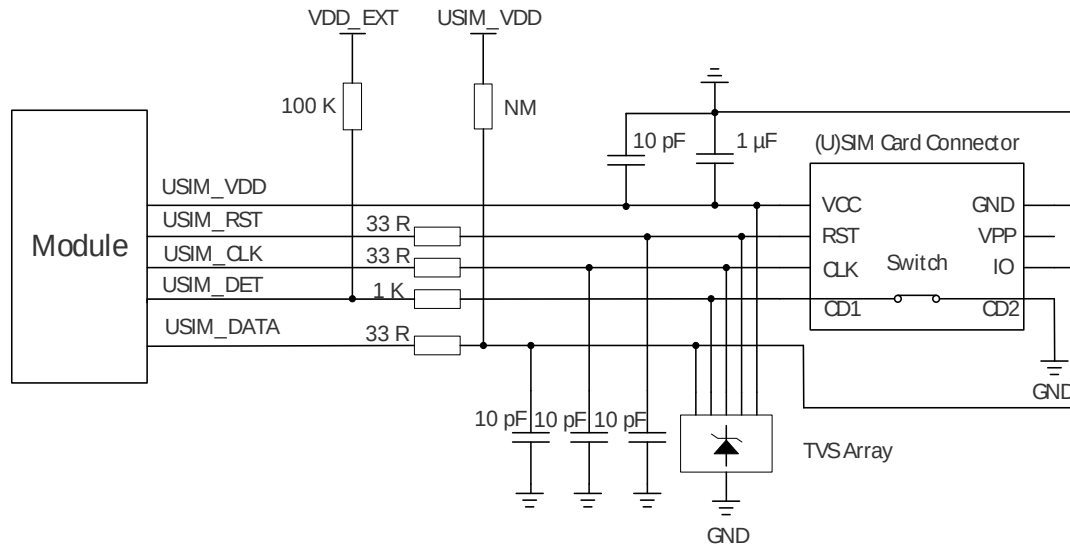
105

DI

(U)SIM2 card hot-plug detect

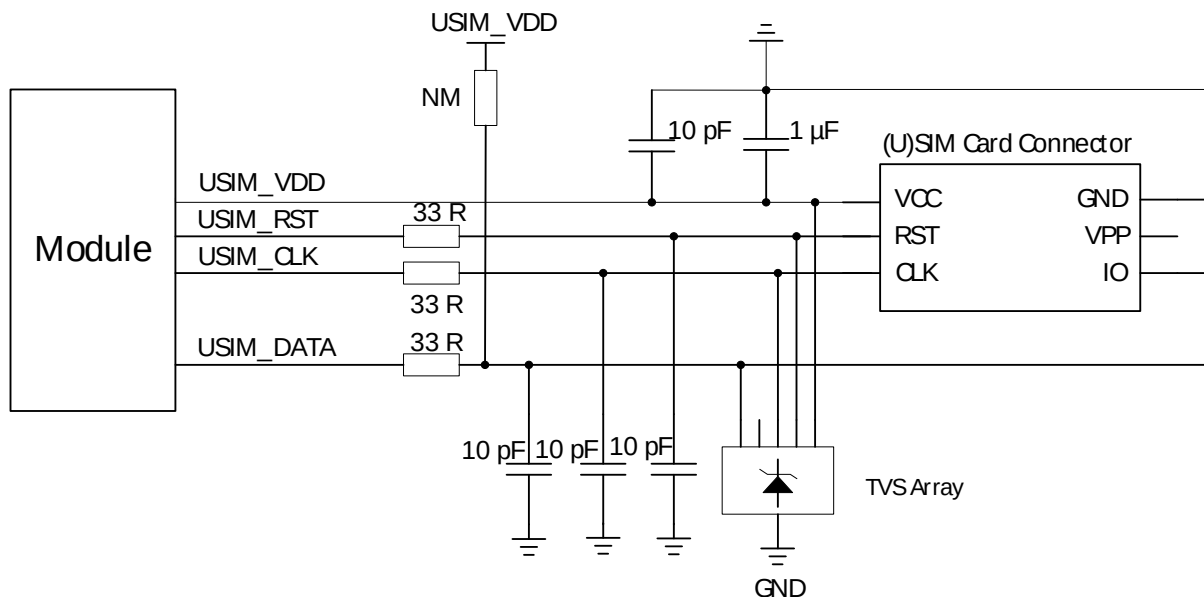
The module supports (U)SIM card hot-plug via the USIM_DET pin, which is a level-triggered pin.

Figure 18: Reference Design of (U)SIM Interface with an 8-pin (U)SIM Card Connector



If the function of (U)SIM card hot-plug is not needed, keep USIM_DET disconnected.

Figure 19: Reference Design of (U)SIM Interface with a 6-pin (U)SIM Card Connector



To enhance the reliability and availability of the (U)SIM card in applications, you should follow the principles below in the (U)SIM circuit design:

- Place the (U)SIM card connector close to the module. Keep the trace length less than 200 mm if possible.
- Route (U)SIM card traces at the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. For signal traces, provide clearance from power supply traces, crystal-oscillators, magnetic devices, sensitive signals such as RF signals, analog signals, noisy signals generated by clock and DC-DC.
- Ensure the tracing between the (U)SIM card connector and the module is short and wide. Keep the trace width of ground and USIM_VDD at least 0.5 mm to maintain the same electric potential.

- To avoid cross-talk between USIM_DATA and USIM_CLK, keep the traces away from each other and shield them with surrounded ground.
- To offer better ESD protection, you can add a TVS array of which the parasitic capacitance should be less than 45 pF. Add 33 Ω resistors in series between the module and the (U)SIM card connector to facilitate debugging. Additionally, add 10 pF capacitors in parallel among USIM_DATA, USIM_CLK and USIM_RST signal traces to filter out RF interference.

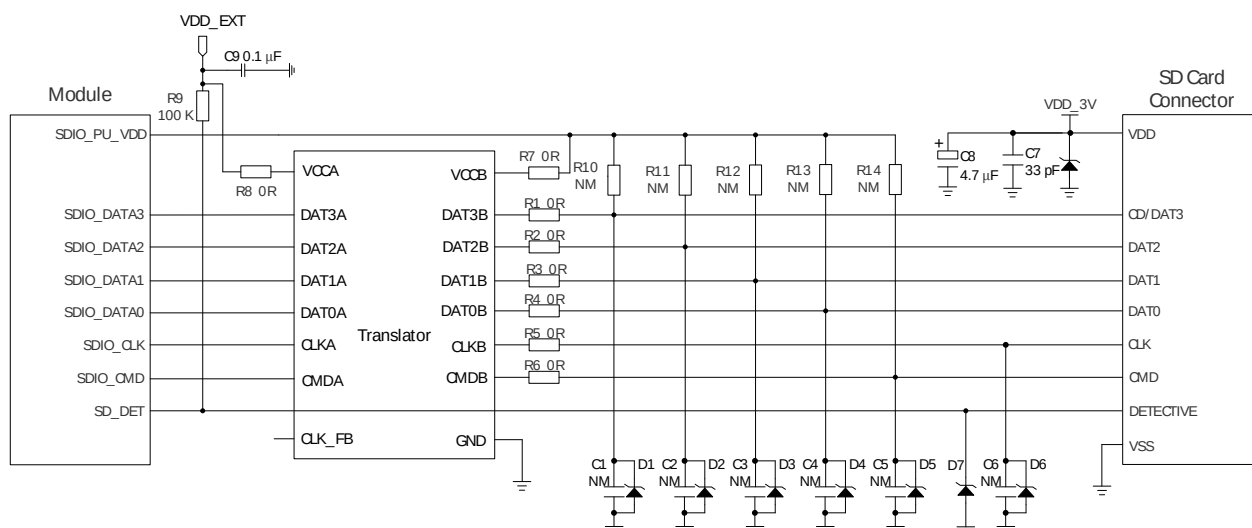
4.4. SDIO Interface

The module provides one SDIO interface which supports SD 3.0 protocol.

Table 16: Pin Description of SDIO Interface

Pin Name	Pin No.	I/O	Description
SDIO_CLK	365	DO	SDIO clock
SDIO_CMD	369	DIO	SDIO command
SDIO_DATA0	370	DIO	SDIO data bit 0
SDIO_DATA1	362	DIO	SDIO data bit 1
SDIO_DATA2	361	DIO	SDIO data bit 2
SDIO_DATA3	366	DIO	SDIO data bit 3
SD_DET	374	DI	SD card hot-plug detect
SDIO_PWR_EN	363	DO	SDIO power supply enable
SDIO_PU_VDD	373	PO	SD card IO pull-up power supply

Figure 20: Reference Design of SDIO Interface



To ensure communication performance, the following conditions should be taken into considerations when designing SDIO interface:

- The voltage range of VDD_3V is 2.7–3.6 V and it should provide a current up to 800 mA. SDIO_PU_VDD can provide up to 200 mA current.
- To avoid the impact of jitter, pull up SDIO_CMD and SDIO_DATA[0:3] to SDIO_PU_VDD. Resistance of these pull-up resistors (R10–R14) can be 10–100 k Ω . If there is a pull-up resistor inside the voltage-level translator, an external pull-up resistor is not needed.
- To enhance signal quality, add 0 Ω resistors R1–R6 in series and bypass capacitors C1–C6 (not mounted by default) between the module and the SD card connector. All resistors and bypass capacitors should be placed close to the connector.
- Add a TVS component with capacitance value of less than 3 pF on each SD card pin for better ESD protection.
- It is important to route SDIO signal traces at the inner-layer of the PCB and with surrounded ground. The impedance of SDIO signal trace is 50 Ω $\pm$ 10 %.
- Keep SDIO signal traces far away from power supply traces, crystal-oscillators, magnetic devices, and sensitive signals such as RF signals, analog signals, as well as noisy signals generated by clock, and DC-DC.
- Keep the trace length matching between SDIO_CLK and SDIO_DATA[0:3]/SDIO_CMD less than 7.6 mm and the total routing length less than 102 mm. The total trace length inside the module is 41 mm, so the exterior total trace length should be less than 61 mm.
- Keep the adjacent trace clearance twice the trace width and the load capacitance of SDIO bus less than 5 pF.

NOTE

For SD 3.0 SDR104 mode, a sufficient current of up to 800 mA and a 4.7 μ F capacitor for the power supply is necessary.

4.5. UART Interfaces

The module provides three UART interfaces:

Table 17: UART Interfaces Information

UART Type	Baud Rate (Typ.)	Functions
-----------	------------------	-----------

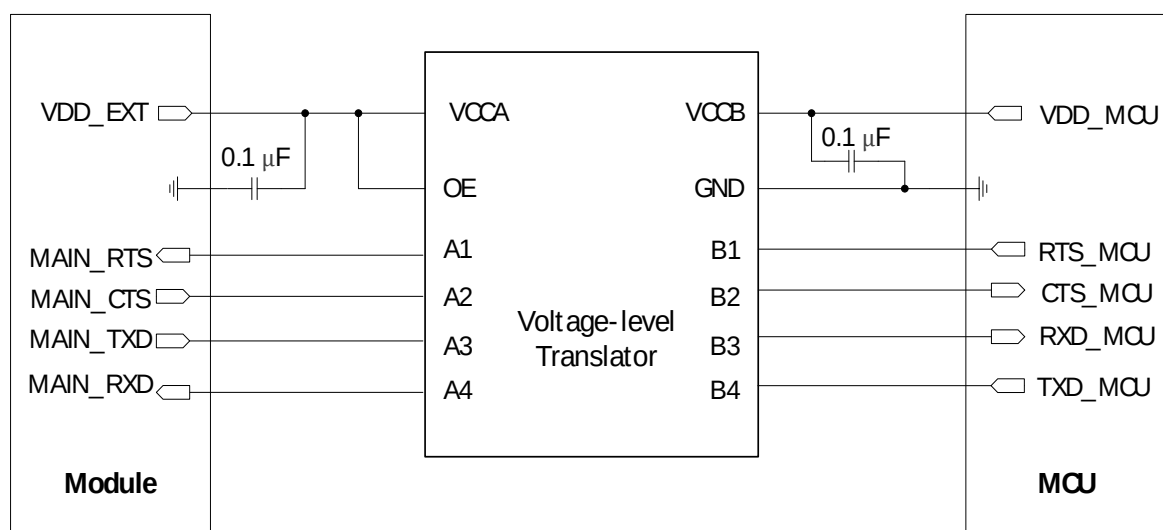
Main UART	115200 bps	Data transmission and AT command communication
Debug UART	921600 bps	Linux console and log output
Bluetooth UART	115200 bps	Bluetooth communication

Table 18: Pin Description of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	303	DO	Clear to send signal from the module	Connect to the MCU's CTS.
MAIN_RTS	306	DI	Request to send signal to the module	Connect to the MCU's RTS.
MAIN_RXD	300	DI	Main UART receive	
MAIN_TXD	302	DO	Main UART transmit	
BT_TXD	41	DO	Bluetooth UART transmit	
BT_RXD	49	DI	Bluetooth UART receive	
BT_RTS	45	DI	Request to send signal to the module	Connect to the Wi-Fi&Bluetooth module's RTS.
BT_CTS	53	DO	Clear to send signal from the module	Connect to the Wi-Fi&Bluetooth module's CTS.
DBG_RXD	309	DI	Debug UART receive	Test points must be reserved.
DBG_TXD	305	DO	Debug UART transmit	

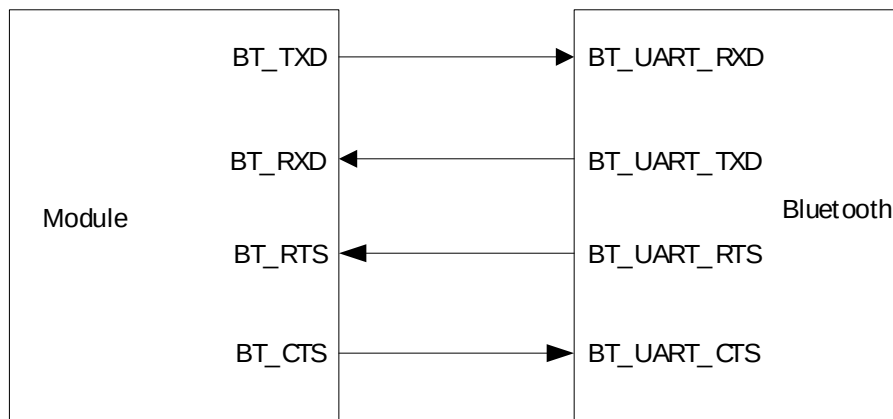
The module provides 1.8 V UART. You can use a voltage-level translator between the module and MCU's UART if the MCU is equipped with a 3.3 V UART.

Figure 21: Reference Design of UART Interface with Voltage-level Translator (Main UART)



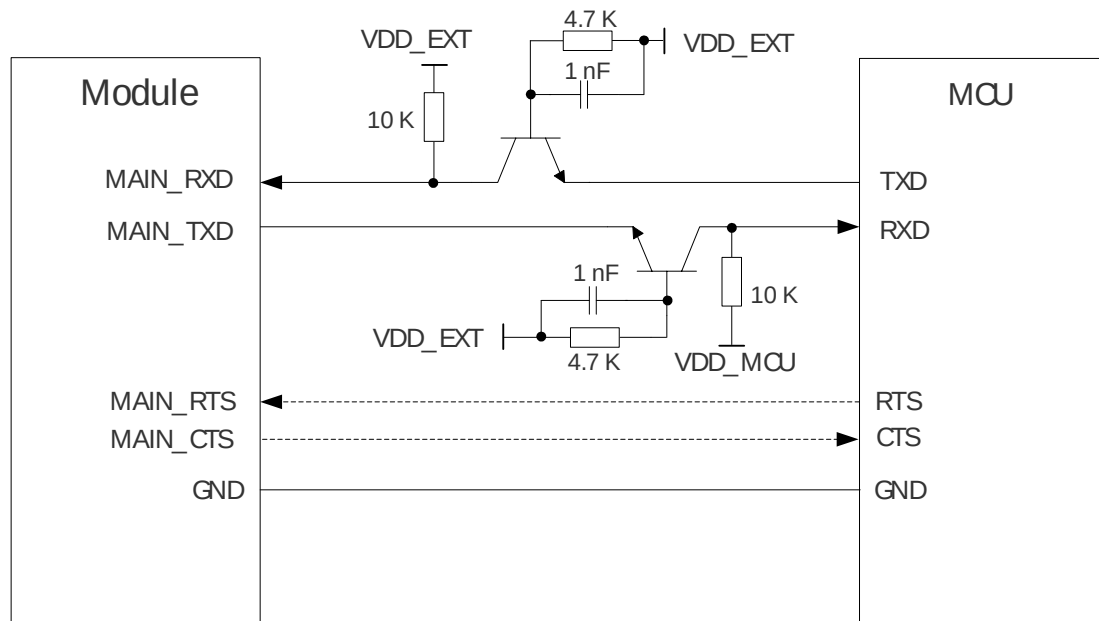
The following figure illustrates the reference design for Bluetooth UART interface connection between HMT89 series and Wi-Fi/Bluetooth module.

Figure 22: Bluetooth UART Interface Connection



Another example of level-shifting circuit is shown as below. For the design of input/output circuits in dotted lines, see that shown in solid lines, but pay attention to the direction of the connection.

Figure 23: Reference Design of UART Interface with Transistor Level-shifting Circuit (Main UART)



NOTE

1. Transistor level-shifting circuit above is not suitable for applications with baud rates exceeding 460 kbps.
2. Note that the module's CTS is connected to the MCU/Wi-Fi&Bluetooth module's CTS, and the module's RTS is connected to the MCU/Wi-Fi&Bluetooth module's RTS.
3. The level-shifting circuits (**Figure 21** and **Figure 23**) take the main UART as an example. The circuits of the debug UART and the Bluetooth UART are connected in the same way as the main UART, but the Bluetooth UART is connected to the Wi-Fi&Bluetooth module.

4.6. I2C Interfaces

The module provides four I2C interfaces:

Table 19: Pin Description of I2C Interfaces

Pin Name	Pin No.	Alternate Function	I/O	Description	Comment
TP_I2C_SCL	359	-	OD	TP I2C clock	External pull-up resistor is required. 1.8 V only. If unused, keep them open.
TP_I2C_SDA	358	-	OD	TP I2C data	
I2C4_SCL	133	-	OD	I2C serial clock	
I2C4_SDA	129	-	OD	I2C serial data	
SPI0_CS	364	I2C_SDA2	OD	I2C serial data	External pull-up resistor is required. 1.8 V only. If unused, keep them open.
SPI0_CLK	367	I2C_SCL2	OD	I2C serial clock	
SPI0_MOSI	371	I2C_SCL3	OD	I2C serial data	
SPI0_MISO	368	I2C_SDA3	OD	I2C serial clock	

NOTE

For more details about pin multiplexing, see **document 6**.

4.7. PCM Interfaces

The module provides two PCM interfaces:

Table 20: Pin Description of PCM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM0_SYNC	69	DIO	PCM data frame sync	In master mode, they are output signals. In slave mode, they are input signals. If unused, keep them open.
PCM0_CLK	81	DIO	PCM clock	
PCM0_DIN	77	DI	PCM data input	If unused, keep them open.
PCM0_DOUT	73	DO	PCM data output	
PCM1_SYNC	325	DIO	PCM data frame sync	In master mode, they are output signals. In slave mode, they are input signals. If unused, keep them open.
PCM1_CLK	322	DIO	PCM clock	
PCM1_DIN	318	DI	PCM data input	If unused, keep them open.

PCM1_DOUT	317	DO	PCM data output
I2S0_MCLK	314	DO	I2S0 master clock
I2S4_MCLK	65	DO	I2S4 master clock

NOTE

PCM1 is used for SLIC by default.

4.8. ADC Interfaces

The module provides 7 ADC interfaces. To improve the accuracy of ADC, the trace of ADC interface should be surrounded by ground.

Table 21: Pin Description of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	357	AI	General-purpose ADC interface	Max input 1.78 V. If unused, connect them to GND directly.
ADC1	312	AI	General-purpose ADC interface	
ADC2	316	AI	General-purpose ADC interface	
ADC3	320	AI	General-purpose ADC interface	
ADC4	324	AI	General-purpose ADC interface	
ADC5	210	AI	General-purpose ADC interface	
ADC6	214	AI	General-purpose ADC interface	

With **AT+QADC=<port>**, you can:

- **AT+QADC=0**: read the voltage value on ADC0
- **AT+QADC=1**: read the voltage value on ADC1
- **AT+QADC=2**: read the voltage value on ADC2
- **AT+QADC=3**: read the voltage value on ADC3
- **AT+QADC=4**: read the voltage value on ADC4
- **AT+QADC=5**: read the voltage value on ADC5
- **AT+QADC=6**: read the voltage value on ADC6

For more details about the **AT+QADC**, see **Chapter 9.3**.

Table 22: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
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ADC[0:6] input voltage range	0.04	-	1.78	V
ADC resolution	-	15	-	bits

NOTE

1. The input voltage of every ADC interface should not exceed its corresponding voltage range.
2. It is prohibited to directly supply any voltage to ADC interface when the module is not powered by the VBAT.
3. It is recommended to use resistor divider circuit for ADC interface application.

4.9. USXGMII Interfaces

The module includes two integrated Ethernet MAC with two USXGMII interfaces and one MDIO management interface. Key features of the USXGMII interfaces are shown below:

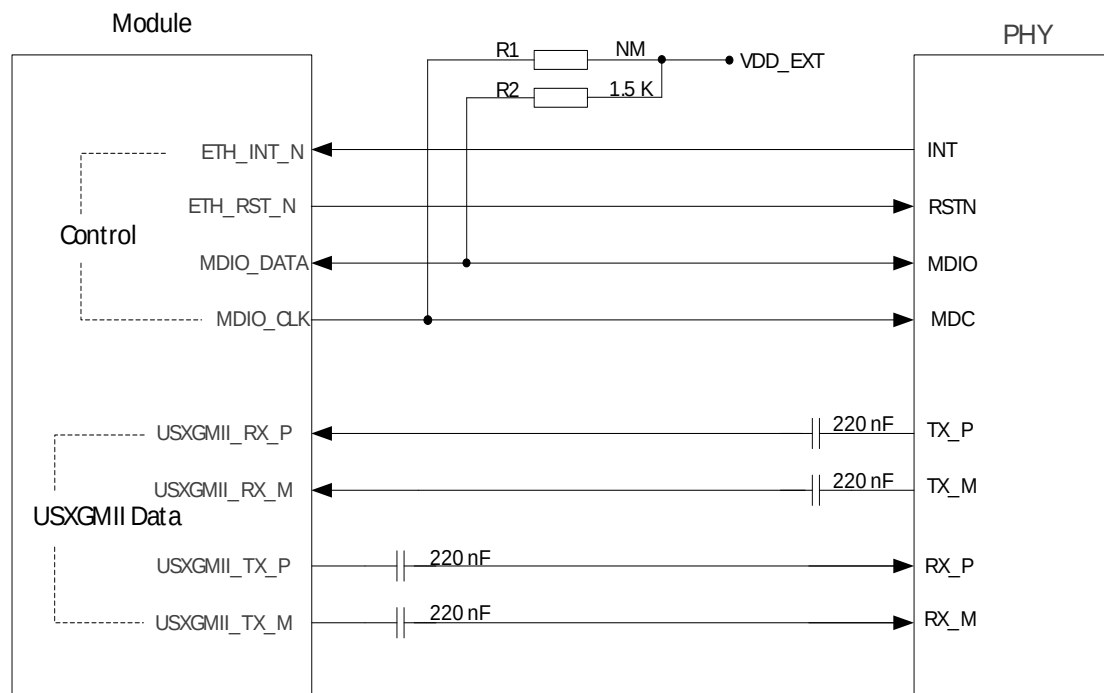
- IEEE 802.3x compliant
- Full duplex mode for 100 Mbps, 1000 Mbps, 2500 Mbps, 5000 Mbps and 10000 Mbps.
- Can be connected to an external Ethernet Switch or PHY, such as AN8855H, EN8811HN and AQR113C.
- The MDIO management interface and USXGMII interrupt/reset signals support 1.8 V power domain

Table 23: Pin Definition of USXGMII Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MDIO_DATA	384	DIO	MDIO data	
MDIO_CLK	387	DO	MDIO clock	
ETH0_INT_N	388	DI	Ethernet PHY 0 interrupt	
ETH0_RST_N	391	DO	Ethernet PHY 0 reset	
ETH1_INT_N	380	DI	Ethernet PHY 1 interrupt	
ETH1_RST_N	383	DO	Ethernet PHY 1 reset	
USXGMII0_CLK_M	397	AO	USXGMII0 clock (-)	
USXGMII0_CLK_P	399	AO	USXGMII0 clock (+)	
USXGMII0_TX_M	400	AO	USXGMII0 transmit (-)	Require differential impedance of 100 Ω. If unused, connect Rx to GND directly.
USXGMII0_TX_P	401	AO	USXGMII0 transmit (+)	
USXGMII0_RX_P	402	AI	USXGMII0 receive (+)	
USXGMII0_RX_M	403	AI	USXGMII0 receive (-)	

USXGMII1_CLK_M	382	AO	USXGMII1 clock (-)
USXGMII1_CLK_P	385	AO	USXGMII1 clock (+)
USXGMII1_RX_P	386	AI	USXGMII1 receive (+)
USXGMII1_RX_M	389	AI	USXGMII1 receive (-)
USXGMII1_TX_P	390	AO	USXGMII1 transmit (+)
USXGMII1_TX_M	393	AO	USXGMII1 transmit (-)

Figure 24: Reference Circuit of USXGMII Interface with PHY Application



To enhance the reliability and availability of your application, please follow the criteria below in the Ethernet PHY circuit design:

- Keep USXGMII data and control signals away from RF and VBAT traces.
- Keep the maximum trace length less than 200 mm and keep length matching within each differential pair less than 0.125 mm.
- The differential impedance of USXGMII data traces is $100 \Omega \pm 10\%$.
- To minimize crosstalk, the distance between separate adjacent pairs on the same layer must be equal to or larger than 1 mm.
- Less than 2 vias should be designed in each differential pair.
- Reserve enough GND planes between MDC and MDIO to prevent crosstalk.
- 0.22 μ F AC coupling capacitors should be placed close to the transmitter source.

Table 24: USXGMII Interface Trace Length Inside the Module (Unit: mm)

Pin Name.	Pin No.	Length (mm)	Length Mismatch
USXGMII0_CLK_M	397	21.71	-0.07

USXGMII0_CLK_P	399	21.78	
USXGMII0_TX_M	400	21.54	-0.03
USXGMII0_TX_P	401	21.57	
USXGMII0_RX_P	402	22.86	-0.02
USXGMII0_RX_M	403	22.84	
USXGMII1_CLK_M	382	27.70	0.06
USXGMII1_CLK_P	385	27.64	
USXGMII1_RX_P	386	25.02	-0.03
USXGMII1_RX_M	389	24.99	
USXGMII1_TX_P	390	24.49	0.08
USXGMII1_TX_M	393	24.57	

4.10. LCM Interface

The module provides an LCM interface and also supports 4-wire SPI communication. LCM interface of the module has a multiplexing relationship, and the function can be realized through DBI-C and other interfaces.

Table 25: Pin Description of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
LSDI	153	DI	SPI serial input data	
LSA0	161	DO	Indicate transmission of data or command	
LSCE0B	157	DO	SPI chip select	Pins 150,153, 157, 161,165 and 169 are belong to DBI-C interface.
LSRSTB	150	DO	SPI reset	
LSCK	169	DO	SPI serial clock	
LSDA	165	DO	SPI serial output data	
PWM	131	DO	PWM output	For LCD only
LCD_TE	149	DI	LCM tearing effect	
LCD_RST	141	DO	LCM reset	

The following figures show the reference design for LCM interface.

Figure 25: Reference Circuit Design for LCM Interface

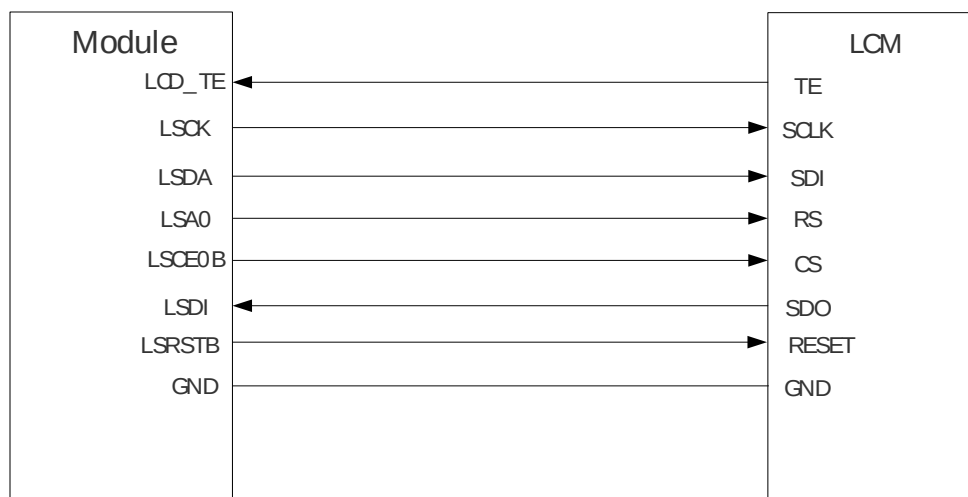
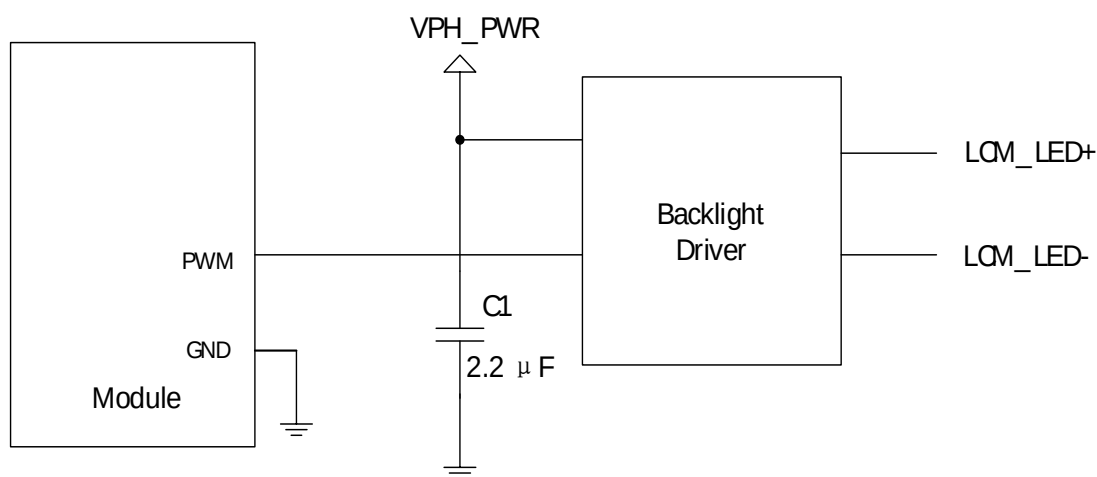


Figure 26: Reference Circuit of LCM External Backlight Driver



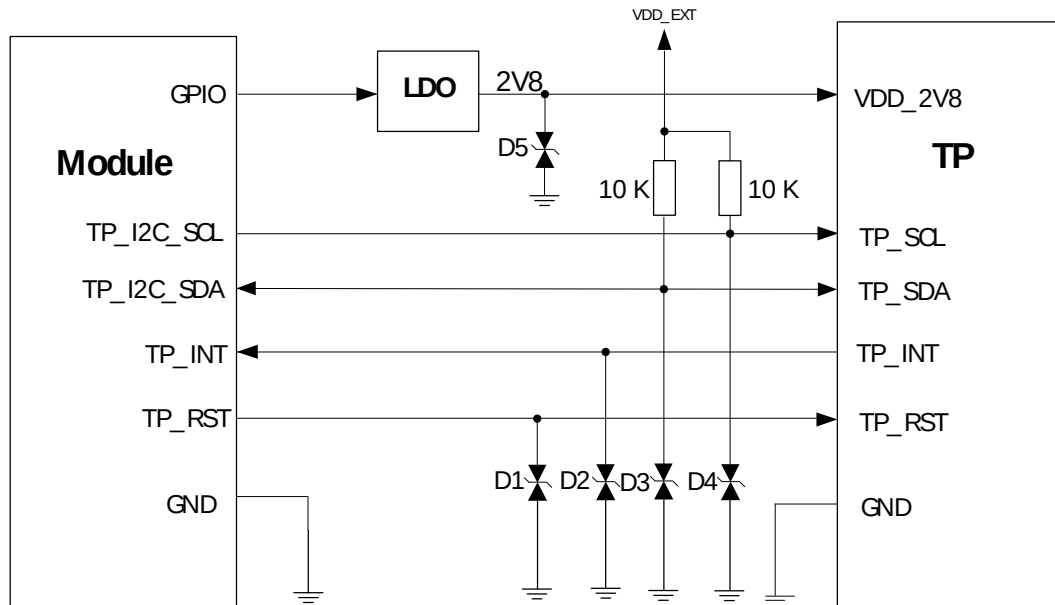
4.11. Touch Panel Interface

The module provides one group of I2C interface for connection with touch panel (TP) by default. Also, reset pin and interrupt pin are provided.

Table 26: Pin Description of Touch Panel Interface

Pin Name	Pin No.	I/O	Description	Comment
TP_I2C_SCL	359	OD	TP I2C clock	External pull-up resistor is required. 1.8 V only. If unused, keep it open.
TP_I2C_SDA	358	OD	TP I2C data	
TP_RST	351	DO	TP reset	
TP_INT	352	DI	TP interrupt	

Figure 27: Reference Design of Touch Panel Interface



NOTE

The power domain of touch panel interface is 1.8 V, and pay attention to the level match in design.

4.12. Matrix Keypad Interfaces^{dev}

The matrix keypad interfaces support 3 × 3 of nine keypads. They can be used as general GPIOs.

Table 27: Pin Description of Matrix Keypad Interfaces

Pin Name	Pin No.	I/O	Description	Comment
KPCOL0	146	DIO	Matrix keypad column0	Do not pull it low before startup, otherwise it will force the module into download mode.
KPCOL1	142	DIO	Matrix keypad column1	
KPCOL2	138	DIO	Matrix keypad column2	
KPROW0	134	DIO	Matrix keypad row0	
KPROW1	130	DIO	Matrix keypad row1	

KPROW2	126	DIO	Matrix keypad row2
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4.13. PCIe Interfaces

The module provides three PCIe interfaces. PCIe1 is in compliance with *PCI Express Base Specification Revision 4.0*. PCIe2 and PCIe3 are in compliance with *PCI Express Base Specification Revision 3.0*. Key features of the PCIe interface are as below:

- Data rate: PCIe1 16 Gbps/lane, PCIe2/3 8 Gbps/lane.
- Can be used to connect to Wi-Fi IC

Table 28: Pin Description of PCIe Interfaces

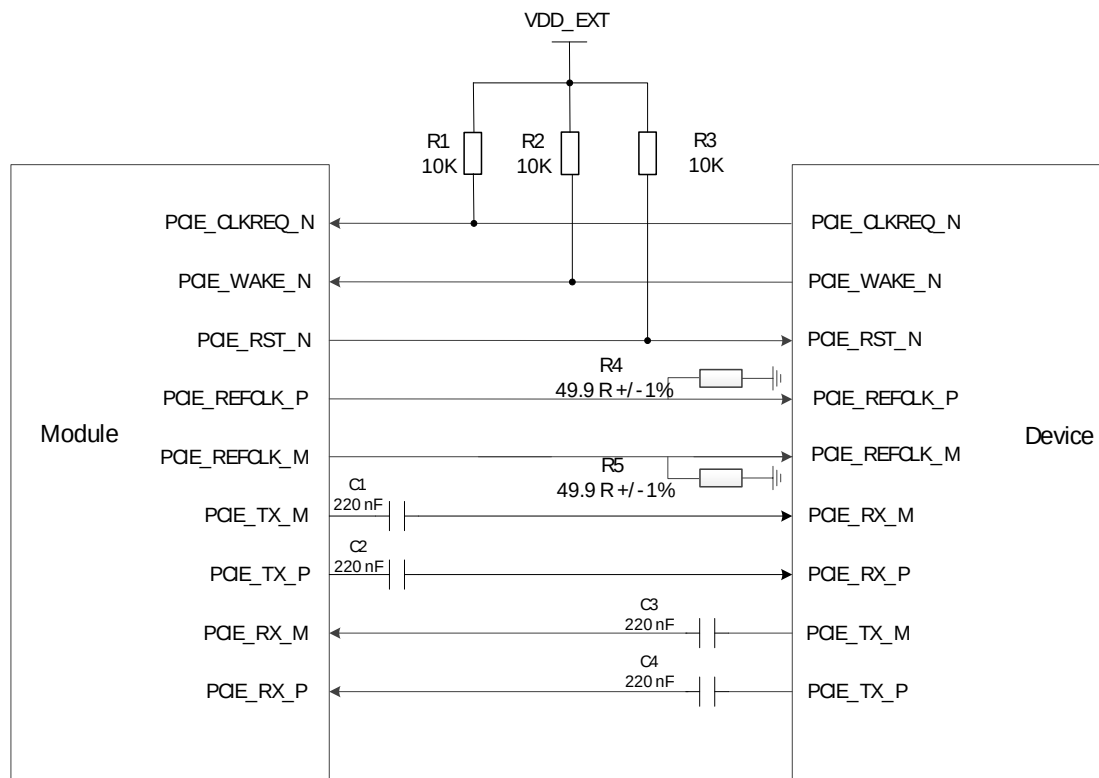
Pin Name	Pin No.	I/O	Description	Comment
PCIE1_REFCLK_M	50	AO	PCIe1 reference clock (-)	The REFCLK requires differential impedance of 100 Ω . The Tx/Rx requires differential impedance of 85 Ω . PCIe Gen 4 compliant. If unused, connect Rx to GND directly.
PCIE1_REFCLK_P	51	AO	PCIe1 reference clock (+)	
PCIE1_RX0_M	42	AI	PCIe1 receive 0 (-)	
PCIE1_RX0_P	43	AI	PCIe1 receive 0 (+)	
PCIE1_TX0_M	39	AO	PCIe1 transmit 0 (-)	
PCIE1_TX0_P	38	AO	PCIe1 transmit 0 (+)	
PCIE1_RX1_M	55	AI	PCIe1 receive 1 (-)	
PCIE1_RX1_P	54	AI	PCIe1 receive 1 (+)	
PCIE1_TX1_M	59	AO	PCIe1 transmit 1 (-)	
PCIE1_TX1_P	58	AO	PCIe1 transmit 1 (+)	
PCIE1_RST_N	52	DO	PCIe1 reset	
PCIE1_WAKE_N	48	DI	PCIe1 wake up	
PCIE1_CLKREQ_N	44	DI	PCIe1 clock request	
PCIE2_REFCLK_M	22	AO	PCIe2 reference clock (-)	The REFCLK requires differential impedance of 100 Ω . The Tx/Rx requires differential impedance of 85 Ω . PCIe Gen 3 compliant. If unused, connect Rx to GND directly.
PCIE2_REFCLK_P	23	AO	PCIe2 reference clock (+)	
PCIE2_RX0_M	14	AI	PCIe2 receive 0 (-)	
PCIE2_RX0_P	15	AI	PCIe2 receive 0 (+)	
PCIE2_TX0_M	11	AO	PCIe2 transmit 0 (-)	
PCIE2_TX0_P	10	AO	PCIe2 transmit 0 (+)	
PCIE2_RX1_M	27	AI	PCIe2 receive 1 (-)	

PCIE2_RX1_P	26	AI	PCIE2 receive 1 (+)
PCIE2_TX1_M	31	AO	PCIE2 transmit 1 (-)
PCIE2_TX1_P	30	AO	PCIE2 transmit 1 (+)
PCIE2_RST_N	24	DO	PCIE2 reset
PCIE2_WAKE_N	20	DI	PCIE2 wake up
PCIE2_CLKREQ_N	16	DI	PCIE2 clock request
PCIE3_REFCLK_M	78	AO	PCIE3 reference clock (-)
PCIE3_REFCLK_P	79	AO	PCIE3 reference clock (+)
PCIE3_RX0_M	70	AI	PCIE3 receive 0 (-)
PCIE3_RX0_P	71	AI	PCIE3 receive 0 (+)
PCIE3_TX0_M	67	AO	PCIE3 transmit 0 (-)
PCIE3_TX0_P	66	AO	PCIE3 transmit 0 (+)
PCIE3_RX1_M	83	AI	PCIE3 receive 1 (-)
PCIE3_RX1_P	82	AI	PCIE3 receive 1 (+)
PCIE3_TX1_M	86	AO	PCIE3 transmit 1 (-)
PCIE3_TX1_P	85	AO	PCIE3 transmit 1 (+)
PCIE3_RST_N	80	DO	PCIE3 reset
PCIE3_WAKE_N	76	DI	PCIE3 wake up
PCIE3_CLKREQ_N	72	DI	PCIE3 clock request

The REFCLK requires differential impedance of 100 Ω .
The Tx/Rx require differential impedance of 85 Ω .
PCIE Gen 3 compliant.
If unused, connect Rx to GND directly.

The following figure illustrates the PCIe interface connection.

[*Figure 28: Reference Design of PCIe Interface Connection*](#)



To ensure the signal integrity of the PCIe interface, place C1 and C2 near the module and place C3 and C4 near the PCIe device. Keep the traces as short as possible.

To ensure the PCIe interface design meets PCIe specifications, you should follow the principles below:

- Route PCIe signal traces (Tx/Rx/REFCLK) as differential pairs with surrounded ground. The differential impedance should be $85 \Omega \pm 10\%$ of Tx/Rx and $100 \Omega \pm 10\%$ of REFCLK.
- For PCIe signal traces, the recommended maximum length for Tx and Rx differential data pairs should be less than 200 mm, and the intra-lane length matching of Tx and Rx differential data pairs should be less than 0.125 mm.
- The spacing between Tx and Rx signal traces and that among Tx, Rx and all other signal traces should be wider than 3 and 4 times of the trace width respectively.
- Add capacitors in series on Tx/Rx traces to immune from leakage current.
- Route PCIe differential signal traces at the inner-layer of PCB, and surround the traces with ground on that layer and with ground planes above and below. Meanwhile, protect them from interferences such as crystal-oscillators, VBAT traces, and RF signal traces.
- For the PCIe_REFCLK pairs, add resistors near the slot (EP) side and the recommended resistor value is $49.9 \Omega \pm 1\%$.

Table 29: PCIe Interface Trace Length Inside the Module (Unit: mm)

Pin Name	Pin No.	Length (mm)	Length Mismatch
PCIE1_REFCLK_M	50	12.68	-0.12
PCIE1_REFCLK_P	51	12.80	
PCIE1_RX0_M	42	13.20	0.09
PCIE1_RX0_P	43	13.11	
PCIE1_TX0_M	39	12.67	0.04

PCIE1_TX0_P	38	12.63	
PCIE1_RX1_M	55	12.66	
PCIE1_RX1_P	54	12.66	0.00
PCIE1_TX1_M	59	12.62	
PCIE1_TX1_P	58	12.63	-0.01
PCIE2_REFCLK_M	22	13.83	
PCIE2_REFCLK_P	23	13.87	-0.04
PCIE2_RX0_M	14	14.08	
PCIE2_RX0_P	15	13.98	0.10
PCIE2_TX0_M	11	14.22	
PCIE2_TX0_P	10	14.32	-0.10
PCIE2_RX1_M	27	13.87	
PCIE2_RX1_P	26	13.92	-0.05
PCIE2_TX1_M	31	13.84	
PCIE2_TX1_P	30	13.85	-0.01
PCIE3_REFCLK_M	78	18.67	
PCIE3_REFCLK_P	79	18.67	0.00
PCIE3_RX0_M	70	18.61	
PCIE3_RX0_P	71	18.61	0.00
PCIE3_TX0_M	67	18.59	
PCIE3_TX0_P	66	18.56	0.03
PCIE3_RX1_M	83	19.01	
PCIE3_RX1_P	82	19.02	-0.01
PCIE3_TX1_M	86	19.08	
PCIE3_TX1_P	85	19.04	0.04

4.14. SPI Interfaces

The module provides three SPI interfaces which support both master and slave modes with a maximum

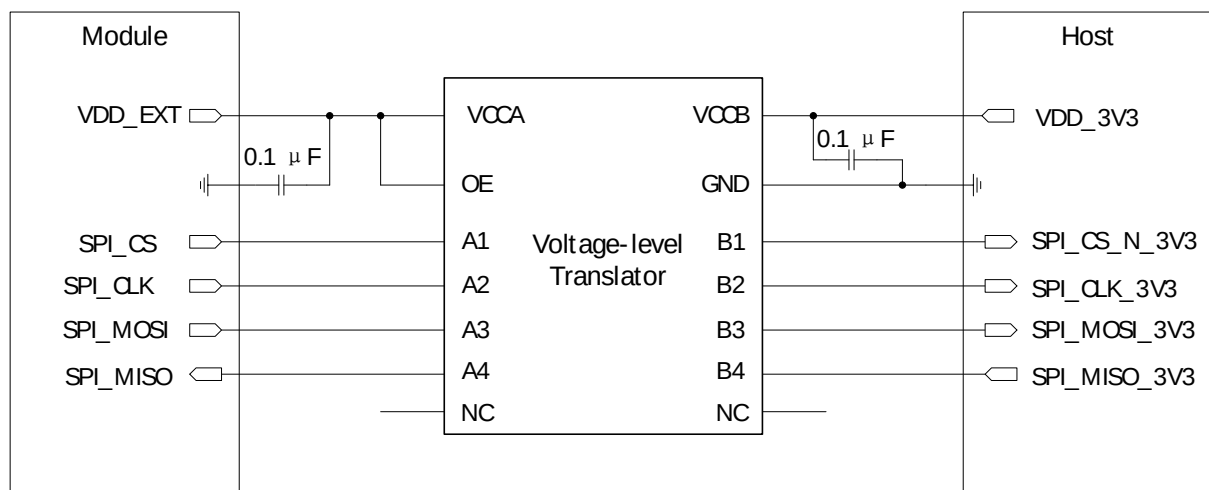
clock frequency up to 52 MHz.

Table 30: Pin Description of SPI Interfaces

Pin Name	Pin No.	I/O	Description	Comment
SPI0_CS	364	DO	SPI0 chip select	
SPI0_CLK	367	DO	SPI0 clock	
SPI0_MOSI	371	DO	SPI0 master-out slave-in	
SPI0_MISO	368	DI	SPI0 master-in slave-out	
SPI2_CS	376	DO	SPI2 chip select	
SPI2_CLK	377	DO	SPI2 clock	
SPI2_MOSI	375	DO	SPI2 master-out slave-in	
SPI2_MISO	378	DI	SPI2 master-in slave-out	
SPI3_CS	326	DO	SPI3 chip select	Recommended for SLIC IC communication.
SPI3_CLK	329	DO	SPI3 clock	
SPI3_MOSI	333	DO	SPI3 master-out slave-in	
SPI3_MISO	330	DI	SPI3 master-in slave-out	

The module provides 1.8 V SPI interfaces. A voltage-level translator should be used between the module and the host if the application is equipped with a 3.3 V processor or device interface. The following figure shows a reference design:

Figure 29: Reference Design of SPI Interfaces with a Voltage-level Translator



4.15. Time Service and Repeater Interface

'Time service' means to provide time information for other devices or systems through standard or customized interfaces and protocols. Basic channels include shortwave, TV signals, cables, networks, satellites, and base stations.

'Repeater' is a kind of wireless signal relay device, which can amplify the base station signal and then transmits it to areas with weak signal coverage, to expand the network coverage.

With GNSS time service and repeater functions, the module can provide 1PPS pulse output and execute time service through AT commands based on baseline SIB9 system messages.

Table 31: Pin Description of Time Service and Repeater Interface

Pin Name	Pin No.	I/O	Description
GNSS_LNA_EN ^{dev}	313	DO	GNSS LNA enable control; 1PPS pulse output and frame synchronization

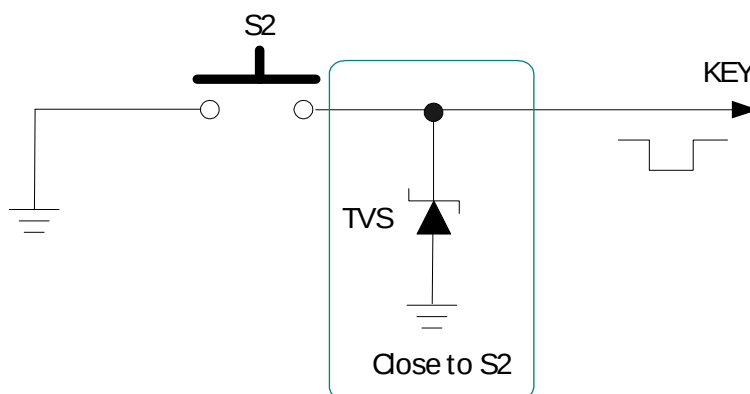
4.16. Control Signals

Table 32: Pin Description of Control Signals

Pin Name	Pin No.	I/O	Description	Comment
RESTORE_KEY	311	DI	Restore the module	
WPS_KEY	307	DI	Wi-Fi protected setup	

Reference circuit is shown as below.

Figure 30: Reference Circuit of Control KEY



4.16.1. WWAN/WLAN Control Interface

The module provides some WWAN/WLAN control interfaces for WLAN function.

Table 33: Pin Description of WWAN/WLAN Control Interface

Pin Name	Pin No.	I/O	Description	Comment
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WLAN_SYSRST_5G	21	DO	WLAN 5 GHz system reset	
WLAN_2.4G_EN ^{dev}	29	DO	WLAN 2.4 GHz function enable control	
WLAN_SYSRST_2.4G	25	DO	WLAN 2.4 GHz system reset	
WLAN_5G_EN ^{dev}	392	DO	WLAN 5 GHz function enable control	
BT_ACT_0 ^{dev}	61	DO	Coexistence interface for WWAN and WLAN	Used for WWAN/WLAN coexistence by default.
BT_PRI_0 ^{dev}	37	DO	Coexistence interface for WWAN and WLAN	
WLAN_ACT_0 ^{dev}	57	DI	Coexistence interface for WWAN and WLAN	
PTA_TX_0 ^{dev}	64	DO	Coexistence interface for WWAN and WLAN	
PTA_RX_0 ^{dev}	60	DO	Coexistence interface for WWAN and WLAN	
BT_ACT_1 ^{dev}	13	DO	Coexistence interface for WWAN and WLAN	
BT_PRI_1 ^{dev}	9	DO	Coexistence interface for WWAN and WLAN	
WLAN_ACT_1 ^{dev}	33	DI	Coexistence interface for WWAN and WLAN	
PTA_TX_1 ^{dev}	36	DO	Coexistence interface for WWAN and WLAN	
PTA_RX_1 ^{dev}	32	DO	Coexistence interface for WWAN and WLAN	

4.17. Indication Signals

Table 34: Pin Description of Indication Signals

Pin Name	Pin No.	I/O	Description	Comment
STATUS	331	OD	Indicate the module's operation status	PMIC_ISINK3
W_DISABLE#	335	OD	Indicate the module's airplane mode	PMIC_ISINK1
NET_STATUS	354	OD	Indicate the module's network activity status	PMIC_ISINK2
NET_MODE	327	DO	Indicate the module's network registration mode	
WIFI_MESH ^{dev}	315	DO	Indicate the Wi-Fi mesh function status	
USIM_LED	323	DO	Indicate the (U)SIM card function status	

VOIP_LED ^{dev}	319	DO	Indicate the VoIP function status
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4.17.1. Network Status Indication

The module provides two network status indication pins: the NET_MODE for the module's network registration status indication and the NET_STATUS for the module's network activity status indication. Both can drive corresponding LEDs.

Table 35: Network Status Indication Pin Level and Module Network Status

Pin Name	NET_MODE/NET_STATUS Level Status	Module Network Status
NET_MODE	Always high	Registered on network
	Always low	Others
	Blink slowly (200 ms high/1800 ms low)	Network searching
NET_STATUS	Blink slowly (1800 ms high/200ms low)	Idle
	Blink quickly (125 ms high/125 ms low)	Data transmission is ongoing
	Always high	Voice calling
	Always low	Minimum functionality mode

Reference circuit is shown as below.

Figure 31: Reference Circuit of NET_MODE Indicator

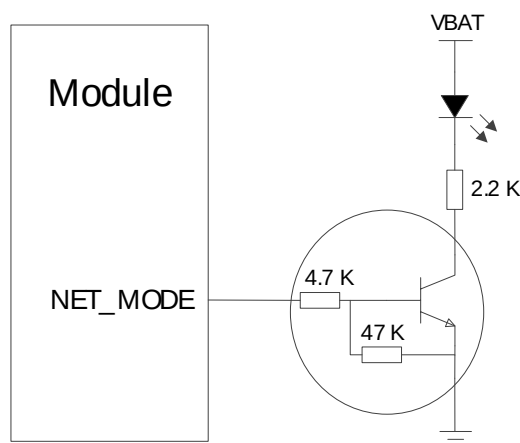
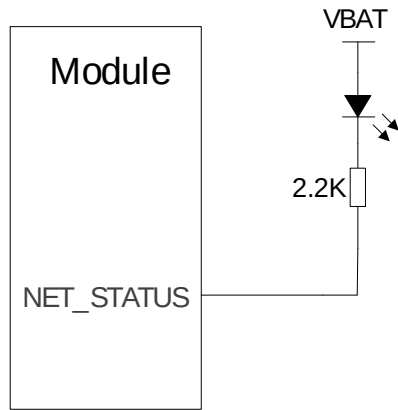


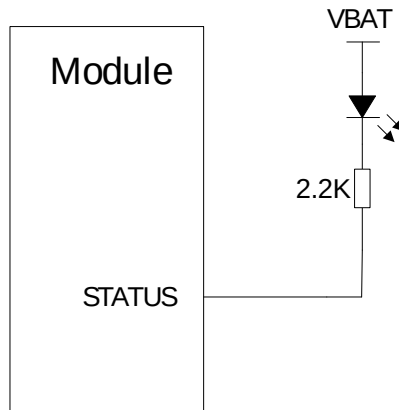
Figure 32: Reference Circuit of NET_STATUS Indicator



4.17.2. STATUS

The STATUS is used for indicating module's operation status. It will output low level when the module is turned on.

Figure 33: Reference Design of STATUS

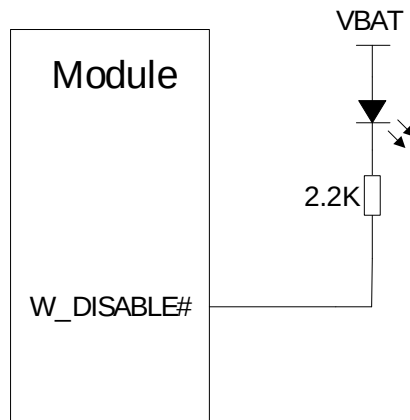


4.17.3. W_DISABLE#

The W_DISABLE# pin is an open drain output for indicating the module's airplane mode status. It will output low level when the module enters airplane mode successfully.

A reference circuit is shown as below.

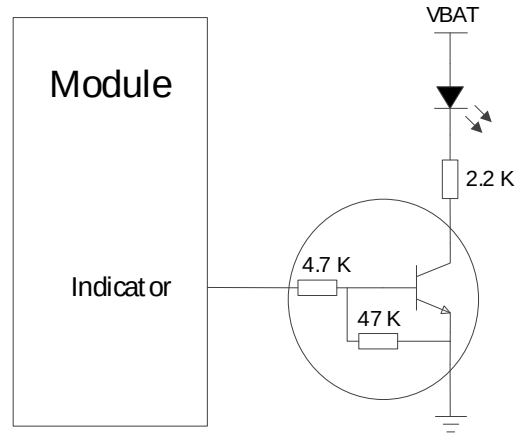
Figure 34: Reference Circuit of W_DISABLE# Indicator



4.17.4. Other Indication Signals

The WIFI_MESH^{dev}, USIM_LED and VOIP_LED^{dev} pins are output signals for indicating the functional state of the module. A reference circuit is shown as below.

Figure 35: Reference Circuit of Other Indicators



5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

Table 36: Pin Description of Cellular Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT0	191	AIO	Antenna 0 interface	50 Ω characteristic impedance
ANT1	199	AIO	Antenna 1 interface	
ANT2	208	AIO	Antenna 2 interface	
ANT3	220	AIO	Antenna 3 interface	
ANT4	232	AIO	Antenna 4 interface	
ANT5	244	AIO	Antenna 5 interface	
ANT6	256	AIO	Antenna 6 interface	
ANT7	268	AIO	Antenna 7 interface	

Table 37: HMT89-LD Cellular Antenna Interfaces Mapping

Pin Name	LTE	5G NR			LB (MHz)	MHB (MHz)	n77/n78 (MHz)	LAA (MHz)
		Refarming	n41	n77/n78				
ANT0	UHB TX1/PRX	-	-	TRX0	-	-	3300–4200	-
ANT1	MHB + B5/B26 TX1 LMHB DRX	MHB TX0 n5/n71 TX0 LMHB DRX	TX0/DRX	MIMO5 (HW Ready) ⁴	617–894	1695–2690	3300–4200	-
ANT2	UHB PRX1 LAA PRX	-	-	PRX1	-	-	3300–4200	5150–5925
ANT3	LMHB DRX1 B29 DRX	LMHB DRX1 n29 DRX	DRX1	MIMO4 (HW Ready) ⁴	617–894	1695–2690	3300–4200	-
ANT4	UHB DRX1 LAA DRX	-	-	DRX1	-	-	3300–4200	5150–5925
ANT5	LMHB PRX1 B29 PRX	LMHB PRX1 n29 PRX	PRX1	MIMO6 (HW Ready) ⁴	617–894	1695–2690	3300–4200	-
ANT6	UHB TX0/DRX	-	-	TRX1	-	-	3300–4200	-
ANT7	LMHB TRX0	LB TX0 (Except n5/n71) n5/n71 TX1 MHB TX1 LMHB PRX	TX1/PRX	MIMO7 (HW Ready) ⁴	617–894	1695–2690	3300–4200	-

⁴ 'HW Ready' means that the module has reserved the ability to support 8 Rx in hardware design, which needs to be supported by customized projects. For details, please contact NetPrisma Technical Support.

Table 38: HMT89-EPV Cellular Antenna Interfaces Mapping

Pin Name	WCDMA	LTE	5G NR			LB (MHz)	MHB (MHz)	n77/n78 (MHz)
			Refarming	n41	n77/n78			
ANT0	-	UHB TX1/PRX	-	-	TRX0	-	-	3300–4200
ANT1	B1/B5/ B8 DRX	MHB + B28 TX1 LMHB DRX	MHB TX0/n28 TX0 LMHB DRX	TX0/DRX	MIMO5 (HW Ready) ⁴	617–960	1695–2690	3300–4200
ANT2	-	UHB PRX1	-	-	PRX1	-	-	3300–4200
ANT3	-	LMHB DRX1 B32 DRX	LMHB DRX1/ n75 DRX	DRX1	MIMO4 (HW Ready) ⁴	617–960	1427–2690	3300–4200
ANT4	-	UHB DRX1	-	-	DRX1	-	-	3300–4200
ANT5	-	LMHB PRX1 B32 PRX	LMHB PRX1/ n75 PRX	PRX1	MIMO6 (HW Ready) ⁴	617–960	1427–2690	3300–4200
ANT6	-	UHB TX0/DRX	-	-	TRX1	-	-	3300–4200
ANT7	B1/B5/ B8 TRX0	LMHB TRX0	LB TX0 (Except n28) n28 TX1 MHB TX1 LMHB PRX	TX1/PRX	MIMO7 (HW Ready) ⁴	617–960	1695–2690	3300–4200

NOTE

1. Only passive antennas are supported.
2. LTE L/M/H/UHB_TRX1 is activated when 5G NR FDD low/middle/high bands are supported in NSA mode.
3. UHB frequency range: 3300–4200 MHz.
4. TRX0/1 = TX0/1 + PRX/DRX; DRX1 = DRX MIMO; PRX1 = PRX MIMO.

5.1.2. Antenna Tuner Control Interfaces^{dev}

The module can use GRFC (generic RF control) interfaces to control external antenna tuner.

Table 39: Pin Description of GRFC Interfaces

Pin Name	Pin No.	I/O	Description
GRFC1	266	DO	Generic RF Controller
GRFC2	238	DO	Generic RF Controller
GRFC3	242	DO	Generic RF Controller
RFFE1_DATA	262	DIO	Used for external MIPI IC control
RFFE1_CLK	258	DO	Used for external MIPI IC control
RFFE2_DATA	234	DIO	Used for external MIPI IC control
RFFE2_CLK	230	DO	Used for external MIPI IC control

5.1.3. Transmitting Power

Table 40: RF Transmitting Power of HMT89-LD

Mode	Frequency Band	Max.	Min.	Power Class
LTE	LTE bands	23 dBm $\pm$ 2 dB	<-40 dBm	PC3
	LTE HPUE bands (B38/B41)	26 dBm +2/-3 dB	<-40 dBm	PC2
5G NR	5G NR bands	23 dBm $\pm$ 2 dB	<-40 dBm	PC3
	5G NR HPUE bands (n38/n41/n77/n78)	26 dBm +2/-3 dB	<-40 dBm	PC2
	5G NR HPUE bands (n41/n77/n78)	29 dBm +2/-3 dB	<-40 dBm	PC1.5

Table 41: RF Transmitting Power of HMT89-EPV

Mode	Frequency Band	Max.	Min.	Power Class
WCDMA	B1/B5/B8	23 dBm $\pm$ 2 dB	<-50 dBm	PC3
LTE	LTE bands	23 dBm $\pm$ 2 dB	<-40 dBm	PC3
	LTE HPUE bands (B41)	26 dBm +2/-3 dB	<-40 dBm	PC2
5G NR	5G NR bands	23 dBm $\pm$ 2 dB	<-40 dBm	PC3
	5G NR HPUE bands (n41/n77/n78)	26 dBm +2/-3 dB	<-40 dBm	PC2
	5G NR HPUE bands (n41/n77/n78)	29 dBm +2/-3 dB	<-40 dBm	PC1.5

5.1.4. Receiver Sensitivity

Table 42: Conducted RF Receiver Sensitivity of HMT89-LD (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)			3GPP Requirements (SIMO)
	Primary	Diversity	SIMO ⁵	
LTE-FDD B2 (10 MHz)	-99.5	-99	-102	-94.3
LTE-FDD B4 (10 MHz)	-98.5	-98	-101	-96.3
LTE-FDD B5 (10 MHz)	-99.5	-99.5	-102.5	-93.3
LTE-FDD B7 (10 MHz)	-97.5	-97	-100	-93.3
LTE-FDD B12 (10 MHz)	-100	-100	-103	-93.3
LTE-FDD B13 (10 MHz)	-99.5	-100	-102.5	-93.3
LTE-FDD B14 (10 MHz)	-100	-100	-103	-93.3
LTE-FDD B17 (10 MHz)	-100	-100	-103	-93.3
LTE-FDD B25 (10 MHz)	-99.5	-99	-102.5	-92.8
LTE-FDD B26 (10 MHz)	-99.5	-99.5	-102.5	-93.8
LTE-FDD B29 (10 MHz)	-100.5	-100.5	-103.5	-93.3
LTE-FDD B30 (10 MHz)	-97	-97.5	-100	-95.3
LTE-TDD B38 (10 MHz)	-97	-97	-100	-96.3
LTE-TDD B41 (10 MHz)	-96.5	-96.5	-99.5	-94.3
LTE-TDD B42 (10 MHz)	-99	-99	-102	-95
LTE-TDD B43 (10 MHz)	-99	-99.5	-102	-95
LTE LAA B46 (10 MHz)	-96.5	-96	-99.5	-95
LTE-TDD B48 (10 MHz)	-99	-99.5	-102	-95
LTE-FDD B66 (10 MHz)	-98.5	-98	-101	-95.8
LTE-FDD B70 (10 MHz)	-98.6	-98.1	-101	-95.8
LTE-FDD B71 (10 MHz)	-100.5	-101.5	-103.5	-93.5
5G NR-FDD n2 (10 MHz) (SCS: 15 kHz)	-100	-100	-103	-94.8
5G NR-FDD n5 (10 MHz) (SCS: 15 kHz)	-99	-99	-102	-94.1

⁵ For the SIMO receiving sensitivity, LTE bands and 5G n5/n12/n13/n14/n26/n29/n71 bands are tested with 2 Rx antennas, and 5G n2/n7/n25/n30/n38/n41/n48/n66/n70/n77/n78 bands are tested with 4 Rx antennas.

5G NR-FDD n7 (10 MHz) (SCS: 15 kHz)	-100	-100	-103	-94.8
5G NR-FDD n12 (10 MHz) (SCS: 15 kHz)	-98.5	-98.8	-101.5	-93.1
5G NR-FDD n13 (10 MHz) (SCS: 15 kHz)	-98.7	-99	-101.7	-93.1
5G NR-FDD n14 (10 MHz) (SCS: 15 kHz)	-98.8	-99	-101.8	-93.1
5G NR-FDD n25 (10 MHz) (SCS: 15 kHz)	-100.7	-101	-103.7	-93.3
5G NR-FDD n26 (10 MHz) (SCS: 15 kHz)	-98.5	-98.5	-101.5	-93.8
5G NR-FDD n29 (10 MHz) (SCS: 15 kHz)	-100	-100	-103	-93.8
5G NR-FDD n30 (10 MHz) (SCS: 15 kHz)	-98.7	-99	-101.7	-97.8
5G NR-TDD n38 (10 MHz) (SCS: 30 kHz)	-100	-100	-103	-97.1
5G NR-TDD n41 (100 MHz) (SCS: 30 kHz)	-90	-90	-93	-84.7
5G NR-TDD n48 (100 MHz) (SCS: 30 kHz)	-92	-92	-95	-86.7
5G NR-FDD n66 (10 MHz) (SCS: 15 kHz)	-100.5	-100.5	-103.5	-96.3
5G NR-FDD n70 (10 MHz) (SCS: 15 kHz)	-100.5	-100.5	-103.5	-96.8
5G NR-FDD n71 (10 MHz) (SCS: 15 kHz)	-100	-100	-103	-93.3
5G NR-TDD n77 (100 MHz) (SCS: 30 kHz)	-91.5	-91.5	-94.5	-85.1
5G NR-TDD n78 (100 MHz) (SCS: 30 kHz)	-91.5	-91.5	-94.5	-85.6

Table 43: Conducted RF Receiver Sensitivity of HMT89-EPV (Unit: dBm)

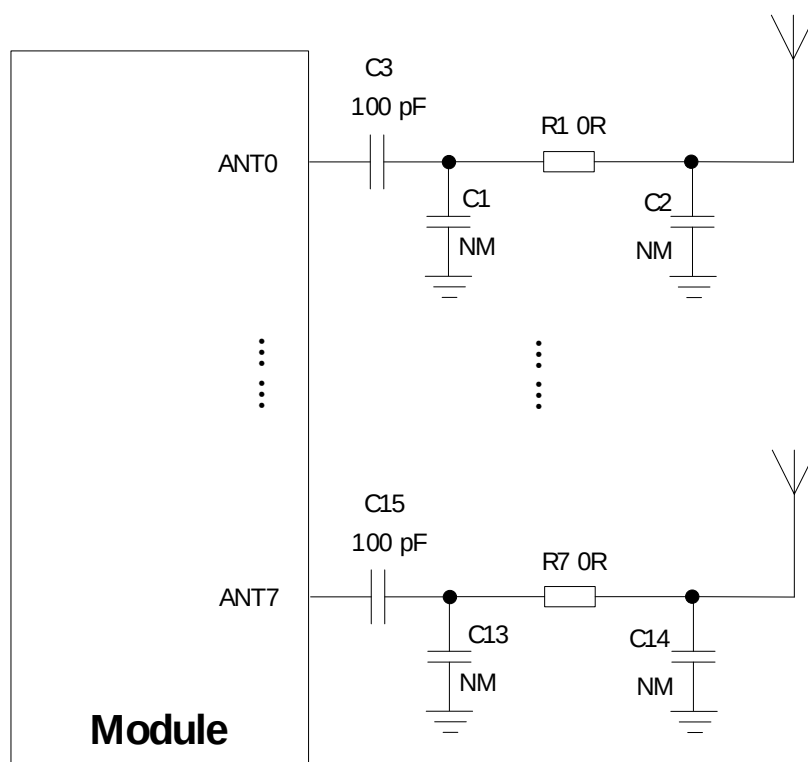
Frequency	Receiver Sensitivity (Typ.)			3GPP Requirements (SIMO)
	Primary	Diversity	SIMO ⁶	
WCDMA-FDD B1 (5 MHz)	-112	-	-112	-106.7
WCDMA-FDD B5 (5 MHz)	-112	-	-112	-104.7
WCDMA-FDD B8 (5 MHz)	-111.7	-	-111.7	-103.7
LTE-FDD B1 (10 MHz)	-100.3	-99.8	-102.5	-96.3
LTE-FDD B3 (10 MHz)	-100.8	-100.6	-103.5	-93.3
LTE-FDD B5 (10 MHz)	-100.2	-98.7	-101.7	-94.3
LTE-FDD B7 (10 MHz)	-98.1	-97.8	-100.8	-94.3
LTE-FDD B8 (10 MHz)	-99.8	-100.1	-102.8	-93.3

⁶ For the SIMO receiving sensitivity, WCDMA bands, LTE bands and 5G n5/n8/n20/n28 bands are tested with 2 Rx antennas, and 5G n1/n3/n7/n38/n40/n41/n75/n76/n77/n78 bands are tested with 4 Rx antennas.

LTE-FDD B20 (10 MHz)	-100.5	-99.3	-102.3	-93.3
LTE-FDD B28 (10 MHz)	-101	-100.5	-103.5	-94.8
LTE-FDD B32 (10 MHz)	-99.5	-99.5	-102	-
LTE-TDD B38 (10 MHz)	-98.5	-97.4	-100.4	-96.3
LTE-TDD B40 (10 MHz)	-98.6	-97.1	-100.1	-96.3
LTE-TDD B41 (10 MHz)	-98.5	-97	-100	-94.3
LTE-TDD B42 (10 MHz)	-99.7	-100.1	-102.7	-95
LTE-TDD B43 (10 MHz)	-99.8	-100.1	-102.8	-95
5G NR-FDD n1 (10 MHz) (SCS: 15 kHz)	-99	-98.8	-103.9	-96.8
5G NR-FDD n3 (10 MHz) (SCS: 15 kHz)	-100.2	-98.8	-103.4	-93.8
5G NR-FDD n5 (10 MHz) (SCS: 15 kHz)	-97.8	-97.4	-100.4	-94.8
5G NR-FDD n7 (10 MHz) (SCS: 15 kHz)	-98.3	-97.7	-103.7	-94.8
5G NR-FDD n8 (10 MHz) (SCS: 15 kHz)	-98	-99.3	-101	-93.8
5G NR-FDD n20 (10 MHz) (SCS: 15 kHz)	-99.9	-98.6	-101.6	-93.8
5G NR-FDD n28 (10 MHz) (SCS: 15 kHz)	-98.5	-98.5	-101.5	-95.5
5G NR-TDD n38 (10 MHz) (SCS: 30 kHz)	-98.3	-97.5	-104.2	-97.1
5G NR-TDD n40 (10 MHz) (SCS: 30 kHz)	-98.5	-97.2	-104.2	-97.1
5G NR-TDD n41 (100 MHz) (SCS: 30 kHz)	-88.8	-86.7	-93.7	-84.7
5G NR-SDL n75 (10 MHz) (SCS: 15 kHz)	-98.8	-98.8	-101.8	-96.8
5G NR-SDL n76 (10 MHz) (SCS: 15 kHz)	-99	-99	-102	-96.8
5G NR-TDD n77 (100 MHz) (SCS: 30 kHz)	-89.8	-89.6	-95	-85.1
5G NR-TDD n78 (100 MHz) (SCS: 30 kHz)	-89.8	-89.6	-95	-85.6

5.1.5. Reference Design

[Figure 36: Reference Design of Cellular Antenna](#)



NOTE

1. Use a dual L-type circuit for all the antenna interfaces for better RF performance and for the ease of debugging.
2. Capacitors (C1/C2/C13/C14) are not mounted by default.
3. Place the dual L-type components to antennas as close as possible.
4. Keep the characteristic impedance of cellular antenna (ANT0–ANT7) traces as 50 Ω when routing.
5. Keep at least 15 dB isolation between RF antennas on PCB to improve the receiver sensitivity, and at least 20 dB isolation between 5G NR UL MIMO antennas. Keep at least 23 dB isolation between 5G NR UL MIMO antennas when PC1.5 is supported.
6. The isolation between each two antenna traces on PCB is recommended to be over 75 dB.
7. Keep digital signals such as (U)SIM interface, USB interface, camera module, SDIO and display module away from the antenna traces.
8. It is recommended that the straight-line distance between the antenna and the module be greater than 15 mm to achieve better wireless performance of the whole device.
9. Notes on C3 and C15:
 - 1) If there is DC power at the antenna ports, place capacitors on C3 and C15 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
 - 2) If there is no DC power in the peripheral design:
 - a) Do not reserve C3 and C15.
 - b) If C3 and C15 have already been reserved, they should be mounted with components, and it is recommended to use 0 Ω resistors. You can also match the components according to the debugging results.

5.2. GNSS

GNSS information of the module is as follows:

- Supports GPS, GLONASS, BDS, Galileo, QZSS positioning system.
- Supports *NMEA 0183* protocol and outputs NMEA sentences via USB interface (data update rate for positioning: 1–5 Hz, 1 Hz by default).
- The module's GNSS function is OFF by default. It must be ON via AT commands.

For more details about GNSS technology and configurations, see **document 2**.

5.2.1. Antenna Interface & Frequency Bands

Table 44: Pin Description of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	290	AI	GNSS antenna interface	50 Ω impedance.

Table 45: GNSS Frequency (Unit: MHz)

Antenna Type	Frequency
GPS	1575.42 $\pm$ 1.023 (L1) 1176.45 $\pm$ 10.23 (L5)
GLONASS	1601.7 $\pm$ 4.2 (L1)
BDS	1561.098 $\pm$ 2.046 (B1I)
Galileo	1575.42 $\pm$ 2.046 (E1) 1176.45 $\pm$ 10.23 (E5a)
QZSS	1575.42 $\pm$ 1.023 (L1) 1176.45 $\pm$ 10.23 (L5)

5.2.2. GNSS Performance

Table 46: GNSS Performance

Parameter	Mode	Condition	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-147	dBm
	Reacquisition		-159	
	Tracking		-166	
TTFF	Cold start @ open sky	Autonomous	25.609	s
		AGNSS start	2.26	
	Warm start @ open sky	Autonomous	23.078	
		AGNSS start	2.98	
	Hot start @ open sky	Autonomous	1.255	
		AGNSS start	2.28	

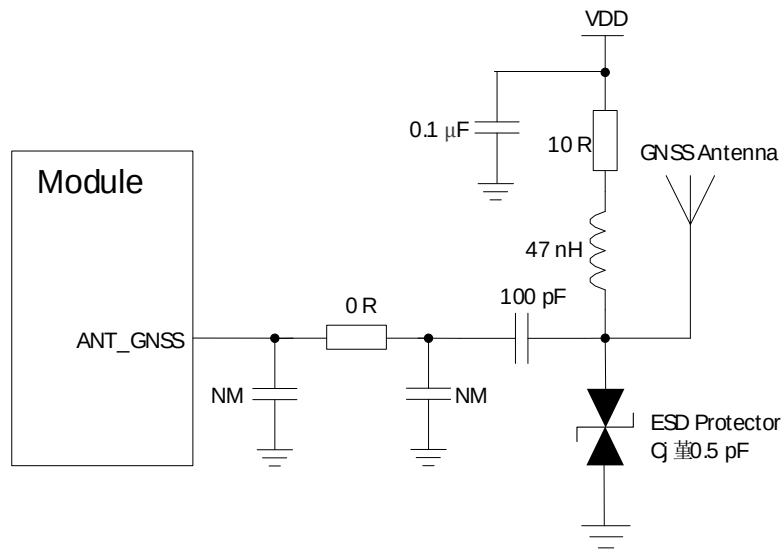
Accuracy	CEP-50	Autonomous @ open sky	1.8	m
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NOTE

1. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position of navigation signals successfully within 3 minutes after executing cold start command.
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock of navigation signals within 3 minutes after loss of lock.
3. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock of navigation signals (keep positioning for at least 3 minutes continuously).

5.2.3. Reference Design

Figure 37: Reference Design of GNSS Antenna



NOTE

1. You can select an external LDO according to the active antenna types. If you design the module with a passive antenna, you will not need the VDD circuit.
2. Junction capacitance of ESD protection components on the antenna interface should not exceed 0.5 pF.
3. Keep the characteristic impedance for ANT_GNSS trace as 50 Ω when routing.
4. Place the dual-L type components as close to the antenna as possible.
5. Keep digital circuits such as switch-mode power supply, (U)SIM interface, USB interface, camera module, display connector and SD card interface away from the antenna traces.
6. Keep 75 dB isolation between GNSS and cellular antenna traces on PCB.
7. Keep 15 dB isolation between GNSS and cellular antennas on PCB to improve receiver sensitivity.
8. It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to $50\ \Omega$. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

Figure 38: Microstrip Design on a 2-layer PCB

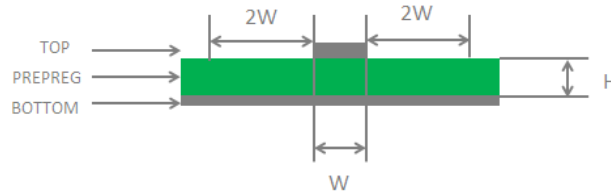


Figure 39: Coplanar Waveguide Design on a 2-layer PCB

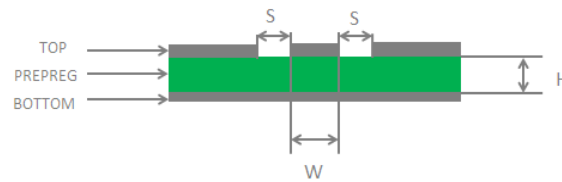


Figure 40: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

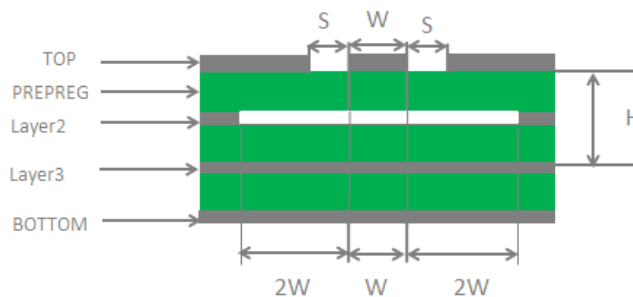
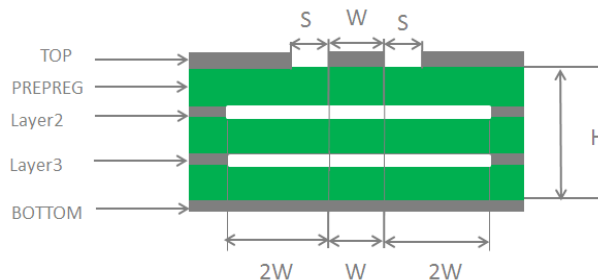


Figure 41: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)



To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to $50\ \Omega$.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135° .
- There should be clearance under the signal pin of the antenna connector or solder joint.

- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces ($2 \times W$).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see **document 3**.

5.4. Requirements for Antenna Design

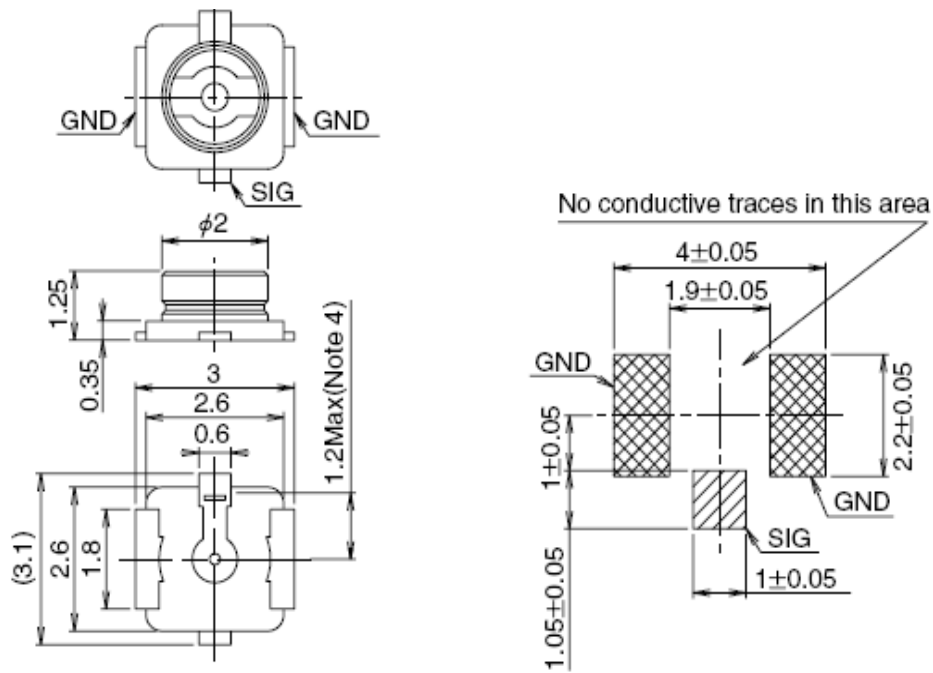
Table 47: Requirements for Antenna Design

Antenna Type	Requirements
GNSS	Frequency range: ● L1: 1559–1609 MHz ● L5: 1166–1187 MHz RHCP or linear polarization VSWR: ≤ 2 (Typ.)
Cellular	For passive antenna application: Passive antenna gain: > 0 dBi For active antenna application: Active antenna noise coefficient: < 1.5 dB Active antenna embedded LNA gain: < 17 dB VSWR: ≤ 2 Efficiency: > 30 % Gain: > 0 dBi Max input power: 50 W Input impedance: 50Ω Vertical polarization Cable insertion loss: ● < 1 dB: LB (< 1 GHz) ● < 1.5 dB: MB (1–2.3 GHz) ● < 2 dB: HB (> 2.3 GHz)

5.5. RF Connector Recommendation

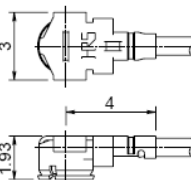
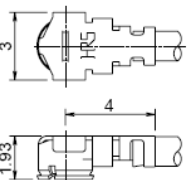
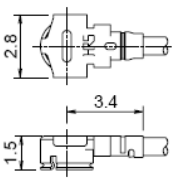
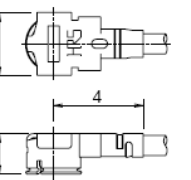
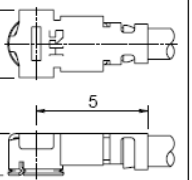
If the RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

Figure 42: Dimensions of the Receptacle (Unit: mm)



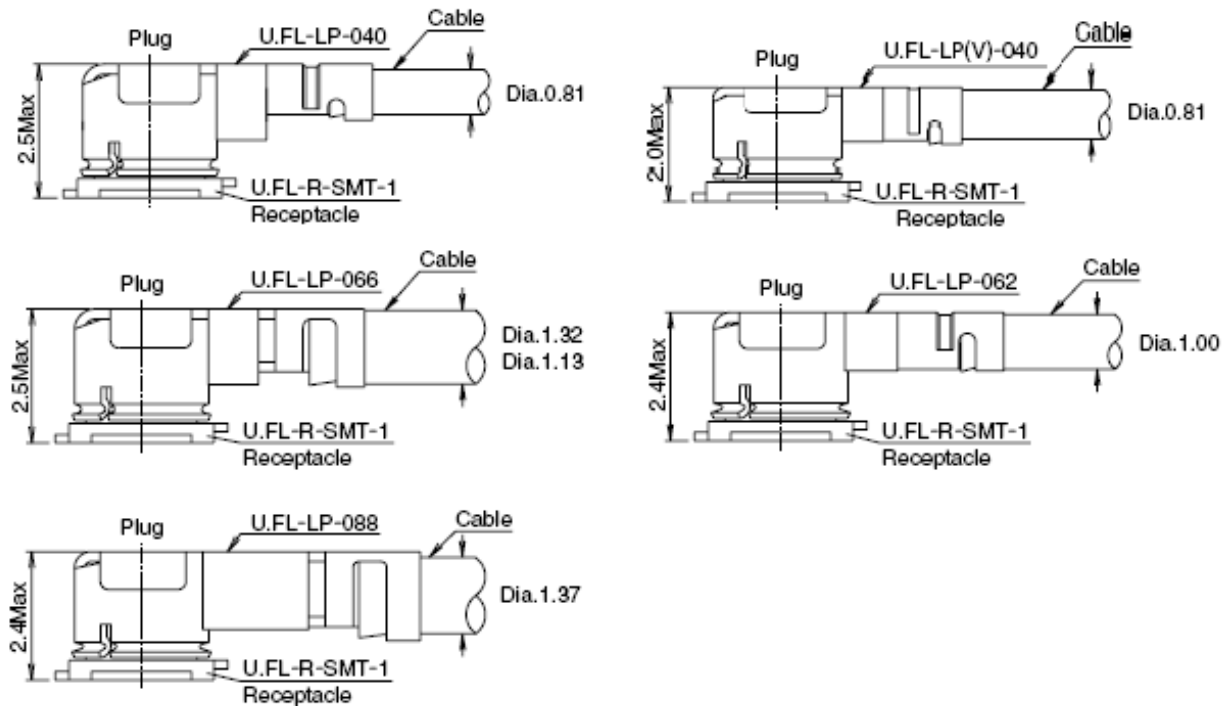
U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

Figure 43: Specifications of Mated Plugs (Unit: mm)

Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

The following figure describes the space factor of the mated connector.

Figure 44: Space Factor of the Mated Connectors (Unit: mm)



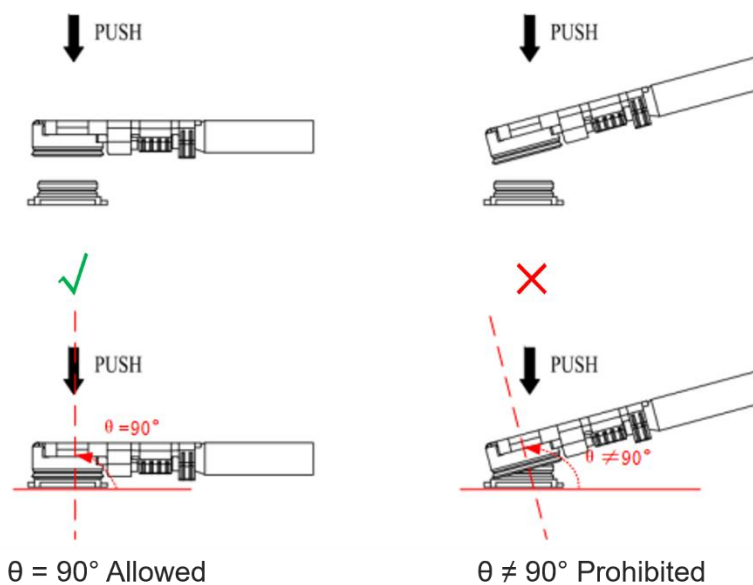
For more details, visit <http://www.hirose.com>.

5.5.1. Recommended RF Connector for Installation

5.5.1.1. Assemble Coaxial Cable Plug Manually

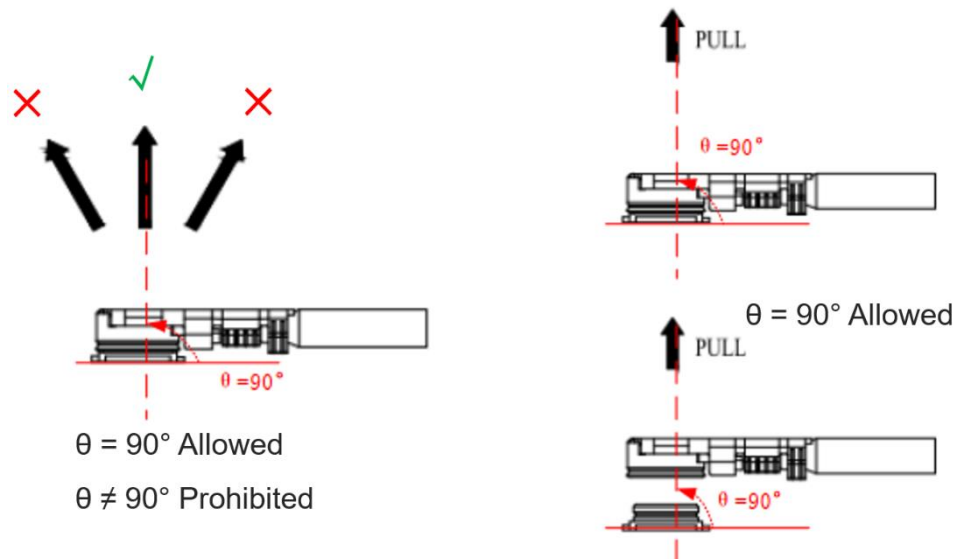
The pictures for plugging in a coaxial cable plug is shown below, $\theta = 90^\circ$ is acceptable, while $\theta \neq 90^\circ$ is not.

Figure 45: Plug in a Coaxial Cable Plug



The pictures of pulling out the coaxial cable plug is shown below, $\theta = 90^\circ$ is acceptable, while $\theta \neq 90^\circ$ is not.

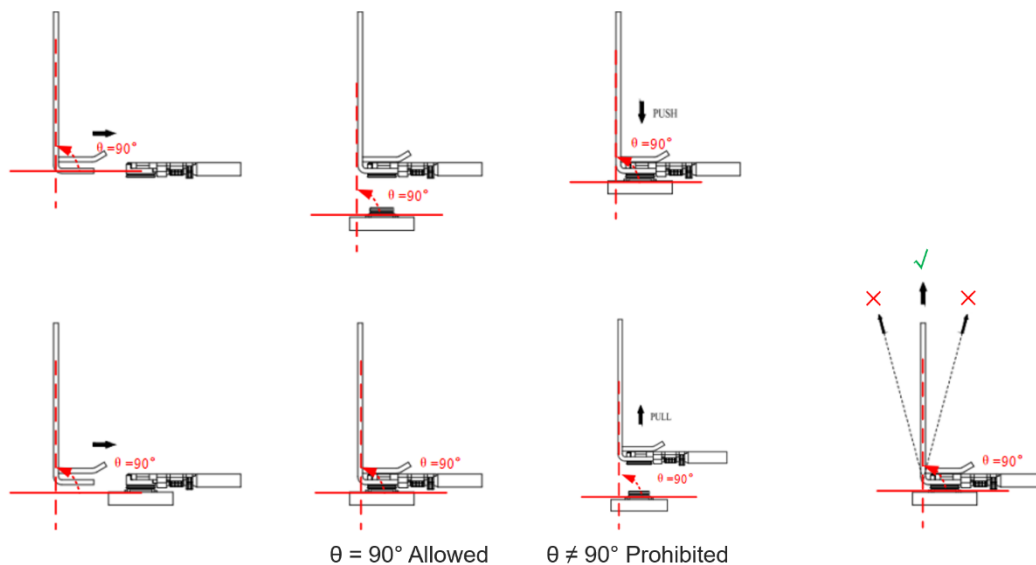
Figure 46: Pull out a Coaxial Cable Plug



5.5.1.2. Assemble Coaxial Cable Plug with Jig

The pictures of installing the coaxial cable plug with a jig is shown below, $\theta = 90^\circ$ is acceptable, while $\theta \neq 90^\circ$ is not.

Figure 47: Install the Coaxial Cable Plug with Jig



5.5.2. Recommended Manufacturers of RF Connector and Cable

RF connectors and cables by I-PEX are recommended. For more details, visit <https://www.i-pex.com>.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Table 48: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Voltage at VBAT_RF & VBAT_BB	-0.5	5	V
Voltage at USB_VBUS	0	21	V
Voltage at digital pins	-0.5	2.48	V
Voltage at ADC[0:6]	-0.5	2.48	V
Current at VBAT_BB	-	2	A
Current at VBAT_RF	-	3	A

NOTE

Exceeding the conditions of use as shown above may cause permanent damage to the module.

6.2. Power Supply Ratings

Table 49: Module's Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB & VBAT_RF	The actual input voltage must be within this range	3.3	3.8	4.4	V
USB_VBUS	USB connection detection	-	4.2	5.0	15	V

6.3. Power Consumption

Table 50: HMT89-LD Power Consumption

Test Item	Condition	Band/Combination	Typ.	Unit
Turn off	Power off	-	135	μ A
Sleep	AT+CFUN=0 (USB disconnected)	-	6	mA
Idle	SA PF = 64 (USB 2.0 active)	-	145	mA
	SA PF = 64 (USB 3.2 active)	-	165	mA
LTE	LTE LB @ 23 dBm	B5 (10 MHz 12 RB)	780	mA
	LTE MB @ 23 dBm	B2 (20 MHz 18 RB)	865	mA
	LTE HB @ 23 dBm	B7 (20 MHz 18 RB)	1070	mA
LTE CA	DL 3CA, 256QAM	CA_2A-66A-30A	920	mA
	UL 1CA, 256QAM			
	Tx power @ 23 dBm			
5G SA FR1 (1 Tx)	5G NR LB @ 23 dBm	n5 (20 MHz Inner Full)	760	mA
	5G NR, MB @ 23 dBm	n2 (20 MHz Inner Full)	850	mA
	5G NR HB @ 23 dBm	n7 (20 MHz Inner Full)	1140	mA
	5G NR UHB @ 26 dBm	n78 (100 MHz Inner Full)	435	mA
5G SA FR1 (2 Tx)	5G NR UL 2 × 2 MIMO @ 26 dBm	n78 (100 MHz Inner Full)	580	mA
5G SA FR1 CA	DL 2CA, 256QAM	n78C	580	mA
	UL 1CA, 256QAM			
	Tx power @ 26 dBm			
LTE + 5G FR1 EN-DC	LTE DL, 256QAM	DC_2A_n78A	1200	mA
	LTE UL, QPSK			
	NR DL, 256QAM			
	NR UL, QPSK			
	LTE Tx Power @ 23 dBm			
	NR Tx Power @ 26 dBm			

Table 51: HMT89-EPV Power Consumption

Test Item	Condition	Band/Combination	Typ.	Unit
Turn off	Power off	-	135	μ A
Sleep	AT+CFUN=0 (USB disconnected)	-	6	mA
Idle	SA PF = 64 (USB 2.0 active)	-	145	mA
	SA PF = 64 (USB 3.2 active)	-	165	mA
LTE	LTE LB @ 23 dBm	B5	850	mA
	LTE MB @ 23 dBm	B1	820	mA
	LTE HB @ 23 dBm	B7	1100	mA
LTE CA	DL 3CA, 256QAM	CA_1A-3A-7A	1300	mA
	UL 1CA, 256QAM			
	Tx power @ 23 dBm			
5G SA FR1 (1 Tx)	5G NR LB @ 23 dBm	n5	824	mA
	5G NR, MB @ 23 dBm	n1	890	mA
	5G NR HB @ 23 dBm	n7	990	mA
	5G NR UHB @ 26 dBm	n78	390	mA
5G SA FR1 (2 Tx)	5G NR UL 2 × 2 MIMO @ 26 dBm	n78	468	mA
5G SA FR1 CA	DL 2CA, 256QAM	n78C	600	mA
	UL 1CA, 256QAM			
	Tx power @ 26 dBm			
LTE + 5G FR1 EN-DC	LTE DL, 256QAM	DC_3A_n78A	1052	mA
	LTE UL, QPSK			
	NR DL, 256QAM			
	NR UL, QPSK			
	LTE Tx Power @ 23 dBm			
	NR Tx Power @ 26 dBm			

NOTE

1. Power consumption test is carried out under 3.8 V, 25 °C with EVB and thermal dissipation measures.
2. The power consumption data above is for reference only, which may vary among different modules. For detailed information, contact NetPrisma Technical Support for the power consumption test report of the specific module.

6.4. Digital I/O Characteristics

Table 52: VDD_EXT I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V _{IH}	High-level input voltage	$0.65 \times VDD_EXT$	$VDD_EXT + 0.3$
V _{IL}	Low-level input voltage	-0.3	$0.35 \times VDD_EXT$
V _{OH}	High-level output voltage	$0.75 \times VDD_EXT$	-
V _{OL}	Low-level output voltage	-	$0.25 \times VDD_EXT$

Table 53: SDIO I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V _{IH}	High-level input voltage	$0.65 \times VDD_EXT$	$VDD_EXT + 0.3$
V _{IL}	Low-level input voltage	-0.3	$0.35 \times VDD_EXT$
V _{OH}	High-level output voltage	$VDD_EXT - 0.45$	-
V _{OL}	Low-level output voltage	-	0.45

Table 54: (U)SIM Low-voltage I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V _{IH}	High-level input voltage	$0.7 \times USIM_VDD$	USIM_VDD
V _{IL}	Low-level input voltage	0	$0.15 \times USIM_VDD$
V _{OH}	High-level output voltage	1.4	USIM_VDD
V _{OL}	Low-level output voltage	0	0.27

Table 55: (U)SIM High-voltage I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V _{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD
V _{IL}	Low-level input voltage	0	0.15 × USIM_VDD
V _{OH}	High-level output voltage	2.6	USIM_VDD
V _{OL}	Low-level output voltage	0	0.4

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 56: ESD Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %; Unit: kV)

Test Point	Contact Discharge	Air Discharge
VBAT & GND	±5	±10
All antenna interfaces	±4	±8
Other interfaces	±0.25	±1

6.6. Operating and Storage Temperatures

Table 57: Operating and Storage Temperatures (Unit: °C)

Parameter	Min.	Typ.	Max.
Normal Operating Temperature ⁷	-30	+25	+70
Extended Operating Temperature ⁸	-40	+25	+85

⁷ To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

⁸ To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within the range of -40 to -30 °C or 70 to 85 °C, the module retains the ability to establish and maintain functions such as voice, SMS, and emergency call, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

Storage Temperature

-40

-

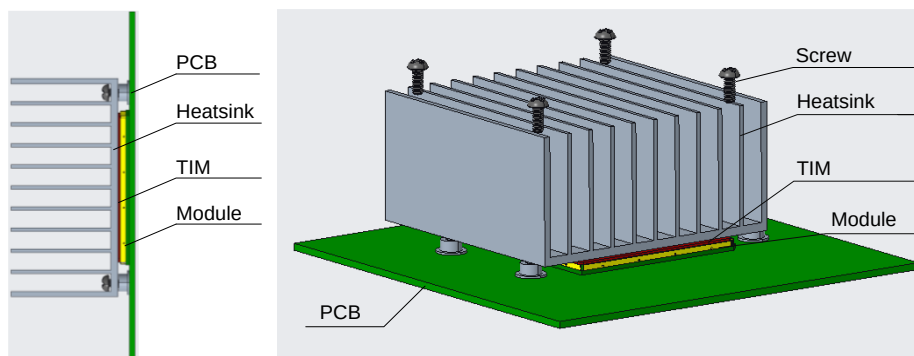
+90

6.7. Thermal Dissipation

The module offers the best performance when all internal IC chips are working within their operating temperatures. When the IC chip reaches or exceeds the maximum junction temperature, the module may still work but the performance and functions (such as RF output power and data rate) will be affected to a certain extent. Therefore, the thermal design should be maximally optimized to ensure all internal IC chips always work within the recommended operating temperature range. The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on your PCB, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Follow the principles below when the heatsink is necessary:
 - Do not place large size components in the area where the module is mounted on your PCB to reserve enough place for heatsink installation.
 - Attach the heatsink to the shielding cover of the module; In general, the base plate area of the heatsink should be larger than the module area to cover the module completely;
 - Choose the heatsink with adequate fins to dissipate heat;
 - Choose a TIM (Thermal Interface Material) with high thermal conductivity, good softness and good wettability and place it between the heatsink and the module;
 - Fasten the heatsink with four screws to ensure that it is in close contact with the module to prevent the heatsink from falling off during the drop, vibration test, or transportation.

Figure 48: Placement and Fixing of the Heatsink



7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ± 0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

Figure 49: Top and Side Dimensions

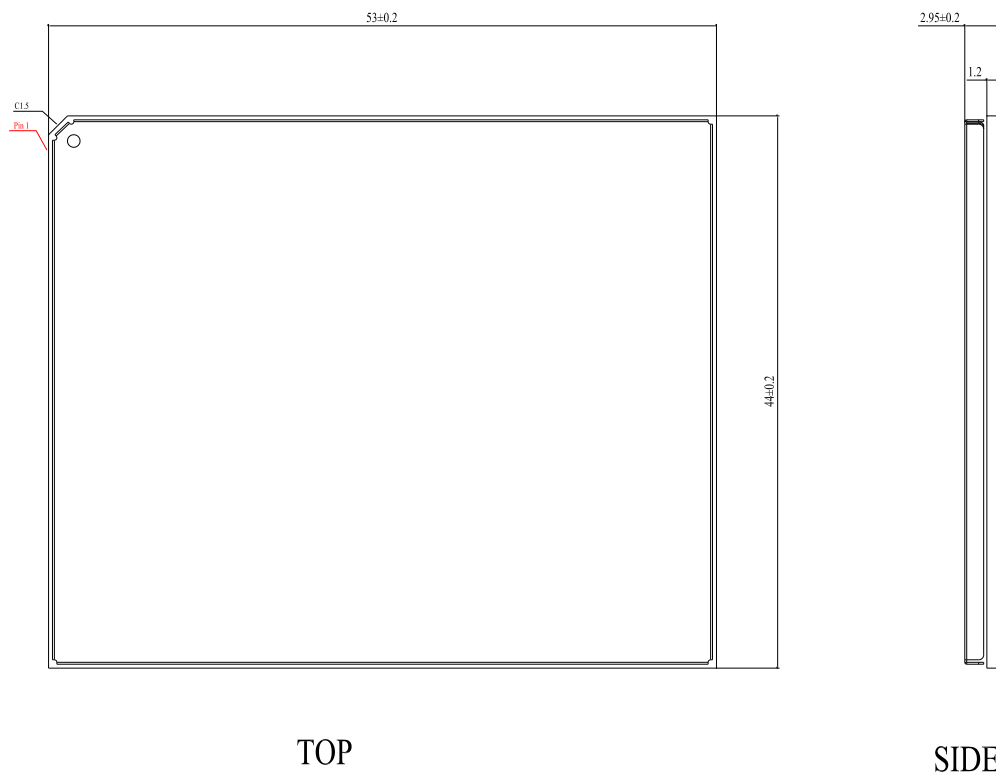
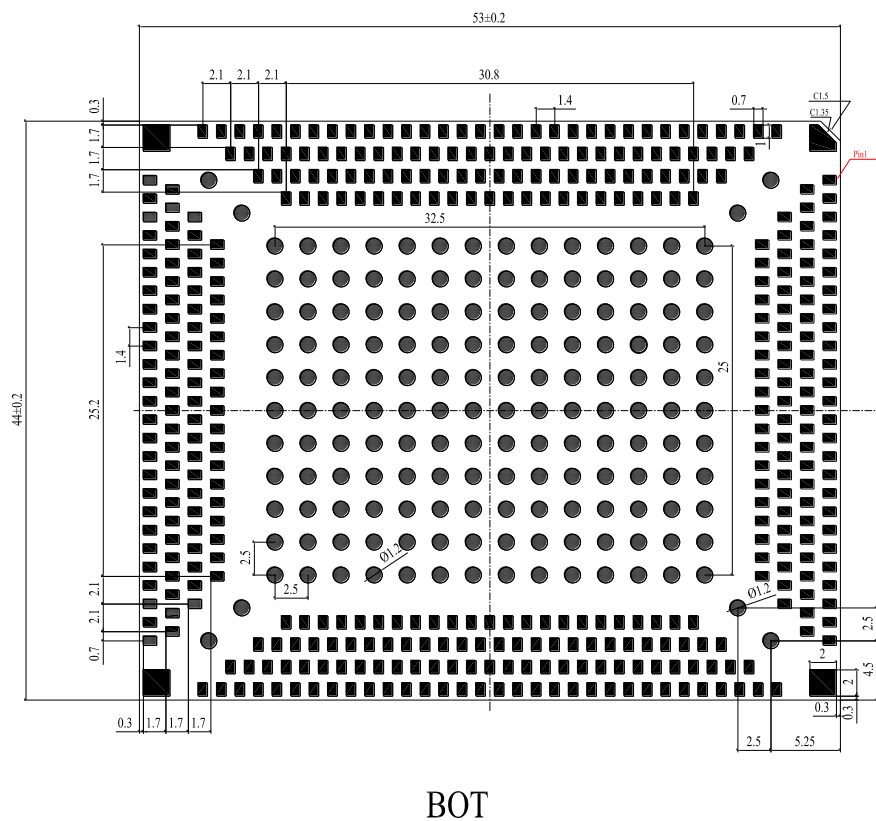


Figure 50: Bottom Dimensions

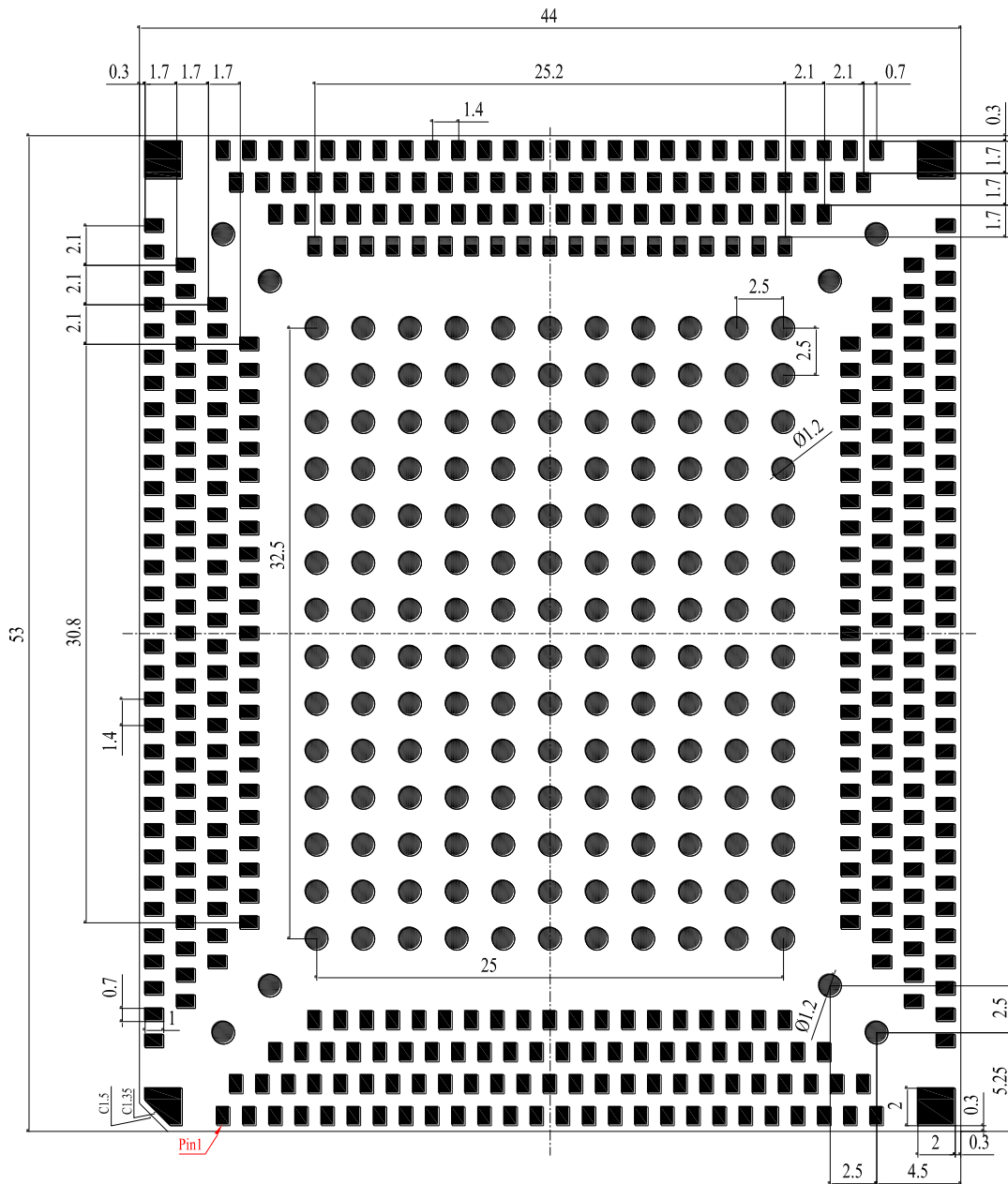


NOTE

The module's coplanarity standard: ≤ 0.13 mm.

7.2. Recommended Footprint

Figure 51: Recommended Footprint



Unlabeled tolerance: $\pm 0.2\text{mm}$

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

Figure 52: Top & Bottom Views of the HMT89-LD Module

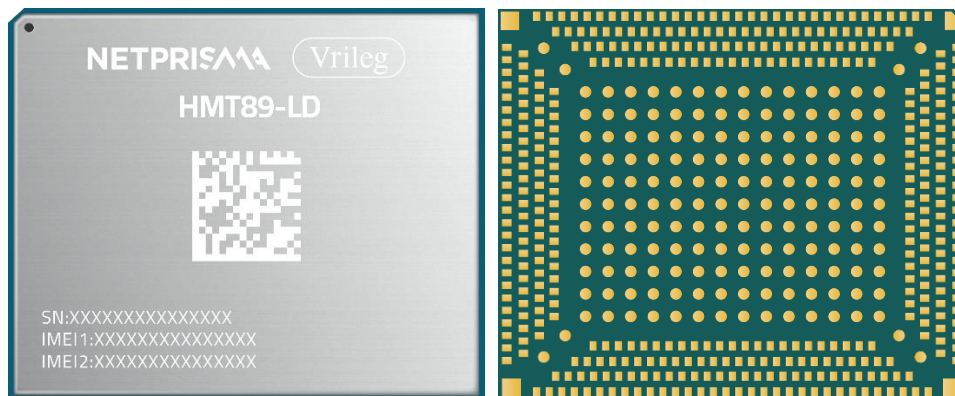
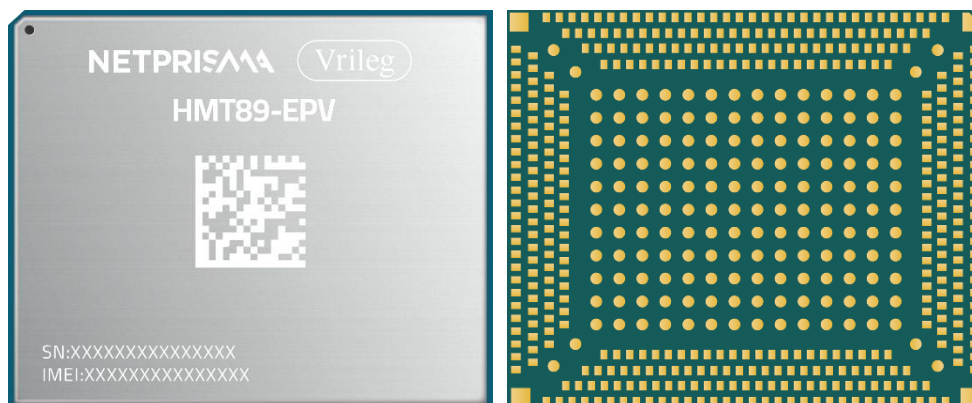


Figure 53: Top & Bottom Views of the HMT89-EPV Module



NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from NetPrisma.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ± 5 °C and the relative humidity should be 35–60 %.
2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.
3. Floor life: 168 hours ⁹ in a factory where the temperature is 23 ± 5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).
4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:
 - The module is not stored in Recommended Storage Condition;
 - Violation of the third requirement mentioned above;
 - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
 - Before module repairing.
5. If needed, the pre-baking should follow the requirements below:
 - The module should be baked for 24 hours at 120 ± 5 °C;
 - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

NOTE

-
1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
 2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
 3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.
-

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see **document 4**.

⁹ This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

The recommended peak reflow temperature should be 235–246 °C, with 246 °C as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below:

Figure 54: Recommended Reflow Soldering Thermal Profile

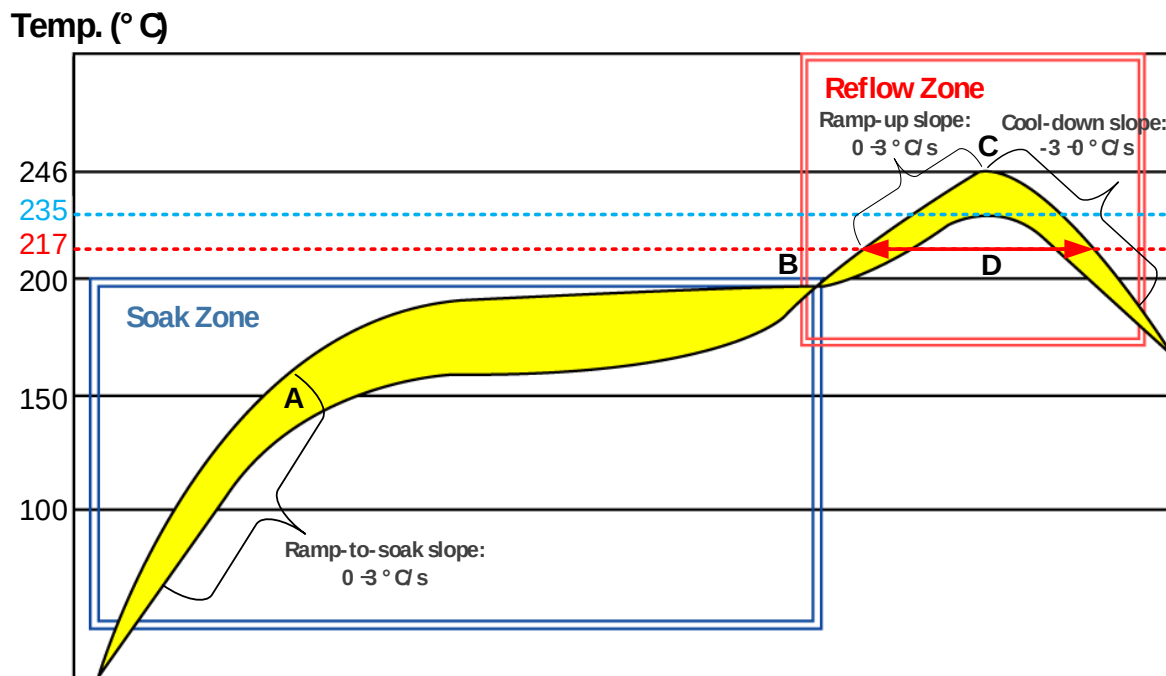


Table 58: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217 °C)	40–70 s
Max Temperature	235–246 °C
Cool-down Slope	-3–0 °C/s
Reflow Cycle	
Max Reflow Cycle	1

NOTE

1. For large-form-factor modules (that is, minimum side length ≥ 30 mm) with two-piece shielding covers, use a cool-down slope of -1 to 0 °C/s to reduce the thermal stress, preventing cover lifting. Due to the large-size form factors of such modules, an excessive temperature change may cause excessive thermal deformation of the metal shielding frame and cover. Therefore, reduce the ramp-up and cool-down slopes in the liquid phase of the solder paste to avoid excessive temperature change. If possible, choose a reflow oven with more than 10 temperature zones during production so that there are more temperature zones to set up to meet the optimal temperature curve.
2. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
3. If a conformal coating is necessary for the module, do not use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
6. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
7. Due to the complexity of the SMT process, please contact NetPrisma Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective wave soldering, ultrasonic soldering) that is not mentioned in **document 5**.

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

Figure 55: Carrier Tape Dimension Drawing (Unit: mm)

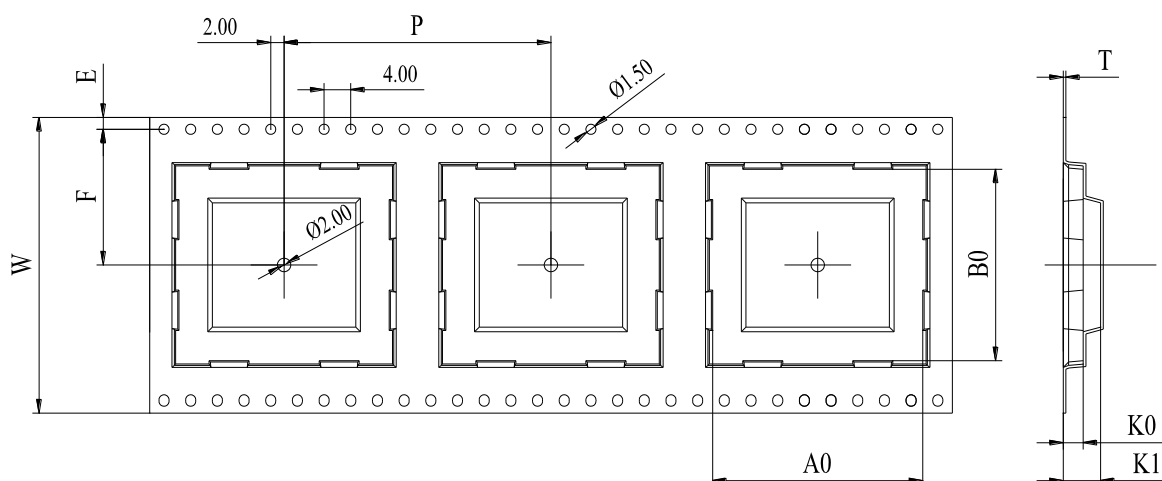


Table 59: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
72	72	0.5	53.6	44.6	4.25	7.6	34.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

Figure 56: Plastic Reel Dimension Drawing

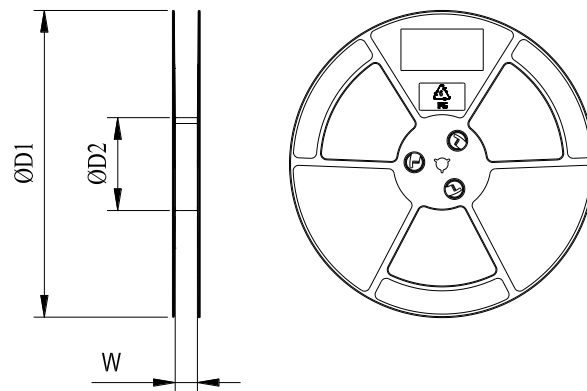
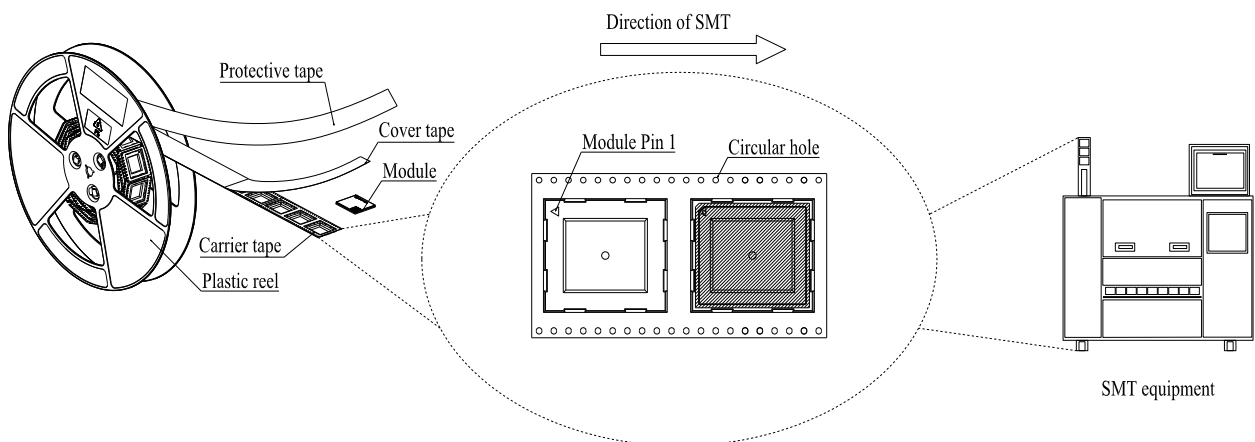


Table 60: Plastic Reel Dimension Table (Unit: mm)

ØD1	ØD2	W
380	180	72.5

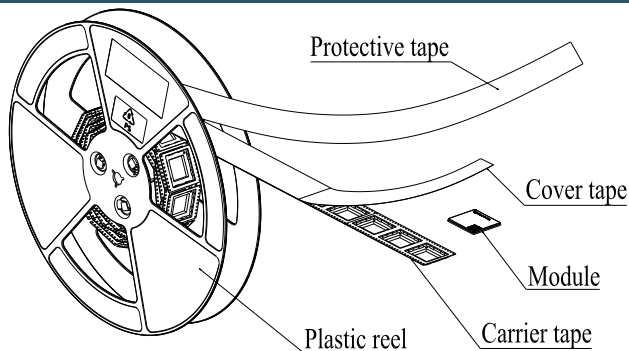
8.3.3. Mounting Direction

Figure 57: Mounting Direction



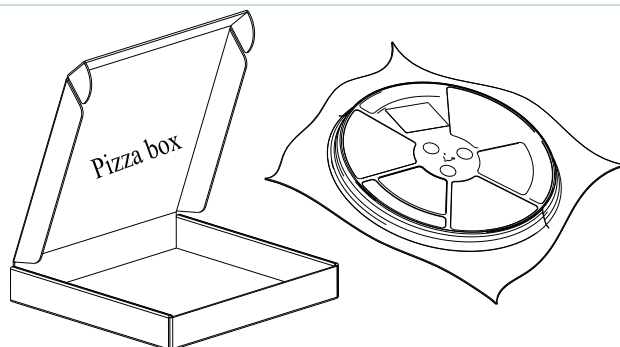
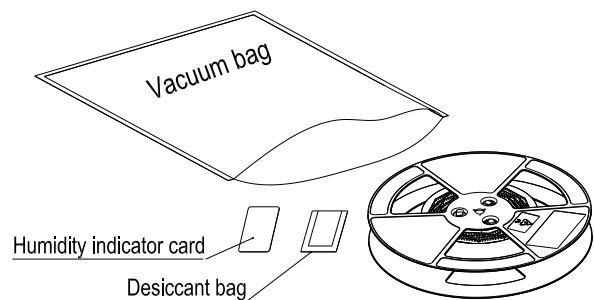
8.3.4. Packaging Process

Figure 58: Packaging Process



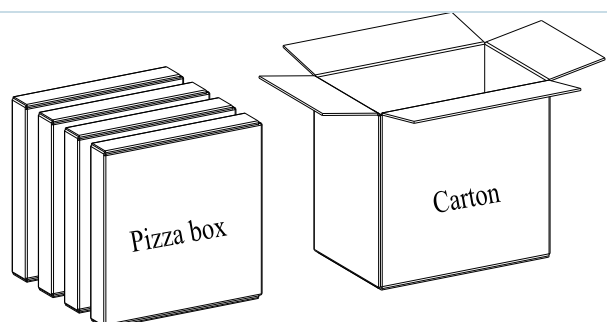
Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 100 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.



Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 400 modules.



9 Related AT Commands

9.1. AT+CFUN Set UE Functionality

This command controls the functionality level. It can also be used to reset the UE.

- **AT+CFUN=0** turns off radio and (U)SIM power.
- **AT+CFUN=1,1** or **AT+CFUN=4,1** can reset the UE.
- **AT+CFUN=1** enters full functionality mode.
- **AT+CFUN=4** enters airplane mode.

AT+CFUN Set UE Functionality

Test Command AT+CFUN=?	Response +CFUN: (list of supported <fun>s),(list of supported <rst>s)
	OK
Read Command AT+CFUN?	Response +CFUN: <fun>
	OK
Write Command AT+CFUN=<fun>[,<rst>]	Response OK
	If there is any error related to MT functionality: +CME ERROR: <err> Or ERROR
Maximum Response Time	15 s, determined by the network.
Characteristics	-
Reference	3GPP TS 27.007

Parameter

<fun>	Integer type. Functionality level.
	0 Minimum functionality (Turn off radio and (U)SIM power)
	1 Full functionality
	4 Airplane mode (Disable RF function)
	15 Reboot the modem and AP synchronously
<rst>	Integer type. Whether to reset the UE before setting it to <fun> power level.
	0 Do not reset (Default value when <rst> is omitted)
	1 Reset
<err>	Error code.

Example

```
AT+CFUN=0 //Switch UE to minimum functionality.
OK
```

AT+CFUN=1 OK	//Switch UE to full functionality.
-------------------------------	------------------------------------

NOTE

1. **AT+CFUN=1,1** or **AT+CFUN=4,1** can only reset the UE, which is not fully compliant with 3GPP TS 27.007.
2. The execution of **AT+CFUN** command will not affect GNSS function.

9.2. AT+QSCLK Enable/Disable Sleep Mode

This command controls whether MT enters sleep mode. When entering into sleep mode is enabled, the MT can directly enter sleep mode.

AT+QSCLK Enable/Disable Sleep Mode

Test Command AT+QSCLK=?	Response +QSCLK: (list of supported <n>s) OK
Read Command AT+QSCLK?	Response +QSCLK: <n> OK
Write Command AT+QSCLK=<n>	Response OK
Maximum Response Time	300 ms
Characteristics	-

Parameter

<n>	Integer type. Enable/disable sleep mode.
0	Disable
1	Enable

NOTE

1. **AT+QSCLK=1** enables the module to enter sleep mode. At this time, the USB is powered down and the module's modem part enters airplane mode.
2. **AT+QSCLK=0** disables the module to enter sleep mode. At this time, the USB is powered up and the module's modem part is in normal operating mode. Under such condition, the module will never go into sleep mode.

9.3. AT+QADC Read ADC Value

This command reads the voltage value of specified ADC channel.

AT+QADC Read ADC Value

Test Command AT+QADC=?	Response +QADC: (range of supported <port> s)
	OK
Read Command AT+QADC=<port>	Response +QADC: <status> , <value>
	OK
Maximum Response Time	300 ms
Characteristics	-

Parameter

<port>	Integer type. Channel number of the ADC. 0 ADC channel 0 1 ADC channel 1 2 ADC channel 2 3 ADC channel 3 4 ADC channel 4 5 ADC channel 5 6 ADC channel 6
<status>	Integer type. Indicates whether the ADC value read is successful. 0 Failed 1 Successful
<value>	Integer type. The voltage of specified ADC channel. Unit: mV.

10 Appendix A References

Table 61: Related Documents

Document Name
1. NetPrisma-5G-SOC-EVB-User-Guide
2. NetPrisma-HMT89-Series-Open(SDK)-GNSS-Application-Note
3. NetPrisma-RF-Layout-Application-Note
4. NetPrisma-Module-Stencil-Design-Requirements
5. NetPrisma-Module-SMT-Application-Note
6. NetPrisma-HMT89-Series-Open-GPIO-Configuration

Table 62: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AP	Application Processor
APT	Average Power Tracking
bps	Bits Per Second
BPSK	Binary Phase Shift Keying
BW	Bandwidth
CA	Carrier Aggregation
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear to Send
DAI	Digital Audio Interface
DBI	Display Bus Interface
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DL	Downlink
DRF	Digital Radio Frequency

DRX	Discontinuous Reception
DRX	Diversity Receive
DTR	Data Terminal Ready
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
FOTA	Firmware Over-The-Air
GLONASS	Global Navigation Satellite System (Russia)
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GRFC	General RF Control
HB	High Band
HPUE	High Power User Equipment
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
IC	Integrated Circuit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
I/O	Input/Output
Inom	Normal Current
LAA	License Assisted Access
LB	Low Band
LCD	Liquid Crystal Display
LDO	Low-dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array

LMHB	Low/Middle/High Band
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MAC	Media Access Control
MB	Middle Band
MCU	Microcontroller Unit
MDC	Management Data Clock
MDIO	Management Data Input/Output
MHB	Middle/High Band
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MT	Mobile Terminated
NR	New Radio
NSA	Non-Stand Alone
OTG	On-The-Go
PA	Power Amplifier
PAP	Password Authentication Protocol
PC	Power Class
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PHY	Physical Layer
PMIC	Power Management Integrated Circuit
PMU	Power Management Unit
PRX	Primary Receive
QAM	Quadrature Amplitude Modulation

QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RI	Ring Indicator
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SA	Stand Alone
SCS	Sub-Carrier Space
SD	Secure Digital
SIMO	Single Input Multiple Output
SMD	Surface Mount Device
SMS	Short Message Service
SPI	Serial Peripheral Interface
SPMI	System power management interface
STB	Set Top Box
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TRX	Transmit & Receive
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UHB	Ultra High Band
UL	Uplink
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
USXGMII	The Universal Serial 10 Gigabit Media Independent Interface
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage

V _{nom}	Nominal Voltage
V _{min}	Minimum Voltage
V _{IHmax}	Maximum High-level Input Voltage
V _{IHmin}	Minimum High-level Input Voltage
V _{ILmax}	Maximum Low-level Input Voltage
V _{ILmin}	Minimum Low-level Input Voltage
V _{imax}	Absolute Maximum Input Voltage
V _{imin}	Absolute Minimum Input Voltage
V _{OHmax}	Maximum High-level Output Voltage
V _{OHmin}	Minimum High-level Output Voltage
V _{OLmax}	Maximum Low-level Output Voltage
V _{OLmin}	Minimum Low-level Output Voltage
VoIP	Voice over Internet Protocol
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WWAN	Wireless Wide Area Network

11 Appendix B Operating Frequency

Table 63: Operating Frequencies (5G)

5G	Duplex Mode	Uplink Operating Band	Downlink Operating Band	Unit
n1	FDD	1920–1980	2110–2170	MHz
n2	FDD	1850–1910	1930–1990	MHz
n3	FDD	1710–1785	1805–1880	MHz
n5	FDD	824–849	869–894	MHz
n7	FDD	2500–2570	2620–2690	MHz
n8	FDD	880–915	925–960	MHz
n12	FDD	699–716	729–746	MHz
n13	FDD	777–787	746–756	MHz
n14	FDD	788–798	758–768	MHz
n18	FDD	815–830	860–875	MHz
n20	FDD	832–862	791–821	MHz
n24	FDD	1626.5–1660.5	1525–1559	MHz
n25	FDD	1850–1915	1930–1995	MHz
n26	FDD	814–849	859–894	MHz
n28	FDD	703–748	758–803	MHz
n29	SDL	-	717–728	MHz
n30	FDD	2305–2315	2350–2360	MHz
n34	TDD	2010–2025	2010–2025	MHz
n38	TDD	2570–2620	2570–2620	MHz
n39	TDD	1880–1920	1880–1920	MHz
n40	TDD	2300–2400	2300–2400	MHz
n41	TDD	2496–2690	2496–2690	MHz
n46	TDD	5150–5925	5150–5925	MHz
n47	TDD	5855–5925	5855–5925	MHz
n48	TDD	3550–3700	3550–3700	MHz

n50	TDD	1432–1517	1432–1517	MHz
n51	TDD	1427–1432	1427–1432	MHz
n53	TDD	2483.5–2495	2483.5–2495	MHz
n65	FDD	1920–2010	2110–2200	MHz
n66	FDD	1710–1780	2110–2200	MHz
n67	SDL	-	738–758	MHz
n70	FDD	1695–1710	1995–2020	MHz
n71	FDD	663–698	617–652	MHz
n74	FDD	1427–1470	1475–1518	MHz
n75	SDL	-	1432–1517	MHz
n76	SDL	-	1427–1432	MHz
n77	TDD	3300–4200	3300–4200	MHz
n78	TDD	3300–3800	3300–3800	MHz
n79	TDD	4400–5000	4400–5000	MHz
n80	SUL	1710–1785	-	MHz
n81	SUL	880–915	-	MHz
n82	SUL	832–862	-	MHz
n83	SUL	703–748	-	MHz
n84	SUL	1920–1980	-	MHz
n85	FDD	698–716	728–746	MHz
n86	SUL	1710–1780	-	MHz
n89	SUL	824–849	-	MHz
n90	TDD	2496–2690	2496–2690	MHz
n91	FDD	832–862	1427–1432	MHz
n92	FDD	832–862	1432–1517	MHz
n93	FDD	880–915	1427–1432	MHz
n94	FDD	880–915	1432–1517	MHz
n95	SUL	2010–2025	-	MHz
n96	TDD	5925–7125	5925–7125	MHz

n97	SUL	2300–2400	-	MHz
n98	SUL	1880–1920	-	MHz
n99	SUL	1626.5–1660.5	-	MHz
n257	-	26.50–29.50	26.50–29.50	GHz
n258	-	24.25–27.50	24.25–27.50	GHz
n260	-	37.00–40.00	37.00–40.00	GHz
n261	-	27.50–28.35	27.50–28.35	GHz

Table 64: Operating Frequencies (2G + 3G + 4G; Unit: MHz)

2G	3G	4G	Duplex Mode	Uplink Operating Band	Downlink Operating Band
-	B1	B1	FDD	1920–1980	2110–2170
PCS1900	B2/BC1	B2	FDD	1850–1910	1930–1990
DCS1800	B3	B3	FDD	1710–1785	1805–1880
-	B4	B4	FDD	1710–1755	2110–2155
GSM850	B5/BC0	B5	FDD	824–849	869–894
-	B6	-	FDD	830–840	875–885
-	B7	B7	FDD	2500–2570	2620–2690
EGSM900	B8	B8	FDD	880–915	925–960
-	B9	B9	FDD	1749.9–1784.9	1844.9–1879.9
-	B10	B10	FDD	1710–1770	2110–2170
-	B11	B11	FDD	1427.9–1447.9	1475.9–1495.9
-	B12	B12	FDD	699–716	729–746
-	B13	B13	FDD	777–787	746–756
-	B14	B14	FDD	788–798	758–768
-	-	B17	FDD	704–716	734–746
-	-	B18	FDD	815–830	860–875
-	B19	B19	FDD	830–845	875–890
-	B20	B20	FDD	832–862	791–821
-	B21	B21	FDD	1447.9–1462.9	1495.9–1510.9

-	B22	B22	FDD	3410–3490	3510–3590
-	-	B24	FDD	1626.5–1660.5	1525–1559
-	B25	B25	FDD	1850–1915	1930–1995
-	B26	B26	FDD	814–849	859–894
-	-	B27	FDD	807–824	852–869
-	-	B28	FDD	703–748	758–803
-	-	B29	FDD ¹⁰	-	717–728
-	-	B30	FDD	2305–2315	2350–2360
-	-	B31	FDD	452.5–457.5	462.5–467.5
-	-	B32	FDD ¹⁰	-	1452–1496
-	B33	B33	TDD	1900–1920	1900–1920
-	B34	B34	TDD	2010–2025	2010–2025
-	B35	B35	TDD	1850–1910	1850–1910
-	B36	B36	TDD	1930–1990	1930–1990
	B37	B37	TDD	1910–1930	1910–1930
-	B38	B38	TDD	2570–2620	2570–2620
-	B39	B39	TDD	1880–1920	1880–1920
-	B40	B40	TDD	2300–2400	2300–2400
-	-	B41	TDD	2496–2690	2496–2690
-	-	B42	TDD	3400–3600	3400–3600
-	-	B43	TDD	3600–3800	3600–3800
-	-	B44	TDD	703–803	703–803
-	-	B45	TDD	1447–1467	1447–1467
-	-	B46	TDD	5150–5925	5150–5925
-	-	B47	TDD	5855–5925	5855–5925
-	-	B48	TDD	3550–3700	3550–3700
-	-	B50	TDD	1432–1517	1432–1517
-	-	B51	TDD	1427–1432	1427–1432

¹⁰ Restricted to E-UTRA operation when carrier aggregation is configured. The downlink operating band is paired with the uplink operating band (external) of the carrier aggregation configuration that is supporting the configured Pcell.

-	-	B52	TDD	3300–3400	3300–3400
-	-	B65	FDD	1920–2010	2110–2200
-	-	B66	FDD ¹¹	1710–1780	2110–2200
-	-	B67	FDD ¹⁰	-	738–758
-	-	B68	FDD	698–728	753–783
-	-	B69	FDD ¹⁰	-	2570–2620
-	-	B70	FDD ¹²	1695–1710	1995–2020
-	-	B71	FDD	663–698	617–652
-	-	B72	FDD	451–456	461–466
-	-	B73	FDD	450–455	460–465
-	-	B74	FDD	1427–1470	1475–1518
-	-	B75	FDD ¹⁰	-	1432–1517
-	-	B76	FDD ¹⁰	-	1427–1432
-	-	B85	FDD	698–716	728–746
-	-	B87	FDD	410–415	420–425
-	-	B88	FDD	412–417	422–427

¹¹ The range 2180–2200 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured.

¹² The range 2010–2020 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured and TX-RX separation is 300 MHz. The range 2005–2020 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured and TX-RX separation is 295 MHz.

Document History

Revision	Date	Changes
A	2025-02-28	The first revision.

9.1 FCC

9.1.1. Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations.
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).

The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

9.1.2. Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to NetPrisma that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

9.1.3. End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text:

“Contains FCC ID: 2BEY3HMT89LDA” “Contains IC: 32052-HMT89LDA “

The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

9.1.4. Antenna Installation

- (1)The antenna must be installed such that 20 cm is maintained between the antenna and users,
- (2)The transmitter module may not be co-located with any other transmitter or antenna.
- (3)Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

radiation, maximum antenna gain (including cable loss) must not exceed: Operating Band	FCC Max Antenna Gain (dBi)
LTE Band 2	8.00
LTE Band 4	5.00
LTE Band 5/LTE CA_5B	9.41

LTE Band 7/LTE CA_7C	8.00
LTE Band 12	8.70
LTE Band 13	9.16
LTE Band 14	9.23
LTE Band 17	8.74
LTE Band 25	8.00
LTE Band 26(814-824)	9.36
LTE Band 26(824-849)	9.41
LTE Band 30	-1.02
LTE Band 38/LTE CA_38C	5.00
LTE Band 41/LTE CA_41C	5.00
LTE Band 42(3450-3550) /LTE CA_42C	5.00
LTE Band 43(3700-3800)	5.00
LTE Band 48/LTE CA_48C	-2.00
LTE Band 66/LTE CA_66B/LTE CA_66C	5.00
LTE Band70	5.00
LTE Band71/N71	8.48
NR Band n2	12.01
NR Band n2 (MIMO)	12.01
NR Band n5	9.42
NR Band n5 (MIMO)	9.42
NR Band n7	8.00
NR Band n12	8.71
NR Band n13	8.99
NR Band n14	9.23
NR Band n25	8.00
NR Band n25(MIMO)	8.00
NR Band n26(814-824)	9.37
NR Band n26(824-849)	9.42
NR Band n30	-1.02
NR Band n38	5.00
NR Band n38(MIMO)	5.00
NR Band n41	5.00
NR Band n41(MIMO)	3.00
NR Band n48	-2.00
NR Band n48(MIMO)	-2.00

NR Band n66	5.00
NR Band n66(MIMO)	5.00
NR Band n70	5.00
NR Band n70(MIMO)	5.00
NR Band n71	8.48
NR Band n71(MIMO)	8.48
NR Band n77 (3450-3550)	2.00
NR Band n77 (3450-3550)(MIMO)	0.00
NR Band n77 (3700-3980)	2.00
NR Band n77 (3700-3980)(MIMO)	0.00
NR Band n78 (3450-3550)	2.00
NR Band n78 (3450-3550)(MIMO)	0.00
NR Band n78 (3700-3800)	2.00
NR Band n78 (3700-3800)(MIMO)	0.00

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

9.1.5. Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

9.1.6. Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency

energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

9.1.7. List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27 and part 90 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

9.1.8. This device is intended only for OEM integrators under the following conditions:(For module device use)

- 1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
- 2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

9.1.9. Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

9.2. IC

9.2.1. Industry Canada Statement

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:

- (1) This device may not cause interference; and
- (2) This device must accept any interference, including interference that may cause undesired operation of the device

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

- (1) l'appareil ne doit pas produire de brouillage, et
- (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

9.2.2. Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

9.2.3. Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISSED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

9.2.4. This device is intended only for OEM integrators under the following conditions: (For module device use)

- 1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
- 2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

9.2.5. Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

- 1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
- 2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

9.2.6. IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can

not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

9.2.7. NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada

9.2.8. End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains IC: 32052-HMT89LDA".

9.2.9. Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 32052-HMT89LDA".

9.2.10. Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

9.2.11. Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.

Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

9.2.12 Antenna Requirements

The following antennae were approved with the prototype:

This radio transmitter [32052-HMT89LDA] has been approved by innovation, Science and development Economic Canada to operate with the types of antennas listed below, with the maximum allowable gain indicated. The types of antennas not included in this list that have a gain of any type listed are strictly prohibited for use with this device.

Les antennes suivantes ont été approuvées avec le prototype:

Cet émetteur radio [32052-HMT89LDA] a été approuvé par innovation, Science et développement

économique Canada pour fonctionner avec les types d'antennes énumérés ci-dessous, avec le gain maximal autorisé indiqué. Les types d'antennes non inclus dans cette liste qui ont un gain tout type listé sont strictement interdits pour une utilisation avec cet appareil.

radiation, maximum antenna gain (including cable loss) must not exceed: Operating Band	Antenna Gain (dBi)
LTE Band 2	2.00
LTE Band 4	3.20
LTE Band 5/LTE CA_5B	1.00
LTE Band 7/LTE CA_7C	2.60
LTE Band 12	0.20
LTE Band 13	0.2
LTE Band 14	0.20
LTE Band 17	0.20
LTE Band 25	2.00
LTE Band 26(824-849)	1.00
LTE Band 30	-3.06
LTE Band 38/LTE CA_38C	2.60
LTE Band 41/LTE CA_41C	2.60
LTE Band 42(3450-3550) /LTE CA_42C	3.10
LTE Band 43(3700-3800)	3.10
LTE Band 48/LTE CA_48C	-4.29
LTE Band 66/LTE CA_66B/LTE CA_66C	3.20
LTE Band71	-0.50
NR Band n2	2.00
NR Band n2 (MIMO)	2.00
NR Band n5	1.00
NR Band n5 (MIMO)	1.00
NR Band n7	2.60
NR Band n12	0.20
NR Band n13	0.20
NR Band n14	0.20
NR Band n25	2.00
NR Band n25(MIMO)	2.00
NR Band n26(824-849)	1.00
NR Band n30	-3.06
NR Band n38	2.60

NR Band n38(MIMO)	2.60
NR Band n41	2.60
NR Band n41(MIMO)	2.60
NR Band n48	-4.29
NR Band n48(MIMO)	-4.29
NR Band n66	3.20
NR Band n66(MIMO)	3.20
NR Band n71	-0.50
NR Band n71(MIMO)	-0.50
NR Band n77 (3450-3900)	-3.48
NR Band n77 (3450-3900)(MIMO)	-3.48
NR Band n77 (3900-3980)	-3.48
NR Band n77 (3000-3980)(MIMO)	-3.48
NR Band n78 (3450-3800)	-4.11
NR Band n78 (3450-3800)(MIMO)	-4.11



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