



# HUC33-WWD

## Hardware Design

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# 1 Introduction

This document helps you gain a quick insight into HUC33-WWD module, its air and hardware interfaces, electrical and mechanical specifications, and other related information, as well. In addition, it includes some reference designs that, coupled with application notes and user guides, facilitate the development and deployment of your 5G RedCap module applications.

## 1.1. Text Conventions

Table 1: Text Conventions

|      |                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| dev  | Unless stated otherwise, the presence of the mark "dev" following a function, feature, interface, pin name, command, argument, etc., signifies that it is still in the development phase and not yet supported. Additionally, when "dev" appears after a model, it indicates that the model sample is currently unavailable.                                                                                                           |
| NOTE | "NOTE" is used to identify important information. When you see "NOTE" in this document, please be aware that the information contained therein may be crucial for understanding, implementing, or operating related technologies or steps. We strongly recommend that you pay special attention to these "NOTE" sections while reading the document to ensure that you can use this technical documentation correctly and efficiently. |

## 2 Product Overview

The module is an SMD module with compact packaging.

The module is an industrial-grade module for industrial and commercial applications only.

Table 2: Basic Information

| HUC33-WWD      |                                                 |
|----------------|-------------------------------------------------|
| Packaging type | LGA                                             |
| Pin counts     | 204 pins                                        |
| Dimensions     | (29.0 ±0.2) mm × (32.0 ±0.2) mm × (2.4 ±0.2) mm |
| Weight         | Approx. 5.2 g                                   |

### 2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

| HUC33-WWD       |                                                            |
|-----------------|------------------------------------------------------------|
| 5G NR SA        | n2/n5/n7/n12/n13/n14/n25/n26/n30/n38/n41/n66/n70/n71/n77   |
| LTE-FDD         | B2/B4/B5/B7/B12/B13/B14/B17/B25/B26/B28/B30<br>B66/B70/B71 |
| LTE-TDD         | B38/B41/B42/B43/B48                                        |
| GNSS (Optional) | GPS/GLONASS/BDS/Galileo/NavIC <sup>dev</sup> /QZSS         |

### 2.2. Key Features

The following table describes the detailed features of HUC33-WWD module.

Table 4: Key Features

| Category     | Description                                                                                                        |
|--------------|--------------------------------------------------------------------------------------------------------------------|
| Power Supply | <ul style="list-style-type: none"> <li>Supply voltage: 3.3–4.3 V</li> <li>Typical supply voltage: 3.8 V</li> </ul> |

|                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SMS                          | <ul style="list-style-type: none"> <li>● Only supports SMS over SGs, IMS and NAS</li> <li>● Text and PDU modes</li> <li>● Point-to-point MO and MT</li> <li>● SMS cell broadcast</li> <li>● SMS storage: ME by default</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                |
| eSIM <sup>1</sup>            | Optional                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| Transmit Power               | <ul style="list-style-type: none"> <li>● 5G NR bands: Class 3 (23 dBm <math>\pm</math>2 dB) <sup>2</sup></li> <li>● 5G NR n38/n41/n77/n78 HPUE <sup>3</sup>: Class 2 (26 dBm <math>\pm</math>2 dB)</li> <li>● LTE bands: Class 3 (23 dBm <math>\pm</math>2 dB) <sup>4</sup></li> <li>● LTE B38/B40/B41/B42/B43 HPUE: Class 2 (26 dBm <math>\pm</math>2 dB)</li> </ul>                                                                                                                                                                                                                                                                                            |
| 5G NR Features               | <ul style="list-style-type: none"> <li>● Supports 3GPP Rel-17 Redcap. 5G NR sub-6</li> <li>● Supported modulations: <ul style="list-style-type: none"> <li>- Uplink: QPSK, 16QAM, 64QAM and 256QAM modulations</li> <li>- Downlink: QPSK, 16QAM, 64QAM and 256QAM modulations</li> </ul> </li> <li>● Supports SCS 15 kHz <sup>5</sup> and 30 kHz <sup>5</sup></li> <li>● Supports SA Option 2</li> <li>● Max. transmission data rates <sup>6</sup>: <ul style="list-style-type: none"> <li>- SA: 223 Mbps (DL), 123 Mbps (UL)</li> </ul> </li> <li>● SRS: <ul style="list-style-type: none"> <li>- SA: 1T2R (n38/n40/n41/n48/n77/n78/n79)</li> </ul> </li> </ul> |
| LTE Features                 | <ul style="list-style-type: none"> <li>● Supports 3GPP Rel-16</li> <li>● Supported modulations: <ul style="list-style-type: none"> <li>- Uplink: QPSK, 16QAM, 64QAM and 256QAM modulations</li> <li>- Downlink: QPSK, 16QAM, 64QAM and 256QAM modulations</li> </ul> </li> <li>● Supports 1.4/3/5/10/15/20 MHz RF bandwidths</li> <li>● Max. transmission data rates <sup>6</sup>: <ul style="list-style-type: none"> <li>- 200 Mbps (DL), 105 Mbps (UL)</li> </ul> </li> </ul>                                                                                                                                                                                  |
| Internet Protocol Features   | Supports TCP/UDP/SSL/TLS/FTP(S)/HTTP(S)/MQTT(S)/SMTP(S)/NTP/PING/NITZ/LwM2M protocols                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| (U)SIM Interfaces            | <ul style="list-style-type: none"> <li>● Supports (U)SIM card: 1.8/3.0 V</li> <li>● Supports Dual SIM Single Standby</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| USB Tethering                | Supports RmNet, RNDIS, ECM, DUN, MBIM <sup>dev</sup>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| USB Interface                | <ul style="list-style-type: none"> <li>● Compliant with USB 2.0 specification; the data transmission rate can reach up to 480 Mbps</li> <li>● Used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging and firmware upgrade</li> <li>● Supports USB serial driver for: Windows 10/11, Linux 2.6–6.7, Android 4.x–14.x</li> </ul>                                                                                                                                                                                                                                                                                     |
| UARTs                        | <p><b>Main UART:</b></p> <ul style="list-style-type: none"> <li>● Used for AT command communication and data transmission</li> <li>● Baud rate reaches up to 4 Mbps, 115200 bps by default</li> <li>● Supports RTS and CTS hardware flow control</li> </ul> <p><b>Debug UART:</b></p> <ul style="list-style-type: none"> <li>● Used for Linux console and log output</li> <li>● 115200 bps baud rate</li> </ul>                                                                                                                                                                                                                                                  |
| PCM Interface <sup>dev</sup> | <ul style="list-style-type: none"> <li>● Used for audio function with external codec</li> <li>● Supports 16-bit linear data format</li> <li>● Supports long frame synchronization and short frame synchronization</li> <li>● Supports master and slave modes, but must be the master in long frame synchronization</li> </ul>                                                                                                                                                                                                                                                                                                                                    |
| SPI Interface                | <ul style="list-style-type: none"> <li>● One SPI interface, only supports master mode</li> <li>● Provides a full-duplex, synchronous and serial communication link with the peripheral devices</li> <li>● 1.8 V operation voltage with a maximum clock frequency of 50 MHz</li> </ul>                                                                                                                                                                                                                                                                                                                                                                            |
| PCIe Interface               | <ul style="list-style-type: none"> <li>● Compliant with PCIe Gen 2, 1 lane</li> <li>● Supports RC (Root Complex) mode and EP (End Point) mode</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

<sup>1</sup> If you need this function, contact NetPrisma Technical Support for more details.

<sup>2</sup> The transmit power of n30 is Class 3 (22 dBm  $\pm$ 2 dB).

<sup>3</sup> HPUE is only for 5G single carrier with bandwidth not more than 20 MHz.

<sup>4</sup> The transmit power of B30 is Class 3 (22 dBm  $\pm$ 2 dB).

<sup>5</sup> 5G NR FDD bands only support 15 kHz SCS, and 5G NR TDD bands only support 30 kHz SCS.

<sup>6</sup> The maximum rates are theoretical and the actual values depend on the network configuration.

|                           |                                                                                                                                                                                                                                                                                               |
|---------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                           | <ul style="list-style-type: none"> <li>● Could be used to connect Wi-Fi</li> </ul>                                                                                                                                                                                                            |
| SGMII Interface           | Supports 10 Mbps/100 Mbps/1000 Mbps Ethernet work mode                                                                                                                                                                                                                                        |
| Network Status Indication | <ul style="list-style-type: none"> <li>● NET_MODE: used for network registration status indication</li> <li>● NET_STATUS: used for network connectivity status indication</li> </ul>                                                                                                          |
| Antenna Interfaces        | <ul style="list-style-type: none"> <li>● Main antenna interface (ANT_MAIN)</li> <li>● Diversity antenna interface (ANT_DRX)</li> <li>● GNSS antenna interface (ANT_GNSS) (optional)</li> <li>● 50 <math>\Omega</math> characteristic impedance</li> </ul>                                     |
| Rx-diversity              | Supports 5G NR/LTE Rx-diversity                                                                                                                                                                                                                                                               |
| GNSS Features (Optional)  | <ul style="list-style-type: none"> <li>● Supports L1/L5</li> <li>● Supports GPS, GLONASS, BDS, Galileo, NavIC <sup>dev</sup>, QZSS</li> <li>● Protocol: NMEA 0183</li> <li>● Data update rate: 1 Hz by default</li> <li>● Supports AGNSS. For more details, see <b>document 1</b>.</li> </ul> |
| AT Commands               | <ul style="list-style-type: none"> <li>● Compliant with 3GPP TS 27.007, 3GPP TS 27.005</li> <li>● NetPrisma enhanced AT commands</li> </ul>                                                                                                                                                   |
| Firmware Upgrade          | USB interface or FOTA                                                                                                                                                                                                                                                                         |
| Temperature Range         | <ul style="list-style-type: none"> <li>● Normal operating temperature <sup>7</sup>: -30 to +75 °C</li> <li>● Extended operating temperature <sup>8</sup>: -40 to +85 °C</li> <li>● Storage temperature: -40 to +90 °C</li> </ul>                                                              |
| RoHS                      | All hardware components are fully complying with EU RoHS directive                                                                                                                                                                                                                            |

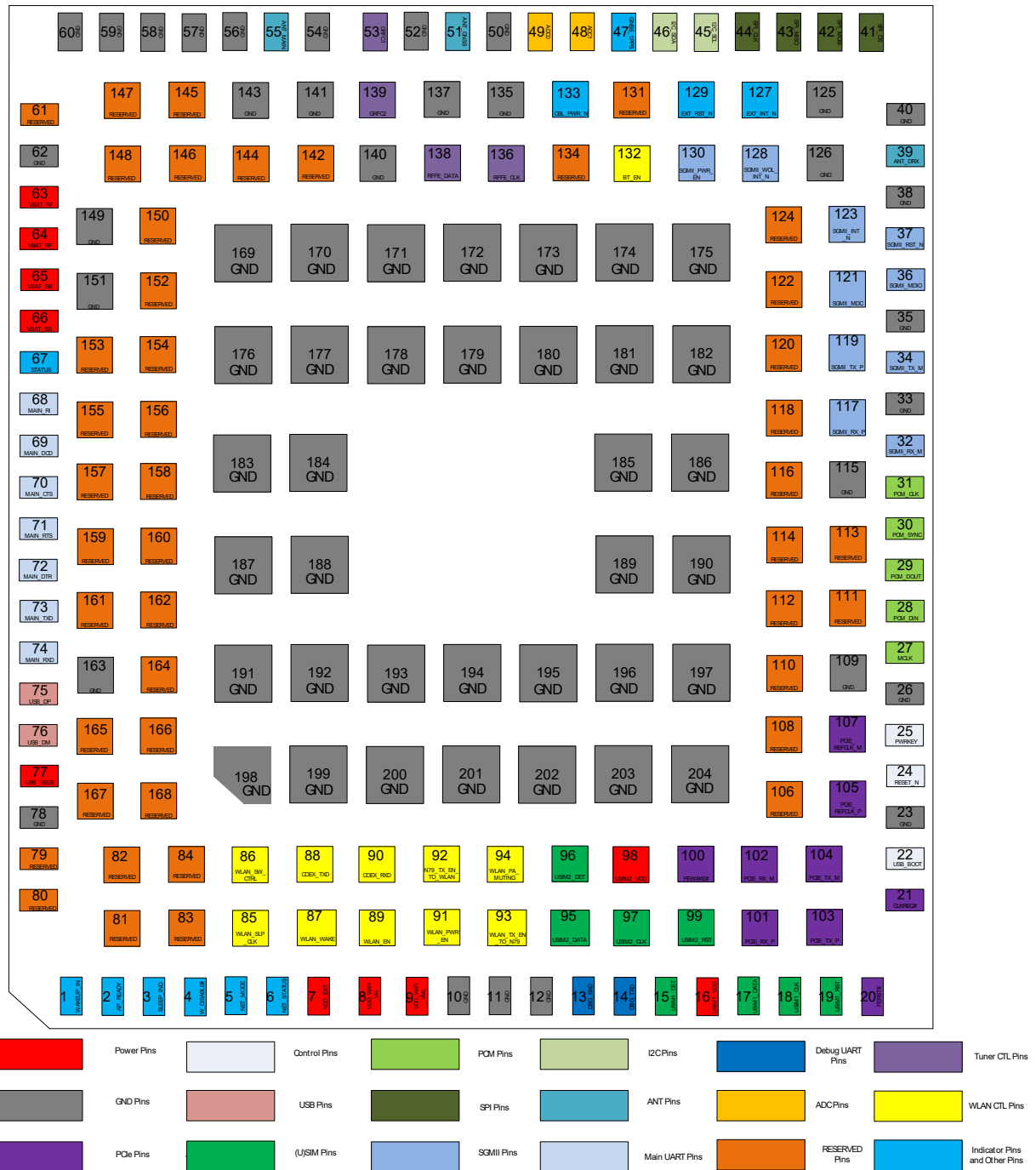
<sup>7</sup> To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

<sup>8</sup> To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within the range of -40 to -30 °C or 75 to 85 °C, the module remains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P<sub>out</sub>, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

## 2.3. Pin Assignment

The following figure shows the pin assignment of the module.

*Figure 1: Pin Assignment (Top View)*



### NOTE

Ensure that the pull-up power supply of the module's pins is VDD\_EXT or controlled by VDD\_EXT, and there is no current sink on the module's pins before the module turns on. For more details, contact NetPrisma Technical Support.

## 2.4. Pin Definitions

The following table shows the DC characteristics and pin descriptions.

Table 5: Parameter Definition

| Parameter | Description          |
|-----------|----------------------|
| AI        | Analog Input         |
| AO        | Analog Output        |
| AIO       | Analog Input/Output  |
| DI        | Digital Input        |
| DO        | Digital Output       |
| DIO       | Digital Input/Output |
| OD        | Open Drain           |
| PI        | Power Input          |
| PO        | Power Output         |

DC characteristics include power domain and rated current.

Table 6: Pin Description

| Power Supply |         |     |                                     |                                              |                                                                                                |
|--------------|---------|-----|-------------------------------------|----------------------------------------------|------------------------------------------------------------------------------------------------|
| Pin Name     | Pin No. | I/O | Description                         | DC Characteristic s                          | Comment                                                                                        |
| VBAT_BB      | 65, 66  | PI  | Power supply for module's BB part   | Vmax = 4.3 V<br>Vmin = 3.3 V<br>Vnom = 3.8 V |                                                                                                |
| VBAT_RF      | 63, 64  | PI  | Power supply for module's RF part   |                                              |                                                                                                |
| VDD_EXT      | 7       | PO  | Provide 1.8 V for external circuits | Vnom = 1.8 V<br>Iomax = 50 mA                | Power supply for external GPIO's pull-up circuits. A test point is recommended to be reserved. |
| VDD_WIFI_VH  | 8       | PO  | Power supply for Wi-Fi              | Vnom = 1.824 V<br>Iomax = 200 mA             | Internal power supply for Wi-Fi. Uncontrollable power supply.                                  |
| VDD_WIFI_VML | 9       | PO  | Power supply for Wi-Fi              | Vnom = 1.244 V<br>Iomax = 800 mA             |                                                                                                |
| GND          |         |     |                                     |                                              |                                                                                                |

| Pin Name | Pin No.                                                                                                                       | Comment                       |
|----------|-------------------------------------------------------------------------------------------------------------------------------|-------------------------------|
| GND      | 10–12, 23, 26, 33, 35, 38, 40, 50, 52, 54, 56–60, 62, 78, 109, 115, 125, 126, 135, 137, 140, 141, 143, 149, 151, 163, 169–204 | Connect these pins to ground. |

#### Turn On/Off

| Pin Name  | Pin No. | I/O | Description                     | DC Characteristic<br>s | Comment                                                                                                       |
|-----------|---------|-----|---------------------------------|------------------------|---------------------------------------------------------------------------------------------------------------|
| PWRKEY    | 25      | DI  | Turn on/off the module          |                        | Pulled up internally to 1.5 V power domain.                                                                   |
| CBL_PWR_N | 133     | DI  | Initiate power on when grounded |                        | Alternate input pin which can be used to initiate the power-up sequence when grounded; pulled up internally.  |
| RESET_N   | 24      | DI  | Reset the module                |                        | Pulled up internally to 1.5 V power domain. Active low. A test point is recommended to be reserved if unused. |

#### Indication Signals

| Pin Name   | Pin No. | I/O | Description                                     | DC Characteristic<br>s | Comment                                                            |
|------------|---------|-----|-------------------------------------------------|------------------------|--------------------------------------------------------------------|
| STATUS     | 67      | OD  | Indicate the module's operation status          |                        | An external pull-up resistor is required. If unused, keep it open. |
| NET_MODE   | 5       | DO  | Indicate the module's network registration mode | VDD_EXT                | If unused, keep them open.                                         |
| NET_STATUS | 6       | DO  | Indicate the module's network activity status   |                        |                                                                    |

#### USB Interface

| Pin Name | Pin No. | I/O | Description                   | DC Characteristic<br>s                        | Comment                                                               |
|----------|---------|-----|-------------------------------|-----------------------------------------------|-----------------------------------------------------------------------|
| USB_VBUS | 77      | PI  | USB connection detect         | Vmax = 5.25 V<br>Vmin = 3.3 V<br>Vnom = 5.0 V | A test point must be reserved.                                        |
| USB_DP   | 75      | AIO | USB 2.0 differential data (+) |                                               | Require differential impedance of 90 Ω. Test points must be reserved. |
| USB_DM   | 76      | AIO | USB 2.0 differential data (-) |                                               |                                                                       |

#### (U)SIM Interfaces

| Pin Name  | Pin No. | I/O | Description               | DC Characteristic<br>s                                                 | Comment                                                         |
|-----------|---------|-----|---------------------------|------------------------------------------------------------------------|-----------------------------------------------------------------|
| USIM1_VDD | 16      | PO  | (U)SIM1 card power supply | <b>High-voltage:</b><br>Vmin = 2.7 V<br>Vnom = 2.85 V<br>Vmax = 3.05 V | Either 1.8 V or 3.0 V is supported by the module automatically. |

|            |         |     |                                      |                                                                                                                                                                                                            |                                                    |
|------------|---------|-----|--------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------|
|            |         |     |                                      | Low-voltage:<br>Vmin = 1.7 V<br>Vnom = 1.8 V<br>Vmax = 1.9 V                                                                                                                                               |                                                    |
| USIM1_DATA | 17      | DIO | (U)SIM1 card data                    | USIM1_VDD                                                                                                                                                                                                  | Pulled up internally with a 20 kΩ resistor.        |
| USIM1_CLK  | 18      | DO  | (U)SIM1 card clock                   |                                                                                                                                                                                                            |                                                    |
| USIM1_RST  | 19      | DO  | (U)SIM1 card reset                   |                                                                                                                                                                                                            |                                                    |
| USIM1_DET  | 15      | DI  | (U)SIM1 card hot-plug detect         | VDD_EXT                                                                                                                                                                                                    | If unused, keep it open.                           |
| USIM2_VDD  | 98      | PO  | (U)SIM2 card power supply            | High-voltage:<br>Vmin = 2.7 V<br>Vnom = 2.85 V<br>Vmax = 3.05 V<br><br>Low-voltage:<br>Vmin = 1.7 V<br>Vnom = 1.8 V<br>Vmax = 1.9 V<br><br>Either 1.8 V or 3.0 V is supported by the module automatically. |                                                    |
| USIM2_DATA | 95      | DIO | (U)SIM2 card data                    | USIM2_VDD                                                                                                                                                                                                  | Pulled up internally with a 20 kΩ resistor.        |
| USIM2_CLK  | 97      | DO  | (U)SIM2 card clock                   |                                                                                                                                                                                                            |                                                    |
| USIM2_RST  | 99      | DO  | (U)SIM2 card reset                   |                                                                                                                                                                                                            |                                                    |
| USIM2_DET  | 96      | DI  | (U)SIM2 card hot-plug detect         | VDD_EXT                                                                                                                                                                                                    | If unused, keep it open.                           |
| Main UART  |         |     |                                      |                                                                                                                                                                                                            |                                                    |
| Pin Name   | Pin No. | I/O | Description                          | DC Characteristics                                                                                                                                                                                         | Comment                                            |
| MAIN_RI    | 68      | DO  | Main UART ring indication            | VDD_EXT                                                                                                                                                                                                    | If unused, keep them open.                         |
| MAIN_DCD   | 69      | DO  | Main UART data carrier detect        |                                                                                                                                                                                                            |                                                    |
| MAIN_CTS   | 70      | DO  | Clear to send signal from the module |                                                                                                                                                                                                            | Connect to the MCU's CTS. If unused, keep it open. |
| MAIN_RTS   | 71      | DI  | Request to send signal to the module |                                                                                                                                                                                                            | Connect to the MCU's RTS. If unused, keep it open. |
| MAIN_DTR   | 72      | DI  | Main UART data terminal ready        |                                                                                                                                                                                                            |                                                    |
| MAIN_TXD   | 73      | DO  | Main UART transmit                   |                                                                                                                                                                                                            | If unused, keep them open.                         |
| MAIN_RXD   | 74      | DI  | Main UART receive                    |                                                                                                                                                                                                            |                                                    |
| Debug UART |         |     |                                      |                                                                                                                                                                                                            |                                                    |
| Pin Name   | Pin No. | I/O | Description                          | DC Characteristics                                                                                                                                                                                         | Comment                                            |
| DBG_TXD    | 14      | DO  | Debug UART transmit                  | VDD_EXT                                                                                                                                                                                                    | Test points must be reserved.                      |

|                |         |        |                               |                        |                                                                                   |
|----------------|---------|--------|-------------------------------|------------------------|-----------------------------------------------------------------------------------|
| DBG_RXD        | 13      | DI     | Debug UART receive            |                        | If unused, keep them open.                                                        |
| ADC Interfaces |         |        |                               |                        |                                                                                   |
| Pin Name       | Pin No. | I/O    | Description                   | DC Characteristic<br>s | Comment                                                                           |
| ADC0           | 49      | AI     | General-purpose ADC interface | 0–VBAT_BB              | If unused, keep them open.                                                        |
| ADC1           | 48      | AI     |                               |                        |                                                                                   |
| PCM Interface  |         |        |                               |                        |                                                                                   |
| Pin Name       | Pin No. | I/O    | Description                   | DC Characteristic      | Comment                                                                           |
| MCLK           | 27      | DO     | Master clock output for codec | VDD_EXT                | If unused, keep them open.                                                        |
| PCM_DIN        | 28      | DI     | PCM data input                |                        |                                                                                   |
| PCM_DOUT       | 29      | DO     | PCM data output               |                        |                                                                                   |
| PCM_SYNC       | 30      | DIO    | PCM data frame sync           |                        |                                                                                   |
| PCM_CLK        | 31      | DIO    | PCM clock                     |                        |                                                                                   |
| I2C Interface  |         |        |                               |                        |                                                                                   |
| Pin Name       | Pin No. | I/O    | Description                   | DC Characteristic      | Comment                                                                           |
| I2C_SCL        | 45      | OD     | I2C serial clock              | VDD_EXT                | Pull each of them up to VDD_EXT with 4.7 kΩ resistors. If unused, keep them open. |
| I2C_SDA        | 46      | OD     | I2C serial data               |                        |                                                                                   |
| PCIe Interface |         |        |                               |                        |                                                                                   |
| Pin Name       | Pin No. | I/O    | Description                   | DC Characteristic<br>s | Comment                                                                           |
| PCIE_REFCLK_P  | 105     | AIO    | PCIe reference clock (+)      | VDD_EXT                | Require differential impedance of 85 Ω. If unused, keep them open.                |
| PCIE_REFCLK_M  | 107     |        | PCIe reference clock (-)      |                        |                                                                                   |
| PCIE_TX_P      | 103     | AO     | PCIe transmit (+)             |                        |                                                                                   |
| PCIE_TX_M      | 104     |        | PCIe transmit (-)             |                        |                                                                                   |
| PCIE_RX_P      | 101     | AI     | PCIe receive (+)              |                        |                                                                                   |
| PCIE_RX_M      | 102     |        | PCIe receive (-)              |                        |                                                                                   |
| PERST#         | 20      | DIO    | PCIe reset                    |                        |                                                                                   |
| CLKREQ#        | 21      | OD/DIO | PCIe clock request            |                        |                                                                                   |
| PEWAKE#        | 100     | OD/DIO | PCIe wake up                  |                        |                                                                                   |

## WLAN Coexistence and Control Interface

| Pin Name          | Pin No. | I/O | Description                                           | DC Characteristic<br>s | Comments     |
|-------------------|---------|-----|-------------------------------------------------------|------------------------|--------------|
| WLAN_SLP_CLK      | 85      | DO  | WLAN sleep clock                                      |                        |              |
| WLAN_PWR_EN       | 91      | DO  | WLAN power supply enable control                      |                        | Active high. |
| WLAN_WAKE         | 87      | DI  | Wake up module by an external Wi-Fi                   |                        |              |
| COEX_RXD          | 90      | DI  | 5G/LTE and WLAN coexistence receive                   | VDD_EXT                |              |
| COEX_TXD          | 88      | DO  | 5G/LTE and WLAN coexistence transmit                  |                        |              |
| N79_TX_EN_TO_WLAN | 92      | DO  | Notify n79 transmission from SDR transceiver to WLAN  |                        |              |
| WLAN_TX_EN_TO_N79 | 93      | DI  | Notify WLAN transmission from WLAN to SDR transceiver | VDD_EXT                |              |
| WLAN_PA_MUTING    | 94      | DO  | GPIO from SDX to disable WLAN PA                      |                        |              |
| WLAN_SW_CTRL      | 86      | DI  | Wi-Fi power control                                   | VDD_EXT                |              |
| WLAN_EN           | 89      | DO  | WLAN function enable control                          |                        | Active high. |
| BT_EN             | 132     | DO  | Bluetooth enable control                              |                        |              |

## SPI Interface

| Pin Name | Pin No. | I/O | Description             | DC Characteristic<br>s | Comments                       |
|----------|---------|-----|-------------------------|------------------------|--------------------------------|
| SPI_CS   | 41      | DO  | SPI chip select         |                        |                                |
| SPI_MOSI | 42      | DO  | SPI master-out slave-in | VDD_EXT                | Only master mode is supported. |
| SPI_MISO | 43      | DI  | SPI master-in slave-out |                        |                                |
| SPI_CLK  | 44      | DO  | SPI clock               |                        |                                |

## SGMII & CTL Interface

| Pin Name        | Pin No. | I/O | Description                         | DC Characteristic<br>s | Comments                                      |
|-----------------|---------|-----|-------------------------------------|------------------------|-----------------------------------------------|
| SGMII_RST_N     | 37      | DO  | SGMII reset external PHY            |                        | If unused, keep them open.                    |
| SGMII_INT_N     | 123     | DI  | SGMII interrupt                     |                        |                                               |
| SGMII_WOL_INT_N | 128     | DI  | Wake-on-LAN interrupt input         | VDD_EXT                |                                               |
| SGMII_PWR_EN    | 130     | DO  | Enable external power for SGMII PHY |                        |                                               |
| SGMII_MDIO      | 36      | DIO | SGMII management data input/output  |                        | Pull it up to VDD_EXT with a 1.5 kΩ resistor. |

|            |     |    |                             |                                                                                       |
|------------|-----|----|-----------------------------|---------------------------------------------------------------------------------------|
|            |     |    |                             | If unused, keep it open.                                                              |
| SGMII_MDC  | 121 | DO | SGMII management data clock | If unused, keep it open.                                                              |
| SGMII_TX_M | 34  | AO | SGMII transmit (-)          | Connect with a 0.1 $\mu$ F capacitor. Require differential impedance of 90 $\Omega$ . |
| SGMII_TX_P | 119 |    | SGMII transmit (+)          |                                                                                       |
| SGMII_RX_M | 32  | AI | SGMII receive (-)           | Require differential impedance of 90 $\Omega$ .                                       |
| SGMII_RX_P | 117 |    | SGMII receive (+)           |                                                                                       |

### Antenna Interfaces

| Pin Name | Pin No. | I/O | Description                 | DC Characteristics | Comment                                         |
|----------|---------|-----|-----------------------------|--------------------|-------------------------------------------------|
| ANT_DRX  | 39      | AIO | Diversity antenna interface |                    | 50 $\Omega$ impedance.                          |
| ANT_MAIN | 55      | AIO | Main antenna interface      |                    | 50 $\Omega$ impedance.                          |
| ANT_GNSS | 51      | AI  | GNSS antenna interface      |                    | 50 $\Omega$ impedance. If unused, keep it open. |

### Antenna Tuner Control Interface

| Pin Name  | Pin No. | I/O | Description                       | DC Characteristic<br>s | Comment                    |
|-----------|---------|-----|-----------------------------------|------------------------|----------------------------|
| RFFE_DATA | 138     | DIO | Used for external MIPI IC control | VDD_EXT                | If unused, keep them open. |
| RFFE_CLK  | 136     | DO  |                                   |                        |                            |
| GRFC1     | 53      | DO  | Generic RF controller             |                        |                            |
| GRFC2     | 139     | DO  |                                   |                        |                            |

### Other Interfaces

| Pin Name                | Pin No. | I/O | Description                      | DC Characteristics | Comment                                                                                                       |
|-------------------------|---------|-----|----------------------------------|--------------------|---------------------------------------------------------------------------------------------------------------|
| WAKEUP_IN               | 1       | DI  | Wake up the module               | VDD_EXT            | Wake up the module at low voltage level. If unused, keep it open.                                             |
| W_DISABLE#              | 4       | DI  | Airplane mode control            |                    | At low voltage level, the module can enter into airplane mode. If unused, keep it open. Pulled up by default. |
| AP_READY <sup>dev</sup> | 2       | DI  | Application processor ready      |                    | If unused, keep them open.                                                                                    |
| SLEEP_IND               | 3       | DO  | Indicate the module's sleep mode |                    |                                                                                                               |

|           |     |    |                           |
|-----------|-----|----|---------------------------|
| EXT_INT_N | 127 | DI | External audio interrupt  |
| EXT_RST_N | 129 | DO | External audio reset      |
| GNSS_1PPS | 47  | DO | Support 1PPS pulse output |

#### USB\_BOOT

| Pin Name | Pin No. | I/O | Description                             | DC Characteristic<br>s | Comment                                                                            |
|----------|---------|-----|-----------------------------------------|------------------------|------------------------------------------------------------------------------------|
| USB_BOOT | 22      | DI  | Force the module to enter download mode | VDD_EXT                | It cannot be pulled up before startup. A test point is recommended to be reserved. |

#### RESERVED Pins

| Pin Name | Pin No.                                                                                              | Comment               |
|----------|------------------------------------------------------------------------------------------------------|-----------------------|
| RESERVED | 61, 79–84, 106, 108, 110–114, 116, 118, 120, 122, 124, 131, 134, 142, 144–148, 150, 152–162, 164–168 | Keep these pins open. |

#### NOTE

To reduce the probability of module damage and extend module service life, do not power up and down frequently.

## 2.5. EVB Kit

NetPrisma supplies an evaluation board (5G-REDCAP EVB) with accessories to develop and test the module. For more details, see **document 3**.

## 3 Operating Characteristics

### 3.1. Operating Modes

The following table briefly outlines the operating modes to be mentioned in the following chapters.

*Table 7: Overview of Operating Modes*

| Mode                       | Details                                                                                                                                                                                          |                                                                                                                              |
|----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------|
| Full Functionality Mode    | Idle                                                                                                                                                                                             | Software is active. The module has registered on the network, and it is ready to send and receive data.                      |
|                            | Data                                                                                                                                                                                             | Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transmission rate. |
| Minimum Functionality Mode | <b>AT+CFUN=0</b> can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card are invalid.                               |                                                                                                                              |
| Airplane Mode              | <b>AT+CFUN=4</b> or W_DISABLE# pin can set the module to enter airplane mode. In this case, RF function is invalid and all AT commands related to it are inaccessible.                           |                                                                                                                              |
| Sleep Mode                 | The power consumption of the module is reduced to an ultra-low level. During this mode, the module can still receive paging message, SMS and TCP/UDP data from the network normally.             |                                                                                                                              |
| Power Down Mode            | The power management unit shuts down the power supply. Software goes inactive. The serial interface is not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) is still maintained. |                                                                                                                              |

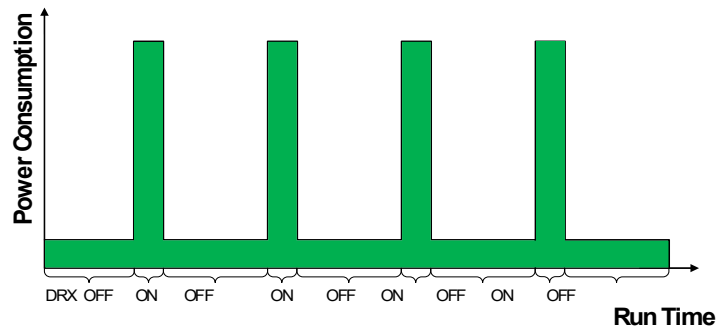
#### NOTE

For more details about **AT+CFUN**, see *document 4*.

### 3.2. Sleep Mode

With DRX technology, power consumption of the module will be reduced to an ultra-low level.

Figure 2: Module Power Consumption in Sleep Mode



## NOTE

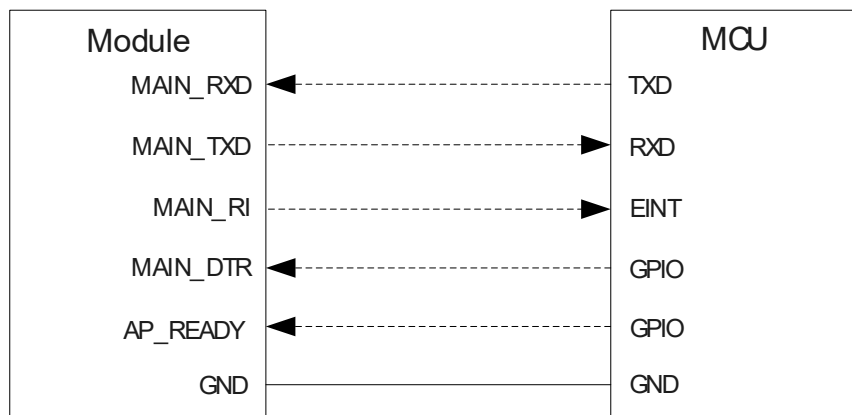
DRX cycle values are transmitted over the wireless network.

### 3.2.1. UART Application Scenario

If the module communicates with the MCU via UART, both the following preconditions should be met to set the module to sleep mode:

- Execute **AT+QSClk=1** to enable sleep mode.
- Drive MAIN\_DTR to high level or keep it open.

Figure 3: Sleep Mode Application via UART



- Driving MAIN\_DTR to low level with MCU will wake up the module.
- When the module has a URC to report, MAIN\_RI signal will wake up MCU. See **Chapter 4.10.3** for details about MAIN\_RI behaviors.
- AP\_READY<sup>dev</sup> detects the sleep state of MCU (can be configured to high level or low level detection). For more details about **AT+QCFG="apready"**, see **document 4**.

### 3.2.2. USB Application Scenarios

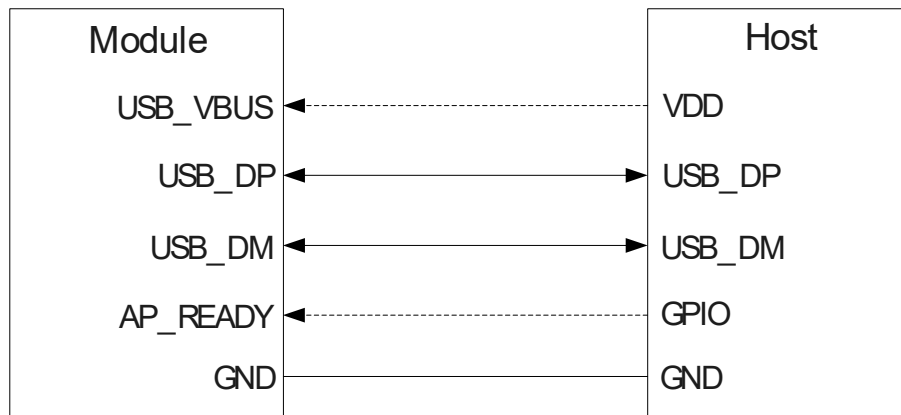
For the two situations ("USB application with USB remote wakeup function" and "USB application with USB Suspend/Resume and MAIN\_RI function") below, three preconditions must be met to set the module to sleep mode:

- Execute **AT+QSClk=1**.
- Ensure MAIN\_DTR is held at high level or is kept unconnected.
- Ensure the host's USB bus, which is connected to the module's USB interface, enters Suspend state.

### 3.2.2.1. USB Application with USB Suspend/Resume and USB Remote Wakeup Function

The following figure shows the connection between the module and the host.

*Figure 4: Sleep Mode Application with USB Suspend/Resume and USB Remote Wakeup*



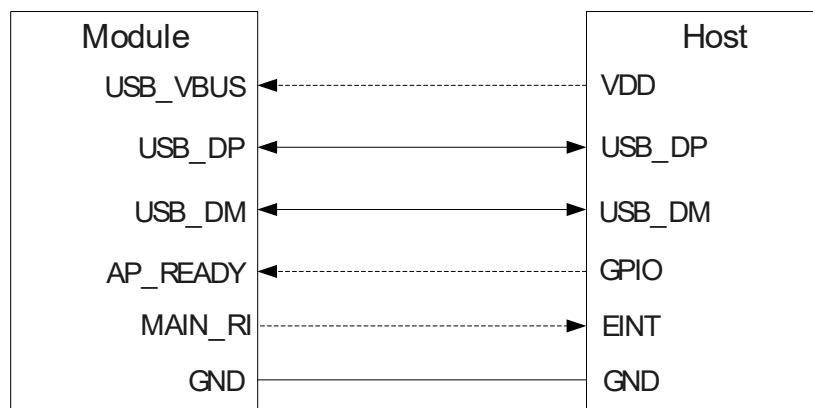
- Sending data to the module via USB will wake up the module.
- When the module has a URC to report, the module will send remote wake-up signals through USB bus to wake up the host.

### 3.2.2.2. USB Application with USB Suspend/Resume and MAIN\_RI Function

If the host supports USB Suspend and Resume, but does not support remote wake-up function, the MAIN\_RI signal is needed to wake up the host.

The following figure shows the connection between the module and the host.

*Figure 5: Sleep Mode Application with MAIN\_RI*



- Sending data to the module via USB will wake up the module.
- When the module has a URC to report, the module will wake up the host through MAIN\_RI signal.

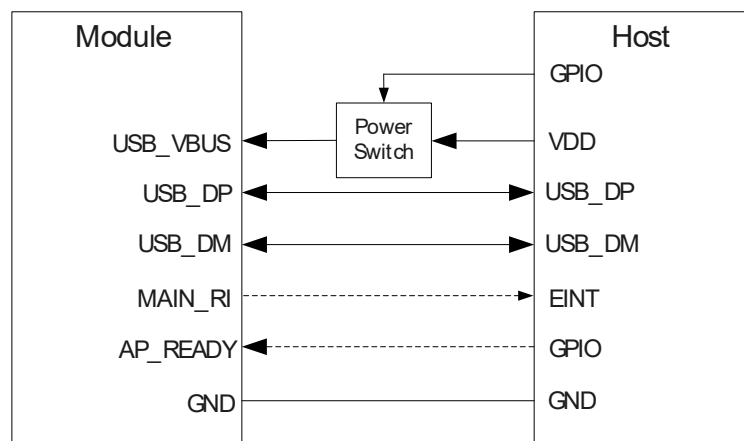
### 3.2.2.3. USB Application without USB Suspend Function

If the host does not support USB Suspend function, the following three preconditions must be met to set the module to sleep mode:

- Execute **AT+QSCLK=1**.
- Ensure MAIN\_DTR is held at high level or is kept unconnected.
- Ensure USB\_VBUS is unconnected via the external control circuit.

The following figure shows the connection between the module and the host.

*Figure 6: Sleep Mode Application without Suspend Function*



Switching on the power switch to power USB\_VBUS will wake up the module.

## NOTE

Pay attention to the level match shown in dotted line between the module and the host.

## 3.3. Airplane Mode

When the module enters airplane mode, the RF function does not work and all AT commands related to the RF function are inaccessible. This mode can be set via the following ways.

### Hardware:

The W\_DISABLE# pin is pulled up by default. Driving W\_DISABLE# to low makes the module enter airplane mode.

### Software:

**AT+CFUN=<fun>** provides choices of the functionality level by setting <fun> into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality. Both RF and (U)SIM functions are disabled.
- **AT+CFUN=1:** Full functionality (default).
- **AT+CFUN=4:** Airplane mode. RF function is disabled.

## NOTE

1. The execution of **AT+CFUN** does not affect GNSS function.
2. For details about the AT commands, see **document 4**.

## 3.4. Power Supply

### 3.4.1. Power Supply Pins

The module provides four VBAT pins for connection with the external power supply. There are two separate voltage domains for VBAT.

- Two VBAT\_RF pins for module's RF part
- Two VBAT\_BB pins for module's BB part

*Table 8: Pin Definition of Power Supply*

| Pin Name | Pin No.                                                                                                                       | Description                       | Min. | Typ. | Max. | Unit |
|----------|-------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|------|------|------|------|
| VBAT_RF  | 63, 64                                                                                                                        | Power supply for module's RF part | 3.3  | 3.8  | 4.3  | V    |
| VBAT_BB  | 65, 66                                                                                                                        | Power supply for module's BB part | 3.3  | 3.8  | 4.3  | V    |
| GND      | 10–12, 23, 26, 33, 35, 38, 40, 50, 52, 54, 56–60, 62, 78, 109, 115, 125, 126, 135, 137, 140, 141, 143, 149, 151, 163, 169–204 |                                   | -    | -    | -    | V    |

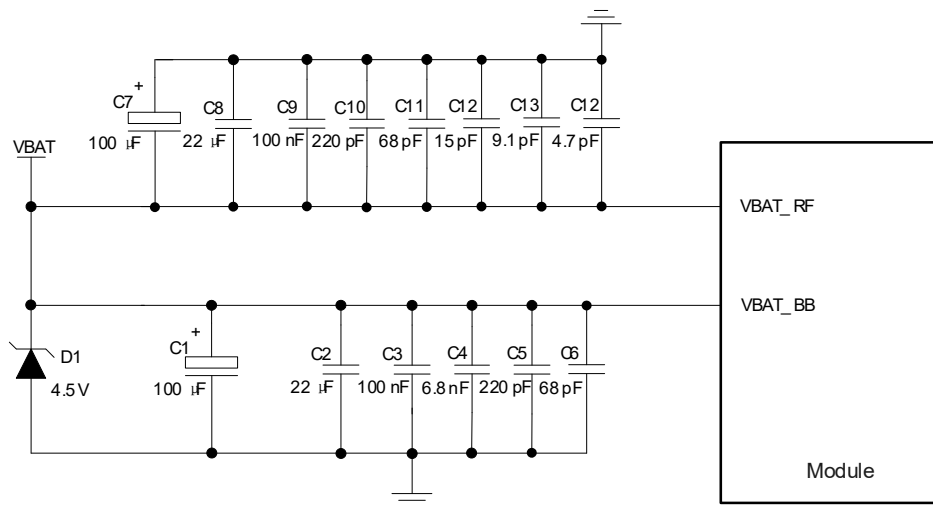
### 3.4.2. Requirements for Voltage Stability

The power supply range of the module is from 3.3 V to 4.3 V. Make sure that the input voltage never drops below 3.3 V.

To decrease the voltage drop, two 100  $\mu$ F capacitors with low ESR ( $ESR \leq 0.7 \Omega$ ) should be used, and a multi-layer ceramic chip (MLCC) array should also be reserved due to its ultra-low ESR. It is recommended to use five ceramic capacitors (22  $\mu$ F, 100 nF, 6.8 nF, 220 pF, 68 pF) for VBAT\_BB pins and seven ceramic capacitors (22  $\mu$ F, 100 nF, 220 pF, 68 pF, 15 pF, 9.1 pF, 4.7 pF) for VBAT\_RF pins for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application has to be a single voltage source which can supply power along two sub paths with star structure. The width of VBAT\_BB trace should be not less than 1.5 mm; and the width of VBAT\_RF trace should be not less than 2 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to avoid the damage caused by electric surge and electrostatics discharge (ESD), it is suggested that a TVS with suggested low reverse stand-off voltage  $V_{RWM}$  4.5 V, low clamping voltage  $V_C$  and high reverse peak pulse current  $I_{PP}$  should be used. The following figure shows the star structure of the power supply.

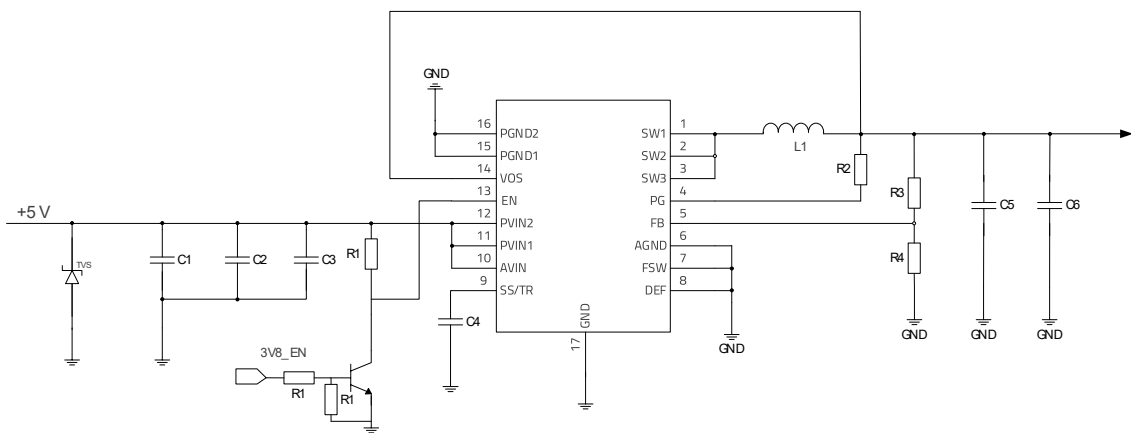
Figure 7: Star Configuration of Power Supply



### 3.4.3. Reference Design for Power Supply

The following figure shows a reference design for 5.0 V input power source. The typical output of the power supply is about 3.8 V. The continuous current of the power supply should be 1.5 A at least and the peak current should be 2.0 A at least.

Figure 8: Reference Circuit of Power Supply



### NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.

### 3.4.4. Power Supply Voltage Monitoring

**AT+CBC** can be used to monitor the VBAT\_BB voltage value. For more details, see **document 4**.

## 3.5. Turn on

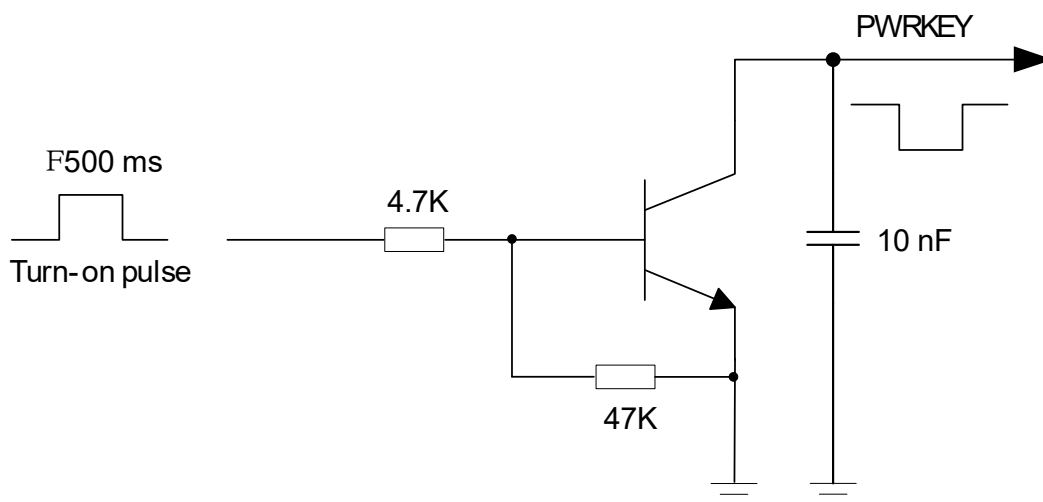
### 3.5.1. Turn on with PWRKEY

*Table 9: Pin Definition of PWRKEY*

| Pin Name | Pin No. | I/O | Description            | Comment                                     |
|----------|---------|-----|------------------------|---------------------------------------------|
| PWRKEY   | 25      | DI  | Turn on/off the module | Pulled up internally to 1.5 V power domain. |

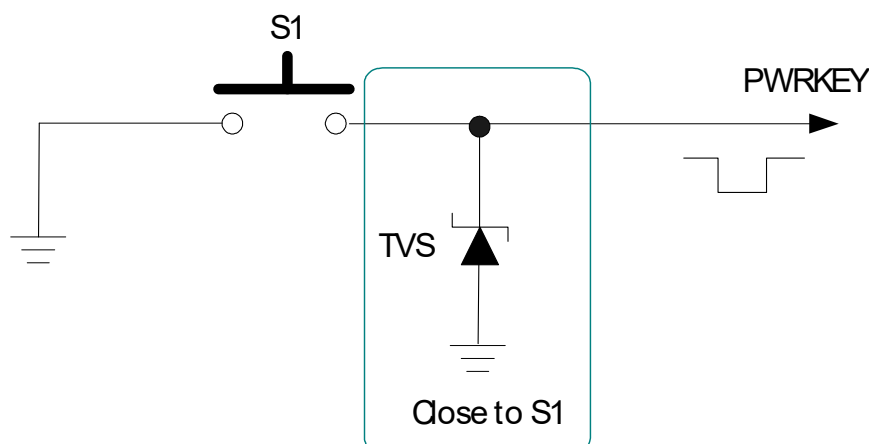
When the module is in turn-off mode, it can be turned on to normal mode by driving PWRKEY to low level for at least 500 ms. It is recommended to use an open drain/collector driver to control PWRKEY. A simple reference circuit is illustrated in the following figure.

*Figure 9: Turn on the Module by Using Driving Circuit*



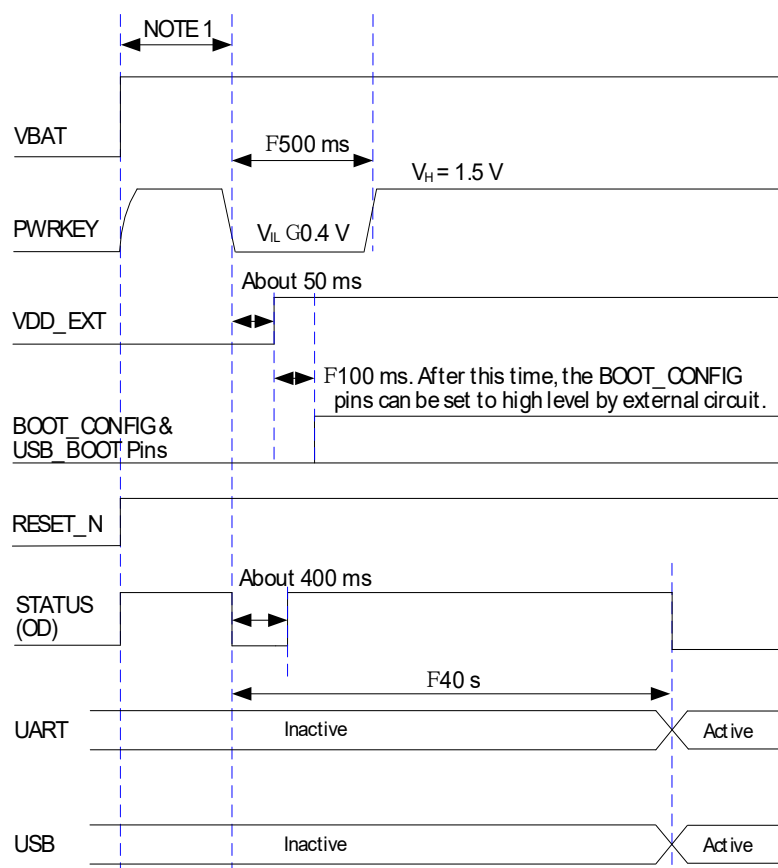
The other way to control PWRKEY is using a button directly. When pressing the button, electrostatic strike may generate from fingers. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

*Figure 10: Reference Circuit of Turning on the Module with a Button*



The turn-on timing is illustrated in the following figure.

Figure 11: Turning-on Timing



## NOTE

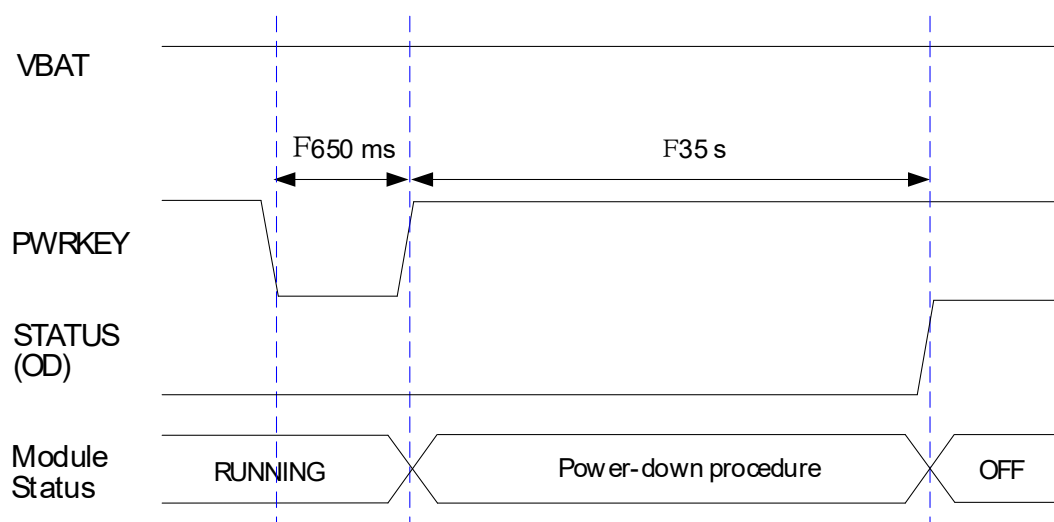
1. Ensure the voltage of VBAT is stable for at least 30 ms before driving PWRKEY low.
2. If the module needs to turn on automatically but does not need turn-off function, PWRKEY can be driven low directly to ground with a recommended 10 k $\Omega$  resistor.

## 3.6. Turn off

### 3.6.1. Turn off with PWRKEY

Driving the PWRKEY pin to low level for at least 650 ms, the module will execute turn-off procedure after PWRKEY is released. The turn-off timing is illustrated in the following figure.

Figure 12: Turning-off Timing



### 3.6.2. Turn off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to turn off the module via PWRKEY.

See **document 4** for details about **AT+QPOWD**.

## NOTE

1. To avoid corrupting the data in the internal flash, do not cut off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.
2. When turning off the module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on automatically again after successful turn-off.

## 3.7. RESET\_N

The module can be reset by driving RESET\_N low for at least 150–460 ms and then releasing it. RESET\_N signal is sensitive to interference, consequently it is recommended to route the trace as short as possible and surround it with ground.

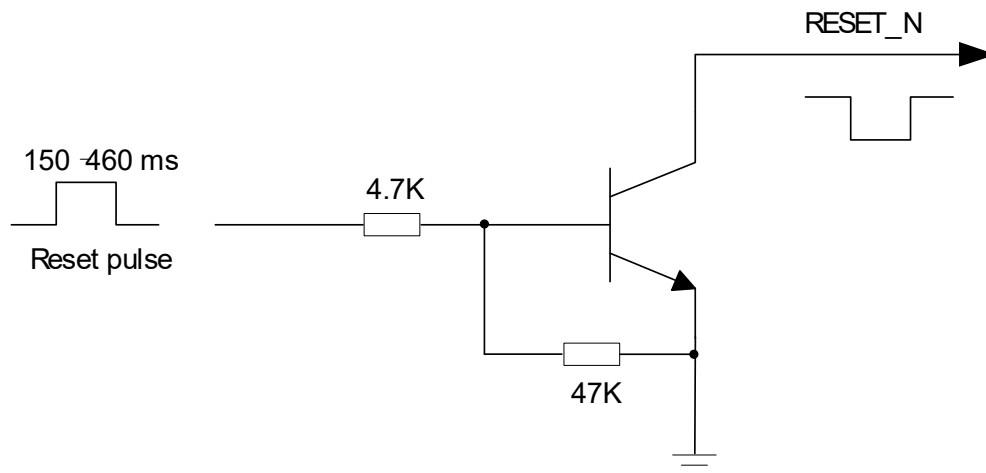
Table 10: Pin Definition of RESET\_N

| Pin Name | Pin No. | I/O | Description      | Comment                                                                                                       |
|----------|---------|-----|------------------|---------------------------------------------------------------------------------------------------------------|
| RESET_N  | 24      | DI  | Reset the module | Pulled up internally to 1.5 V power domain. Active low. A test point is recommended to be reserved if unused. |

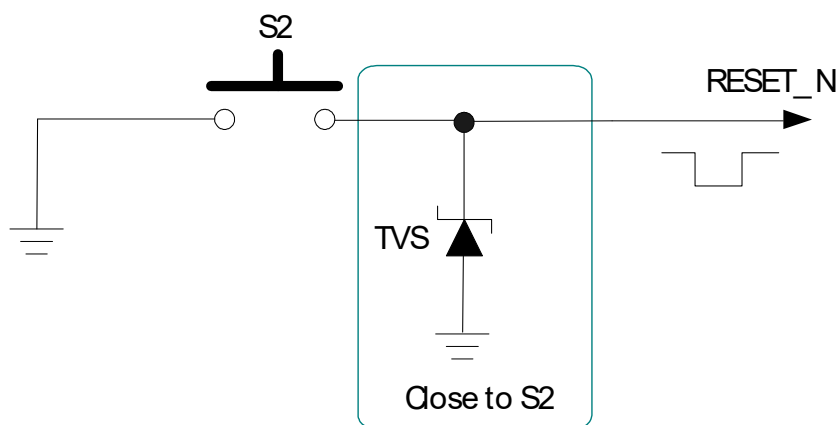
The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or a

button can be used to control RESET\_N.

*Figure 13: Reference Circuit of RESET\_N by Using Driving Circuit*

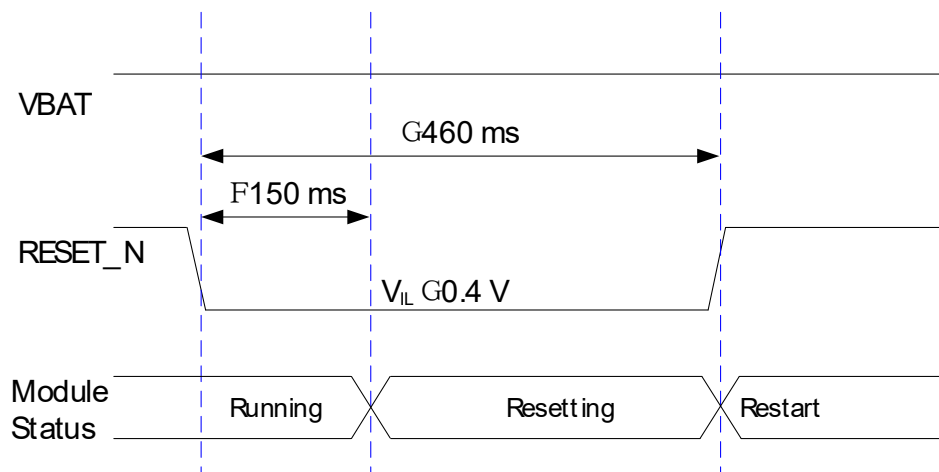


*Figure 14: Reference Circuit of RESET\_N by Using Button*



The reset timing is illustrated in the following figure.

*Figure 15: Reset Timing*



## NOTE

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Ensure there is no large capacitance on PWRKEY and RESET\_N.

---

## 4 Application Interfaces

### 4.1. (U)SIM Interfaces

(U)SIM interfaces circuitry meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported, and Dual SIM Single Standby function is supported.

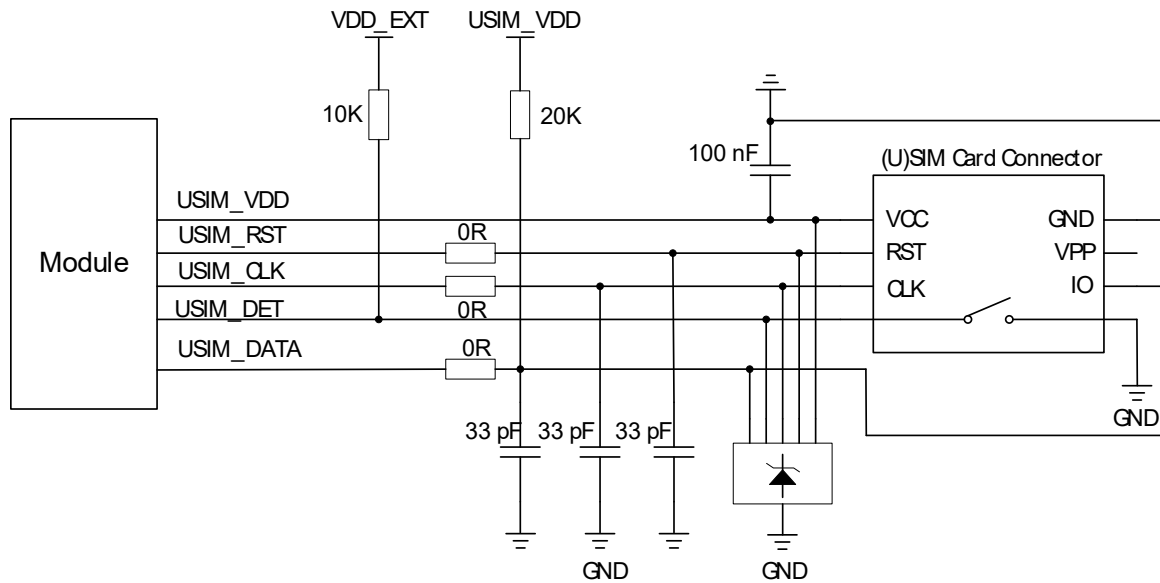
*Table 11: Pin Definition of (U)SIM Interfaces*

| Pin Name   | Pin No. | I/O | Description                  | Comment                                                         |
|------------|---------|-----|------------------------------|-----------------------------------------------------------------|
| USIM1_VDD  | 16      | PO  | (U)SIM1 card power supply    | Either 1.8 V or 3.0 V is supported by the module automatically. |
| USIM1_DATA | 17      | DIO | (U)SIM1 card data            | Pulled up internally with a 20 kΩ resistor.                     |
| USIM1_CLK  | 18      | DO  | (U)SIM1 card clock           |                                                                 |
| USIM1_RST  | 19      | DO  | (U)SIM1 card reset           |                                                                 |
| USIM1_DET  | 15      | DI  | (U)SIM1 card hot-plug detect | If unused, keep it open.                                        |
| USIM2_VDD  | 98      | PO  | (U)SIM2 card power supply    | Either 1.8 V or 3.0 V is supported by the module automatically. |
| USIM2_DATA | 95      | DIO | (U)SIM2 card data            | Pulled up internally with a 20 kΩ resistor.                     |
| USIM2_CLK  | 97      | DO  | (U)SIM2 card clock           |                                                                 |
| USIM2_RST  | 99      | DO  | (U)SIM2 card reset           |                                                                 |
| USIM2_DET  | 96      | DI  | (U)SIM2 card hot-plug detect | If unused, keep it open.                                        |

The module supports (U)SIM card hot-plug via the USIM\_DET pins. The function supports low level and high level detections. It is disabled by default and you can configure it via **AT+QSIMDET** to configure this function. See **document 4** for more details.

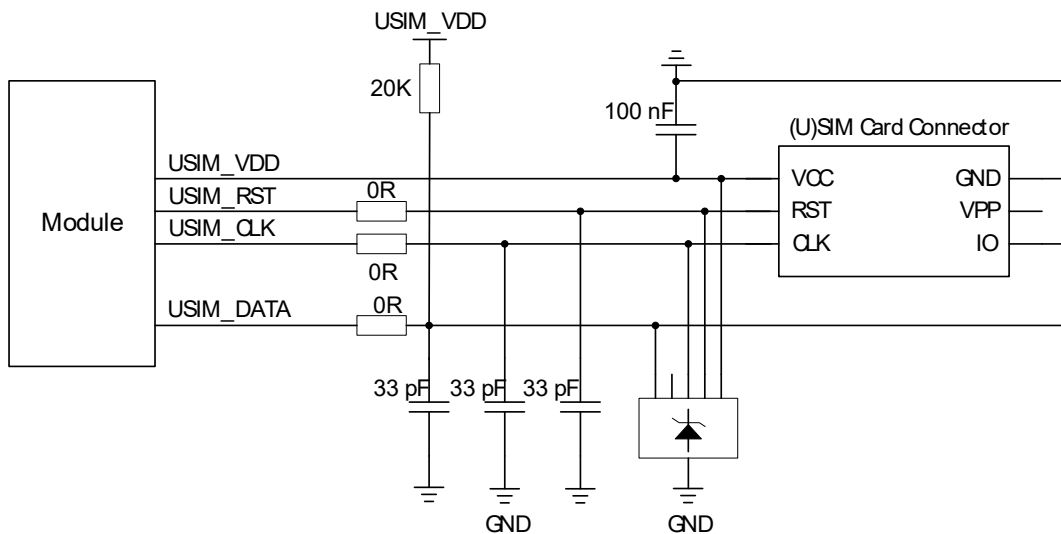
The following figure shows a reference design for (U)SIM card interface with an 8-pin (U)SIM card connector.

**Figure 16: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector**



If (U)SIM card detection function is not needed, keep USIM\_DET unconnected. A reference circuit of (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

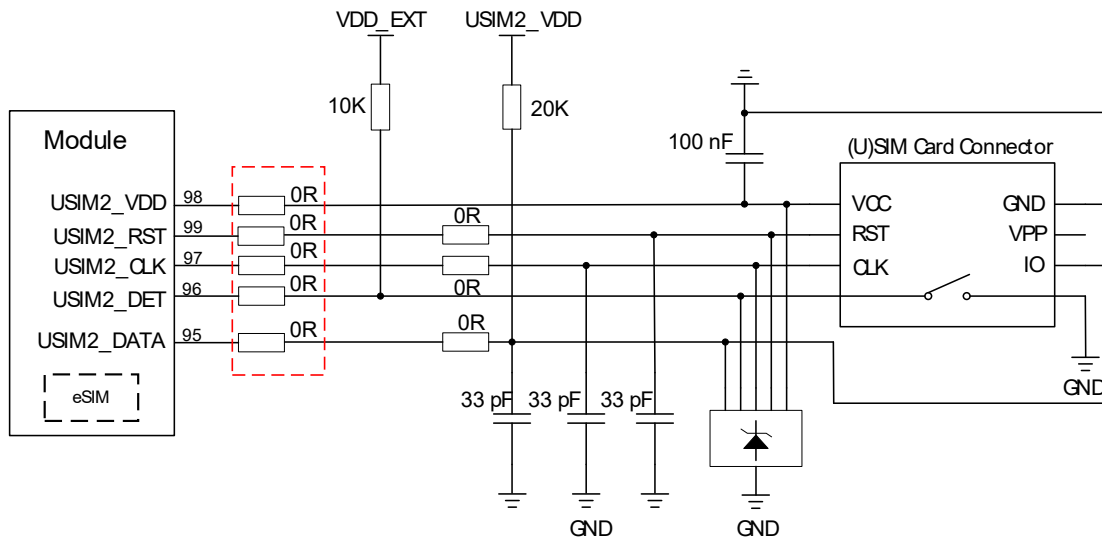
**Figure 17: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector**



It should be noted that when the (U)SIM2 interface is used for an external (U)SIM card, the circuits are the same as those of (U)SIM1 interface. When the (U)SIM2 interface is used for the optional internal eSIM card, pins 95, 96, 97, 98 and 99 of the module must be kept open.

A recommended compatible design for the (U)SIM2 interface is shown below.

**Figure 18: Recommended Compatible Design for (U)SIM2 Interface**



**NOTE:**  
The five 0 Ω resistors must be placed close to the module, and all other components should be placed close to (U)SIM card connector in PCB layout.

To enhance the reliability and availability of the (U)SIM card in applications, follow the principles below in the (U)SIM circuit design:

- Place the (U)SIM card connector close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and power supply traces.
- To avoid cross-talk between USIM\_DATA and USIM\_CLK, keep them away from each other and shield them with ground surrounded.
- To offer better ESD protection, you can add a TVS array of which the parasitic capacitance should be not more than 15 pF. Add 0 Ω resistors in series between the module and the (U)SIM card connector to facilitate debugging. Additionally, add 33 pF capacitors in parallel among USIM\_DATA, USIM\_CLK and USIM\_RST signal traces to filter out RF interference.
- For USIM\_DATA, it is recommended to add a 20 kΩ pull-up resistor near the (U)SIM card connector to improve the anti-jamming capability of the (U)SIM card.

## 4.2. USB\_BOOT

The module provides a USB\_BOOT pin. You can pull up USB\_BOOT to VDD\_EXT before turning on the module, and the module will enter forced download mode when it is turned on. In this mode, the module supports firmware upgrade over USB 2.0 interface.

**Table 12: Pin Definition of USB\_BOOT**

| Pin Name | Pin No. | I/O | Description                             | Comment                                                                               |
|----------|---------|-----|-----------------------------------------|---------------------------------------------------------------------------------------|
| USB_BOOT | 22      | DI  | Force the module to enter download mode | It cannot be pulled up before startup.<br>A test point is recommended to be reserved. |

The following figures show the reference circuit of USB\_BOOT and timing of entering forced download mode.

Figure 19: Reference Circuit of USB\_BOOT

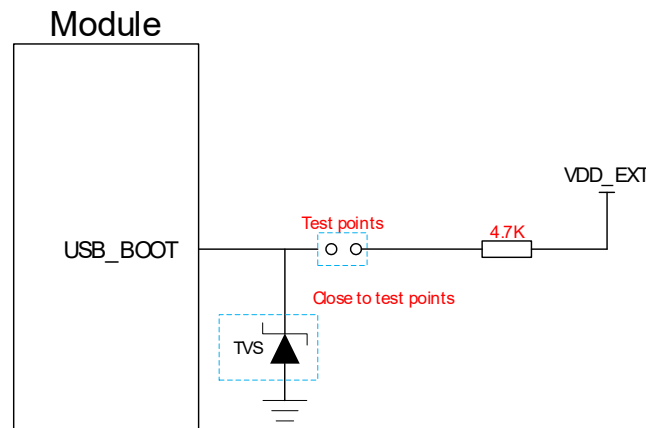
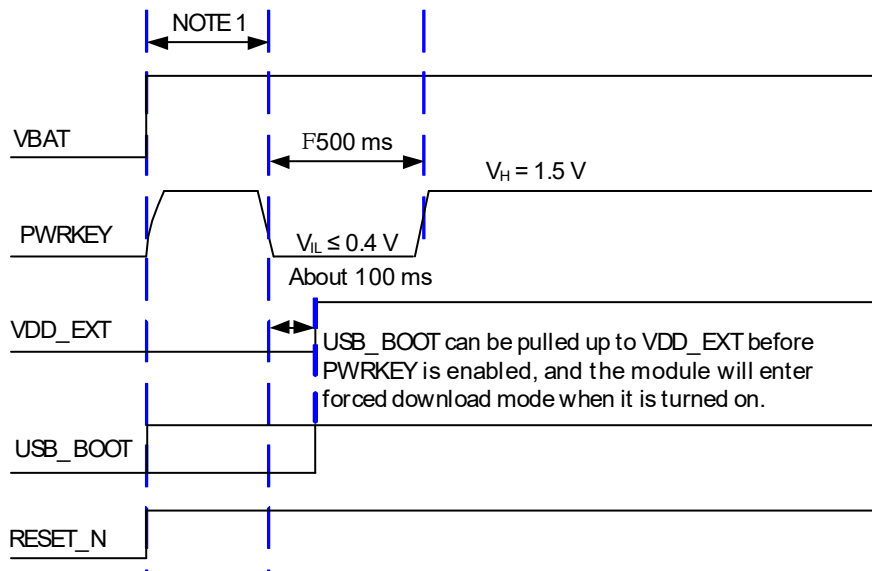


Figure 20: Timing for Entering Forced Download Mode



## NOTE

1. Ensure VBAT is stable before driving PWRKEY low. The time period between powering VBAT up and driving PWRKEY low shall be at least 30 ms.
2. When using MCU to control the module to enter forced download mode, follow the above timing. It is not recommended to pull up USB\_BOOT to VDD\_EXT before powering up VBAT.

## 4.3. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480 Mbps) and full-speed (12 Mbps) modes. The USB interface can only serve as a slave device and is used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging and firmware upgrade. The following table shows the pin definition of USB interface.

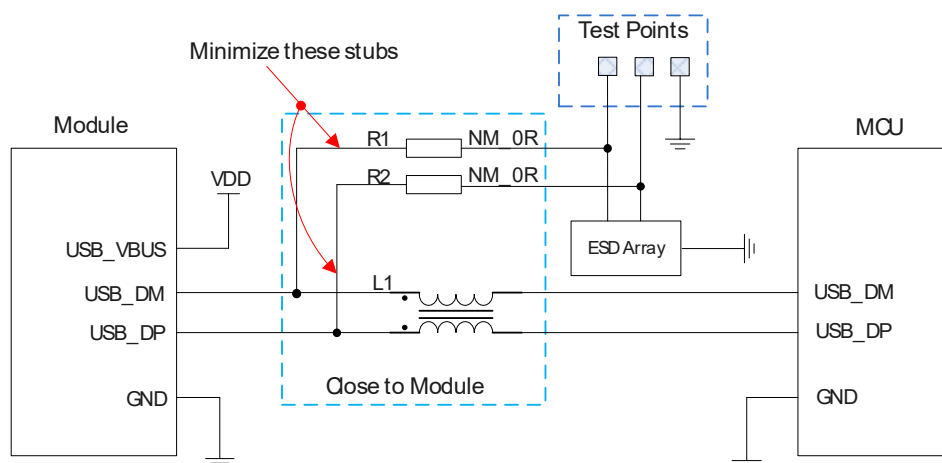
**Table 13: Pin Definition of USB Interface**

| Pin Name | Pin No. | I/O | Description                   | Comment                                                                       |
|----------|---------|-----|-------------------------------|-------------------------------------------------------------------------------|
| USB_DP   | 75      | AIO | USB 2.0 differential data (+) | Require differential impedance of 90 $\Omega$ . Test points must be reserved. |
| USB_DM   | 76      | AIO | USB 2.0 differential data (-) |                                                                               |
| USB_VBUS | 77      | PI  | USB connection detection      | Typical 5.0 V. A test point must be reserved.                                 |

For more details about the USB 2.0 specifications, visit <http://www.usb.org/home>.

USB 2.0 interface can be used for firmware upgrade, and test points must be reserved for debugging in your designs.

**Figure 21: Reference Circuit of USB Interface**



A common mode choke L1 is recommended to be added in series between the module and the MCU in order to suppress EMI. Meanwhile, 0  $\Omega$  resistors (R1 and R2) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data trace signal, L1/R1/R2 components must be placed close to the module, and also the resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

To ensure performance, follow the below principles when designing USB interface:

- Route USB signal traces as differential pairs with ground surrounded. The impedance of USB 2.0 differential trace is 90  $\Omega$ .
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Pay attention to the impact caused by stray capacitance of the ESD protection component on USB data traces. Typically, the stray capacitance should be less than 2 pF for USB 2.0.
- Keep the ESD protection components to the USB connector as close as possible.

## 4.4. UARTs

The module provides two UARTs.

**Table 14: UART Information**

| UART Type  | Supported Baud Rate                                                                                                                                                        | Default Baud Rate | Function                                       |
|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|------------------------------------------------|
| Main UART  | 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, 921600 bps, 2000000 bps, 2900000 bps, 3000000 bps, 3200000 bps, 3686400 bps and 4000000 bps | 115200 bps        | Data transmission and AT command communication |
| Debug UART | 115200 bps                                                                                                                                                                 | 115200 bps        | Linux console and log output                   |

The following table shows the pin definition of UARTs.

**Table 15: Pin Definition of UARTs**

| Pin Name | Pin No. | I/O | Description                          | Comment                                                  |
|----------|---------|-----|--------------------------------------|----------------------------------------------------------|
| MAIN_RI  | 68      | DO  | Main UART ring indication            | If unused, keep them open.                               |
| MAIN_DCD | 69      | DO  | Main UART data carrier detect        |                                                          |
| MAIN_CTS | 70      | DO  | Clear to send signal from the module | Connect to the MCU's CTS. If unused, keep it open.       |
| MAIN_RTS | 71      | DI  | Request to send signal to the module | Connect to the MCU's RTS. If unused, keep it open.       |
| MAIN_DTR | 72      | DI  | Main UART data terminal ready        |                                                          |
| MAIN_TXD | 73      | DO  | Main UART transmit                   | If unused, keep them open.                               |
| MAIN_RXD | 74      | DI  | Main UART receive                    |                                                          |
| DBG_TXD  | 14      | DO  | Debug UART transmit                  | Test points must be reserved. If unused, keep them open. |
| DBG_RXD  | 13      | DI  | Debug UART receive                   |                                                          |

The module provides 1.8 V UARTs. A voltage-level translator should be used if your application is equipped with a 3.3 V UART. The following figure shows a reference design.

**Figure 22: Reference Circuit with a Voltage-level Translator (Main UART)**

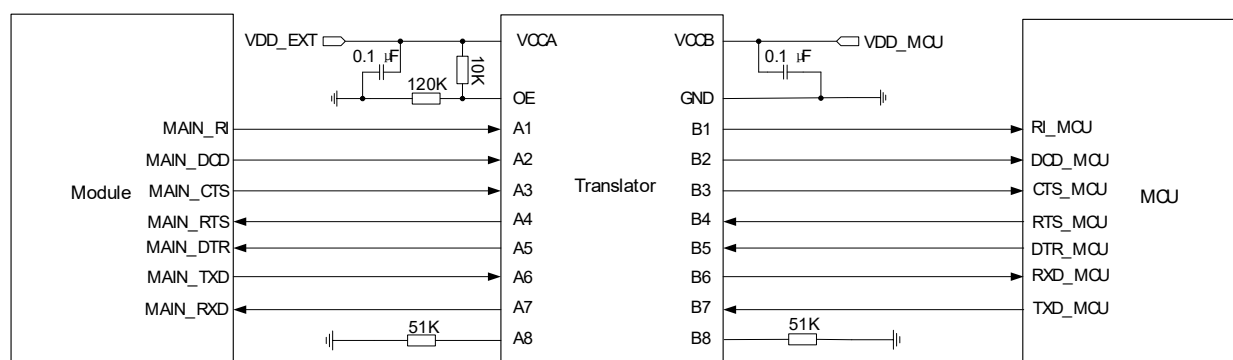
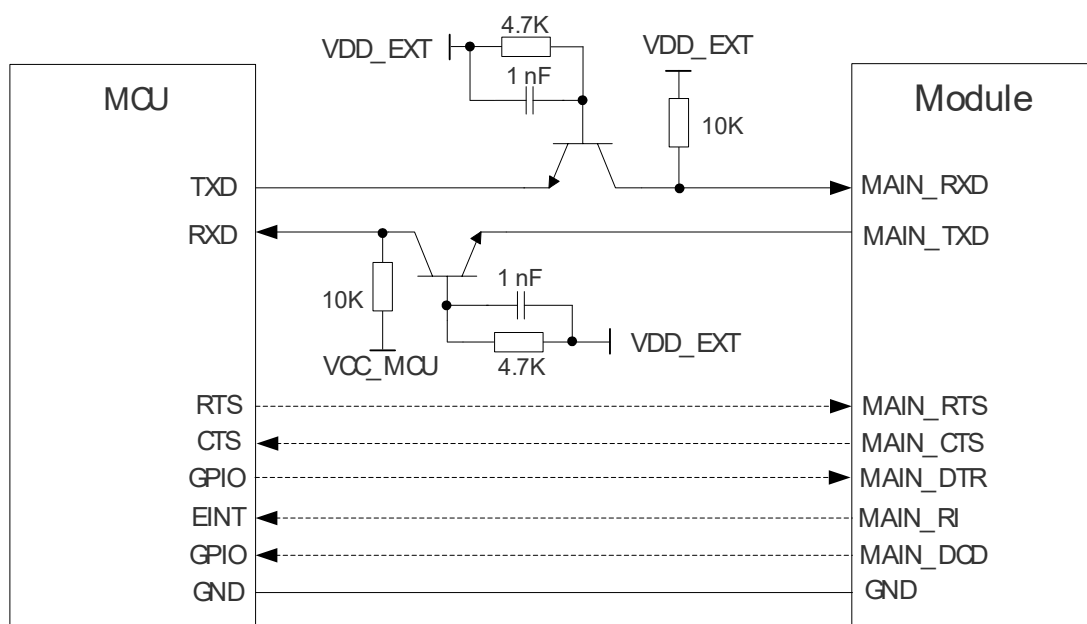


Figure 23: Reference Circuit with Transistor Circuit (Main UART)



## NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.
3. The level-shifting circuits (**Figure 22** and **Figure 23**) take the main UART as an example. The circuits of the debug UART is connected in the same way as the main UART.

## 4.5. PCM<sup>dev</sup> and I2C Interfaces

The module provides one Pulse Code Modulation (PCM) digital interface for audio design, and one I2C interface.

Table 16: Pin Definition of PCM and I2C Interfaces

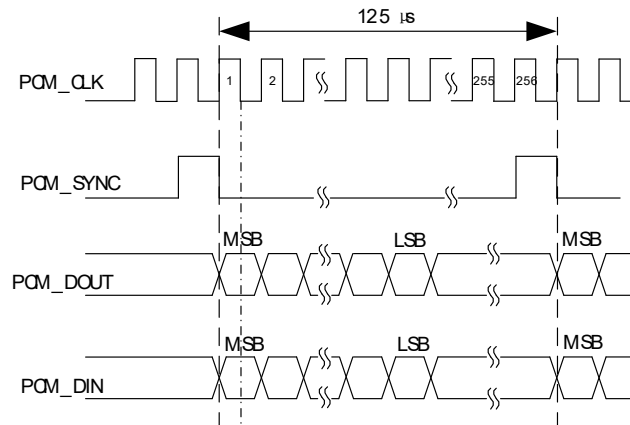
| Pin Name | Pin No. | I/O | Description         | Comment                                                                           |
|----------|---------|-----|---------------------|-----------------------------------------------------------------------------------|
| PCM_DIN  | 28      | DI  | PCM data input      | If unused, keep them open.                                                        |
| PCM_DOUT | 29      | DO  | PCM data output     |                                                                                   |
| PCM_SYNC | 30      | DIO | PCM data frame sync |                                                                                   |
| PCM_CLK  | 31      | DIO | PCM clock           |                                                                                   |
| I2C_SCL  | 45      | OD  | I2C serial clock    | Pull each of them up to VDD_EXT with 4.7 kΩ resistors. If unused, keep them open. |
| I2C_SDA  | 46      | OD  | I2C serial data     |                                                                                   |

The PCM interface supports the following modes.

- Short frame mode: the module works as both the master and slave devices.
- Long frame mode: the module works as the master mode only.

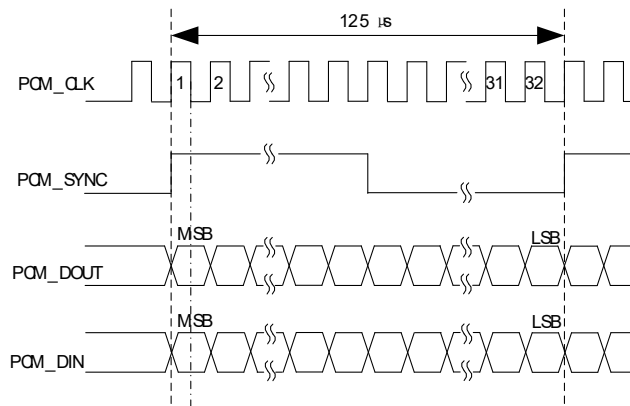
The module supports 16-bit linear encoding format. The following figures are the short frame mode timing diagram (PCM\_SYNC = 8 kHz, PCM\_CLK = 2048 kHz) and the long frame mode timing diagram (PCM\_SYNC = 8 kHz, PCM\_CLK = 256 kHz).

**Figure 24: Timing of Short Frame Mode**



In short frame mode, data is sampled on the falling edge of PCM\_CLK and transmitted on the rising edge. The PCM\_SYNC falling edge represents the MSB. In this mode, PCM\_CLK supports 256 kHz, 512 kHz, 1024 kHz and 2048 kHz when PCM\_SYNC operates at 8 kHz, and also supports 4096 kHz when PCM\_SYNC operates at 16 kHz.

**Figure 25: Timing of Long Frame Mode**

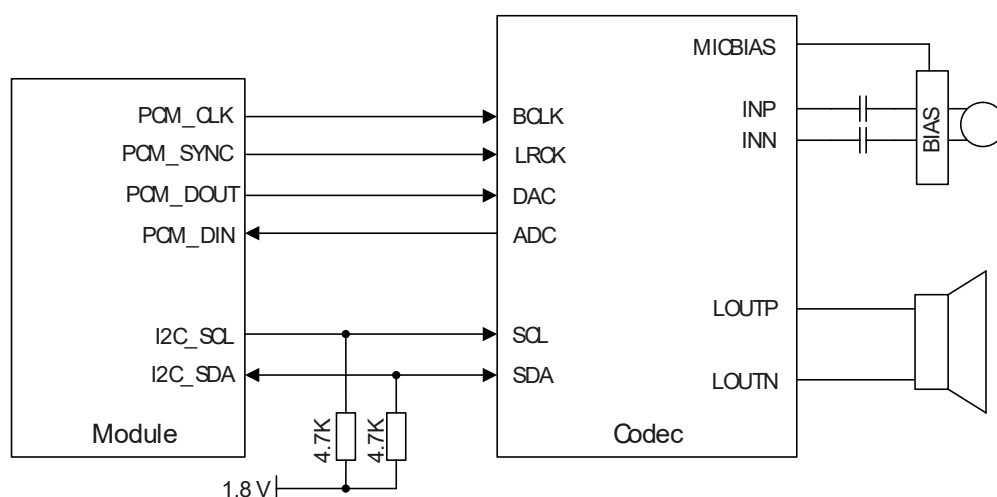


In long frame mode, the data is sampled on the falling edge of the PCM\_CLK and transmitted on the rising edge. The PCM\_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with a 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM\_CLK and an 8 kHz, 50 % duty cycle PCM\_SYNC.

The clock and mode of PCM can be configured by **AT+QDAI**, and the default configuration is short frame mode (PCM\_CLK = 2048 kHz, PCM\_SYNC = 8 kHz). See **document 4** for more details.

The following figure shows a reference design of PCM and I2C interfaces with external codec IC.

Figure 26: Reference Circuit of PCM and I2C Application with Audio Codec



## NOTE

1. It is recommended to reserve an RC ( $R = 22\ \Omega$ ,  $C = 22\ \text{pF}$ ) circuits on the PCM traces, especially for PCM\_CLK.
2. The module works as a master device pertaining to I2C interface.

## 4.6. SPI Interface

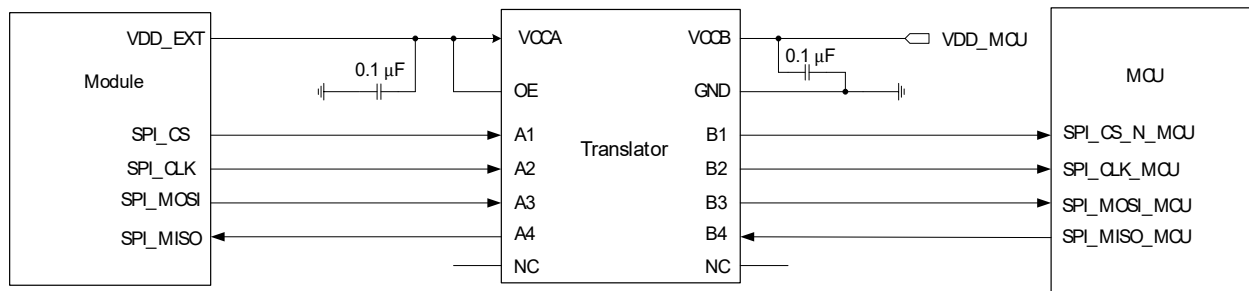
The module provides one SPI interface which only supports master mode with a maximum clock frequency of 50 MHz.

Table 17: Pin Definition of SPI Interface

| Pin Name | Pin No. | I/O | Description             | Comment                        |
|----------|---------|-----|-------------------------|--------------------------------|
| SPI_CLK  | 44      | DO  | SPI clock               | Only master mode is supported. |
| SPI_CS   | 41      | DO  | SPI chip select         |                                |
| SPI_MISO | 43      | DI  | SPI master-in slave-out |                                |
| SPI_MOSI | 42      | DO  | SPI master-out slave-in |                                |

The module provides a 1.8 V SPI interface. Use a voltage-level translator between the module and the peripheral device if the peripheral device is 3.3 V power domain. The following figure shows the reference design.

**Figure 27: Reference Circuit of SPI Interface with a Voltage-level Translator**



## 4.7. Wireless Connectivity Interfaces

The following table shows the pin definition of wireless connectivity interfaces.

**Table 18: Pin Definition of Wireless Connectivity Interfaces**

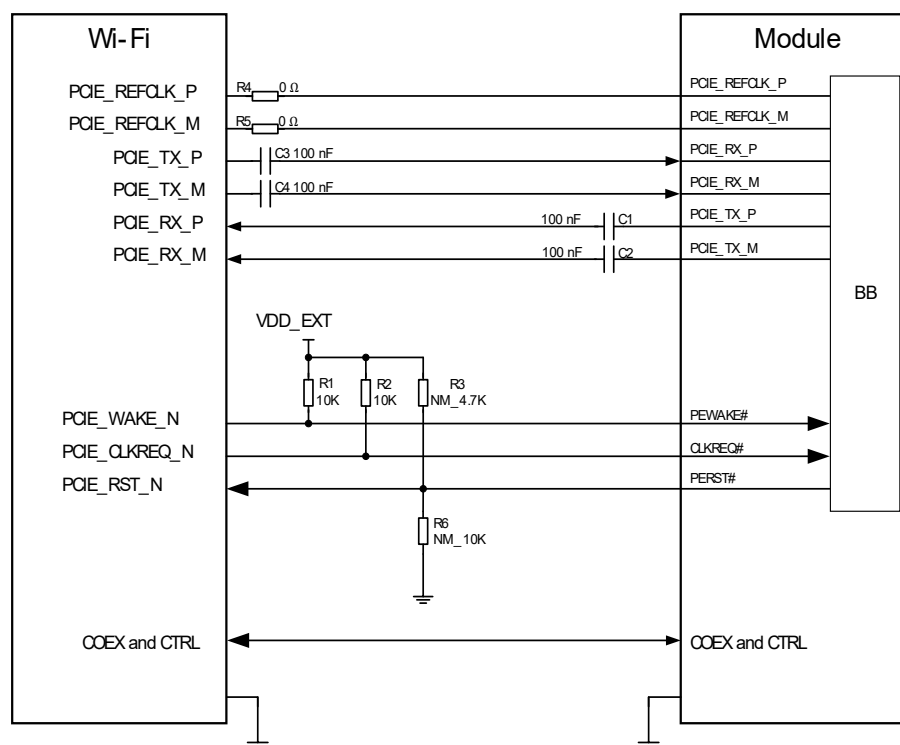
| Pin Name                                 | Pin No. | I/O    | Description                         | Comment                                                            |
|------------------------------------------|---------|--------|-------------------------------------|--------------------------------------------------------------------|
| <b>PCIe Part</b>                         |         |        |                                     |                                                                    |
| PCIe_REFCLK_P                            | 105     | AIO    | PCIe reference clock (+)            | Require differential impedance of 85 Ω. If unused, keep them open. |
| PCIe_REFCLK_M                            | 107     |        | PCIe reference clock (-)            |                                                                    |
| PCIe_TX_P                                | 103     | AO     | PCIe transmit (+)                   |                                                                    |
| PCIe_TX_M                                | 104     |        | PCIe transmit (-)                   |                                                                    |
| PCIe_RX_P                                | 101     | AI     | PCIe receive (+)                    |                                                                    |
| PCIe_RX_M                                | 102     |        | PCIe receive (-)                    |                                                                    |
| PERST#                                   | 20      | DIO    | PCIe reset                          |                                                                    |
| CLKREQ#                                  | 21      | OD/DIO | PCIe clock request                  |                                                                    |
| PEWAKE#                                  | 100     | OD/DIO | PCIe wake up                        |                                                                    |
| <b>WLAN Coexistence and Control Part</b> |         |        |                                     |                                                                    |
| WLAN_SLP_CLK                             | 85      | DO     | WLAN sleep clock                    |                                                                    |
| WLAN_PWR_EN                              | 91      | DO     | WLAN power control                  | Active high.                                                       |
| WLAN_WAKE                                | 87      | DI     | Wake up module by an external Wi-Fi |                                                                    |

|                   |    |    |                                                       |              |
|-------------------|----|----|-------------------------------------------------------|--------------|
| WLAN_EN           | 89 | DO | WLAN function enable control                          | Active high. |
| COEX_RXD          | 90 | DI | 5G/LTE and WLAN coexistence receive                   |              |
| COEX_TXD          | 88 | DO | 5G/LTE and WLAN coexistence transmit                  |              |
| WLAN_SW_CTRL      | 86 | DI | Wi-Fi power control                                   |              |
| N79_TX_EN_TO_WLAN | 92 | DO | Notify n79 transmission from SDR transceiver to WLAN  |              |
| WLAN_PA_MUTING    | 94 | DO | GPIO from SDX to disable WLAN PA                      |              |
| WLAN_TX_EN_TO_N79 | 93 | DI | Notify WLAN transmission from WLAN to SDR transceiver |              |

### WLAN Coexistence and Control Part

|       |     |    |                          |              |
|-------|-----|----|--------------------------|--------------|
| BT_EN | 132 | DO | Bluetooth enable control | Active high. |
|-------|-----|----|--------------------------|--------------|

Figure 28: Reference Circuit of PCIe



## 4.8. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces.

**Table 19: Pin Definition of ADC Interfaces**

| Pin Name | Pin No. | I/O | Description                   | Comment                    |
|----------|---------|-----|-------------------------------|----------------------------|
| ADC0     | 49      | AI  | General-purpose ADC interface | If unused, keep them open. |
| ADC1     | 48      | AI  |                               |                            |

With **AT+QADC=<port>**, you can:

- **AT+QADC=0**: read the voltage value on ADC0.
- **AT+QADC=1**: read the voltage value on ADC1.

For more details about these AT commands, see **document 4**.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded by ground. The resolution of ADC is 15 bits.

The following table describes the characteristic of ADC function.

**Table 20: Characteristics of ADC Interfaces**

| Parameter                | Min. | Max.    | Unit |
|--------------------------|------|---------|------|
| ADC0 Input Voltage Range | 0    | VBAT_BB | V    |
| ADC1 Input Voltage Range | 0    | VBAT_BB | V    |

## NOTE

1. The input voltage of every ADC interface should not exceed its corresponding voltage range.
2. It is prohibited to directly supply any voltage to ADC interface when the module is not powered by the VBAT.
3. It is recommended to use a resistor divider circuit for ADC application.

## 4.9. SGMII Interface

The module provides an integrated Ethernet MAC with an SGMII and CTL interface. The key features of the SGMII interface are shown below:

- IEEE 802.3 compliant.
- Support 10 Mbps/100 Mbps/1000 Mbps Ethernet work mode.
- Support VLAN tagging.
- Support IEEE 1588 and Precision Time Protocol (PTP).

The following table shows the pin definition of SGMII interface.

**Table 21: Pin Definition of SGMII Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|----------|---------|-----|-------------|---------|
|----------|---------|-----|-------------|---------|

### Control Signal Part

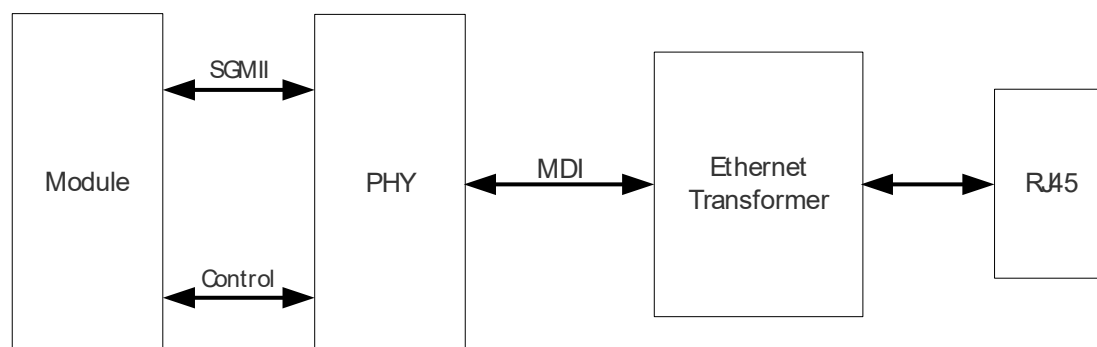
|             |     |     |                                    |                                                                                   |
|-------------|-----|-----|------------------------------------|-----------------------------------------------------------------------------------|
| SGMII_RST_N | 37  | DO  | SGMII reset external PHY           | If unused, keep them open.                                                        |
| SGMII_INT_N | 123 | DI  | SGMII interrupt                    |                                                                                   |
| SGMII_MDIO  | 36  | DIO | SGMII management data input/output | Pull it up to VDD EXT with a 1.5 k $\Omega$ resistor.<br>If unused, keep it open. |
| SGMII_MDC   | 121 | DO  | SGMII management data clock        | If unused, keep it open.                                                          |

### SGMII Signal Part

|            |     |    |                    |                                                                                          |
|------------|-----|----|--------------------|------------------------------------------------------------------------------------------|
| SGMII_TX_M | 34  | AO | SGMII transmit (-) | Connect with a 0.1 $\mu$ F capacitor.<br>Require differential impedance of 90 $\Omega$ . |
| SGMII_TX_P | 119 | AO | SGMII transmit (+) |                                                                                          |
| SGMII_RX_M | 32  | AI | SGMII receive (-)  | Require differential impedance of 90 $\Omega$ .                                          |
| SGMII_RX_P | 117 | AI | SGMII receive (+)  |                                                                                          |

The following figure shows the simplified block diagram for Ethernet application.

*Figure 29: Simplified Block Diagram for Ethernet Application*



To ensure the performance and reliability, follow the design notes below in the SGMII circuit design:

- Keep data traces and control signal traces of SGMII interface far away from power supply traces, crystal-oscillators, magnetic devices, sensitive signals and signals like RF signals, analog signals, and noise signals generated by clock, DC-DC.
- Keep the maximum trace length not more than 10 inch and keep length matching on the differential pairs not more than 20 mil.
- Keep the differential impedance of SGMII data traces within 90  $\Omega \pm 10\%$  and ensure the integrity of the reference ground.
- Make sure the trace spacing between SGMII\_RX and SGMII\_TX is at least 3 times of the trace width, and the same to the adjacent signal traces.

## 4.10. Indication Signals

*Table 22: Pin Definition of Network Status Indication*

| Pin Name   | Pin No. | I/O | Description                                     | Comment                                                            |
|------------|---------|-----|-------------------------------------------------|--------------------------------------------------------------------|
| NET_MODE   | 5       | DO  | Indicate the module's network registration mode | If unused, keep them open.                                         |
| NET_STATUS | 6       | DO  | Indicate the module's network activity status   |                                                                    |
| STATUS     | 67      | OD  | Indicate the module's operation status          | An external pull-up resistor is required. If unused, keep it open. |
| MAIN_RI    | 68      | DO  | Main UART ring indication                       | If unused, keep it open.                                           |

#### 4.10.1. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides two network status indication pins: the NET\_MODE for the module's network registration status indication and the NET\_STATUS for the module's network operation status indication. Both can drive corresponding LEDs.

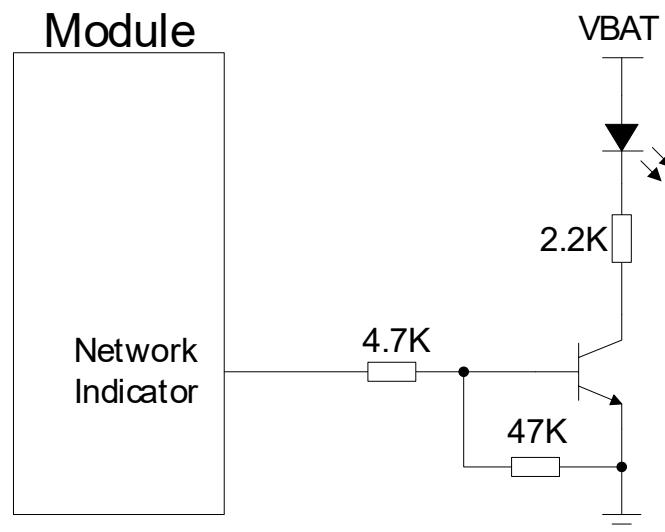
The following table describes the pin definition and logic level changes in different network status.

*Table 23: Network Status Indication Pin Level and Module Network Status*

| Pin Name   | Level Status                           | Module Network Status        |
|------------|----------------------------------------|------------------------------|
| NET_MODE   | Always High                            | Registered on network        |
|            | Always Low                             | Others                       |
| NET_STATUS | Blink slowly (200 ms High/1800 ms Low) | Network searching            |
|            | Blink slowly (1800 ms High/200 ms Low) | Idle                         |
|            | Blink quickly (125 ms High/125 ms Low) | Data transmission is ongoing |
|            | Always High                            | Voice calling                |

A reference circuit is shown in the following figure.

*Figure 30: Reference Circuit of Network Status Indication*

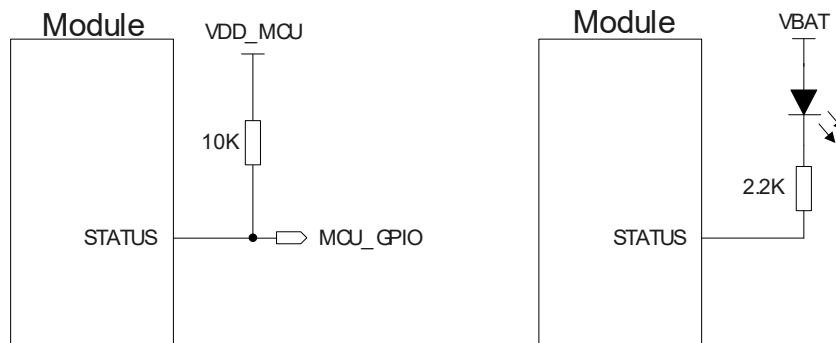


#### 4.10.2. STATUS

The STATUS pin is an open drain output for indicating the module's operation status. It can be connected to a GPIO of MCU with a pull-up resistor, or as LED indication circuit as below. When the module is turned on normally, STATUS will present the low-level state. Otherwise, STATUS will present high-impedance state.

The following figure shows different circuit designs of STATUS, and you can choose either one according to your application demands.

*Figure 31: Reference Circuits of STATUS*



#### NOTE

The status pin cannot be used as indication of module shutdown status when VBAT power supply is removed.

#### 4.10.3. MAIN\_RI

**AT+QCFG="risignaltpe","physical"** can be used to configure MAIN\_RI behavior. No matter on main UART port or USB AT port a URC is presented, the URC will trigger the behaviors of MAIN\_RI.

## NOTE

The **AT+QURCCFG** can set the main UART port or USB AT port as the URC information output port.

The default behavior of MAIN\_RI is shown as below, and can be changed by **AT+QCFG="urc/ri/ring"**.

See **document 4** for details about the above AT commands.

*Table 24: Behaviours of MAIN\_RI*

| Module Status | MAIN_RI Level Status                                     |
|---------------|----------------------------------------------------------|
| Idle          | MAIN_RI keeps at high level.                             |
| URC           | MAIN_RI outputs 120 ms low pulse when a new URC returns. |

## 5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module's antenna interfaces include a main antenna interface, an Rx-diversity antenna interface which is used to resist the fall of signals caused by high-speed movement and multipath effect, and a GNSS antenna interface. The impedance of the antenna interfaces is 50  $\Omega$ .

### 5.1. Cellular Network

#### 5.1.1. Antenna Interface & Frequency Bands

The pin definition of main antenna and Rx-diversity antenna interfaces is shown below.

*Table 25: Pin Definition of Cellular Antenna Interfaces*

| Pin Name | Pin No. | I/O | Description                    | LB (MHz) | MHB (MHz) | UHB (MHz) |
|----------|---------|-----|--------------------------------|----------|-----------|-----------|
| ANT_MAIN | 55      | AIO | <b>Antenna 0 interface:</b>    | 617–960  | 1695–2690 | 3300–5000 |
|          |         |     | - <b>5G NR:</b> LB/MHB/UHB TRX |          |           |           |
| ANT_DRX  | 39      | AIO | - <b>LTE:</b> LB/MHB/UHB TRX   | 617–960  | 1695–2690 | 3300–5000 |
|          |         |     | <b>Antenna 1 interface:</b>    |          |           |           |
| ANT_DRX  | 39      | AIO | - <b>5G NR:</b> LB/MHB/UHB DRX | 617–960  | 1695–2690 | 3300–5000 |
|          |         |     | - <b>LTE:</b> LB/MHB/UHB DRX   |          |           |           |

#### NOTE

The impedance of antenna interface is 50  $\Omega$ .

#### 5.1.2. Antenna Tuner Control Interface

The module can use GRFC (generic RF control) interface to control external antenna tuner.

*Table 26: Pin Description of GRFC Interface*

| Pin Name | Pin No. | I/O | Description           | Comment                    |
|----------|---------|-----|-----------------------|----------------------------|
| GRFC1    | 53      | DO  | Generic RF controller | If unused, keep them open. |
| GRFC2    | 139     | DO  |                       |                            |

#### 5.1.3. Transmit Power

The following table shows the RF transmit power of the module.

*Table 27: RF Transmit Power*

| Mode  | Frequency Band                                   | Max.                                      | Min.      |
|-------|--------------------------------------------------|-------------------------------------------|-----------|
| LTE   | LTE bands                                        | 23 dBm $\pm$ 2 dB (Class 3) <sup>9</sup>  | < -40 dBm |
|       | LTE HPUE bands (B38/B40/B41/B42/B43)             | 26 dBm $\pm$ 2 dB (Class 2)               | < -40 dBm |
| 5G NR | 5G NR bands                                      | 23 dBm $\pm$ 2 dB (Class 3) <sup>10</sup> | < -40 dBm |
|       | 5G NR HPUE bands (n38/n41/n77/n78) <sup>11</sup> | 26 dBm $\pm$ 2 dB (Class 2)               | < -40 dBm |

## NOTE

For 5G NR bands, see the specifications as described in *Clause 6.3.1* of *TS 38.101-1*.

### 5.1.4. Receiving Sensitivity

The following table shows the conducted RF receiving sensitivity of the module.

*Table 28: Conducted RF Receiving Sensitivity (Unit: dBm)*

| Frequency            | Receiving Sensitivity (Typ.) |           |                    | 3GPP Requirements (SIMO) <sup>12</sup> |
|----------------------|------------------------------|-----------|--------------------|----------------------------------------|
|                      | Primary                      | Diversity | SIMO <sup>12</sup> |                                        |
| LTE-FDD B1 (10 MHz)  | -97.3                        | -97.8     | -100.5             | -96.3                                  |
| LTE-FDD B2 (10 MHz)  | -97.2                        | -97.8     | -100.7             | -94.3                                  |
| LTE-FDD B3 (10 MHz)  | -97.2                        | -97.8     | -100.7             | -93.3                                  |
| LTE-FDD B4 (10 MHz)  | -97.4                        | -97.5     | -100.6             | -96.3                                  |
| LTE-FDD B5 (10 MHz)  | -98.3                        | -99.3     | -101.8             | -94.3                                  |
| LTE-FDD B7 (10 MHz)  | -96                          | -97       | -99.2              | -94.3                                  |
| LTE-FDD B8 (10 MHz)  | -97                          | -98.8     | -101.2             | -93.3                                  |
| LTE-FDD B12 (10 MHz) | -98.3                        | -99       | -101.8             | -93.3                                  |

<sup>9</sup> The transmit power of B30 is Class 3 (22 dBm  $\pm$ 2 dB).

<sup>10</sup> The transmit power of n30 is Class 3 (22 dBm  $\pm$ 2 dB).

<sup>11</sup> HPUE is only for 5G single carrier with bandwidth not more than 20 MHz.

<sup>12</sup> SIMO is a smart antenna technology that uses a single antenna at the transmitter side and two antennas at the receiver side, which can improve RX performance.

|                        |       |       |        |       |
|------------------------|-------|-------|--------|-------|
| LTE-FDD B13 (10 MHz)   | -97.1 | -99.4 | -101.5 | -93.3 |
| LTE-FDD B14 (10 MHz)   | -98   | -99   | -101.5 | -93.3 |
| LTE-FDD B17 (10 MHz)   | -98.4 | -99.2 | -102   | -93.3 |
| LTE-FDD B18 (10 MHz)   | -98   | -99.3 | -101.8 | -96.3 |
| LTE-FDD B19 (10 MHz)   | -98.1 | -99.3 | -101.8 | -96.3 |
| LTE-FDD B20 (10 MHz)   | -98.2 | -98.7 | -101.7 | -93.3 |
| LTE-FDD B25 (10 MHz)   | -97.2 | -97.8 | -100.6 | -92.8 |
| LTE-FDD B26 (10 MHz)   | -97.8 | -99.3 | -101.8 | -93.8 |
| LTE-FDD B28 (10 MHz)   | -97.8 | -99   | -101.4 | -94.8 |
| LTE-FDD B30 (10 MHz)   | -96.2 | -97.1 | -99.8  | -95.3 |
| LTE-TDD B34 (10 MHz)   | -97.5 | -99   | -101.4 | -96.3 |
| LTE-TDD B38 (10 MHz)   | -95.1 | -96.3 | -99.2  | -96.3 |
| LTE-TDD B39 (10 MHz)   | -97.3 | -99.2 | -101.7 | -96.3 |
| LTE-TDD B40 (10 MHz)   | -96.1 | -96.6 | -99.8  | -96.3 |
| LTE-TDD B41 (10 MHz)   | -95.1 | -96.1 | -99.2  | -94.3 |
| LTE-TDD B42 (10 MHz)   | -98   | -98   | -101.1 | -95   |
| LTE-TDD B43 (10 MHz)   | -98   | -97.6 | -101   | -95   |
| LTE-TDD B48 (10 MHz)   | -98   | -97.5 | -101   | -95   |
| LTE-FDD B66 (10 MHz)   | -97.2 | -97.6 | -100.7 | -95.8 |
| LTE-FDD B70 (10 MHz)   | -97.5 | -98   | -100.4 | -93.5 |
| LTE-FDD B71 (10 MHz)   | -99   | -98.3 | -101   | -93.5 |
| 5G NR FDD n1 (20 MHz)  | -94   | -94.2 | -97.2  | -93.1 |
| 5G NR FDD n2 (20 MHz)  | -93.5 | -93   | -96.3  | -91.1 |
| 5G NR FDD n3 (20 MHz)  | -93   | -94   | -96.5  | -90.1 |
| 5G NR FDD n5 (20 MHz)  | -94.5 | -95.1 | -98    | -90.1 |
| 5G NR FDD n7 (20 MHz)  | -92.5 | -93.5 | -94.7  | -91.1 |
| 5G NR FDD n8 (20 MHz)  | -93   | -93   | -96    | -89.3 |
| 5G NR FDD n12 (15 MHz) | -95.4 | -95   | -99    | -83.3 |

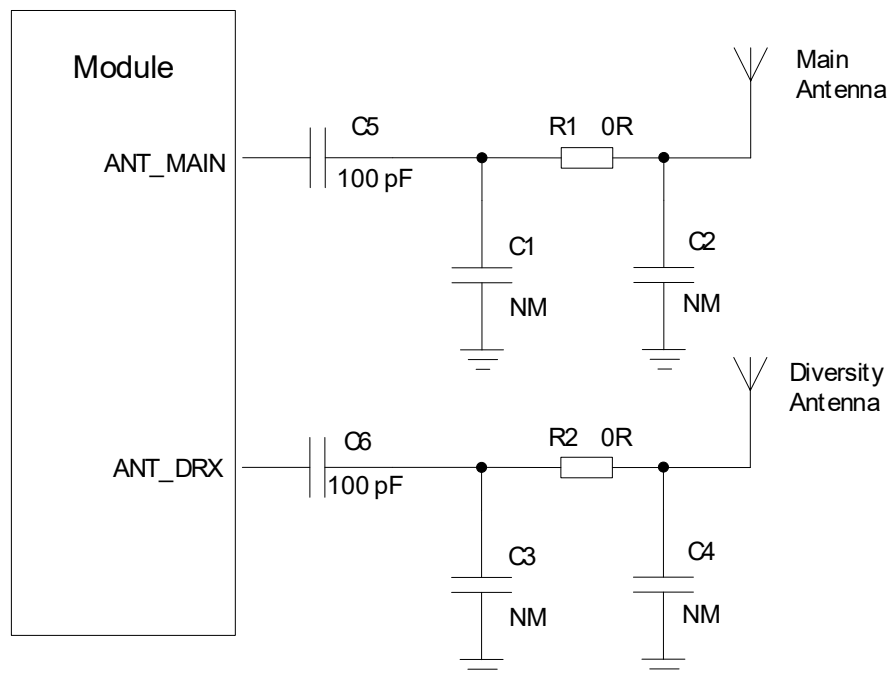
|                        |       |       |        |                     |
|------------------------|-------|-------|--------|---------------------|
| 5G NR FDD n13 (10 MHz) | -96   | -98   | -99.7  | -93.1 <sup>13</sup> |
| 5G NR FDD n14 (10 MHz) | -97.5 | -98.4 | -101.2 | -93.1               |
| 5G NR FDD n18 (10 MHz) | -95   | -96.5 | -100.5 | -96.1 <sup>13</sup> |
| 5G NR FDD n20 (20 MHz) | -95   | -93.7 | -97.7  | -89.1               |
| 5G NR FDD n25 (20 MHz) | -93.5 | -93   | -96.3  | -89.6               |
| 5G NR FDD n26 (20 MHz) | -94   | -95.2 | -97.7  | -86.9               |
| 5G NR FDD n28 (20 MHz) | -94   | -95   | -97.3  | -90.1               |
| 5G NR FDD n30 (10 MHz) | -95.3 | -96.5 | -99    | -95.1               |
| 5G NR TDD n38 (20 MHz) | -93   | -93.5 | -96.5  | -93.1               |
| 5G NR TDD n40 (20 MHz) | -94   | -93.5 | -96.9  | -93.1               |
| 5G NR TDD n41 (20 MHz) | -93.3 | -93   | -96.2  | -91.1               |
| 5G NR TDD n48 (20 MHz) | -96   | -95   | -98    | -91.8               |
| 5G NR FDD n66 (20 MHz) | -96.2 | -94   | -97    | -92.6               |
| 5G NR FDD n70 (15 MHz) | -94.4 | -95.3 | -98    | -94.3               |
| 5G NR FDD n71 (20 MHz) | -95   | -94.2 | -97.2  | -85.3               |
| 5G NR TDD n77 (20 MHz) | -95.2 | -94   | -97.2  | -91.8               |
| 5G NR TDD n78 (20 MHz) | -95.4 | -95   | -97.5  | -91.8               |
| 5G NR TDD n79 (20 MHz) | -94.3 | -94   | -96.2  | -91.9               |

### 5.1.5. Reference Design

A reference design of cellular antenna interfaces is shown as below. A dual L-type circuit should be reserved for better RF performance. The capacitors C1–C4 are not mounted by default.

<sup>13</sup> The 3GPP Rel-17 Redcap protocol has not yet defined the sensitivity thresholds for n13 and n18, this data is for reference only.

Figure 32: Reference Circuit of Cellular Antenna Interfaces



## NOTE

1. To improve RF performance, maintain at least 15 dB isolation between the main antenna and the diversity receiving antenna. It is recommended that the isolation between antenna traces on the PCB be greater than 75 dB.
2. Place the dual L-type components (R1, C1, C2, C5 and R2, C3, C4, C6) as close to the antenna as possible.
3. It is recommended that the straight-line distance between the antenna and the module be greater than 15 mm to achieve better wireless performance of the whole device.
4. Notes on C5 and C6:
  - 1) If there is DC power at the antenna ports, place capacitors on C5 and C6 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
  - 2) If there is no DC power in the peripheral design:
    - a) Do not reserve C5 and C6.
    - b) If C5 and C6 have already been reserved, they should be mounted with components, and it is recommended to use 0  $\Omega$  resistors. You can also match the components according to the debugging results.

## 5.2. GNSS (Optional)

The module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, Galileo, NavIC<sup>dev</sup> and QZSS.

The module supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

By default, the module's GNSS engine is switched off. It has to be switched on via AT command.

### 5.2.1. Antenna Interface & Frequency Bands

Table 29: Pin Definition of GNSS Antenna Interface

| Pin Name | Pin No. | I/O | Description            | Comment                                            |
|----------|---------|-----|------------------------|----------------------------------------------------|
| ANT_GNSS | 51      | AI  | GNSS antenna interface | 50 $\Omega$ impedance.<br>If unused, keep it open. |

Table 30: GNSS Frequency (Unit: MHz)

| GNSS Constellation Type | Frequency                                               |
|-------------------------|---------------------------------------------------------|
| GPS                     | 1575.42 $\pm$ 1.023 (L1)<br>1176.45 $\pm$ 10.23 (L5)    |
| GLONASS                 | 1601.7 $\pm$ 4.2 (L1)                                   |
| BDS                     | 1561.098 $\pm$ 2.046 (B1I)<br>1176.45 $\pm$ 10.23 (B2a) |
| Galileo                 | 1575.42 $\pm$ 2.046 (E1)<br>1176.45 $\pm$ 10.23 (E5a)   |
| NavIC <sup>dev</sup>    | 1176.45 $\pm$ 10.23 (L5)                                |
| QZSS                    | 1575.42 $\pm$ 1.023 (L1)<br>1176.45 $\pm$ 10.23 (L5)    |

### 5.2.2. GNSS Performance

The following table shows the GNSS performance of the module.

Table 31: GNSS Performance

| Parameter   | Mode                     | Condition   | Typ.  | Unit |
|-------------|--------------------------|-------------|-------|------|
| Sensitivity | Acquisition              |             | -147  | dBm  |
|             | Reacquisition            | Autonomous  | -158  | dBm  |
|             | Tracking                 |             | -158  | dBm  |
| TTFF        | Cold start<br>@ open sky | Autonomous  | 32.09 | s    |
|             |                          | AGNSS start | 8.92  | s    |
|             | Warm start<br>@ open sky | Autonomous  | 29.66 | s    |
|             |                          | AGNSS start | 1.61  | s    |
|             | Hot start<br>@ open sky  | Autonomous  | 1.55  | s    |
|             |                          | AGNSS start | 1.42  | s    |

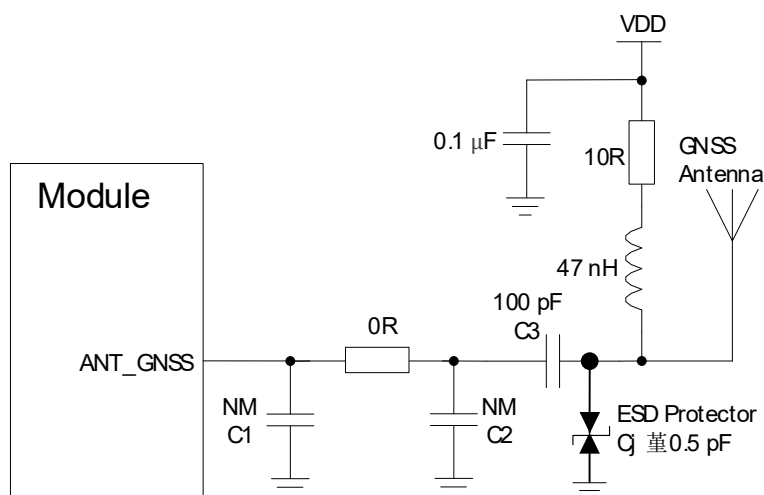
|          |        |                               |     |   |
|----------|--------|-------------------------------|-----|---|
| Accuracy | CEP-50 | L1 Autonomous<br>@ open sky   | 2.5 | m |
|          |        | L1&L5 dual-band<br>@ open sky | 1.8 | m |

## NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Cold start sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

### 5.2.3. Reference Design

*Figure 33: Reference Circuit of GNSS Antenna*



## NOTE

1. It is not recommended to add an external LNA when using a passive antenna.
2. For passive antenna, notes on C3:
  - 1) If there is DC power at the antenna ports, place capacitor on C3 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
  - 2) If there is no DC power in the peripheral design:
    - a) Do not reserve C3.
    - b) If C3 has already been reserved, it should be mounted with component, and it is recommended to use 0 Ω resistor. You can also match the component according to the debugging results.
3. To improve RF performance, maintain at least 15 dB isolation between cellular antennas and the GNSS antenna. It is recommended that the isolation between antenna traces on the PCB be greater than 75 dB.

### 5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to  $50\ \Omega$ . The impedance of the RF traces is usually determined by the trace width ( $W$ ), the materials' dielectric constant, the height from the reference ground to the signal layer ( $H$ ), and the spacing between RF traces and grounds ( $S$ ). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

Figure 34: Microstrip Design on a 2-layer PCB

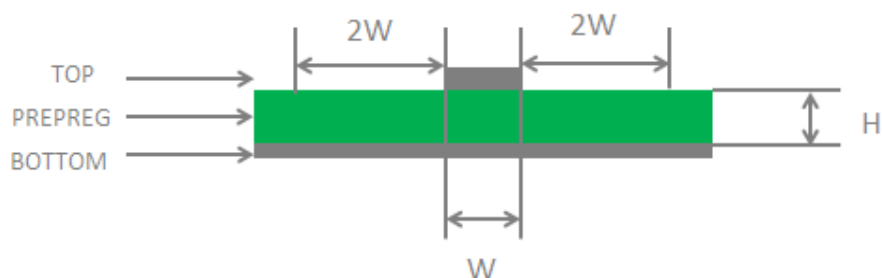


Figure 35: Coplanar Waveguide Design on a 2-layer PCB

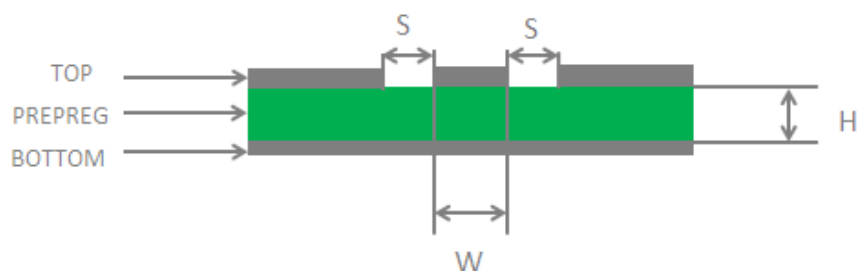


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

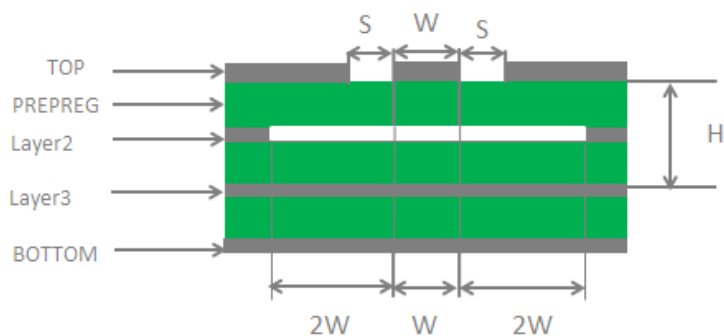
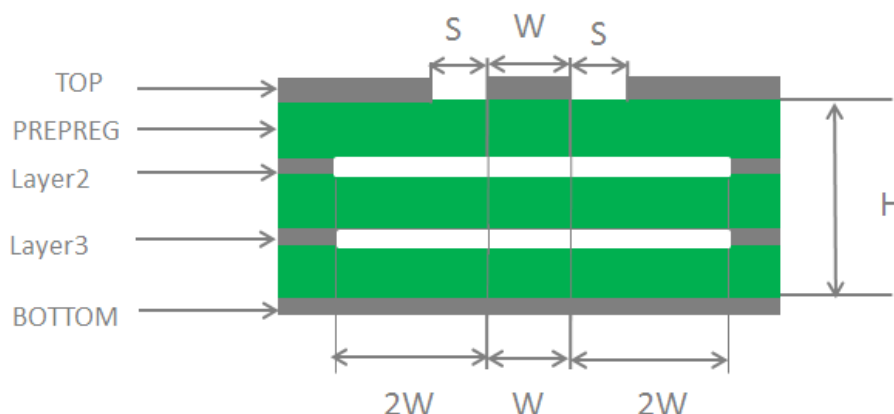


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)



To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to  $50\ \Omega$ .
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is  $135^\circ$ .
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces ( $2 \times W$ ).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see **document 5**.

## 5.4. Requirements for Antenna Design

Table 32: Requirements for Antenna Design

| Antenna Type | Requirements                                                                                                                                                                                                                                                              |
|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GNSS         | <ul style="list-style-type: none"> <li>● Frequency range: <ul style="list-style-type: none"> <li>- L1: 1559–1609 MHz</li> <li>- L5: 1166–1187 MHz</li> </ul> </li> <li>● Polarization: RHCP or linear</li> <li>● VSWR: <math>\leq 2</math> (Typ.)</li> </ul>              |
|              | <b>For passive antenna usage:</b> <ul style="list-style-type: none"> <li>- Passive antenna gain: <math>&gt; 0</math> dBi</li> </ul>                                                                                                                                       |
|              | <b>For active antenna usage:</b> <ul style="list-style-type: none"> <li>- Active antenna noise figure: <math>&lt; 1.5</math> dB (Typ.)</li> <li>- Active antenna embedded LNA gain: <math>&lt; 17</math> dB (Typ.)</li> </ul>                                             |
| Cellular     | <ul style="list-style-type: none"> <li>● VSWR: <math>\leq 2</math></li> <li>● Efficiency: <math>&gt; 30\%</math></li> <li>● Gain: 1 dBi</li> <li>● Max. input power: 50 W</li> <li>● Input impedance: <math>50\ \Omega</math></li> <li>● Cable insertion loss:</li> </ul> |

< 1 dB: LB (< 1 GHz)  
 < 1.5 dB: MB (1–2.3 GHz)  
 < 2 dB: HB (> 2.3 GHz)

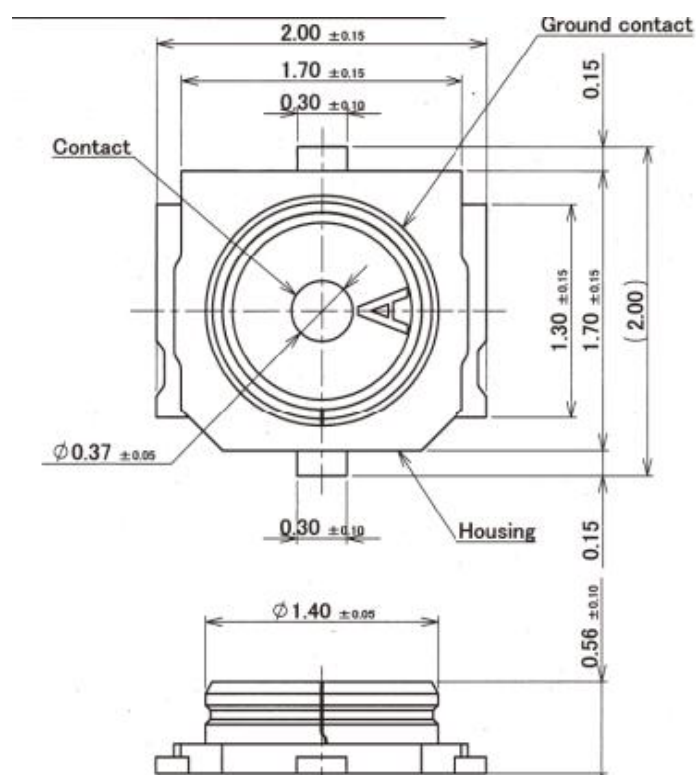
## NOTE

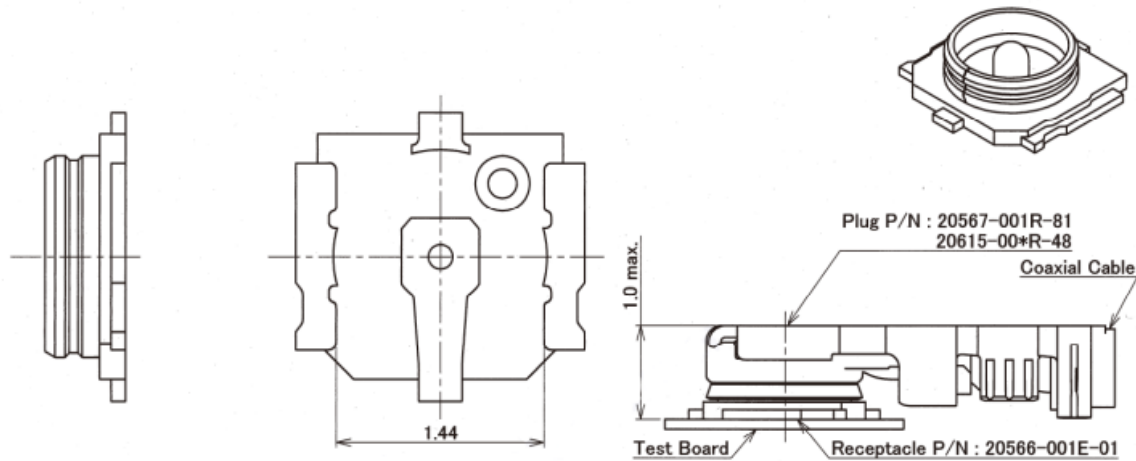
It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

## 5.5. RF Connector Recommendation

The receptacle dimensions are illustrated as below.

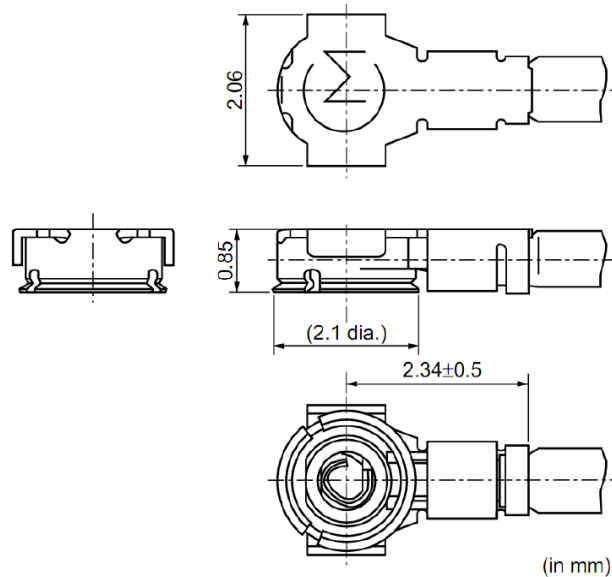
*Figure 38: Dimensions of the Receptacle (Unit: mm)*





The following figure shows the dimensions of mated plugs using Ø0.81 mm coaxial cables.

**Figure 39: Dimensions of Mated Plugs Using Ø0.81 mm Coaxial Cables (Unit: mm)**

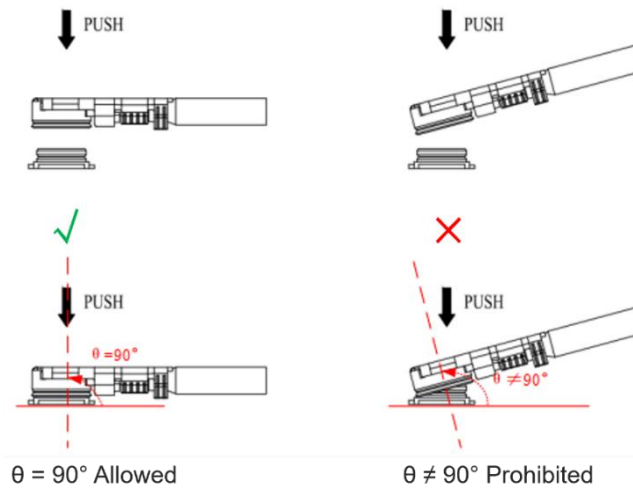


## 5.5.1. Recommended RF Connector for Installation

### 5.5.1.1. Assemble Coaxial Cable Plug Manually

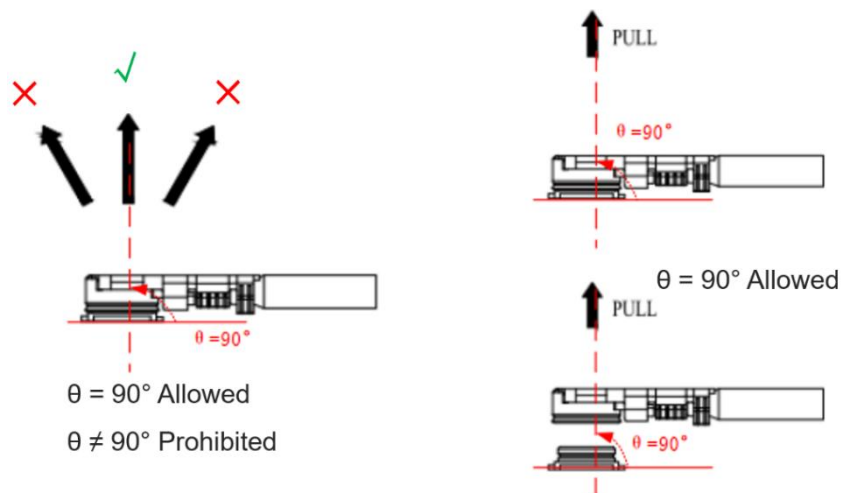
The illustration for plugging in a coaxial cable plug is shown below,  $\theta = 90^\circ$  is acceptable, while  $\theta \neq 90^\circ$  is not.

*Figure 40: Plug in a Coaxial Cable Plug*



The illustration of pulling out the coaxial cable plug is shown below,  $\theta = 90^\circ$  is acceptable, while  $\theta \neq 90^\circ$  is not.

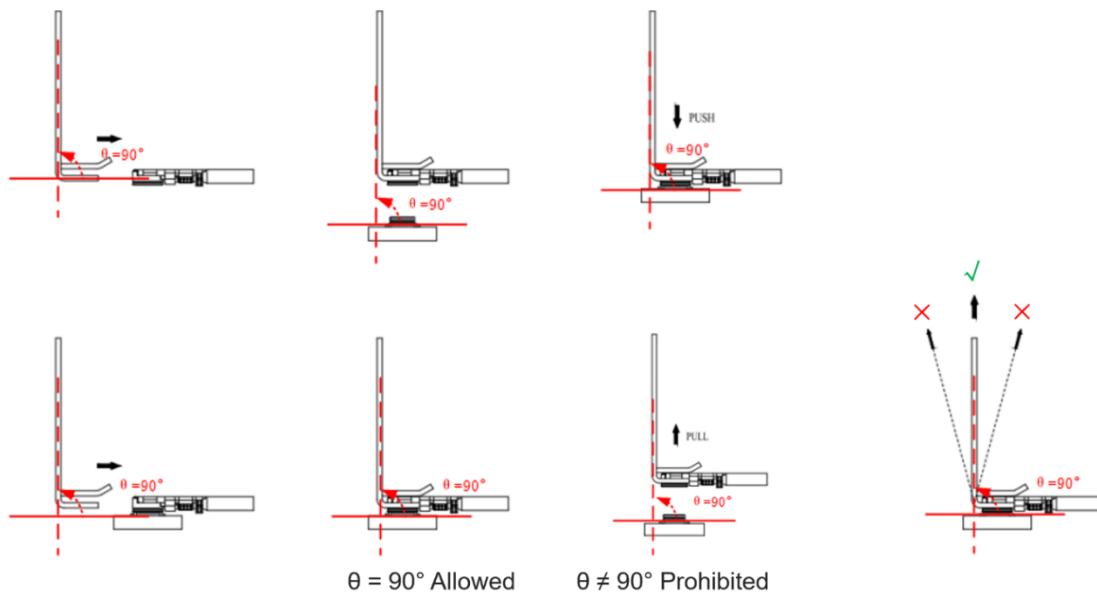
*Figure 41: Pull out a Coaxial Cable Plug*



#### 5.5.1.2. Assemble Coaxial Cable Plug with Jig

The pictures of installing the coaxial cable plug with a jig is shown below,  $\theta = 90^\circ$  is acceptable, while  $\theta \neq 90^\circ$  is not.

Figure 42: Install the Coaxial Cable Plug with Jig



### 5.5.2. Recommended Manufacturers of RF Connector and Cable

RF connectors and cables by I-PEX4 are recommended. For more details, visit <https://www.i-pex.com>.

# 6 Electrical Characteristics and Reliability

## 6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

*Table 33: Absolute Maximum Ratings*

| Parameter                       | Min. | Max.    | Unit |
|---------------------------------|------|---------|------|
| VBAT_RF/VBAT_BB                 | -0.3 | 4.7     | V    |
| USB_VBUS                        | -0.3 | 5.25    | V    |
| Peak Current of VBAT_BB/VBAT_RF | -    | 2.0     | A    |
| Voltage at Digital Pins         | -0.3 | 2.3     | V    |
| Voltage at ADC0                 | 0    | VBAT_BB | V    |
| Voltage at ADC1                 | 0    | VBAT_BB | V    |

### NOTE

Exceeding the conditions of use as shown above may cause permanent damage to the module.

## 6.2. Power Supply Ratings

*Table 34: Module's Power Supply Ratings*

| Parameter | Description         | Condition                                          | Min. | Typ. | Max. | Unit |
|-----------|---------------------|----------------------------------------------------|------|------|------|------|
| VBAT      | VBAT_BB and VBAT_RF | The actual input voltage must be within this range | 3.3  | 3.8  | 4.3  | V    |

|                   |                                        |                                |     |     |      |    |
|-------------------|----------------------------------------|--------------------------------|-----|-----|------|----|
|                   | Voltage drop during burst transmission | At maximum power control level | -   | -   | 400  | mV |
| I <sub>VBAT</sub> | Peak power consumption                 | At Maximum power control level | -   | -   | 2.0  | A  |
| USB_VBUS          | USB connection detection               |                                | 3.3 | 5.0 | 5.25 | V  |

## 6.3. Power Consumption

*Table 35: Power Consumption*

| Test Item                          | Condition                          | Band/Combination | Typ. | Unit |
|------------------------------------|------------------------------------|------------------|------|------|
| Turn off                           | Power off                          | -                | 55   | μA   |
| Sleep                              | <b>AT+CFUN=0</b> (USB 2.0 Suspend) | -                | 2.8  | mA   |
|                                    | <b>AT+CFUN=4</b> (USB 2.0 Suspend) | -                | 3.1  | mA   |
|                                    | SA FDD PF = 64 (USB 2.0 Suspend)   | n1               | 4.2  | mA   |
|                                    | SA TDD PF = 64 (USB 2.0 Suspend)   | n78              | 4.2  | mA   |
| Idle                               | SA FDD PF = 64 (USB 2.0 active)    | n1               | 23   | mA   |
|                                    | SA TDD PF = 64 (USB 2.0 active)    | n78              | 23   | mA   |
| LTE data transmission (GNSS OFF)   | LTE LB @ 23 dBm                    | B5               | 680  | mA   |
|                                    | LTE MB @ 23 dBm                    | B1               | 700  | mA   |
|                                    | LTE HB @ 23 dBm                    | B7               | 800  | mA   |
|                                    | LTE HPUE @ 26 dBm                  | B41              | 580  | mA   |
| 5G SA data transmission (GNSS OFF) | 5G NR LB @ 23 dBm                  | n5               | 680  | mA   |
|                                    | 5G NR MB @ 23 dBm                  | n1               | 780  | mA   |
|                                    | 5G NR HB @ 23 dBm                  | n7               | 850  | mA   |
|                                    | 5G NR UHB @ 23 dBm                 | n78              | 390  | mA   |
|                                    | 5G NR UHB @ 23 dBm                 | n79              | 400  | mA   |

### NOTE

The above power consumption data are tested under 50 Ω impedance.

## 6.4. Digital I/O Characteristics

*Table 36: VDD\_EXT I/O Characteristics (Unit: V)*

| Parameter       | Description               | Min.                   | Max.                   |
|-----------------|---------------------------|------------------------|------------------------|
| V <sub>IH</sub> | High-level input voltage  | $0.65 \times VDD\_EXT$ | $VDD\_EXT + 0.3$       |
| V <sub>IL</sub> | Low-level input voltage   | -0.3                   | $0.35 \times VDD\_EXT$ |
| V <sub>OH</sub> | High-level output voltage | $VDD\_EXT - 0.45$      | -                      |
| V <sub>OL</sub> | Low-level output voltage  | -                      | 0.45                   |

*Table 37: (U)SIM High/Low-voltage I/O Characteristics (Unit: V)*

| Parameter       | Description               | Min.                   | Max.                   |
|-----------------|---------------------------|------------------------|------------------------|
| V <sub>IH</sub> | High-level input voltage  | $0.7 \times USIM\_VDD$ | $USIM\_VDD + 0.3$      |
| V <sub>IL</sub> | Low-level input voltage   | -0.3                   | $0.2 \times USIM\_VDD$ |
| V <sub>OH</sub> | High-level output voltage | $0.8 \times USIM\_VDD$ | -                      |
| V <sub>OL</sub> | Low-level output voltage  | -                      | 0.4                    |

## 6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

*Table 38: Electrostatic Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)*

| Tested Interfaces      | Contact Discharge | Air Discharge | Unit |
|------------------------|-------------------|---------------|------|
| VBAT, GND              | ±5                | ±10           | kV   |
| All Antenna Interfaces | ±4                | ±8            | kV   |
| Other Interfaces       | ±0.5              | ±1            | kV   |

## 6.6. Operating and Storage Temperatures

The operating and storage temperatures are listed in the following table.

*Table 39: Operating and Storage Temperatures*

| Parameter                                    | Min. | Typ. | Max. | Unit |
|----------------------------------------------|------|------|------|------|
| Normal Operating Temperature <sup>14</sup>   | -30  | +25  | +75  | °C   |
| Extended Operating Temperature <sup>15</sup> | -40  | -    | +85  | °C   |
| Storage Temperature                          | -40  | -    | +90  | °C   |

## 6.7. Thermal Dissipation

The module offers the best performance when all internal IC chips are working within their operating temperatures. When the IC chip reaches or exceeds the maximum junction temperature, the module may still work but the performance and function (such as RF output power, data rate) will be affected to a certain extent. Therefore, the thermal design should be maximally optimized to ensure all internal IC chips always work within the recommended operating temperature range.

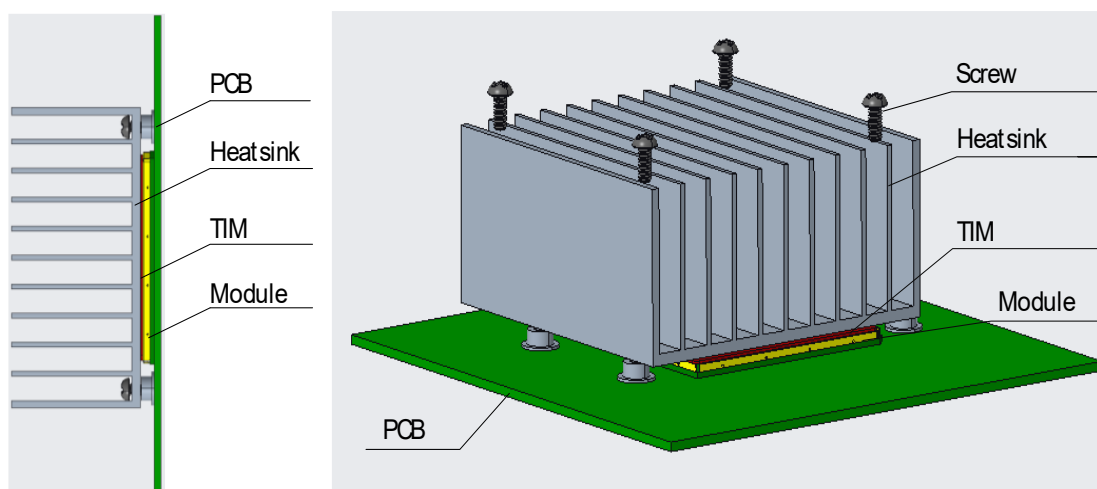
The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on your PCB, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Follow the principles below when the heatsink is necessary:
  - Do not place large size components in the area where the module is mounted on your PCB to reserve enough place for heatsink installation.
  - Attach the heatsink to the shielding cover of the module; In general, the base plate area of the heatsink should be larger than the module area to cover the module completely;
  - Choose the heatsink with adequate fins to dissipate heat;
  - Choose a TIM (Thermal Interface Material) with high thermal conductivity, good softness and good wettability and place it between the heatsink and the module;
  - Fasten the heatsink with four screws to ensure that it is in close contact with the module to prevent the heatsink from falling off during the drop, vibration test, or transportation.

<sup>14</sup> To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

<sup>15</sup> To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within the range of -40 to -30 °C or 75 to 85 °C, the module remains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P<sub>out</sub>, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

Figure 43: Placement and Fixing of the Heatsink



# 7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are  $\pm 0.2$  mm unless otherwise specified.

## 7.1. Mechanical Dimensions

*Figure 44: Top and Side Dimensions*

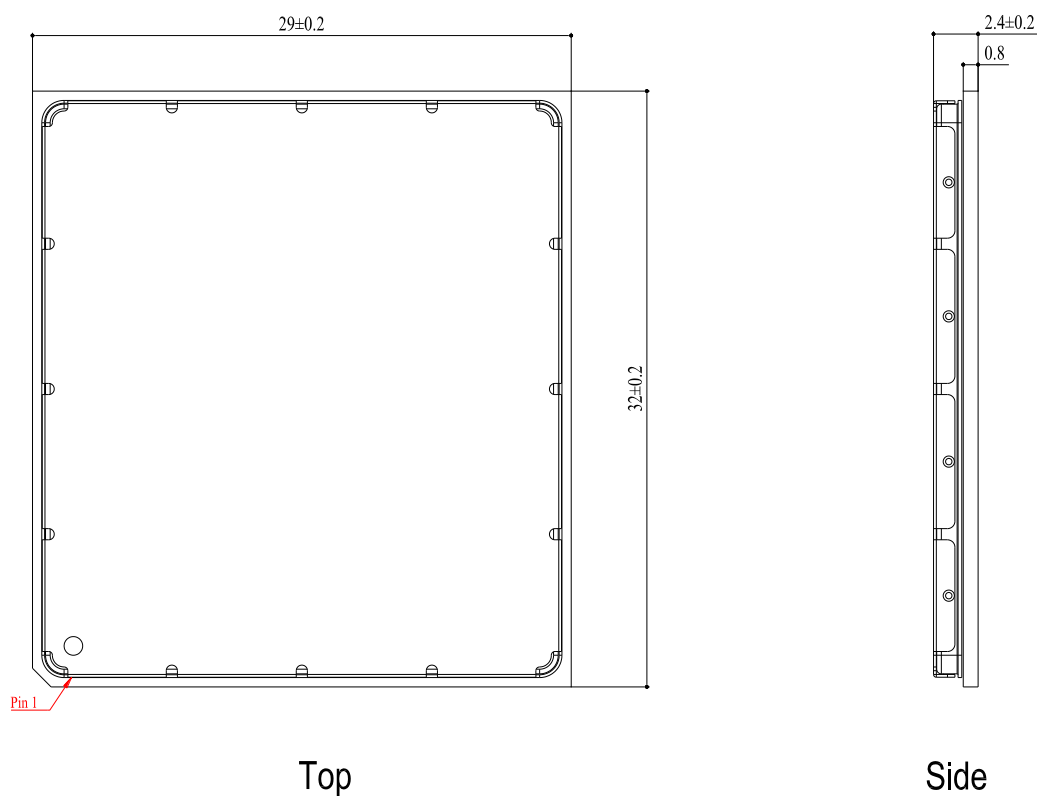
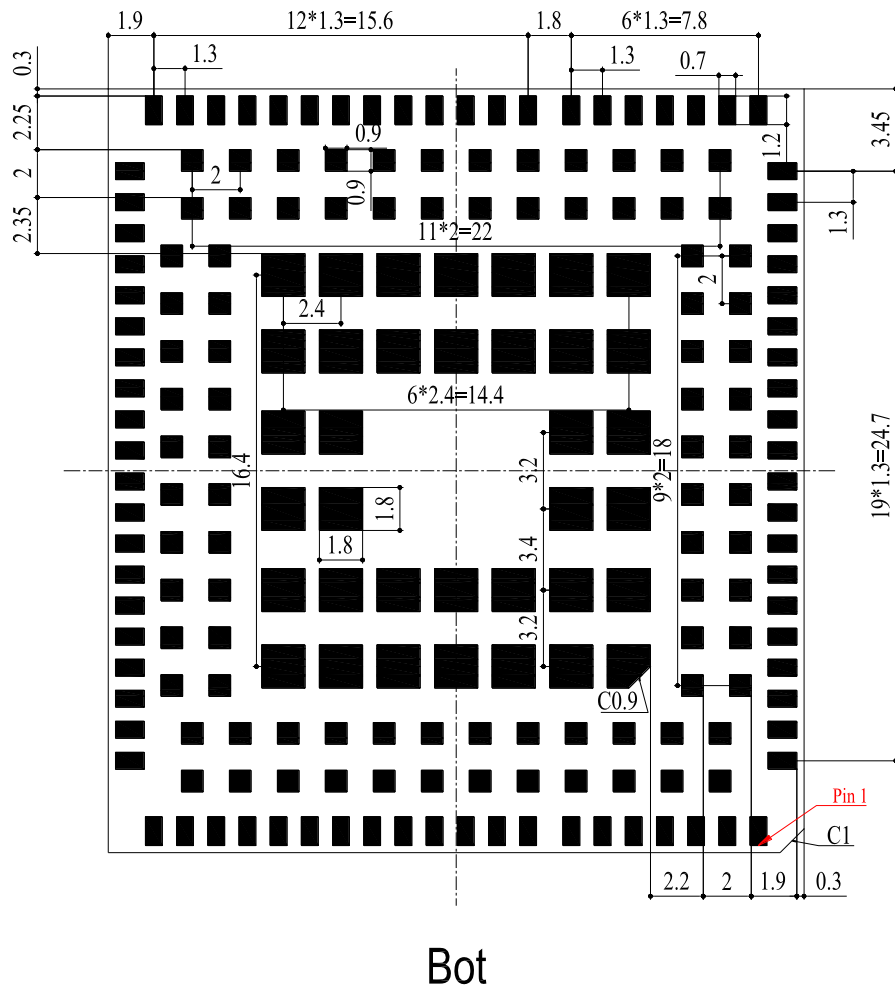


Figure 45: Bottom Dimensions (Bottom View)

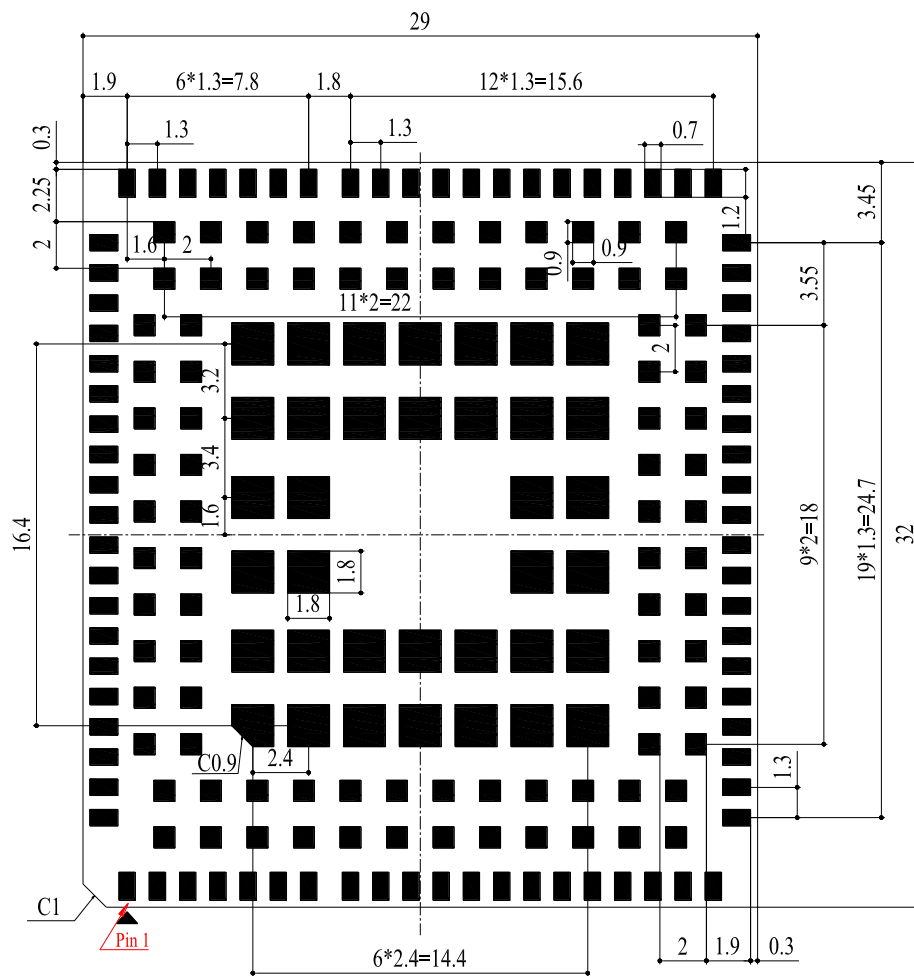


## NOTE

The module's coplanarity standard:  $\leq 0.13$  mm.

## 7.2. Recommended Footprint

Figure 46: Recommended Footprint



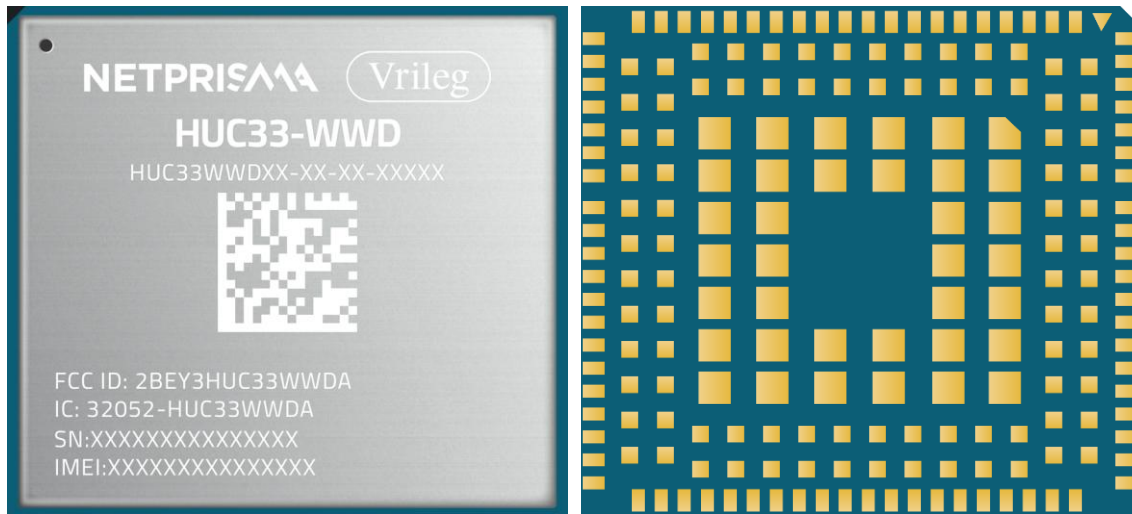
Unlabeled tolerance: +/-0.2mm

## NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

## 7.3. Top and Bottom views

*Figure 47: Top and Bottom Views of the Module*



## NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from NetPrisma.

# 8 Storage, Manufacturing and Packaging

## 8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be  $23 \pm 5$  °C and the relative humidity should be 35–60 %.
2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.
3. Floor life: 168 hours <sup>16</sup> in a factory where the temperature is  $23 \pm 5$  °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).
4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:
  - The module is not stored in Recommended Storage Condition;
  - Violation of the third requirement mentioned above;
  - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
  - Before module repairing.
5. If needed, the pre-baking should follow the requirements below:
  - The module should be baked for 24 hours at  $120 \pm 5$  °C;
  - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

### NOTE

- 
1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
  2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
  3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.
- 

## 8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see **document 6**.

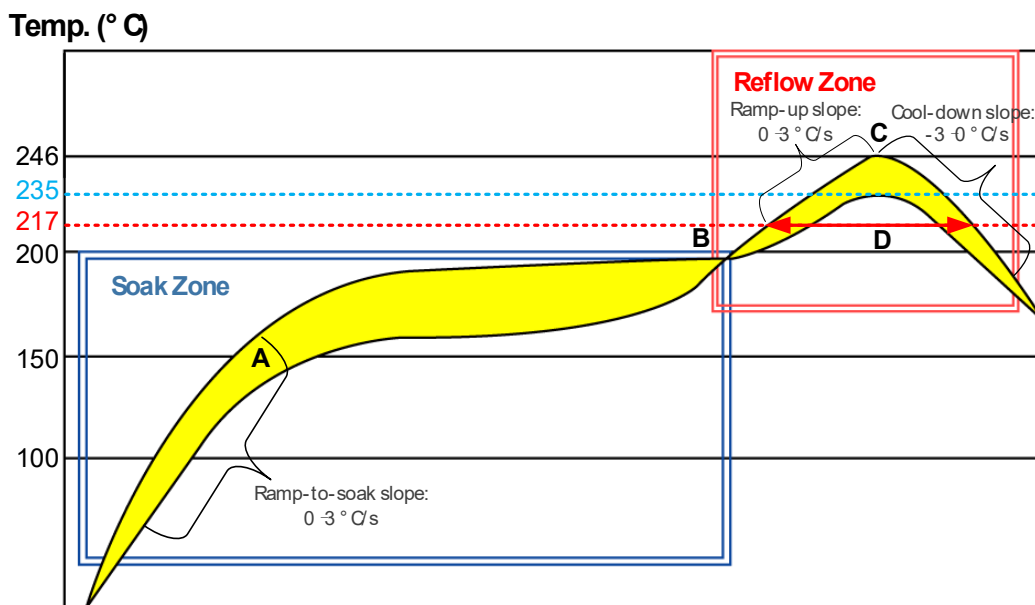
The recommended peak reflow temperature should be 235–246 °C, with 246 °C as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that

---

<sup>16</sup> This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

*Figure 48: Recommended Reflow Soldering Thermal Profile*



*Table 40: Recommended Thermal Profile Parameters*

| Factor                                         | Recommended Value |
|------------------------------------------------|-------------------|
| <b>Soak Zone</b>                               |                   |
| Ramp-to-soak slope                             | 0–3 °C/s          |
| Soak time (between A and B: 150 °C and 200 °C) | 70–120 s          |
| <b>Reflow Zone</b>                             |                   |
| Ramp-up slope                                  | 0–3 °C/s          |
| Reflow time (D: over 217°C)                    | 40–70 s           |
| Max temperature                                | 235–246 °C        |
| Cool-down slope                                | -3–0 °C/s         |
| <b>Reflow Cycle</b>                            |                   |
| Max reflow cycle                               | 1                 |

## NOTE

- The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.

2. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
3. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
4. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
5. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
6. Due to the complexity of the SMT process, please contact NetPrisma Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in **document 7**.

### 8.3. Packaging Specification

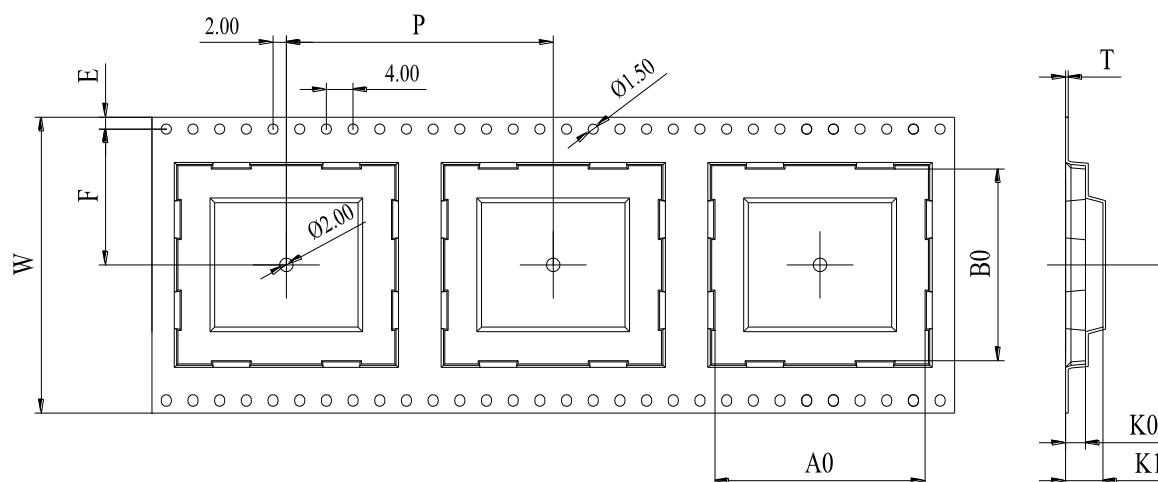
This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

#### 8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

**Figure 49: Carrier Tape Dimension Drawing (Unit: mm)**



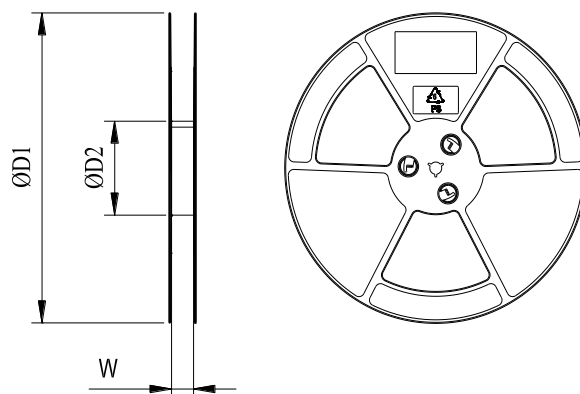
**Table 41: Carrier Tape Dimension Table (Unit: mm)**

| W  | P  | T    | A0   | B0   | K0 | K1  | F    | E    |
|----|----|------|------|------|----|-----|------|------|
| 44 | 44 | 0.35 | 32.5 | 29.5 | 3  | 3.8 | 20.2 | 1.75 |

### 8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

*Figure 50: Plastic Reel Dimension Drawing*

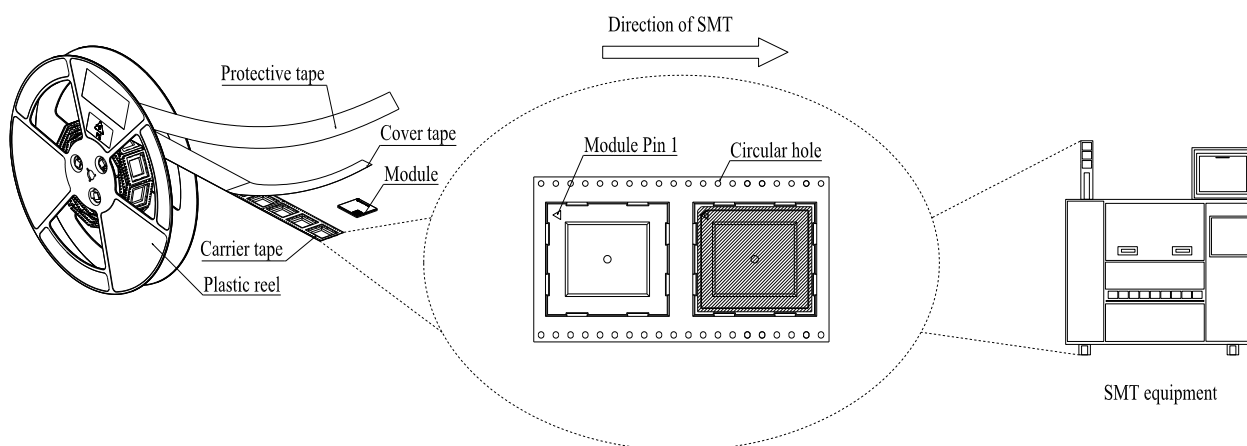


*Table 42: Plastic Reel Dimension Table (Unit: mm)*

| ØD1 | ØD2 | W    |
|-----|-----|------|
| 330 | 100 | 44.5 |

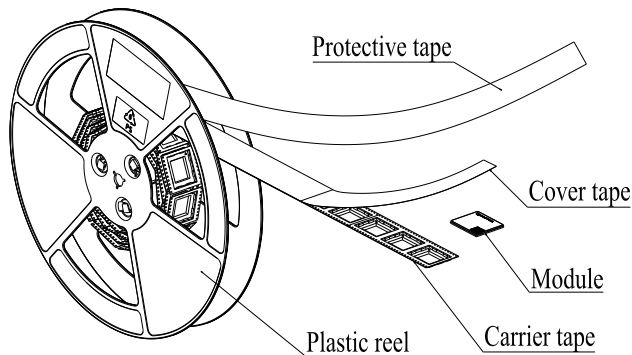
### 8.3.3. Mounting Direction

*Figure 51: Mounting Direction*



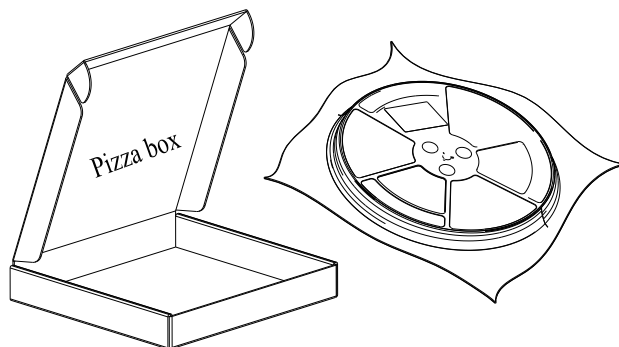
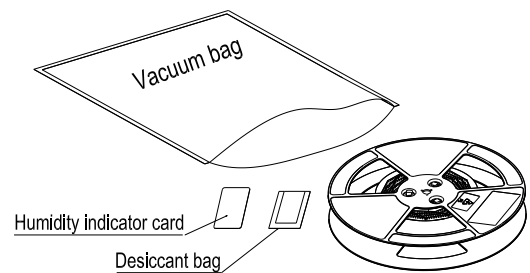
### 8.3.4. Packaging Process

*Figure 52: Packaging Process*



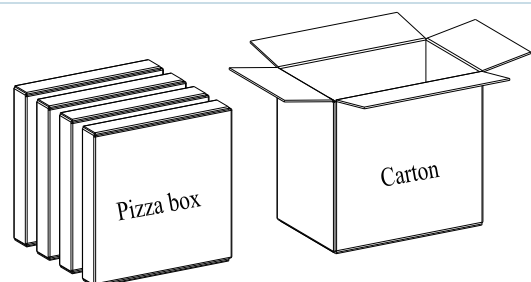
Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.



Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.



# 9 Appendix A References

*Table 43: Related Documents*

| Document Name                                   |
|-------------------------------------------------|
| 1. NetPrisma-HUC33-WWD-GNSS-Application-Note    |
| 2. NetPrisma-HUC33-WWD-Reference-Design         |
| 3. NetPrisma-5G-RedCap-EVB-User-Guide           |
| 4. NetPrisma-HUC33-WWD-AT-Commands-Manual       |
| 5. NetPrisma-RF-Layout-Application-Note         |
| 6. NetPrisma-Module-Stencil-Design-Requirements |
| 7. NetPrisma-Module-SMT-Application-Note        |

*Table 44: Terms and Abbreviations*

| Abbreviation | Description                                 |
|--------------|---------------------------------------------|
| AMR          | Adaptive Multi-rate                         |
| AMR-WB       | Adaptive Multi-Rate Wideband                |
| BDS          | BeiDou Navigation Satellite System          |
| bps          | Bits Per Second                             |
| CHAP         | Challenge Handshake Authentication Protocol |
| CTS          | Clear To Send                               |
| DDR          | Double Data Rate                            |
| DFOTA        | Delta Firmware Upgrade Over The Air         |
| DL           | Downlink                                    |
| DTR          | Data Terminal Ready                         |
| DUN          | Dial-Up Networking                          |
| ECM          | Ethernet Control Model                      |
| ESD          | Electrostatic Discharge                     |

|         |                                             |
|---------|---------------------------------------------|
| FDD     | Frequency Division Duplex                   |
| FR      | Full Rate                                   |
| FTP     | File Transfer Protocol                      |
| FTPS    | FTP over SSL/FTP Secure                     |
| Galileo | Galileo Satellite Navigation System (EU)    |
| GLONASS | Global Navigation Satellite System (Russia) |
| GNSS    | Global Navigation Satellite System          |
| GPS     | Global Positioning System                   |
| HPUE    | High Power User Equipment                   |
| HTTP    | Hypertext Transfer Protocol                 |
| HTTPS   | Hypertext Transfer Protocol Secure          |
| I/O     | Input/Output                                |
| IMS     | IP Multimedia Subsystem                     |
| LED     | Light Emitting Diode                        |
| LTE     | Long Term Evolution                         |
| LwM2M   | Lightweight M2M                             |
| M2M     | Machine to Machine                          |
| MBIM    | Mobile Broadband Interface Model            |
| MCP     | Multiple Chip Package                       |
| ME      | Mobile Equipment                            |
| MIMO    | Multiple Input Multiple Output              |
| MO      | Mobile Originated                           |
| MQTT    | Message Queuing Telemetry Transport         |
| MS      | Mobile Station (GSM engine)                 |
| MSL     | Moisture Sensitivity Level                  |
| MT      | Mobile Terminated                           |
| NAS     | Non-Access Stratum                          |
| NavIC   | Navigation with Indian Constellation        |

|       |                                                                        |
|-------|------------------------------------------------------------------------|
| NITZ  | Network Identity and Time Zone / Network Informed Time Zone            |
| NTP   | Network Time Protocol                                                  |
| NMEA  | NMEA (National Marine Electronics Association) 0183 Interface Standard |
| PAP   | Password Authentication Protocol                                       |
| PCB   | Printed Circuit Board                                                  |
| PDA   | Personal Digital Assistant                                             |
| PDU   | Protocol Data Unit                                                     |
| PING  | Packet Internet Groper                                                 |
| POS   | Point of Sale                                                          |
| PPP   | Point-to-Point Protocol                                                |
| QAM   | Quadrature Amplitude Modulation                                        |
| QPSK  | Quadrature Phase Shift Keying                                          |
| RmNet | Remote Network                                                         |
| RF    | Radio Frequency                                                        |
| RHCP  | Right Hand Circularly Polarized                                        |
| RNDIS | Remote Network Driver Interface Specification                          |
| Rx    | Receive                                                                |
| SA    | Standalone                                                             |
| SCS   | Sub-Carrier Space                                                      |
| SGMII | Serial Gigabit Media Independent Interface                             |
| SIMO  | Single Input Multiple Output                                           |
| SMS   | Short Message Service                                                  |
| SMD   | Surface Mount Device                                                   |
| SMTP  | Simple Mail Transfer Protocol                                          |
| SSL   | Secure Sockets Layer                                                   |
| TCP   | Transmission Control Protocol                                          |
| TDD   | Time Division Duplexing                                                |
| TLS   | Transport Layer Security                                               |

|        |                                        |
|--------|----------------------------------------|
| TX     | Transmitting Direction                 |
| UDP    | User Datagram Protocol                 |
| UL     | Uplink                                 |
| URC    | Unsolicited Result Code                |
| (U)SIM | (Universal) Subscriber Identity Module |
| VLAN   | Virtual Local Area Network             |
| Vmax   | Maximum Voltage                        |
| Vnom   | Nominal Voltage                        |
| Vmin   | Minimum Voltage                        |
| VSWR   | Voltage Standing Wave Ratio            |
| WLAN   | Wireless Local Area Network            |

# 10 Appendix B Operating Frequencies

*Table 45: Operating Frequencies (5G)*

| 5G  | Duplex Mode | Uplink Operating Band | Downlink Operating Band | Unit |
|-----|-------------|-----------------------|-------------------------|------|
| n2  | FDD         | 1850–1910             | 1930–1990               | MHz  |
| n5  | FDD         | 824–849               | 869–894                 | MHz  |
| n7  | FDD         | 2500–2570             | 2620–2690               | MHz  |
| n12 | FDD         | 699–716               | 729–746                 | MHz  |
| n13 | FDD         | 777–787               | 746–756                 | MHz  |
| n14 | FDD         | 788–798               | 758–768                 | MHz  |
| n25 | FDD         | 1850–1915             | 1930–1995               | MHz  |
| n26 | FDD         | 814–849               | 859–894                 | MHz  |
| n30 | FDD         | 2305–2315             | 2350–2360               | MHz  |
| n38 | TDD         | 2570–2620             | 2570–2620               | MHz  |
| n41 | TDD         | 2496–2690             | 2496–2690               | MHz  |
| n66 | FDD         | 1710–1780             | 2110–2200               | MHz  |
| n70 | FDD         | 1695–1710             | 1995–2020               | MHz  |
| n71 | FDD         | 663–698               | 617–652                 | MHz  |
| n77 | TDD         | 3450–3550             | 3450–3550               | MHz  |
| n77 | TDD         | 3700–3980             | 3700–3980               | MHz  |

*Table 46: Operating Frequencies (4G)*

| 4G  | Duplex Mode | Uplink Operating Frequency | Downlink Operating Frequency | Unit |
|-----|-------------|----------------------------|------------------------------|------|
| B2  | FDD         | 1850–1910                  | 1930–1990                    | MHz  |
| B4  | FDD         | 1710–1755                  | 2110–2155                    | MHz  |
| B5  | FDD         | 824–849                    | 869–894                      | MHz  |
| B7  | FDD         | 2500–2570                  | 2620–2690                    | MHz  |
| B12 | FDD         | 699–716                    | 729–746                      | MHz  |

|     |                   |           |           |     |
|-----|-------------------|-----------|-----------|-----|
| B13 | FDD               | 777–787   | 746–756   | MHz |
| B14 | FDD               | 788–798   | 758–768   | MHz |
| B17 | FDD               | 704–716   | 734–746   | MHz |
| B25 | FDD               | 1850–1915 | 1930–1995 | MHz |
| B26 | FDD               | 814–849   | 859–894   | MHz |
| B30 | FDD               | 2305–2315 | 2350–2360 | MHz |
| B38 | TDD               | 2570–2620 | 2570–2620 | MHz |
| B41 | TDD               | 2496–2690 | 2496–2690 | MHz |
| B42 | TDD               | 3400–3600 | 3400–3600 | MHz |
| B43 | TDD               | 3600–3800 | 3600–3800 | MHz |
| B48 | TDD               | 3550–3700 | 3550–3700 | MHz |
| B66 | FDD <sup>17</sup> | 1710–1780 | 2110–2200 | MHz |
| B70 | FDD <sup>18</sup> | 1695–1710 | 1995–2020 | MHz |
| B71 | FDD               | 663–698   | 617–652   | MHz |

**FCC ID: 2BEY3HUC33WWDA**

## OEM/Integrators Installation Manual

### Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band

<sup>17</sup> The range 2180–2200 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured.

<sup>18</sup> The range 2010–2020 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured and Tx-Rx separation is 300 MHz. The range 2005–2020 MHz of the DL operating band is restricted to E-UTRA operation when carrier aggregation is configured and Tx-Rx separation is 295 MHz.

emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are compliant with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

## Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to NETPRISMA INC. that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

## End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: 2BEY3HUC33WWDA”

“Contains IC: 32052-HUC33WWDA”

The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

## Antenna Installation

- (1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
- (2) The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

| Band             | Antenna Type | Allowed Max Gain (dBi) |
|------------------|--------------|------------------------|
| LTE B2 / NR n2   | Dipole       | 8                      |
| LTE B4           |              | 5                      |
| LTE B5           |              | 11.56                  |
| NR n5            |              | 11.57                  |
| LTE B7 / NR n7   |              | 8                      |
| LTE B12          |              | 10.85                  |
| NR n12           |              | 10.86                  |
| LTE B13 / NR n13 |              | 11.31                  |
| LTE B14 / NR n14 |              | 11.38                  |
| LTE B17          |              | 10.89                  |
| LTE B25 / NR n25 |              | 8                      |
| LTE B26(814-824) |              | 11.51                  |

|                    |  |       |
|--------------------|--|-------|
| LTE B26(824-849)   |  | 11.56 |
| NR n26(814-824)    |  | 11.52 |
| NR n26(824-849)    |  | 11.57 |
| LTE B30 / NR n30   |  | 0.98  |
| LTE B38 / NR n38   |  | 5     |
| LTE B41 / NR n41   |  | 5     |
| LTE B42(3450-3550) |  | 2     |
| LTE B42(3550-3600) |  | 1     |
| LTE B43            |  | 1     |
| LTE B48 /          |  | 1     |
| LTE B66 / NR n66   |  | 5     |
| LTE B70 / NR n70   |  | 5     |
| LTE B71 / NR n71   |  | 10.63 |
| NR n77(3450-3550)  |  | 2     |
| NR n77(3700-3980)  |  | 2     |

## Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

## Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

## List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, and part 96 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

## **This device is intended only for OEM integrators under the following conditions: (For module device use)**

- 1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
- 2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

## Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

## IC: 32052-HUC33WWDA

### IC Statement

This device contains licence-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's licence-exempt RSS(s). Operation is subject to the following two conditions:

- (1) This device may not cause interference.
- (2) This device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil contient un ou des émetteurs/récepteurs exemptés de licence, conformes aux normes RSS exemptées du Canada en matière d'innovation, de science et de développement économique. Son fonctionnement est soumis aux deux conditions suivantes :

- (1) Cet appareil ne doit pas provoquer d'interférences.
- (2) Cet appareil doit accepter toute interférence, y compris celles susceptibles de provoquer un fonctionnement indésirable de l'appareil.

### Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

### Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

### **This device is intended only for OEM integrators under the following conditions: (For module device use)**

- 1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
- 2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

### **Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)**

- 1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et

les utilisateurs, et

2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

## **IMPORTANT NOTE:**

In the event that these conditions cannot be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

## **NOTE IMPORTANTE:**

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

## **End Product Labeling**

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains IC: 32052-HUC33WWDA".

## **Plaque signalétique du produit final**

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 32052-HUC33WWDA".

## **Manual Information To the End User**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

## **Manuel d'information à l'utilisateur final**

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.

Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

# Document History

| Revision | Date       | Changes             |
|----------|------------|---------------------|
| A        | 2025-08-11 | The first revision. |



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