

LUK64-LD&LUK66-LD

Hardware Design

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Contents

Contents	2
Table Index.....	4
Figure Index	5
1 Introduction	6
1.1. Text Conventions.....	6
2 Product Overview.....	7
2.1. Frequency Bands and Functions	7
2.2. Key Features	7
2.3. Pin Assignment.....	9
2.4. Pin Definitions.....	11
3 Operating Characteristics	17
3.1. Operating Modes	17
3.1.1. Sleep Mode	17
3.1.1.1. UART Application	18
3.1.1.2. USB Application.....	19
3.1.2. Airplane Mode	20
3.2. Power Supply	21
3.2.1. Power Supply Pins	21
3.2.2. Reference Design for Power Supply.....	22
3.2.3. Power Supply Voltage Monitoring.....	23
3.3. Turn On.....	23
3.4. Turn Off.....	25
3.4.1. Turn Off with PWRKEY	25
3.4.2. Turn Off with AT Command	26
3.5. Reset	26
4 Application Interfaces	28
4.1. (U)SIM Interfaces	28
4.2. USB Interface	30
4.3. UART Interfaces	32
4.3.1. Main UART Interface	32
4.3.2. Debug UART Interface.....	33
4.3.3. Bluetooth UART Interface ^{dev}	33
4.3.4. UART Application.....	33
4.4. SPI	35
4.5. PCM and I2C Interfaces	35
4.6. ADC Interfaces	37
4.7. Status Indication	38
4.7.1. Network Status Indication	38
4.7.2. Module Status Indication.....	39
4.8. RI	40
4.9. PCIe Interface	40
4.10. SDIO Interface.....	42
4.11. Antenna Tuner Control Interfaces ^{dev}	44
4.12. USB_BOOT Interface	44
5 RF Specifications	45
5.1. Cellular Network	45
5.1.1. Antenna Interface & Frequency Bands.....	45
5.1.2. Tx Power	46
5.1.3. Rx Sensitivity.....	46
5.1.4. Reference Design	47
5.2. GNSS (Optional).....	48
5.2.1. Antenna Interface & Frequency Bands.....	48
5.2.2. GNSS Performance	49
5.2.3. Passive Antenna Reference Design	50
5.2.4. Active Antenna Reference Design.....	50
5.3. RF Routing Guidelines	51
5.4. Antenna Design Requirements	52
5.5. RF Connector Recommendation.....	53
6 Electrical Characteristics and Reliability	56

6.1.	Absolute Maximum Ratings.....	56
6.2.	Power Supply Ratings	56
6.3.	Power Consumption	56
6.4.	Digital I/O Characteristics	59
6.5.	ESD Protection	60
6.6.	Operation and Storage Temperatures	60
6.7.	Thermal Dissipation.....	61
7	Mechanical Information.....	62
7.1.	Mechanical Dimensions	62
7.2.	Recommended Footprint.....	64
7.3.	Top and Bottom Views	64
8	Storage, Manufacturing & Packaging.....	66
8.1.	Storage Conditions	66
8.2.	Manufacturing and Soldering	66
8.3.	Packaging Specification	68
8.3.1.	Carrier Tape	68
8.3.2.	Plastic Reel	69
8.3.3.	Mounting Direction	69
8.3.4.	Packaging Process	70
9	Appendix References	71
	Document History	79

Table Index

Table 1: Text Conventions	6
Table 2: Frequency Bands and GNSS Types.....	7
Table 3: Key Features.....	7
Table 4: Parameter Definition	11
Table 5: Pin Description	11
Table 6: Overview of Operating Modes	17
Table 7: Pin Description of W_DISABLE#.....	20
Table 8: RF Function Status	20
Table 9: VBAT and GND Pins.....	21
Table 10: Pin Definition of PWRKEY	23
Table 11: Pin Definition of RESET_N	26
Table 12: Pin Definition of (U)SIM Interfaces	28
Table 13: Pin Definition of USB Interface	30
Table 14: USB Trace Length Inside the Module.....	32
Table 15: Pin Definition of Main UART Interface	32
Table 16: Pin Definition of Debug UART Interface	33
Table 17: Pin Definition of Bluetooth UART Interface	33
Table 18: Pin Definition of SPI	35
Table 19: Pin Definition of PCM and I2C Interfaces	37
Table 20: Pin Definition of the ADC Interface	38
Table 21: Characteristics of ADC Interfaces.....	38
Table 22: Pin Definition of NET_MODE and NET_STATUS.....	38
Table 23: Working Status of NET_MODE and NET_STATUS.....	39
Table 24: Pin Definition of STATUS.....	39
Table 25: Default Behaviors of MAIN_RI.....	40
Table 26: Pin Definition of PCIe Interface.....	41
Table 27: PCIe Trace Length Inside the Module	42
Table 28: Pin Definition of SDIO Interface.....	42
Table 29: Pin Definition of RFFE Interfaces	44
Table 30: Pin Definition of USB_BOOT Interface	44
Table 31: Pin Definition of the Main/Rx-diversity/MIMO Antenna Interfaces	45
Table 32: Frequency Bands	45
Table 33: Tx Power	46
Table 34: LUK64-LD & LUK66-LD Dual-Antenna Conducted RF Rx Sensitivity	46
Table 35: LUK64-LD & LUK66-LD Four-Antenna Conducted RF Rx Sensitivity	47
Table 36: Pin Definition of GNSS Antenna Interface	49
Table 37: GNSS Frequency	49
Table 38: GNSS Performance	49
Table 39: Antenna Design Requirements.....	52
Table 40: Absolute Maximum Ratings.....	56
Table 41: Power Supply Ratings.....	56
Table 42: LUK64-LD Power Consumption.....	57
Table 43: LUK66-LD Power Consumption.....	58
Table 44: VDD_EXT I/O Requirements	59
Table 45: USIM_VDD High/Low-voltage I/O Requirements.....	59
Table 46: SDIO_VDD Low-voltage I/O Requirements.....	59
Table 47: SDIO_VDD High-voltage I/O Requirements.....	60
Table 48: Electrostatic Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %).....	60
Table 49: Operating and Storage Temperatures.....	60
Table 50: Recommended Thermal Profile Parameters	67
Table 51: Carrier Tape Dimension Table (Unit: mm).....	69
Table 52: Plastic Reel Dimension Table (Unit: mm).....	69
Table 53: Related Documents.....	71
Table 54: Term and Abbreviation.....	71

Figure Index

Figure 2: Pin Assignment (Top View)	10
Figure 3: Module Power Consumption in Sleep Mode	18
Figure 4: Sleep Mode Application via UART Interfaces	18
Figure 5: Sleep Mode Application with USB Remote Wake-up.....	19
Figure 6: Sleep Mode Application with Suspend function	19
Figure 7: Sleep Mode Application without Suspend Function	20
Figure 8: Power Supply Limits during Burst Transmission.....	22
Figure 9: Star Structure of the Power Supply	22
Figure 10: Reference Circuit of Power Supply.....	23
Figure 11: Turn on the Module with a Driving Circuit	24
Figure 12: Turn on the Module with a Button.....	24
Figure 13: Turn-on Timing.....	25
Figure 14: Turn-off Timing.....	26
Figure 15: Reference Circuit of RESET_N with a Driving Circuit.....	27
Figure 16: Reset Timing.....	27
Figure 17: Reference Circuit of (U)SIM Interfaces with an 8-Pin (U)SIM Card Connector	29
Figure 18: Reference Circuit of (U)SIM Interfaces with a 6-Pin (U)SIM Card Connector	30
Figure 19: Reference Circuit of USB Application.....	31
Figure 20: Reference Circuit (IC Solution) (Main UART).....	34
Figure 21: Reference Circuit (Transistor Solution) (Main UART).....	34
Figure 22: Reference Circuit of PCM and SPI Application with SLIC.....	35
Figure 23: Primary Mode Timing.....	36
Figure 24: Auxiliary Mode Timing	36
Figure 25: Reference Circuit of PCM and I2C Application with Audio Codec	37
Figure 26: Reference Circuit of the Network Indicator.....	39
Figure 27: Reference Circuits of STATUS.....	40
Figure 28: PCIe Interface Reference Circuit (RC Mode)	42
Figure 29: Reference Circuit of SD Card Application	43
Figure 30: Reference Circuit of USB_BOOT	44
Figure 31: Reference Circuit of RF Antenna Interfaces.....	48
Figure 32: Reference Circuit of Passive Antenna Interface.....	50
Figure 33: Reference Circuit of Active Antenna Interface	51
Figure 34: Microstrip Line Design on a 2-layer PCB	51
Figure 35: Coplanar Waveguide Line Design on a 2-layer PCB	51
Figure 36: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 3 as Reference Ground).....	52
Figure 37: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 4 as Reference Ground).....	52
Figure 38: Dimensions of the Receptacle (Unit: mm).....	54
Figure 39: Specifications of Mated Plugs	54
Figure 40: Space Factor of Mated Connectors (Unit: mm).....	55
Figure 41: Placement and Fixing of the Heatsink.....	61
Figure 42: Module Top and Side Dimensions.....	62
Figure 43: Module Bottom Dimensions (Bottom View).....	63
Figure 44: Recommended Footprint (Unit: mm)	64
Figure 45: Top and Bottom Views of LUK64-LD.....	64
Figure 46: Top and Bottom Views of LUK66-LD.....	65
Figure 47: Reflow Soldering Thermal Profile	67
Figure 48: Carrier Tape Dimension Drawing (Unit: mm)	68
Figure 49: Plastic Reel Dimension Drawing	69
Figure 50: Mounting Direction	69
Figure 51: Packaging Process	70

1 Introduction

This document defines LUK64-LD and LUK66-LD modules and describes their air and hardware interfaces which are connected to your applications.

With this document, you can quickly understand module interfaces, electrical and mechanical specifications, as well as other related information of the modules. The document, coupled with application notes and user guides, makes it easy to design and sets up mobile applications with the modules.

1.1. Text Conventions

Table 1: Text Conventions

dev	Unless stated otherwise, the presence of the mark "dev" following a function, feature, interface, pin name, command, argument, etc., signifies that it is still in the development phase and not yet supported. Additionally, when "dev" appears after a model, it indicates that the model sample is currently unavailable.
NOTE	"NOTE" is used to identify important information. When you see "NOTE" in this document, please be aware that the information contained therein may be crucial for understanding, implementing, or operating related technologies or steps. We strongly recommend that you pay special attention to these "NOTE" sections while reading the document to ensure that you can use this technical documentation correctly and efficiently.
[...]	Brackets ([...]) enclosing a range of numbers after a pin name indicate all pins of the same type within that range. For instance, SDIO_DATA[0:3] denotes all four SDIO pins, namely: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

The module is an LTE wireless communication module with receiving diversity. It provides data connectivity on LTE-FDD, LTE-TDD, networks.

The module supports embedded operating systems such as Windows, Linux and Android. It also provides GNSS and voice functionality ¹ to meet specific application demands.

2.1. Frequency Bands and Functions

The following table shows the frequency bands and GNSS systems supported by the module. For details about CA combinations, see **document 1**.

Table 2: Frequency Bands and GNSS Types

Mode	LUK64-LD	LUK66-LD
LTE-FDD (with Rx-diversity)	B2/B4/B5/B7/B12/B13/B14/B25/ B26/B29 ² /B30/B66/B71	B2/B4/B5/B7/B12/B13/B14/B25/ B26/B29 ² /B30/B66/B71
LTE-TDD (with Rx-diversity)	B41/B48	B41/B48
LTE DL MIMO (with Rx-diversity)	B2/B4/B7/B25/B30/B41/B48/B66	B2/B4/B7/B25/B30/B41/B48/B66
GNSS ³	GPS, GLONASS, BDS, Galileo	GPS, GLONASS, BDS, Galileo

With a compact profile of 37.0 mm × 39.5 mm × 2.8 mm, the module is an SMD type module and can be embedded in applications through its 299 LGA pins.

2.2. Key Features

Table 3: Key Features

Feature	Details
Power Supply	- Supply voltage range: 3.3–4.4 V - Typical supply voltage: 3.8 V
Transmitting Power ⁴	Class 3 (23 dBm ±2 dB) for LTE bands
LTE Features	LUK64-LD: - Supports 3GPP Rel-12 Cat 6 LTE-FDD and LTE-TDD - Supports UL QPSK and 16QAM modulations - Supports DL QPSK, 16QAM and 64QAM modulations - Supports 1.4/3/5/10/15/20 MHz RF bandwidths - Supports MIMO in DL direction

¹ LUK64-LD and LUK66-LD modules contain **Data + Voice** version and **Data-only** version. **Data + Voice** version supports voice and data functions, while **Data-only** version only supports data function.

² LTE-FDD B29 supports Rx only and is only for secondary component carrier.

³ GNSS is optional.

⁴ B48 only supports 23 dBm +1/-2 dB.

	● LTE-FDD: Max. 300 Mbps (DL)/50 Mbps (UL) ● LTE-TDD: Max. 226 Mbps (DL)/28 Mbps (UL) LUK66-LD: ● Supports 3GPP Rel-12 Cat 12 LTE-FDD and LTE-TDD ● Supports UL QPSK, 16QAM and 64QAM modulations ● Supports DL QPSK, 16QAM, 64QAM and 256QAM modulations ● Supports 1.4/3/5/10/15/20 MHz RF bandwidths ● Supports MIMO in DL direction ● LTE-FDD: Max. 600 Mbps (DL)/150 Mbps (UL) ● LTE-TDD: Max. 430 Mbps (DL)/90 Mbps (UL)
Internet Protocol Features	Supports QMI/MBIM/NITZ/HTTP/HTTPS/FTP/LwM2M ^{dev} /PING ^{dev} protocols
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interfaces	● Supports (U)SIM card: 1.8/3.0 V ● Supports Dual (U)SIM Single Standby
eSIM ⁵	Optional
USB Interface	● Complies with USB 3.0 and 2.0 specifications, with max. transmission rates up to 5 Gbps on USB 3.0 and 480 Mbps on USB 2.0 ● Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output, and voice over USB ● Supports USB serial drivers: Windows 8.1/10/11, Linux 2.6–6.7, Android 4.x–14.x
UART Interfaces	Main UART interface: ● Used for AT command communication and data transmission ● Baud rate reaches up to 921600 bps, 115200 bps by default ● Supports RTS and CTS hardware flow control Debug UART interface: ● Used for Linux console and log output ● 115200 bps baud rate Bluetooth UART interface ^{dev}: ● Multiplexed from SPI ● Used for Bluetooth communication ● 115200 bps baud rate
SPI	● Works in master mode only ● Max. clock frequency rate: 50 MHz
Audio Features	● Provides one digital audio interface: PCM interface ● LTE: AMR/AMR-WB ● Supports echo cancellation and noise suppression
PCM Interface	● Used for audio function with an external codec or SLIC ● Supports 16-bit linear data format ● Supports long and short frame synchronization ● Supports master and slave modes, but the module must work as master in long frame synchronization
PCIe Interface ⁶	● Complies with <i>PCI Express Base Specification Revision 2.0</i> ● PCIe × 1, supporting 5 GT/s × 1 lane ● Used for data transmission ● RC mode only ● For WLAN, Ethernet functions
Antenna Interfaces	● ANT[0:3] ● ANT_GNSS ● 50 Ω characteristic impedance
Rx-diversity	Supports LTE Rx-diversity
GNSS Features	● Supports GPS, GLONASS, BDS, and Galileo ● Protocol: NMEA 0183 ● Data update rate: 1 Hz

⁵ The eSIM function of partial modules is not optional. For more details, please contact NetPrisma Technical Support.

⁶ Partial modules do not support PCIe interface. For more details, please contact NetPrisma Technical Support.

	● Supports AGNSS. For more details, see document 2.
AT Commands	● Complies with 3GPP TS 27.007 and 3GPP TS 27.005 ● NetPrisma enhanced AT commands
Network Indication	● NET_MODE ● NET_STATUS ● For network connectivity status indication
Physical Characteristics	● Dimensions: (37.0 ±0.2) mm × (39.5 ±0.2) mm × (2.8 ±0.2) mm ● Package: LGA ● Weight: approx. 9.1 g
Temperature Ranges	● Operating temperature range ⁷: -30 to +75 °C ● Extended temperature range ⁸: -40 to +85 °C ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	● USB 2.0 interface ● DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

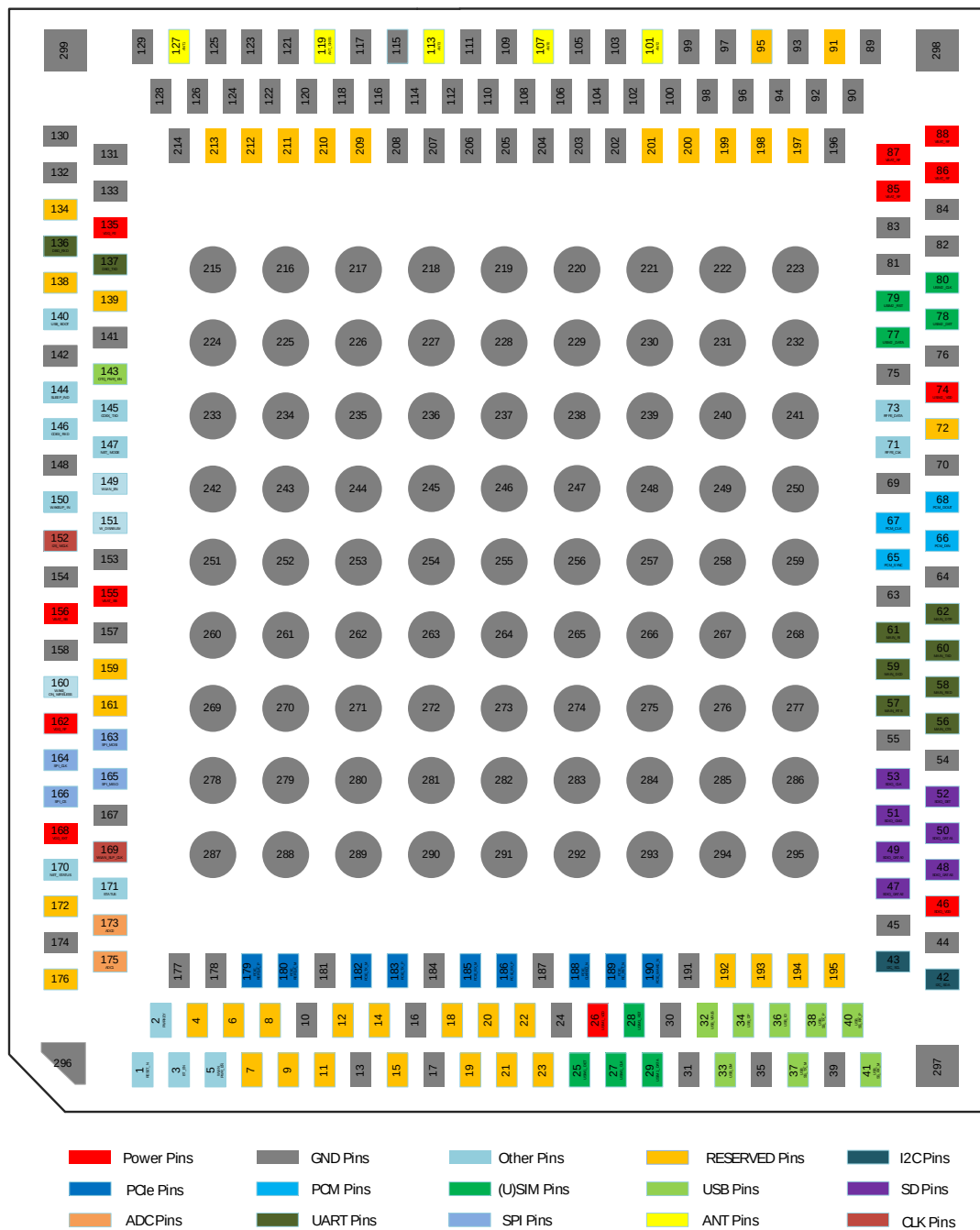
2.3. Pin Assignment

The following figure illustrates the pin assignment of the module.

⁷ To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

⁸ To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within the range of -40 to -30 °C or 75 to 85 °C, the module retains the ability to establish and maintain functions such as voice, SMS, emergency call ^{dev}, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

Figure 1: Pin Assignment (Top View)



NOTE

1. Keep all RESERVED pins and unused pins open.
2. GND pins should be connected to ground in the design.
3. Ensure that the pull-up power supply of the module's pins is VDD_EXT or controlled by VDD_EXT, and there is no current sink on the module's pins before the module turns on. For more details, contact NetPrisma Technical Support.

2.4. Pin Definitions

Table 4: Parameter Definition

Parameter	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 5: Pin Description

Power Supply					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VBAT_BB	155, 156	PI	Power supply for the module's baseband part	Vmax = 4.4 V Vmin = 3.3 V Vnom = 3.8 V	Sufficient current up to 1 A is requisite.
VBAT_RF	85–88	PI	Power supply for the module's RF part		A transmitting burst requires a sufficient current up to 1.2 A.
VDD_EXT	168	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V Iomax = 50 mA	A test point is recommended to be reserved.
VDD_RF	162	PO	Provide VDD for external RF circuit	Vnom = 2.7 V Iomax = 120 mA	If unused, keep it open.
GND	10, 13, 16, 17, 24, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76, 81–84, 89, 90, 92–94, 96–100, 102–106, 108–112, 114–118, 120–126, 128–133, 141, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191, 196, 202–208, 214–299				
Turn On/Off					
Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RESET_N	1	DI	Reset the module	VIHmin = 1.17 V VILmax = 0.54 V	Pulled up to 1.8 V internally. Active low. A test point is recommended to be reserved if unused.

PWRKEY	2	DI	Turn on/off the module		Pulled up to 1.8 V internally. Active low.
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Status Indication

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
NET_MODE	147	DO	Indicate the module's network registration mode	VDD_EXT	If unused, keep them open.
NET_STATUS	170	DO	Indicate the module's network activity status		
STATUS	171	DO	Indicate the module's operation status		
SLEEP_IND	144	DO	Indicate the module's sleep mode		

(U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USIM1_DET	25	DI	(U)SIM1 card hot-plug detect	VDD_EXT	If unused, keep it open.
USIM1_VDD	26	PO	(U)SIM1 card power supply	High-voltage: Vmax = 3.05 V Vnom = 2.85 V Vmin = 2.7 V Low-voltage: Vmax = 1.95 V Vnom = 1.8 V Vmin = 1.65 V	
USIM1_CLK	27	DO	(U)SIM1 card clock	USIM1_VDD	
USIM1_RST	28	DO	(U)SIM1 card reset		
USIM1_DATA	29	DIO	(U)SIM1 card data		
USIM2_VDD	74	PO	(U)SIM2 card power supply	High-voltage: Vmax = 3.05 V Vnom = 2.85 V Vmin = 2.7 V Low-Voltage: Vmax = 1.95 V Vnom = 1.8 V Vmin = 1.65 V	If (U)SIM2 interface is unused, keep it open.
USIM2_DATA	77	DIO	(U)SIM2 card data	USIM2_VDD	If (U)SIM2 interface is unused, keep these pins open.
USIM2_DET	78	DI	(U)SIM2 card detect	VDD_EXT	
USIM2_RST	79	DO	(U)SIM2 card reset	USIM2_VDD	
USIM2_CLK	80	DO	(U)SIM2 card clock		

USB Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
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USB_VBUS	32	AI	USB connection detect		Detection threshold: Vmin = 3.3 V Vnom = 5 V Vmax = 5.25 V A test point must be reserved.
USB_DM	33	AIO	USB 2.0 differential data (-)		USB 2.0 compliant. Require differential impedance of 90 Ω. Test points must be reserved.
USB_DP	34	AIO	USB 2.0 differential data (+)		
USB_SS_TX_M	37	AO	USB 3.0 super-speed transmit (-)		USB 3.0 compliant. Require differential impedance of 90 Ω.
USB_SS_TX_P	38	AO	USB 3.0 super-speed transmit (+)		
USB_SS_RX_P	40	AI	USB 3.0 super-speed receive (+)		
USB_SS_RX_M	41	AI	USB 3.0 super-speed receive (-)		
USB_ID ^{dev}	36	DI	USB ID detect	VDD_EXT	If unused, keep them open.
OTG_PWR_EN ^{dev}	143	DO	OTG power control		

SDIO Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VDD_P2	135	PI	Power input for SDIO interface		If a SD card is used, connect VDD_P2 to SDIO_VDD. If unused, connect VDD_P2 to VDD_EXT.
SDIO_VDD	46	PO	SD card application: SDIO pull up power supply	High-voltage: Vmax = 3.05 V Vnom = 2.85 V Vmin = 2.7 V Low-voltage: Vmax = 1.95 V Vnom = 1.8 V Vmin = 1.65 V	Cannot work as SD card power supply. SD card must be powered by an external power supply.
SDIO_DATA0	49	DIO	SDIO data bit 0	SDIO_VDD	If unused, keep them open.
SDIO_DATA1	50	DIO	SDIO data bit 1		
SDIO_DATA2	47	DIO	SDIO data bit 2		
SDIO_DATA3	48	DIO	SDIO data bit 3		
SDIO_CMD	51	DIO	SDIO command		
SDIO_CLK	53	DO	SDIO clock		
SDIO_DET	52	DI	SD card detect	VDD_EXT	If unused, keep it open.

Main UART Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
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MAIN_CTS	56	DO	Clear to send signal from the module	VDD_EXT	Connect to the MCU's CTS. If unused, keep it open.
MAIN_RTS	57	DI	Request to send signal to the module		Connect to the MCU's RTS. If unused, keep it open.
MAIN_RXD	58	DI	Main UART receive		
MAIN_DCD	59	DO	Main UART data carrier detect		If unused, keep them open.
MAIN_TXD	60	DO	Main UART transmit		
MAIN_RI	61	DO	Main UART ring indication		
MAIN_DTR	62	DI	Main UART data terminal ready		Pulled up by default. Pulling low will awaken the module. If unused, keep it open. Sleep mode control.

Debug UART Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
DBG_RXD	136	DI	Debug UART receive	VDD_EXT	Test points must be reserved.
DBG_TXD	137	DO	Debug UART transmit		

SPI

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SPI_MOSI	163	DO	SPI master-out slave-in	VDD_EXT	If unused, keep it open. It can be multiplexed into BT_TXD ^{dev} .
SPI_CLK	164	DO	SPI clock		If unused, keep it open. It can be multiplexed into BT_CTS ^{dev} .
SPI_MISO	165	DI	SPI master-in slave-out		If unused, keep it open. It can be multiplexed into BT_RXD ^{dev} .
SPI_CS	166	DO	SPI chip select		If unused, keep it open. It can be multiplexed into BT_RTS ^{dev} .

PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
I2C_SDA	42	OD	I2C serial data (for an external codec)	VDD_EXT	An external pull-up resistor is requisite. If unused, keep them open.
I2C_SCL	43	OD	I2C serial clock (for an external codec)		
PCM_SYNC	65	DIO	PCM data frame sync		Output signal in master mode. Input signal in slave mode. If unused, keep it open.
PCM_DIN	66	DI	PCM data input		If unused, keep it open.

PCM_CLK	67	DIO	PCM clock		Output signal in master mode. Input signal in slave mode. If unused, keep it open.
PCM_DOUT	68	DO	PCM data output		If unused, keep it open.
I2S_MCLK	152	DO	Clock output for codec		Provide a digital clock output for an external codec. If unused, keep it open.

Antenna Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ANT0	107	AIO	Main antenna interface		
ANT1	127	AI	Rx-diversity antenna interface		
ANT2	101	AI	MIMO antenna interface		50 Ω characteristic impedance.
ANT3	113	AI			
ANT_GNSS	119	AI	GNSS antenna interface		

WLAN Control Interface^{dev}

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
WLAN_PWR_EN	5	DO	WLAN power supply enable control		
COEX_TXD	145	DO	LTE/WLAN coexistence transmit	VDD_EXT	If unused, keep them open.
COEX_RXD	146	DI	LTE/WLAN coexistence receive		
WLAN_EN	149	DO	WLAN function enable control		Active high. If unused, keep it open.
WAKE_ON_WIRELESS	160	DI	Awaken the host (the module) via an external Wi-Fi module		Active low. If unused, keep it open.
WLAN_SLP_CLK	169	DO	WLAN sleep clock		If unused, keep it open.

ADC Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ADC0	173	AI	General-purpose ADC interface	0–1.875 V	If unused, keep them open.
ADC1	175	AI			

PCIe Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
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PCIE_REFCLK_P	179	AO	PCie reference clock (+)		
PCIE_REFCLK_M	180	AO	PCie reference clock (-)		
PCIE_TX_M	182	AO	PCie transmit (-)		Require differential impedance of 85 Ω. If unused, keep them open.
PCIE_TX_P	183	AO	PCie transmit (+)		
PCIE_RX_M	185	AI	PCie receive (-)		
PCIE_RX_P	186	AI	PCie receive (+)		
PCIE_CLKREQ_N	188	DI	PCie clock request		Input signal in master mode. If unused, keep it open.
PCIE_RC_RST_N	189	DO	PCie RC reset	VDD_EXT	Output signal in master mode. If unused, keep it open.
PCIE_WAKE_N	190	DI	PCie awake		Input signal, in master mode only. If unused, keep it open.

Antenna Tuner Control Interfaces^{dev} (RFFE Interface)

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RFFE_CLK	71	DO	Used for external MIPI IC control	VDD_EXT	If unused, keep them open.
RFFE_DATA	73	DIO	Used for external MIPI IC control		

Other Pins

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_BOOT	140	DI	Force the module into download mode	VDD_EXT	Active high. A test point is recommended to be reserved.
BT_EN ^{dev}	3	DO	Bluetooth function enable control		If unused, keep it open.
WAKEUP_IN	150	DI	Wake up the module		Pulled up by default. Low level awakens the module. If unused, keep it open.
W_DISABLE#	151	DI	Airplane mode control		Pulled up by default. In low level, the module will enter airplane mode. If unused, keep it open.

RESERVED Pins

Pin Name	Pin No.	Comment
RESERVED	4, 6–9, 11, 12, 14, 15, 18–23, 72, 91, 95, 134, 138, 139, 159, 161, 172, 176, 192–195, 197–201, 209–213	Keep these pins open.

3 Operating Characteristics

3.1. Operating Modes

Table 6: Overview of Operating Modes

Mode	Details
Full Functionality Mode	Idle Software is active. The module has registered on the network, and it is ready to send and receive data.
	Voice/Data Network is connected. In this mode, the power consumption is decided by network setting and data transmission rate.
Minimum Functionality Mode	AT+CFUN=0 sets the module to minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card are invalid.
Airplane Mode	AT+CFUN=4 or driving W_DISABLE# low will set the module to airplane mode. In this case, the RF function is invalid.
Sleep Mode	When AT+QSCLK=1 is executed and the host's USB bus enters Suspend state, the module will enter sleep mode. The module keeps receiving paging messages, SMS, voice call and TCP/UDP data from the network with its power consumption reducing to the minimal level.
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is inactive, all application interfaces are inaccessible, and the operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.

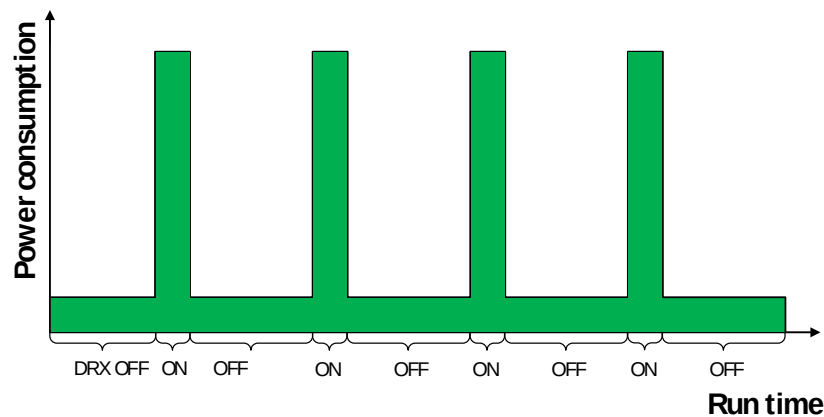
NOTE

See **document 3** for details about **AT+CFUN=0**, **AT+CFUN=4** and **AT+QSCLK=1**.

3.1.1. Sleep Mode

DRX can reduce the current power consumption of the module to an ultra-low level during sleep mode, and DRX cycle index values are broadcasted by the wireless network. The figure below shows the relationship between the DRX run time and the current power consumption in sleep mode. The longer the DRX cycle is, the lower the power consumption will be.

Figure 2: Module Power Consumption in Sleep Mode



NOTE

DRX cycle values are transmitted over the wireless network.

The following part of this section presents the power saving procedure and sleep mode of the module.

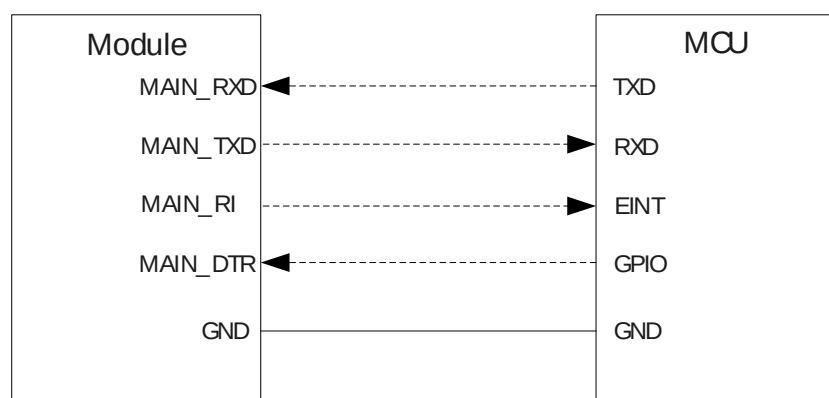
3.1.1.1. UART Application

If the MCU communicates with the module via UART interfaces, the following two conditions must be met simultaneously to bring the module into sleep mode.

- Execute **AT+QSCCLK=1**.
- Drive MAIN_DTR high.

The following figure shows the connection between the module and the MCU.

Figure 3: Sleep Mode Application via UART Interfaces



Driving MAIN_DTR low will wake up the module. When the module has a URC to report, MAIN_RI signal will wake up the host. See **Chapter 4.8** for details about MAIN_RI behavior.

3.1.1.2. USB Application

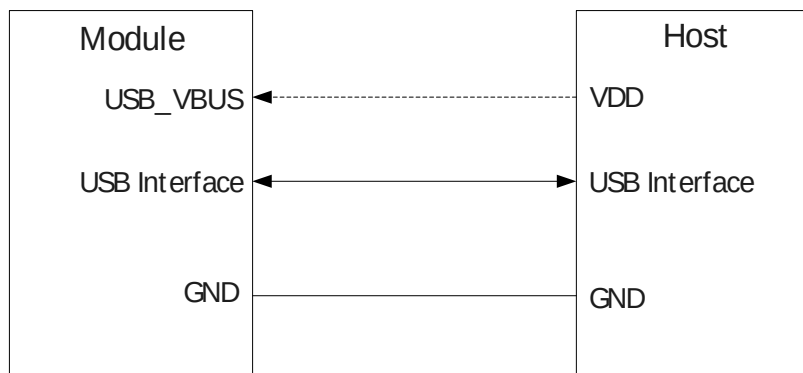
USB application can be applied with USB remote wake-up function or USB Suspend/Resume and RI functions.

If the host supports USB Suspend/Resume and remote wake-up function, meeting the following three requirements will bring the module into sleep mode.

- Execute **AT+QSCLK=1**.
- Keep MAIN_DTR high (pulled up by default).
- The host's USB bus, connected to the module's USB interface, has entered Suspend state.

The following figure shows the above-mentioned connection between the module and the host.

Figure 4: Sleep Mode Application with USB Remote Wake-up



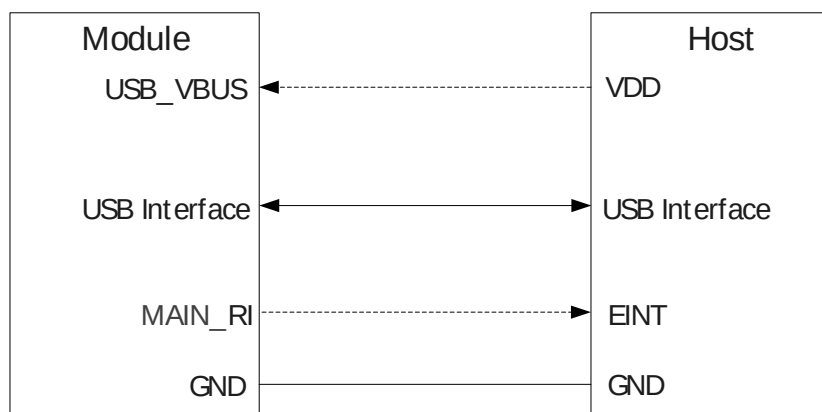
Sending data to the module through USB will wake up the module. When the module has a URC to report, the module will send remote wake-up signals via USB bus to awaken the host.

If the host supports USB Suspend/Resume but does not support remote wake-up function, meeting the following three requirements will bring the module into sleep mode.

- Execute **AT+QSCLK=1**.
- Keep MAIN_DTR high (pulled up by default).
- The host's USB bus, connected with the module's USB interface, has entered Suspend state.

The following figure shows the connection between the module and the host.

Figure 5: Sleep Mode Application with Suspend function



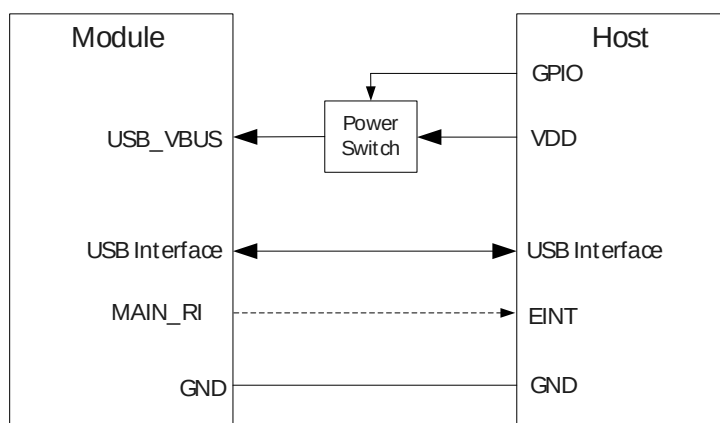
Sending data to the module through USB will awaken the module. When the module has a URC to report, MAIN_RI will wake up the host.

If the host does not support USB Suspend function, USB_VBUS should be disconnected with an external control circuit to bring the module into sleep mode.

- Execute **AT+QSCLK=1**.
- Keep MAIN_DTR high (pulled up by default).
- Disconnect USB_VBUS.

The following figure shows the above-mentioned connection between the module and the host.

Figure 6: Sleep Mode Application without Suspend Function



To awaken the module, power USB_VBUS by turning on the power switch.

NOTE

Pay attention to the level match shown in dotted line between the module and the MCU/host.

3.1.2. Airplane Mode

The module provides W_DISABLE# to disable or enable airplane mode via hardware operation. W_DISABLE# is pulled up by default. Driving it low will bring the module into airplane mode.

Table 7: Pin Description of W_DISABLE#

Pin Name	Pin No.	I/O	Description	Comment
W_DISABLE#	151	DI	Airplane mode control	Pulled up by default. In low level, the module will enter airplane mode. If unused, keep it open.

In airplane mode, the RF function is disabled by default, but it can also be enabled or disabled through AT commands. The following table shows the RF function status of the module.

Table 8: RF Function Status

W_DISABLE# Logic Level	AT Command	RF Function Status	Operating Modes
---------------------------	------------	--------------------	-----------------

High Level	AT+CFUN=1	Enable	Full functionality mode
	AT+CFUN=0	Disable	Minimum functionality mode
	AT+CFUN=4	Disable	Airplane mode
Low Level	AT+CFUN=0 AT+CFUN=1 AT+CFUN=4	Disable	Airplane mode

NOTE

1. W_DISABLE# for airplane mode control function is disabled by default.
2. The execution of **AT+CFUN** will not affect GNSS function.
3. See **document 3** for details about related AT commands mentioned in the above table.

3.2. Power Supply

3.2.1. Power Supply Pins

The module provides six VBAT pins dedicated to the connection to an external power supply. There are two separate voltage domains for VBAT.

- Four VBAT_RF pins for module's RF part.
- Two VBAT_BB pins for module's baseband part.

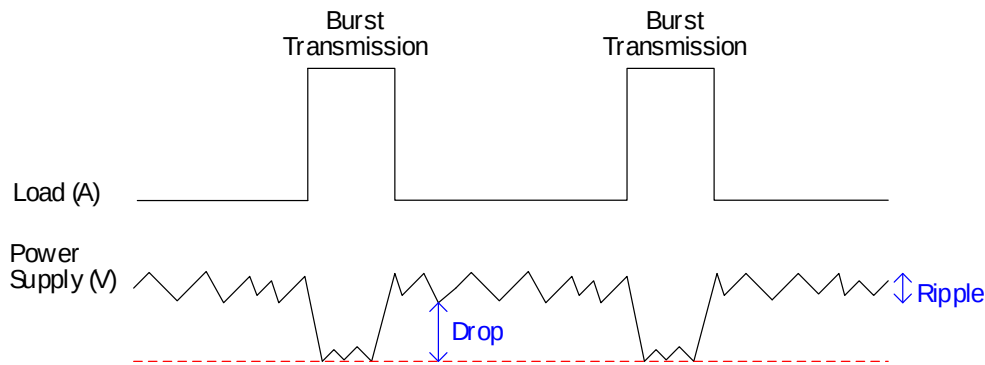
The following table shows details of VBAT pins and ground pins.

Table 9: VBAT and GND Pins

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT_RF	85–88	PI	Power supply for the module's RF part	3.3	3.8	4.4	V
VBAT_BB	155, 156	PI	Power supply for the module's baseband part	3.3	3.8	4.4	V
GND	10, 13, 16, 17, 24, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76, 81–84, 89, 90, 92–94, 96–100, 102–106, 108–112, 114–118, 120–126, 128–133, 141, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191, 196, 202–208, 214–299						

The power supply of the module ranges from 3.3 V to 4.4 V. Make sure the input voltage never drops below 3.3 V, otherwise the module will be turned off automatically. The following figure shows the voltage drop during Tx power in 4G networks.

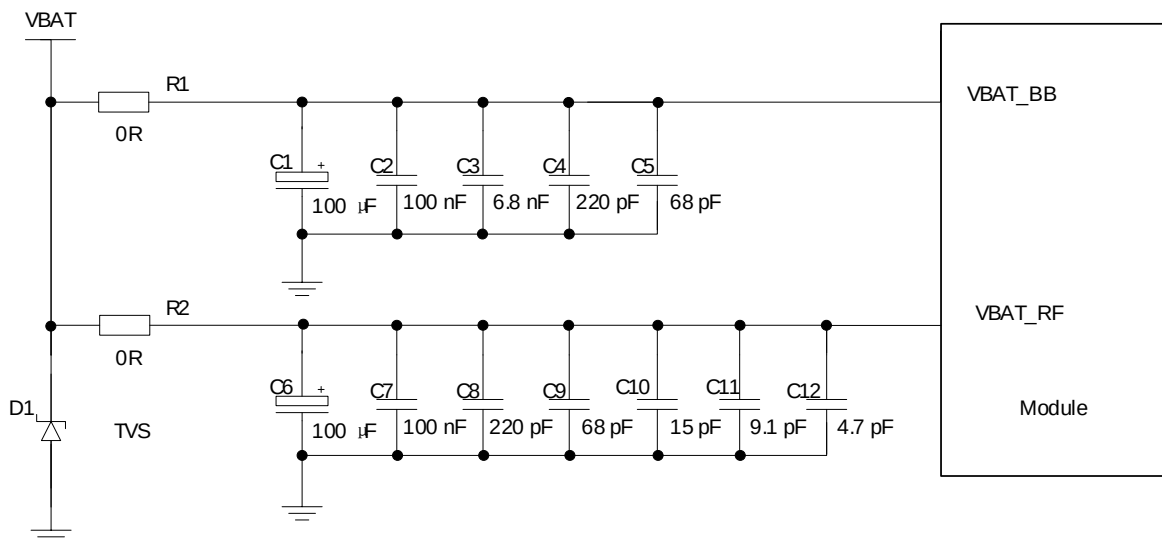
Figure 7: Power Supply Limits during Burst Transmission



To decrease the voltage drop, use a bypass capacitor of about 100 μF with low ESR and reserve a multi-layer ceramic chip (MLCC) capacitor array with ultra-low ESR for VBAT_BB/RF. It is recommended to adopt ceramic capacitors for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application must be a single voltage source which can be expanded to two sub paths with star structure. The width of VBAT_BB trace and VBAT_RF trace should be at least 1 mm and 2 mm respectively. In principle, the longer the VBAT trace is, the wider it should be.

In addition, for stable power supply, it is necessary to add a high-power TVS near VBAT_BB and VBAT_RF. The star structure of the power supply is shown below.

Figure 8: Star Structure of the Power Supply

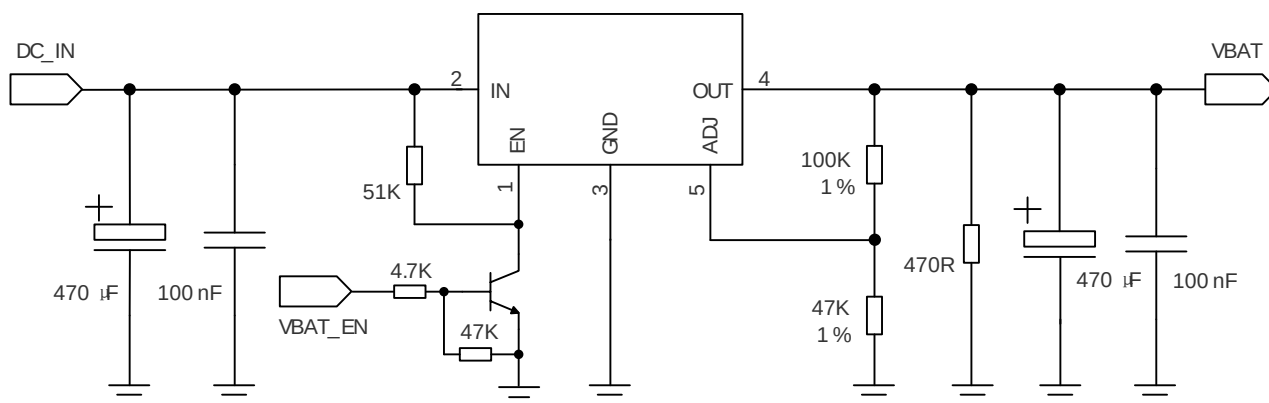


3.2.2. Reference Design for Power Supply

The performance of the module largely depends on the power supply design. The continuous current of the power supply should be at least 2.0 A and the peak current should be at least 3.0 A.

The following figure shows a reference design for +5 V input power source. In this design, the typical power supply output is about 3.8 V.

Figure 9: Reference Circuit of Power Supply



NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut off the power supply.

3.2.3. Power Supply Voltage Monitoring

AT+CBC can monitor the VBAT_BB voltage value. See **document 3** for details.

3.3. Turn On

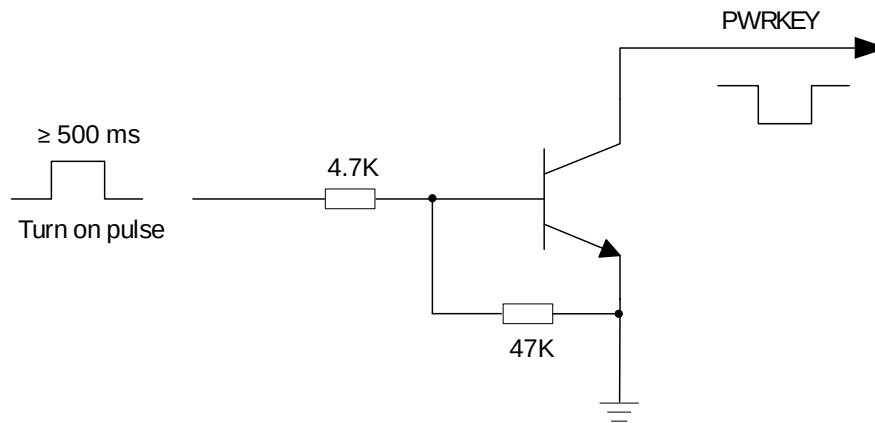
The module can be turned on via PWRKEY.

Table 10: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	2	DI	Turn on/off the module	Pulled up internally. Active low.

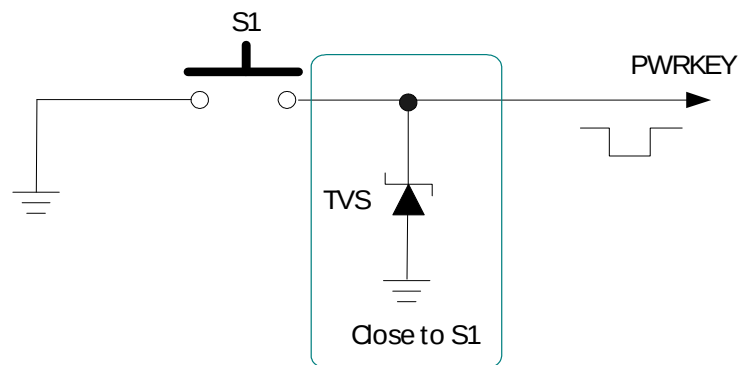
When the module is in turn-off mode, it can be turned on by driving PWRKEY low for at least 500 ms. It is recommended to control PWRKEY with an open drain/collector driver. After STATUS outputs a high level, PWRKEY can be released. A simple reference circuit is shown below.

Figure 10: Turn on the Module with a Driving Circuit



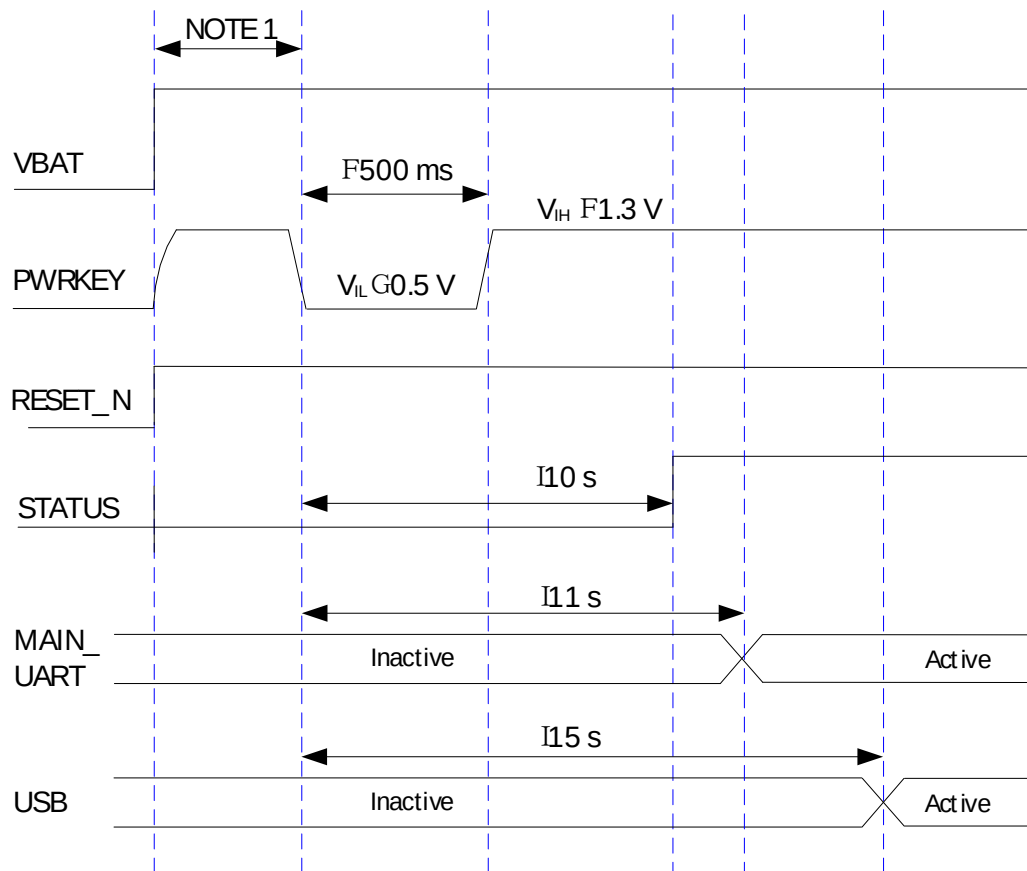
The other way to control the PWRKEY is using a button directly. When you are pressing the button, electrostatic strike may be generated from fingers. Therefore, it is necessary to place a TVS component nearby the button for ESD protection. A reference circuit is shown in the following figure.

Figure 11: Turn on the Module with a Button



The turn-on timing is illustrated in the following figure.

Figure 12: Turn-on Timing



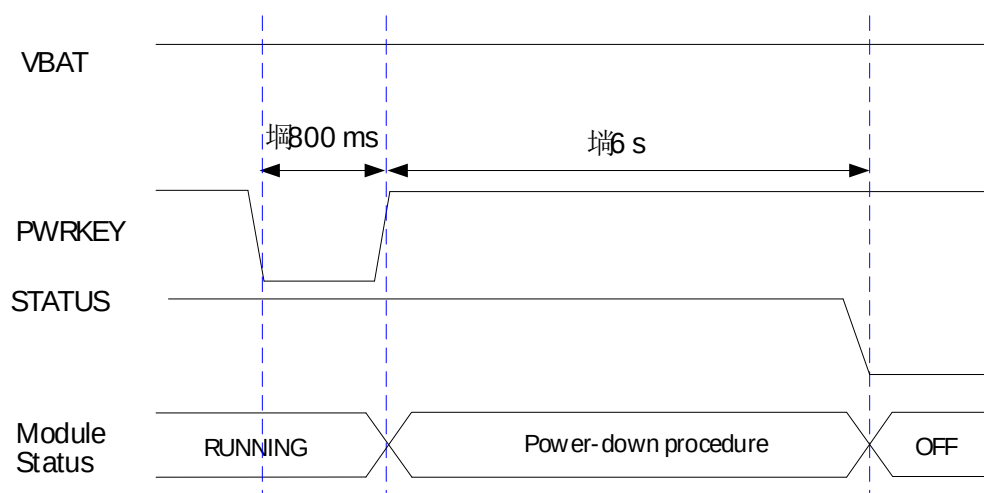
3.4. Turn Off

The module can be turned off normally via two methods: using PWRKEY or executing **AT+QPOWD**. See **document 3** for details about the AT command.

3.4.1. Turn Off with PWRKEY

Driving PWRKEY low for at least 800 ms, the module will execute the power-down procedure after PWRKEY is released. The turn-off timing is illustrated in the following figure.

Figure 13: Turn-off Timing



3.4.2. Turn Off with AT Command

It is also a safe method to turn off the module via **AT+QPOWD**. When turning off the module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on automatically again after a successful turn-off. See **document 3** for details about the AT command.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.
2. When turning off module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on automatically again after successful turn-off.

3.5. Reset

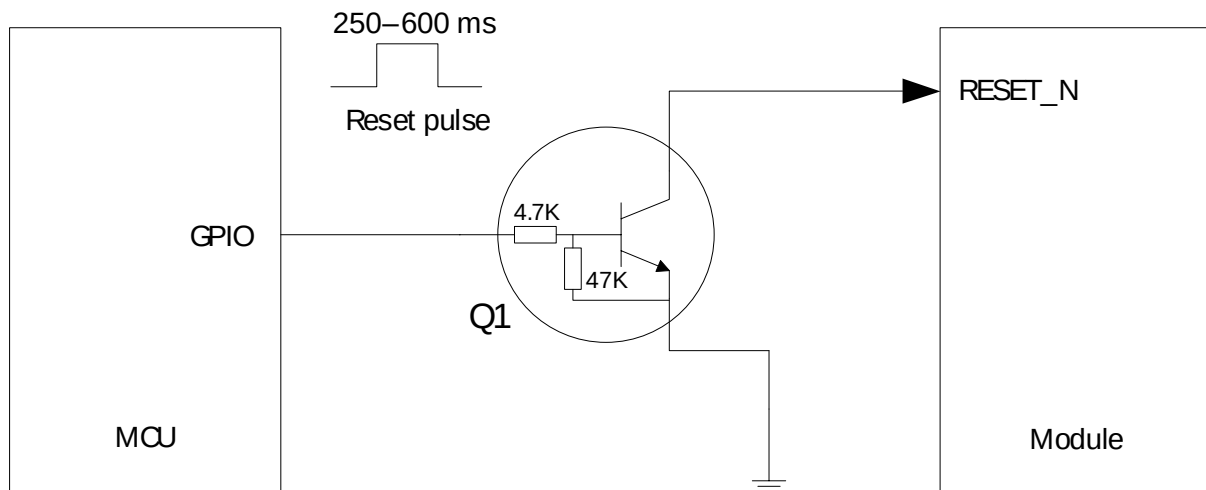
The module can be reset by driving RESET_N low for 250–600 ms and then releasing it.

Table 11: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	1	DI	Reset the module	Pulled up internally. Active low. A test point is recommended to be reserved if unused.

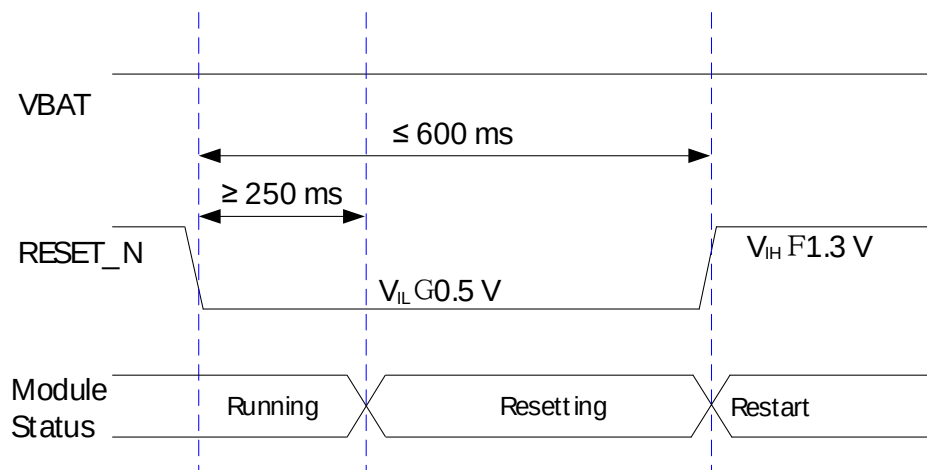
The recommended circuit is similar to the PWRKEY control circuit. You can use an open drain/collector driver or a button to control RESET_N.

Figure 14: Reference Circuit of RESET_N with a Driving Circuit



The reset timing is illustrated in the following figure.

Figure 15: Reset Timing



NOTE

1. RESET_N is internally pulled up to 1.8 V with a 40 kΩ resistor.
2. Use RESET_N only when you fail to turn off the module with the **AT+QPOWD** and PWRKEY.
3. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

4 Application Interfaces

The module is designed with 299 LGA pins that can be connected to cellular application platform. This chapter mainly describes the following application interfaces and indication signals of the module:

- (U)SIM interfaces
- USB interface
- UART interfaces
- SPI ⁹
- PCM and I2C interfaces
- ADC interfaces
- Network status indication
- Module status indication
- RI
- PCIe interface
- SDIO interface
- Antenna tuner control interfaces ^{dev}
- USB_BOOT interface

4.1. (U)SIM Interfaces

The module provides two (U)SIM interfaces. The circuitry of (U)SIM interfaces meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported, and Dual SIM Single Standby function is supported. (U)SIM card hot-plug is enabled by **AT+QUIMSL0T**. See **document 3** for details about the AT command.

Table 12: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_DET	25	DI	USIM1 card hot-plug detect	If unused, keep it open.
USIM1_VDD	26	PO	USIM1 card power supply	
USIM1_CLK	27	DO	USIM1 card clock	
USIM1_RST	28	DO	USIM1 card reset	

⁹ SPI can be multiplexed as Bluetooth UART interface ^{dev}.

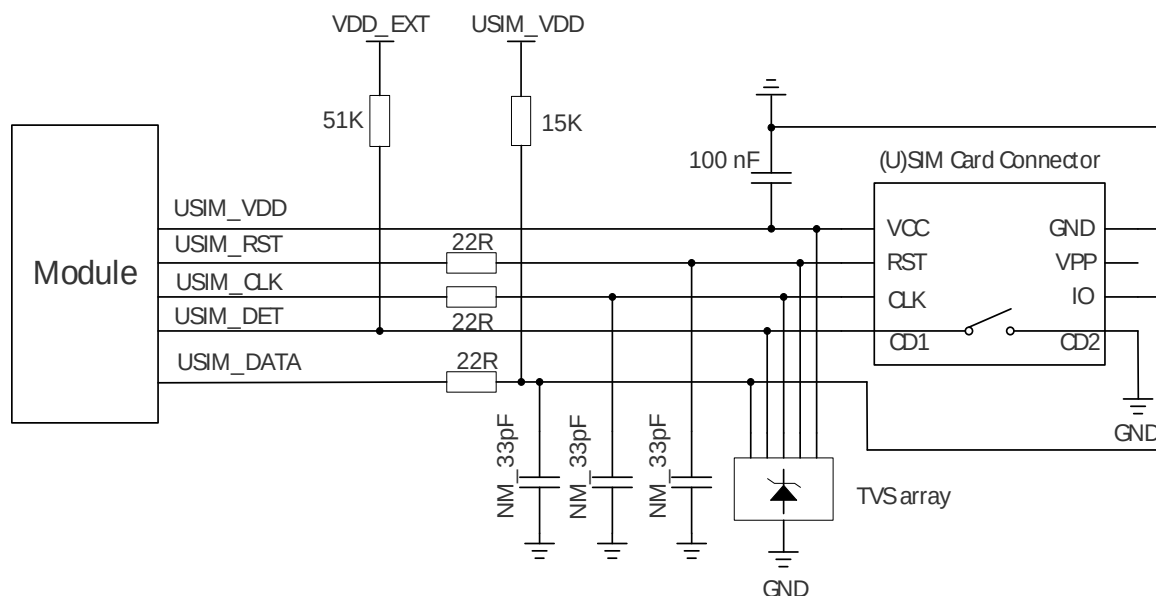
USIM1_DATA	29	DIO	USIM1 card data
USIM2_VDD	74	PO	USIM2 card power supply
USIM2_DATA	77	DIO	USIM2 card data
USIM2_DET	78	DI	USIM2 card hot-plug detect
USIM2_RST	79	DO	USIM2 card reset
USIM2_CLK	80	DO	USIM2 card clock

If USIM2 interface is unused, keep them open.

The module supports (U)SIM card hot-plug via USIM_DET pins, and both high and low level detection are supported. The function is disabled by default, and see **AT+QSIMDET** in **document 3** for more details.

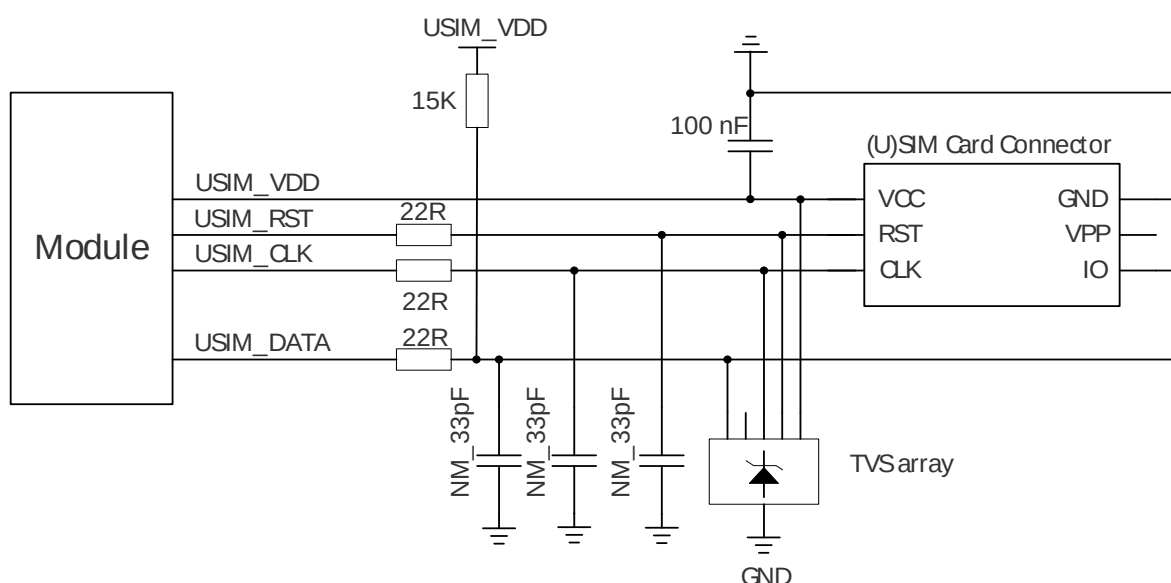
The following figure shows a reference design for (U)SIM interfaces with an 8-pin (U)SIM card connector.

Figure 16: Reference Circuit of (U)SIM Interfaces with an 8-Pin (U)SIM Card Connector



If (U)SIM card detection function is unnecessary, keep USIM_DET open. A reference circuit for (U)SIM interfaces with a 6-pin (U)SIM card connector is illustrated in the following figure.

Figure 17: Reference Circuit of (U)SIM Interfaces with a 6-Pin (U)SIM Card Connector



For better reliability and availability of the (U)SIM card in applications, follow the criteria below in the (U)SIM circuit design:

- Put the (U)SIM card connector as close as possible to the module. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Make sure the ground between the module and the (U)SIM card connector is short and wide. Keep the trace width of ground and USIM_VDD not less than 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- For better ESD protection, it is recommended to add an ESD protection component of which parasitic capacitance should be less than 50 pF. 22 Ω resistors should be added in series between the module and the (U)SIM card connector to facilitate debugging. The (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability with the application of long layout trace and sensitive occasions, and it should be close to the (U)SIM card connector.

4.2. USB Interface

The module provides one integrated USB (Universal Serial Bus) interface which complies with the USB 3.0 and 2.0 specifications and supports SuperSpeed (5 Gbps) mode on USB 3.0 and high-speed (480 Mbps) and full-speed (12 Mbps) modes on USB 2.0. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade, and voice over USB.

Table 13: Pin Definition of USB Interface

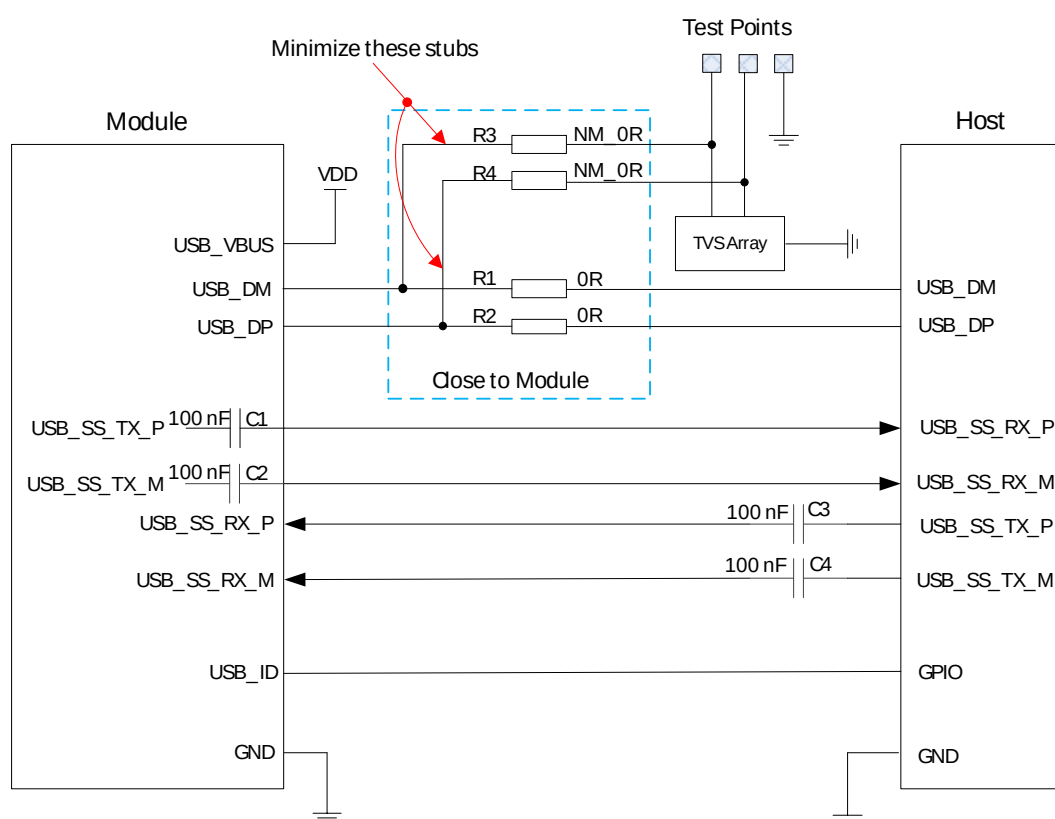
Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	32	DI	USB connection detect	Typical 5.0 V A test point must be reserved.
USB_DP	34	AIO	USB 2.0 differential data (+)	USB 2.0 compliant.

USB_DM	33	AIO	USB 2.0 differential data (-)	Require differential impedance of 90 Ω . Test points must be reserved.
USB_SS_TX_M	37	AO	USB 3.0 super-speed transmit (-)	USB 3.0 compliant. Require differential impedance of 90 Ω .
USB_SS_TX_P	38	AO	USB 3.0 super-speed transmit (+)	
USB_SS_RX_P	40	AI	USB 3.0 super-speed receive (+)	
USB_SS_RX_M	41	AI	USB 3.0 super-speed receive (-)	
USB_ID ^{dev}	36	DI	USB ID detect	If unused, keep it open.
OTG_PWR_EN ^{dev}	143	DO	OTG power control	

For more details about the USB 2.0 and USB 3.0 specifications, visit <http://www.usb.org/home>.

The USB 2.0 interface must be reserved for firmware upgrade in your designs. The following figure shows a reference circuit of USB 2.0 and USB 3.0 interfaces.

Figure 18: Reference Circuit of USB Application



To ensure the signal integrity of USB data traces, C1, and C2 have already been integrated in the module; C3 and C4 must be placed close to the host; and R1 to R4 should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles of USB interface should be followed during USB interface design to meet USB 2.0 and USB 3.0 specifications.

- Route the USB 2.0 and USB 3.0 signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω .

- For USB 2.0 signal traces, the trace should be shorter than 120 mm, and the differential data pair matching should be less than 2 mm. For USB 3.0 signal traces, the maximum length of each differential data pair (Tx/Rx) is recommended to be less than 100 mm, and each differential data pair matching should be less than 0.7 mm. While the matching between Tx and Rx should be less than 15.24 mm.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. It is vital to route the USB differential traces in inner-layers of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- If a USB connector is used, keep the ESD protection components as close to the USB connector as possible.
- Pay attention to the selection of the ESD protection component since the component's junction capacitance may cause influences on USB data traces. Typically, the stray capacitance should be less than 2.0 pF for USB 2.0, and less than 0.4 pF for USB 3.0.
- If possible, reserve a 0 Ω resistor on USB_DP and USB_DM traces respectively.

Table 14: USB Trace Length Inside the Module

Pin No.	Pin Name	Length (mm)	Length Difference (P-M) (mm)
34	USB_DP	16.02	0.32
33	USB_DM	16.34	
37	USB_SS_TX_M	20.57	0.36
38	USB_SS_TX_P	20.21	
40	USB_SS_RX_P	19.62	0.16
41	USB_SS_RX_M	19.46	

4.3. UART Interfaces

The module provides three UART interfaces: one main UART interface, one debug UART interface, and one Bluetooth UART interface^{dev} (multiplexed from SPI). Features of these interfaces are shown as below:

- Main UART interface supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps (default), 230400 bps, 460800 bps and 921600 bps baud rates. This interface is used for data transmission and AT command communication.
- Debug UART interface supports 115200 bps baud rate. It is used for Linux console and log output.
- Bluetooth UART interface supports 115200 bps baud rate. It is used for Bluetooth communication and can be multiplexed from SPI.

4.3.1. Main UART Interface

Table 15: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	56	DO	Clear to send signal from the module	Connect to the MCU's CTS. If unused, keep it open.
MAIN_RTS	57	DI	Request to send signal to the module	Connect to the MCU's RTS.

				If unused, keep it open.
MAIN_RXD	58	DI	Main UART receive	If unused, keep them open.
MAIN_DCD	59	DO	Main UART data carrier detect	
MAIN_TXD	60	DO	Main UART transmit	
MAIN_RI	61	DO	Main UART ring indication	
MAIN_DTR	62	DI	Main UART data terminal ready	Pulled up by default. Pulling low will awaken the module. If unused, keep it open. Sleep mode control.

4.3.2. Debug UART Interface

Table 16: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	136	DI	Debug UART receive	Test points must be reserved.
DBG_TXD	137	DO	Debug UART transmit	

4.3.3. Bluetooth UART Interface^{dev}

The module provides one Bluetooth UART interface multiplexed from SPI. The following table shows the pin definition of Bluetooth UART interface.

Table 17: Pin Definition of Bluetooth UART Interface

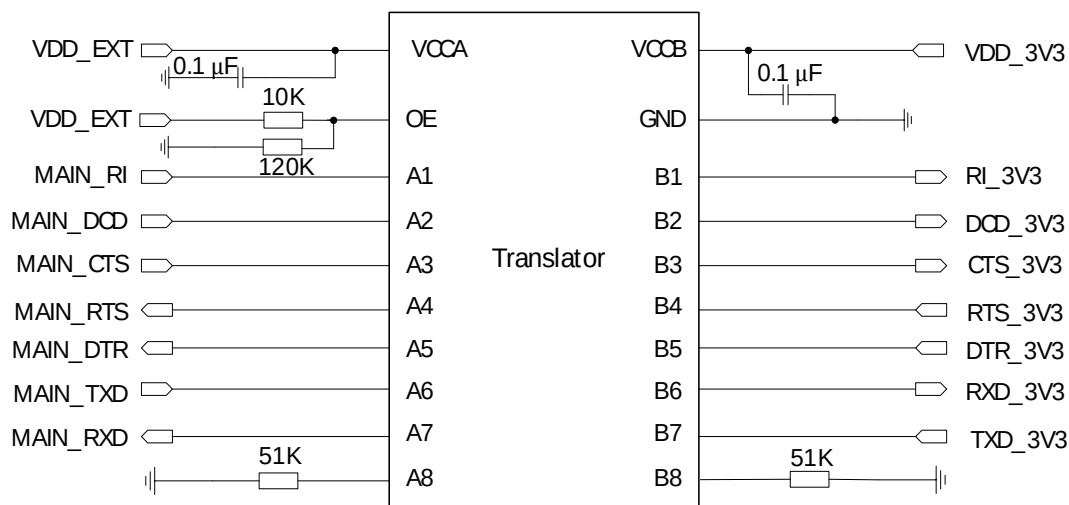
Pin Name	Pin No.	Multiplexed Function	I/O	Description	Comment
BT_EN	3	-	DO	Bluetooth function enable control	If unused, keep it open.
SPI_MOSI	163	BT_TXD	DO	Bluetooth UART transmit	Connect to the Wi-Fi&Bluetooth module's CTS. If unused, keep it open.
SPI_CLK	164	BT_CTS	DO	Clear to send signal from the module	
SPI_MISO	165	BT_RXD	DI	Bluetooth UART receive	Connect to the Wi-Fi&Bluetooth module's RTS. If unused, keep it open.
SPI_CS	166	BT_RTS	DO	Request to send signal to the module	

4.3.4. UART Application

The module provides 1.8 V UART interfaces. A level-shifting circuit should be used if the application is equipped with a 3.3 V UART interface. A voltage-level translator TXS0108EPWR provided by Texas

Instruments is recommended. The following figure shows a reference design.

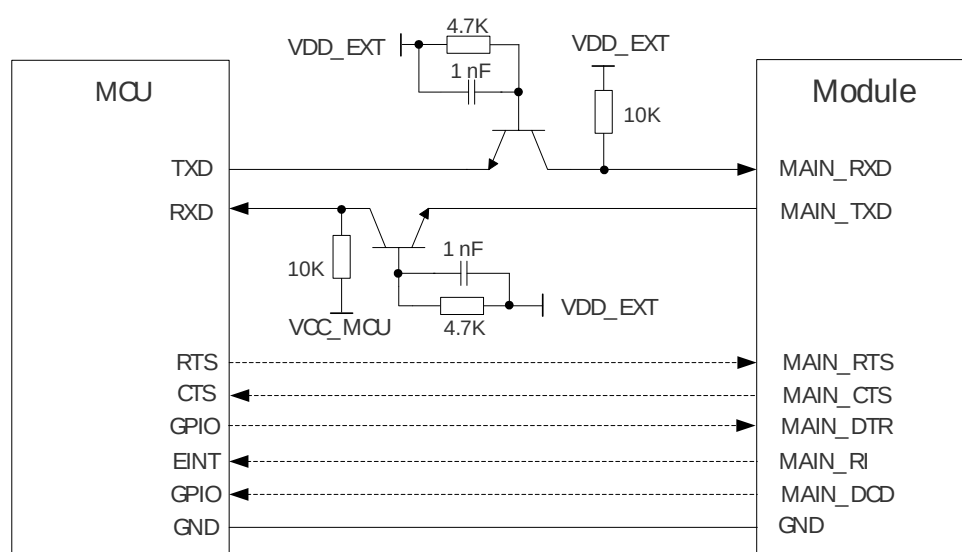
Figure 19: Reference Circuit (IC Solution) (Main UART)



Please visit <http://www.ti.com> for more information.

Another example with a transistor circuit is shown below. For the design of circuits shown in dotted lines, refer to that shown in solid lines, but pay attention to the direction of the connection.

Figure 20: Reference Circuit (Transistor Solution) (Main UART)



NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates over 460 kbps.
2. Please note that the module's CTS is connected to the MCU/Wi-Fi&Bluetooth module's CTS, and the module's RTS is connected to the MCU/Wi-Fi&Bluetooth module's RTS.
3. The level-shifting circuits (**Figure 19** and **Figure 20**) take the main UART as an example. The circuits of the debug UART and the Bluetooth UART are connected in the same way as the main UART, but the Bluetooth UART is connected to the Wi-Fi&Bluetooth module.

4.4. SPI

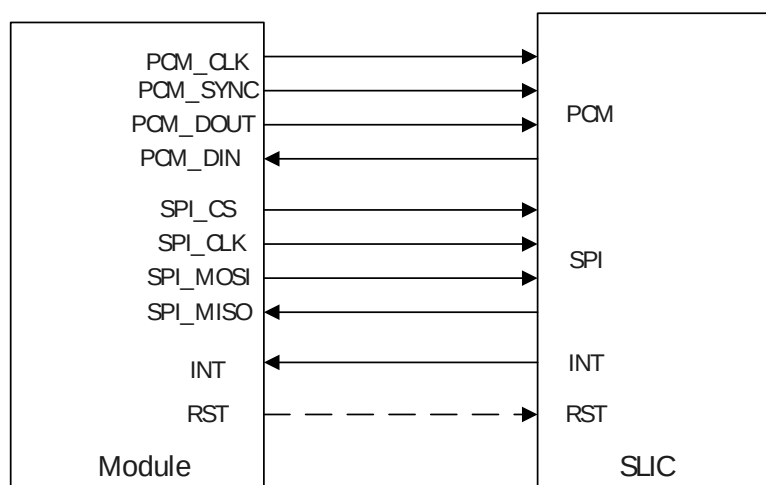
The module provides one SPI which only supports master mode with a maximum clock frequency up to 50 MHz.

Table 18: Pin Definition of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI_MOSI	163	DO	SPI master output slave input	Master mode only.
SPI_CLK	164	DO	SPI clock	
SPI_MISO	165	DI	SPI master input slave output	
SPI_CS	166	DO	SPI chip select	

The following figure shows a reference design of PCM interface and SPI with an external SLIC IC. The dotted line in the figure below means an optional connection since some SLIC ICs need RST while some do not.

Figure 21: Reference Circuit of PCM and SPI Application with SLIC



4.5. PCM and I2C Interfaces

The module supports audio communication via PCM (Pulse Code Modulation) digital interface and I2C interfaces. The PCM interface supports the following modes:

- Primary mode (short frame synchronization): the module works as both master and slave.
- Auxiliary mode (long frame synchronization): the module works as master only.

In primary mode, the data is sampled on the falling edge of PCM_CLK and transmitted on the rising edge. The falling edge of PCM_SYNC represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The rising edge of PCM_SYNC represents the MSB. In this mode, the PCM interface operates with 256 kHz PCM_CLK and 8 kHz, 50 % duty cycle PCM_SYNC only.

The module supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

Figure 22: Primary Mode Timing

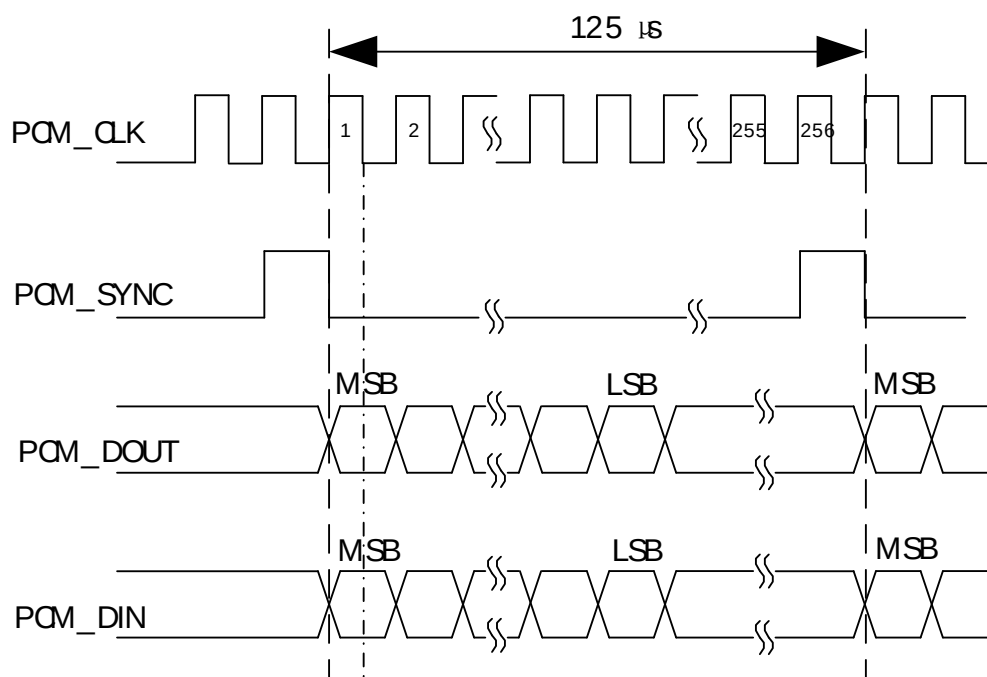
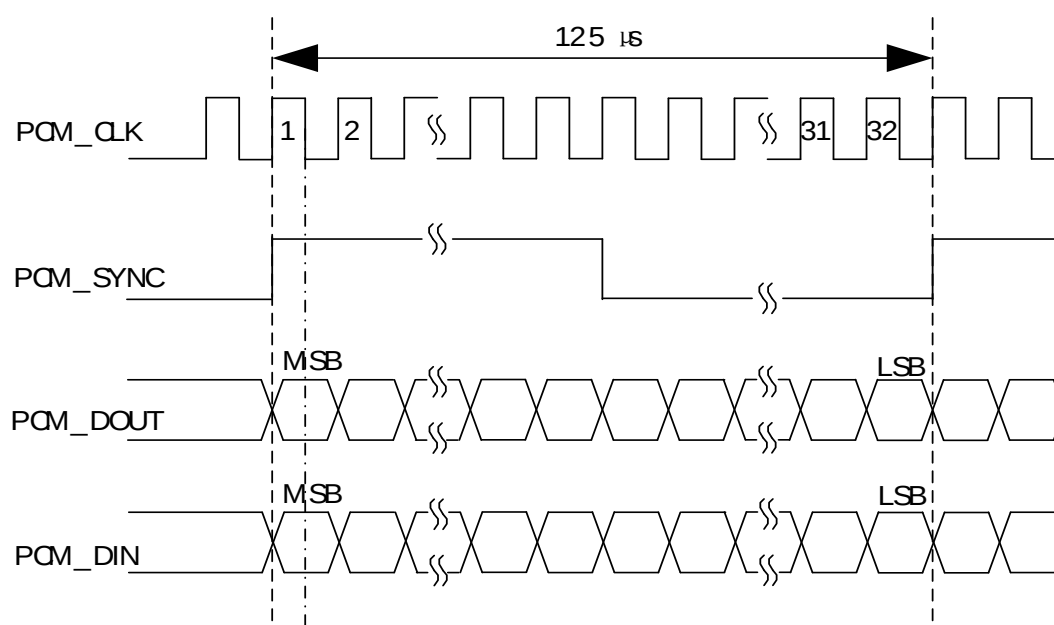


Figure 23: Auxiliary Mode Timing



The following table shows the pin definition of the PCM interface and I2C interface, both of which can be applied to audio codec design.

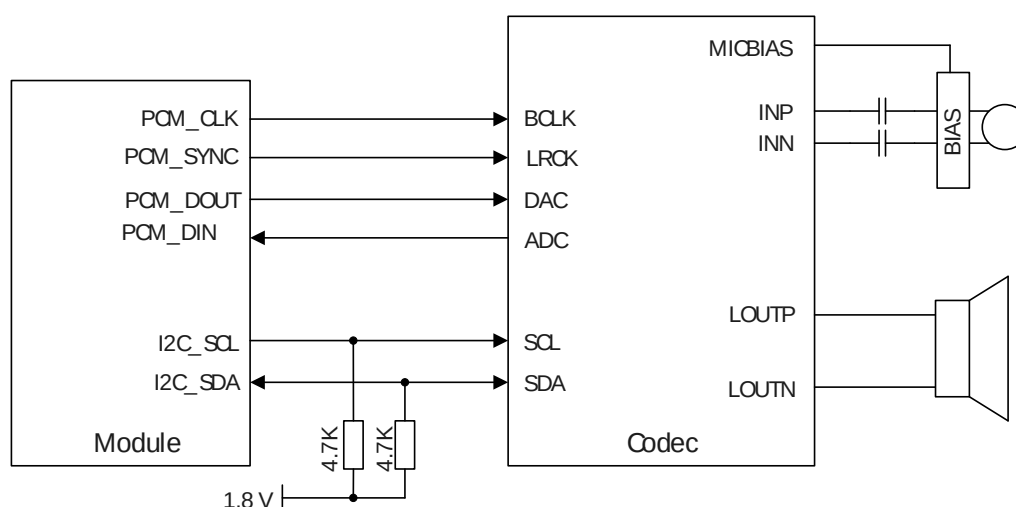
Table 19: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	66	DI	PCM data input	If unused, keep them open.
PCM_DOUT	68	DO	PCM data output	
PCM_SYNC	65	DIO	PCM data frame sync	Output signal in master mode. Input signal in slave mode. If unused, keep them open.
PCM_CLK	67	DIO	PCM clock	
I2C_SDA	42	OD	I2C serial data (for an external codec)	An external pull-up resistor is requisite. If unused, keep them open.
I2C_SCL	43	OD	I2C serial clock (for an external codec)	
I2S_MCLK	152	DO	Clock output for codec	Provide a digital clock output for an external audio codec. If unused, keep it open. Master mode only.

Clock and mode can be configured by **AT+QDAI**, and the default configuration is master mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. See **document 3** for details about the AT command.

The following figure shows a reference design of PCM and I2C interfaces with an external codec IC.

Figure 24: Reference Circuit of PCM and I2C Application with Audio Codec



NOTE

The module works as a master device pertaining to I2C interface.

4.6. ADC Interfaces

The module provides two ADC (Analog-to-Digital Converter) interfaces. Execute **AT+QADC=0** to read the voltage value on ADC0. Execute **AT+QADC=1** to read the voltage value on ADC1. See **document 3** for details about these AT commands.

For higher accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 20: Pin Definition of the ADC Interface

Pin Name	I/O	Pin No.	Description	Comment
ADC0	AI	173	General-purpose ADC interface	0–1.875 V. If unused, keep them open.
ADC1	AI	175		

Table 21: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC0 Input Voltage Range	0	-	1.875	V
ADC1 Input Voltage Range	0	-	1.875	V
ADC Resolution	-	114.441	-	μV

NOTE

1. The input voltage of ADC should not exceed 1.875 V.
2. It is prohibited to supply any voltage to ADC pins without VBAT.
3. It is recommended to use a resistor divider circuit for ADC application.

4.7. Status Indication

4.7.1. Network Status Indication

The network indication pins NET_MODE and NET_STATUS can be used to drive network status indication LEDs. Their definitions and logic level change upon the switch of network mode/status, which is described in the following tables.

Table 22: Pin Definition of NET_MODE and NET_STATUS

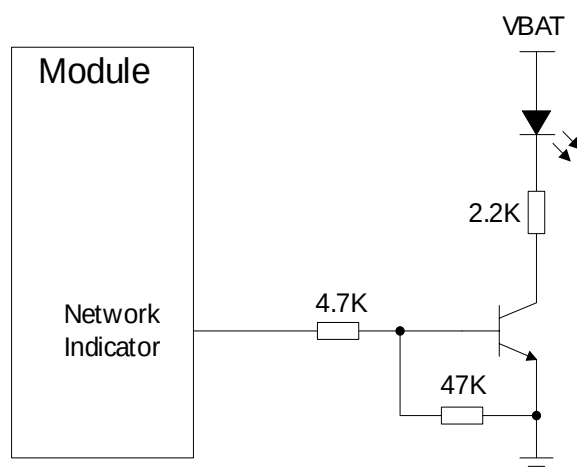
Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	147	DO	Indicate the module's network registration mode	If unused, keep them open.
NET_STATUS	170	DO	Indicate the module's network activity status	

Table 23: Working Status of NET_MODE and NET_STATUS

Pin Name	Status	Description
NET_MODE	Always High	Registered on network
	Always Low	Others
NET_STATUS	Blink slowly (200 ms High/1800 ms Low)	Network searching
	Blink slowly (1800 ms High/200 ms Low)	Idle
	Blink quickly (125 ms High/125 ms Low)	Data transmission ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

Figure 25: Reference Circuit of the Network Indicator



4.7.2. Module Status Indication

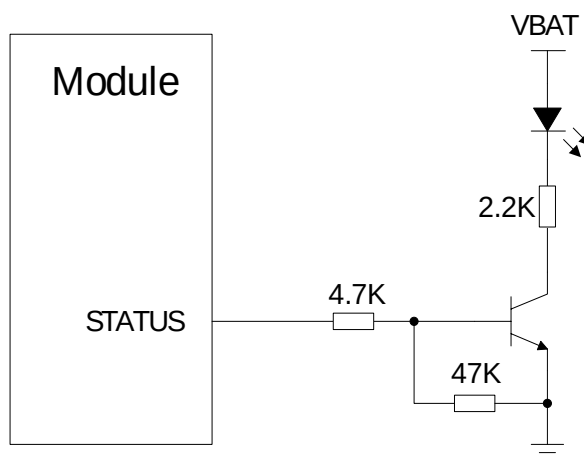
The STATUS pin is set as the module's status indicator. It outputs high-level voltage when the module is turned on.

Table 24: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	171	DO	Indicate the module's operation status	If unused, keep it open.

A reference circuit is shown as below.

Figure 26: Reference Circuits of STATUS



4.8. RI

Execute **AT+QCFG="risignalttype","physical"** to configure MAIN_RI behavior. No matter on which port a URC is presented, the URC will trigger the behavior of MAIN_RI. The behavior of MAIN_RI can be altered by executing **AT+QCFG="urc/ri/ring"**. See **document 3** for details about these AT commands.

In addition, MAIN_RI behavior can be configured flexibly. The default behavior of the MAIN_RI is shown as below.

Table 25: Default Behaviors of MAIN_RI

State	Response
Idle	MAIN_RI keeps at a high level.
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns.

NOTE

The URC can be output from UART port, USB AT port (by default) and USB modem port by executing **AT+QURCCFG**. See **document 3** for details about the AT command.

4.9. PCIe Interface

The module provides one integrated PCIe (Peripheral Component Interconnect Express) interface which can transmit data. The module supports PCIe Root Complex (RC) mode only.

- PCI Express Base Specification Revision 2.0 compliant
- Data rate up to 5 GT/s × 1 lane
- Can be connected to an external Ethernet IC (MAC and PHY) or WLAN IC

Table 26: Pin Definition of PCIe Interface

Pin Name	Pin No.	I/O	Description	Comment
PCIE_REFCLK_P	179	AO	PCIe reference clock (+)	
PCIE_REFCLK_M	180	AO	PCIe reference clock (-)	
PCIE_TX_M	182	AO	PCIe transmit (-)	Require differential impedance of 85 Ω . If unused, keep them open.
PCIE_TX_P	183	AO	PCIe transmit (+)	
PCIE_RX_M	185	AI	PCIe receive (-)	
PCIE_RX_P	186	AI	PCIe receive (+)	
PCIE_CLKREQ_N	188	DI	PCIe clock request	Input signal in master mode. If unused, keep it open.
PCIE_RC_RST_N	189	DO	PCIe RC reset	Output signal in master mode. If unused, keep it open.
PCIE_WAKE_N	190	DI	PCIe awake	Input signal in master mode only. If unused, keep it open.

To enhance the reliability and availability in applications, follow the criteria below in the PCIe interface circuit design:

- Keep the PCIe data and control signals away from sensitive circuits and signals, such as RF, audio, and clock signals.
- Add a capacitor in series on Rx traces to prevent any DC bias.
- Keep the maximum trace length less than 300 mm.
- Keep the length matching of each differential data pair (Tx/Rx/REFCLK) less than 0.7 mm for PCIe routing traces.
- Keep the differential impedance of PCIe data trace as 85 $\Omega \pm 10\%$.
- Do not route PCIe data traces under components or cross them with other traces.

The module only supports Root Complex (RC) mode. In this mode, the module is configured to act as a PCIe RC device. The following figure shows a reference circuit of PCIe RC mode.

Figure 27: PCIe Interface Reference Circuit (RC Mode)

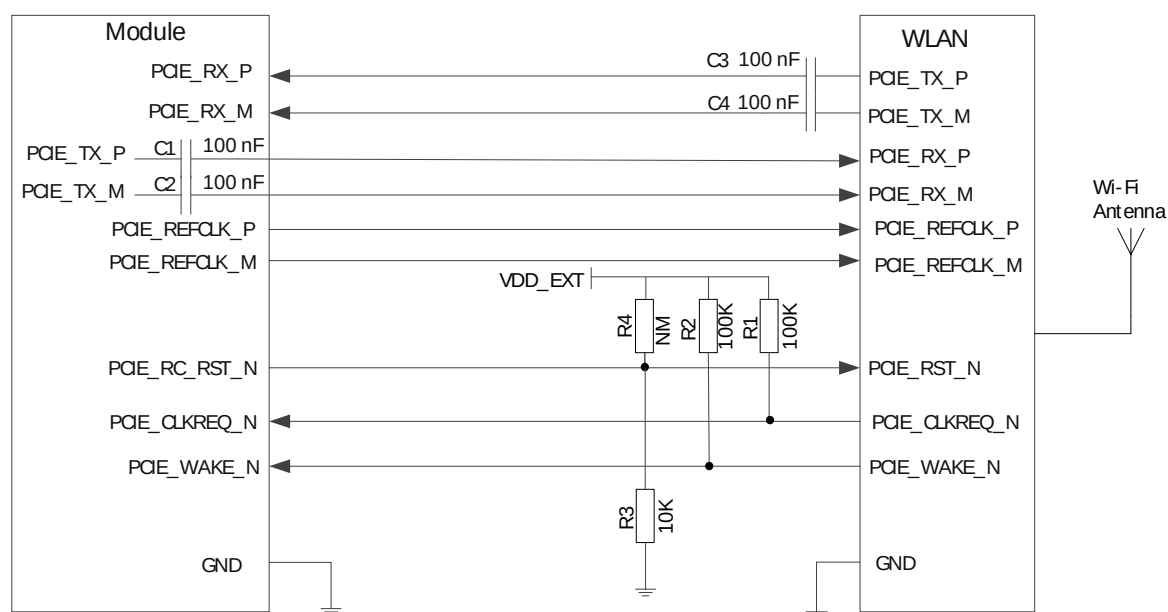


Table 27: PCIe Trace Length Inside the Module

Pin No.	Pin Name	Length (mm)	Length Difference (P-M) (mm)
179	PCIE_REFCLK_P	22.24	0.10
180	PCIE_REFCLK_M	22.14	
182	PCIE_TX_M	17.99	0.08
183	PCIE_TX_P	17.91	
185	PCIE_RX_M	13.91	0.07
186	PCIE_RX_P	13.98	

4.10. SDIO Interface

The module provides one SDIO interface which supports SD 3.0 protocol. The following table shows the pin definition.

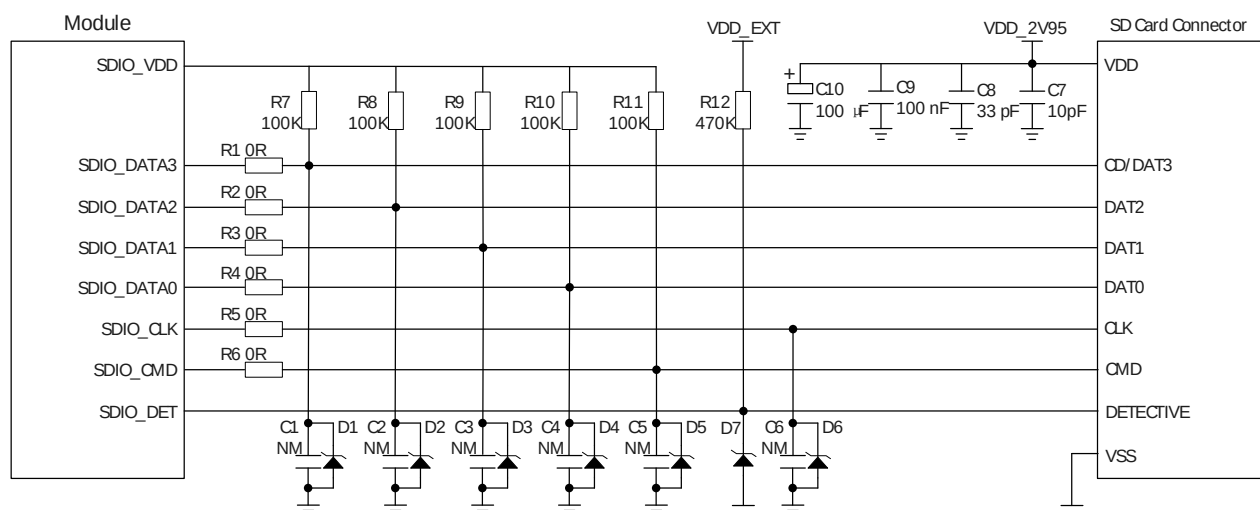
Table 28: Pin Definition of SDIO Interface

Pin Name	Pin No.	I/O	Description	Comment
VDD_P2	135	PI	Power input for SDIO interface	If a SD card is used, connect VDD_P2 to SDIO_VDD.

				If unused, connect VDD_P2 to VDD_EXT.
SDIO_VDD	46	PO	SD card application: SDIO pull up power source	Cannot work as SD card power supply. SD card must be powered by an external power supply.
SDIO_DATA3	48	DIO	SDIO data bit 3	
SDIO_DATA2	47	DIO	SDIO data bit 2	
SDIO_DATA1	50	DIO	SDIO data bit 1	
SDIO_DATA0	49	DIO	SDIO data bit 0	If unused, keep them open.
SDIO_CMD	51	DIO	SDIO command	
SDIO_DET	52	DI	SD card detect	
SDIO_CLK	53	DO	SDIO clock	

The following figure shows an SDIO interface reference design.

Figure 28: Reference Circuit of SD Card Application



Follow the principles below in the SD card circuit design:

- The voltage of SD power supply ranges from 2.7 V to 3.6 V and a sufficient current up to 0.8 A should be provided. As the maximum output current of SDIO_VDD is 50 mA which can only work as SDIO pull-up resistors, the SD card needs an external power supply.
- To avoid the jitter, resistors R7 to R11 are needed to pull up the SDIO signals to SDIO_VDD. The values of these resistors range from 10 kΩ to 100 kΩ and the preferred value is 100 kΩ.
- To improve signal quality, it is recommended to add resistors R1 to R6 of 0 Ω in series between the module and the SD card connector. The bypass capacitors C1 to C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- For better ESD protection, it is recommended to add a TVS array on each SD signal trace.
- It is important to route the SDIO signal traces with ground. The impedance of SDIO data trace is 50 Ω (± 10 %).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, and analog signals, as well as noise signals such as clock signals and DC-DC signals.
- It is recommended to keep the trace length difference between SDIO_CLK and SDIO_DATA/SDIO_CMD within 1 mm and the total routing length less than 50 mm. The trace inside the module is 25 mm long in total, so the exterior trace should be less than 25 mm in total.

- Make sure the adjacent trace spacing is twice the trace width and the load capacitance of SDIO bus should be less than 15 pF.

4.11. Antenna Tuner Control Interfaces^{dev}

The module supports external antenna tuner control through the RFFE interface. The following is the pin definition of the RFFE interfaces.

Table 29: Pin Definition of RFFE Interfaces

Pin Name	Pin No.	I/O	Description	Comment
RFFE_CLK	71	DO	RFFE serial interface for external antenna tuner control	If unused, keep them open.
RFFE_DATA	73	DIO		

4.12. USB_BOOT Interface

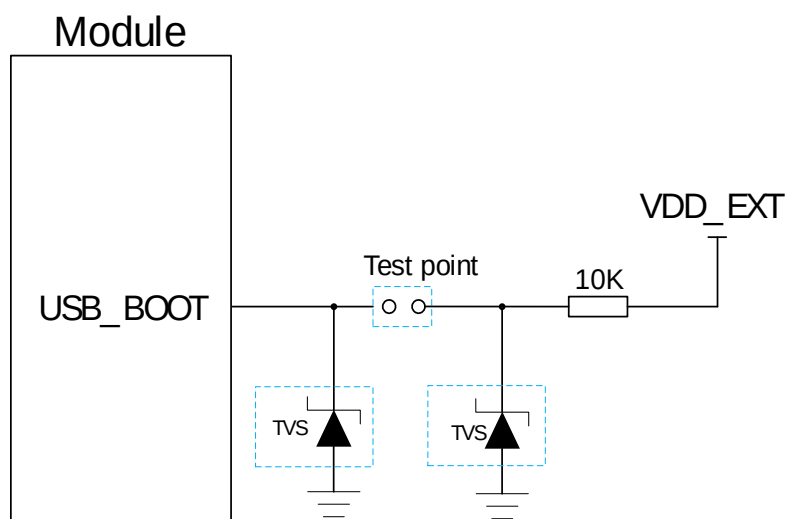
The module provides one USB_BOOT pin. Pull up USB_BOOT to VDD_EXT before turning on the module, then the module will enter forced download mode when turned on. In this mode, the module supports firmware upgrade over USB 2.0 interface.

Table 30: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	140	DI	Force the module into download mode	Active high. A test point is recommended to be reserved.

The following figure shows a reference circuit of USB_BOOT.

Figure 29: Reference Circuit of USB_BOOT



5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module provides one main antenna interface, one Rx-diversity antenna interface, two MIMO antenna interfaces, and one GNSS antenna interface. The impedance of antenna port is 50 Ω .

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

The pin definition of the main antenna interface, Rx-diversity antenna interface and MIMO antenna interfaces are shown as below.

Table 31: Pin Definition of the Main/Rx-diversity/MIMO Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT0	107	AIO	Main antenna interface	50 Ω characteristic impedance.
ANT1	127	AI	Rx-diversity antenna interface	
ANT2	101	AI	MIMO antenna interface	
ANT3	113	AI		

Table 32: Frequency Bands

3GPP Band	Transmit	Receive	Unit
LTE B2	1850–1910	1930–1990	MHz
LTE B4	1710–1755	2110–2155	MHz
LTE B5	824–849	869–894	MHz
LTE B7	2500–2570	2620–2690	MHz
LTE B12	699–716	729–746	MHz
LTE B13	777–787	746–756	MHz
LTE B14	788–798	758–768	MHz
LTE B25	1850–1915	1930–1995	MHz

LTE B26	814–849	859–894	MHz
LTE B29	-	717–728	MHz
LTE B30	2305–2315	2350–2360	MHz
LTE B41	2496–2690	2496–2690	MHz
LTE B48	3550–3700	3550–3700	MHz
LTE B66	1710–1780	2110–2200	MHz
LTE B71	663–698	617–652	MHz

5.1.2. Tx Power

Table 33: Tx Power

Frequency Band	Max. RF Output Power	Min. RF Output Power
LTE bands	23 dBm $\pm$ 2 dB ¹⁰	< -40 dBm

5.1.3. Rx Sensitivity

Table 34: LUK64-LD & LUK66-LD Dual-Antenna Conducted RF Rx Sensitivity

Frequency Band	Primary	Diversity	SIMO ¹¹	3GPP (SIMO)	Unit
LTE-FDD B2 (10 MHz)	-97	-95.3	-99.2	-94.3	dBm
LTE-FDD B4 (10 MHz)	-96	-96	-98.4	-96.3	dBm
LTE-FDD B5 (10 MHz)	-97.1	-99	-100.5	-94.3	dBm
LTE-FDD B7 (10 MHz)	-95.1	-95	-98	-94.3	dBm
LTE-FDD B12 (10 MHz)	-98	-99.5	-101.7	-93.3	dBm
LTE-FDD B13 (10 MHz)	-98	-99.5	-101	-93.3	dBm
LTE-FDD B14 (10 MHz)	-98	-99.7	-101.4	-93.3	dBm
LTE-FDD B25 (10 MHz)	-97	-95.3	-99	-92.8	dBm
LTE-FDD B26 (10 MHz)	-97	-99.1	-101	-93.8	dBm
LTE-FDD B29 (10 MHz) ¹²	-98	-98.3	-101.1	-93.3	dBm

¹⁰ B48 only supports 23 dBm $\pm$ 1/-2 dB.

¹¹ SIMO is a smart antenna technology that uses a single antenna at the transmitter side and multiple (Primary + Diversity or Primary + Diversity + MIMO1 + MIMO2) antennas at the receiver side, which can improve Rx performance. Rx sensitivity values are measured in four antennas condition (Primary + Diversity or Primary + Diversity + MIMO1 + MIMO2).

¹² The test results are based on CA_2A-29A.

LTE-FDD B30 (10 MHz)	-95	-95.3	-97.5	-95.3	dBm
LTE-TDD B41 (10 MHz)	-95.2	-95	-98	-94.3	dBm
LTE-TDD B48 (10 MHz)	-96.5	-98.2	-100.2	-95	dBm
LTE-FDD B66 (10 MHz)	-96	-96	-98.3	-95.8	dBm
LTE-FDD B71 (10 MHz)	-98.2	-100	-102	-94.3	dBm

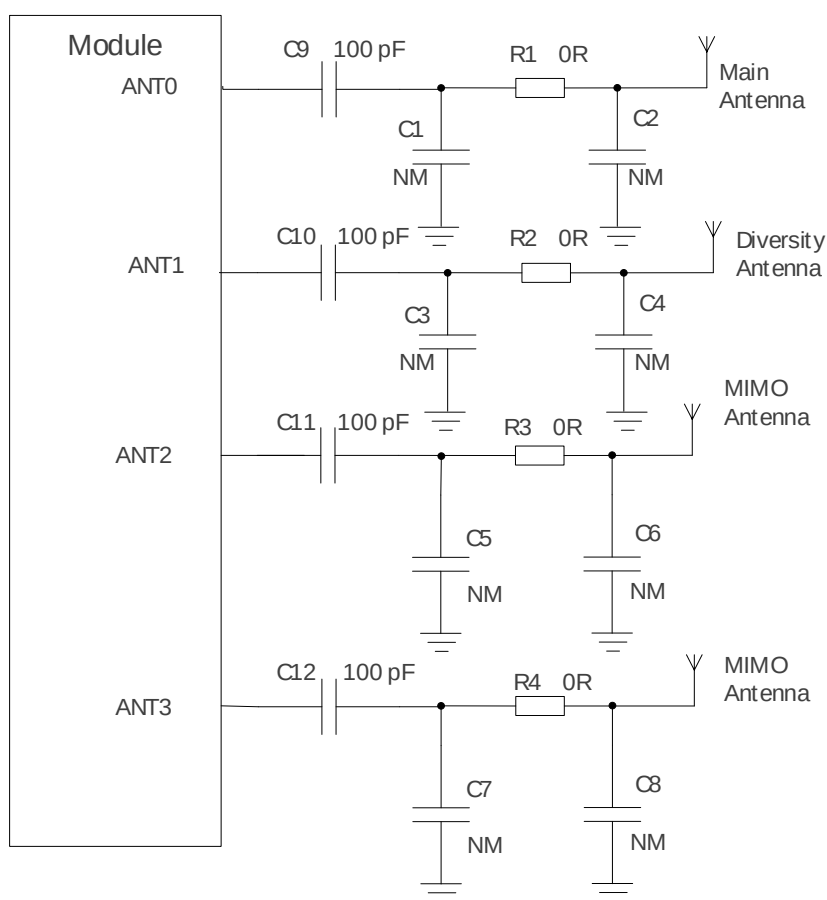
Table 35: LUK64-LD & LUK66-LD Four-Antenna Conducted RF Rx Sensitivity

Frequency Band	SIMO (dBm) ¹¹	3GPP (SIMO)	Unit
LTE-FDD B2 (10 MHz)	-103	-97	dBm
LTE-FDD B4 (10 MHz)	-102.1	-99	dBm
LTE-FDD B7 (10 MHz)	-102	-97	dBm
LTE-FDD B25 (10 MHz)	-103	-95.5	dBm
LTE-FDD B30 (10 MHz)	-101	-	dBm
LTE-TDD B41 (10 MHz)	-101.7	-97	dBm
LTE-TDD B48 (10 MHz)	-104	-	dBm
LTE-FDD B66 (10 MHz)	-102.1	-98.5	dBm

5.1.4. Reference Design

A reference design of ANT0, ANT1, ANT2 and ANT3 interfaces is shown as below. It requires a dual L-type circuit for better RF performance. The dual L-type components (R1/C1/C2/C9, R2/C3/C4/C10, R3/C5/C6/C11, R4/C7/C8/C12) should be placed as close to the antennas as possible and are mounted according to the actual debugging. C1 to C8 are not mounted and a 0 Ω resistor is mounted on R1 to R4 respectively by default. C9/C10/C11/C12 are DC blocking capacitors, if there is DC power at the antenna ports, the capacitance must be used for DC blocked, and the value can be tuned according to the actual debugging.

Figure 30: Reference Circuit of RF Antenna Interfaces



NOTE

1. Keep a proper distance between the main antenna and the Rx-diversity antenna to improve the receiving sensitivity.
2. Notes on C9, C10, C11 and C12:
 - 1) If there is DC power at the antenna ports, place capacitors on C9, C10, C11 and C12 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
 - 2) If there is no DC power in the peripheral design:
 - a) Do not reserve C9, C10, C11 and C12.
 - b) If C9, C10, C11 and C12 have already been reserved, they should be mounted with components, and it is recommended to use 0 Ω resistors. You can also match the components according to the debugging results.

5.2. GNSS (Optional)

5.2.1. Antenna Interface & Frequency Bands

The module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, and Galileo. The module supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

By default, the module GNSS engine is off. It must be switched on via AT command. For more details, see **document 3**.

Table 36: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	119	AI	GNSS antenna interface	50 Ω characteristic impedance. If unused, keep it open.

Table 37: GNSS Frequency

GNSS Constellation Type	Frequency	Unit
GPS	1575.42 $\pm$ 1.023 (L1)	MHz
GLONASS	1601.7 $\pm$ 4.2 (L1)	MHz
Galileo	1575.42 $\pm$ 2.046 (E1)	MHz
BDS	1561.098 $\pm$ 2.046 (B1I)	MHz

5.2.2. GNSS Performance

Table 38: GNSS Performance

Parameter	Description	Condition	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-147	dBm
	Reacquisition	Autonomous	-159	dBm
	Tracking	Autonomous	-159	dBm
TTFF	Cold start @ open sky	Autonomous	30	s
		AGNSS start	10	s
	Warm start @ open sky	Autonomous	27	s
		AGNSS start	3	s
	Hot start @ open sky	Autonomous	1.1	s
		AGNSS start	1.1	s
Accuracy	CEP-50	Autonomous @ open sky	2	m

NOTE

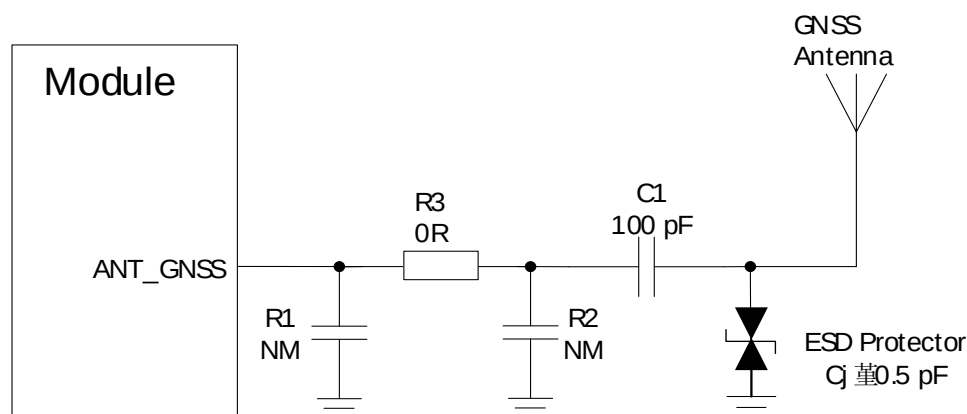
1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).

2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.3. Passive Antenna Reference Design

GNSS Antenna interface supports passive ceramic antenna or other types of passive antennas. The reference design of passive antenna is shown as below.

Figure 31: Reference Circuit of Passive Antenna Interface



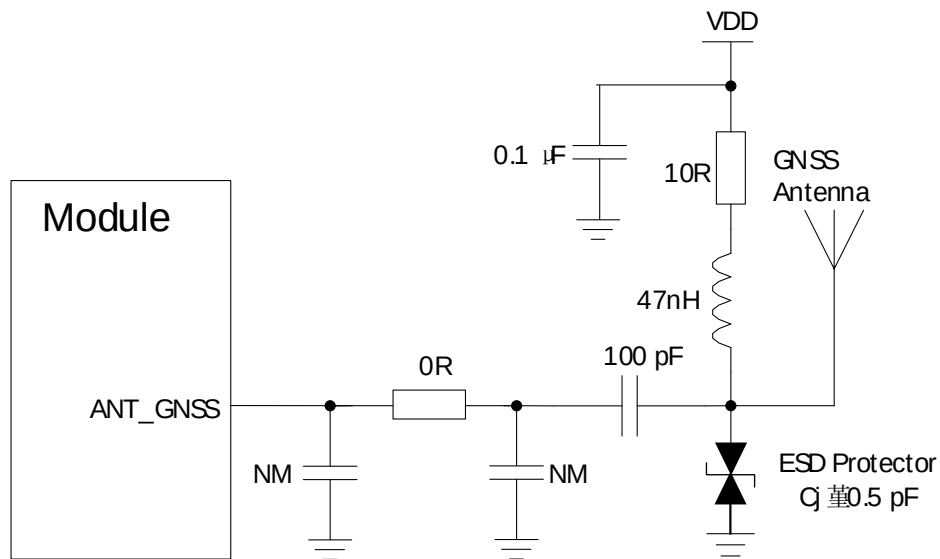
NOTE

1. An external LDO can be used to supply power according to the active antenna requirements.
2. The VDD circuit is unnecessary if the module is equipped with a passive antenna.
3. It is not recommended to add an external LNA when using a passive GNSS antenna.
4. Notes on C1:
 - 1) If there is DC power at the antenna ports, place capacitor on C1 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
 - 2) If there is no DC power in the peripheral design:
 - a) Do not reserve C1.
 - b) If C1 has already been reserved, it should be mounted with component, and it is recommended to use 0 Ω resistor. You can also match the component according to the debugging results.

5.2.4. Active Antenna Reference Design

GNSS Antenna interface also supports active antenna. In any case, it is recommended to use a passive antenna. If active antenna is indeed needed in your application, it is recommended to reserve a dual L-type attenuation circuit provision and use high-performance LDO as the power supply. The reference design of active antenna is shown as below.

Figure 32: Reference Circuit of Active Antenna Interface



5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

Figure 33: Microstrip Line Design on a 2-layer PCB

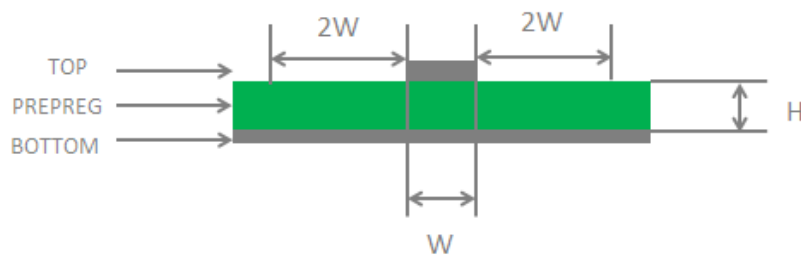


Figure 34: Coplanar Waveguide Line Design on a 2-layer PCB

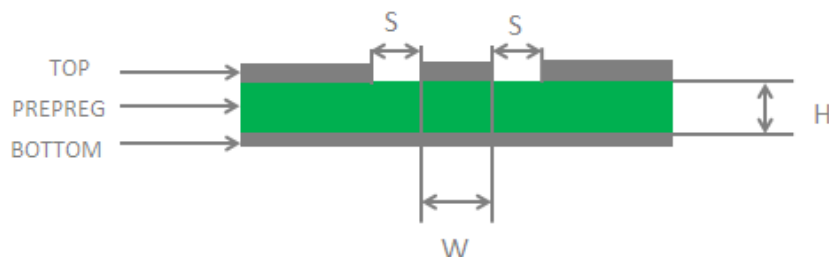


Figure 35: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 3 as Reference Ground)

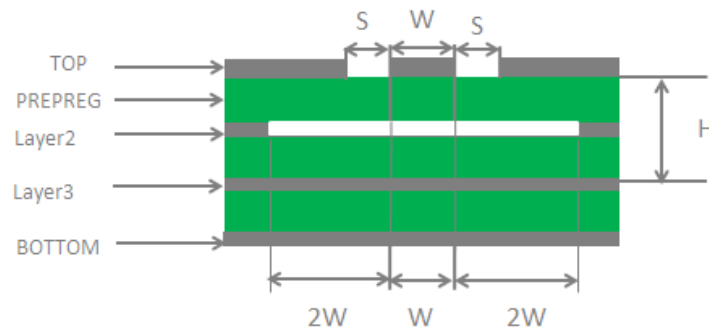
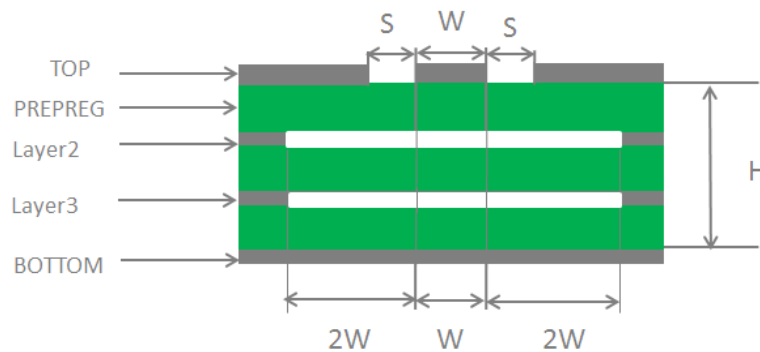


Figure 36: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 4 as Reference Ground)



To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω .
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- Reserve clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice of the width of RF signal traces ($2 \times W$).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see **document 4**.

5.4. Antenna Design Requirements

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 39: Antenna Design Requirements

Antenna Type	Requirements
--------------	--------------

GNSS	● Frequency range: 1559–1609 MHz ● Polarization: RHCP or linear ● VSWR: ≤ 2 (Typ.) For passive antenna usage: Passive antenna gain: > 0 dBi For active antenna usage: Active antenna noise figure: < 1.5 dB Active antenna embedded LNA gain: < 17 dB
Cellular	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Max input power: 50 W ● Input impedance: 50Ω ● Cable insertion loss: – < 1 dB: LB (< 1 GHz) – < 1.5 dB: MB (1–2.3 GHz) – < 2 dB: HB (> 2.3 GHz)

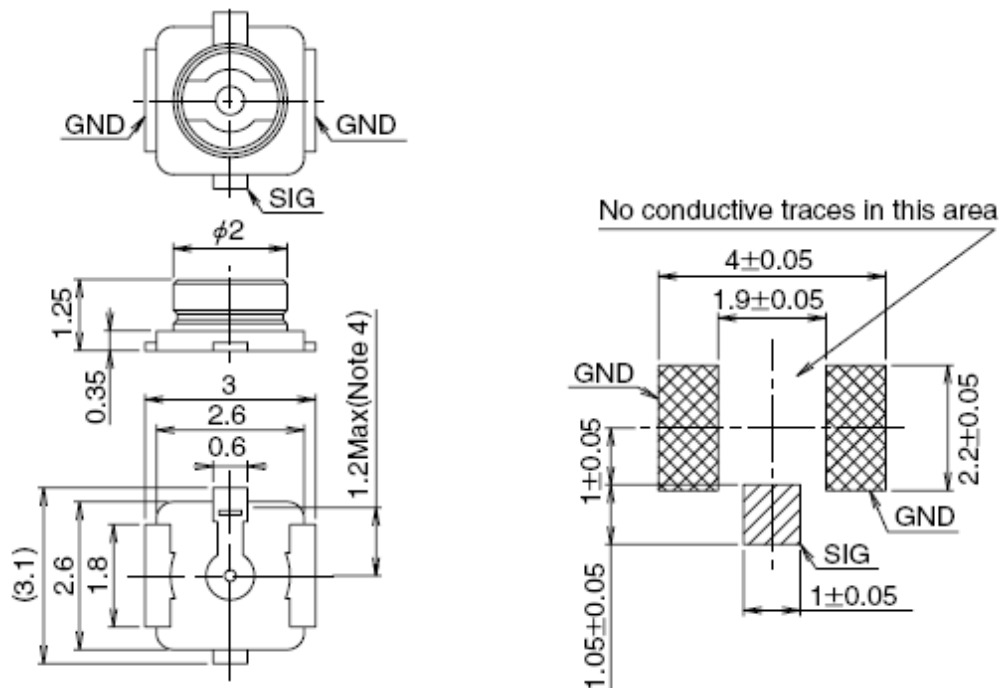
NOTE

It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

Figure 37: Dimensions of the Receptacle (Unit: mm)



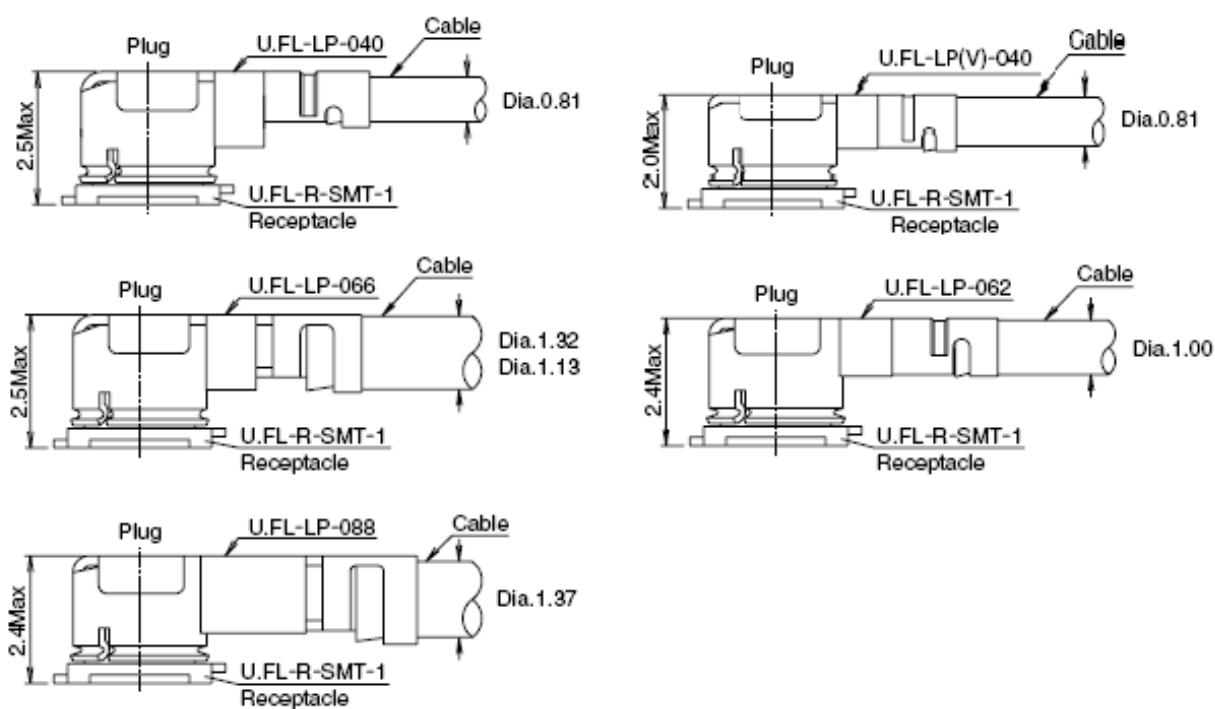
U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

Figure 38: Specifications of Mated Plugs

	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Part No.					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

The following figure describes the space factor of mated plugs.

Figure 39: Space Factor of Mated Connectors (Unit: mm)



For more details, please visit <http://www.hirose.com>.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 40: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	1.0	A
Peak Current of VBAT_RF	-	1.2	A
Voltage at Digital Pins	-0.3	2.3	V
Input Voltage at ADC	-0.5	2.3	V

6.2. Power Supply Ratings

Table 41: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.4	V
USB_VBUS	USB connection detect	-	3.3	5.0	5.25	V

6.3. Power Consumption

Table 42: LUK64-LD Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	12	μA
Sleep state	AT+CFUN=0 (USB disconnected)	1.1	mA
	LTE-FDD PF = 32 (USB disconnected)	3.99	mA
	LTE-FDD PF = 64 (USB disconnected)	2.65	mA
	LTE-FDD PF = 128 (USB disconnected)	1.99	mA
	LTE-FDD PF = 256 (USB disconnected)	1.76	mA
	LTE-TDD PF = 32 (USB disconnected)	4.27	mA
	LTE-TDD PF = 64 (USB disconnected)	2.83	mA
	LTE-TDD PF = 128 (USB disconnected)	2.1	mA
	LTE-TDD PF = 256 (USB disconnected)	1.75	mA
	LTE-FDD PF = 64 (USB disconnected)	11.52	mA
Idle state	LTE-FDD PF = 64 (USB 2.0 connected)	18.71	mA
	LTE-TDD PF = 64 (USB disconnected)	11.87	mA
	LTE-TDD PF = 64 (USB 2.0 connected)	18.83	mA
	LTE-FDD B2 CH1100 @ 22.82 dBm	732	mA
LTE data transmission (GNSS OFF)	LTE-FDD B4 CH2050 @ 22.74 dBm	760	mA
	LTE-FDD B5 CH2525 @ 23.0 dBm	597	mA
	LTE-FDD B7 CH3100 @ 22.61 dBm	779	mA
	LTE-FDD B12 CH5095 @ 22.95 dBm	636	mA
	LTE-FDD B13 CH5230@ 22.84 dBm	623	mA
	LTE-FDD B14 CH5330 @ 22.97 dBm	577	mA
	LTE-FDD B25 CH8590 @ 22.83 dBm	711	mA
	LTE-FDD B26 CH8765 @ 22.94 dBm	631	mA
	LTE-FDD B30 CH9820 @ 22.5 dBm	897	mA
	LTE-TDD B41 CH40620 @ 22.75 dBm	453	mA
	LTE-TDD B48 CH55340 @ 22.67 dBm	426	mA

LTE-FDD B66 CH66536 @ 23.07 dBm	745	mA
LTE-FDD B71 CH68686 @ 22.94 dBm	751	mA

Table 43: LUK66-LD Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	12	μA
Sleep state	AT+CFUN=0 (USB disconnected)	1.1	mA
	LTE-FDD PF = 32 (USB disconnected)	3.9	mA
	LTE-FDD PF = 64 (USB disconnected)	3.4	mA
	LTE-FDD PF = 128 (USB disconnected)	1.9	mA
	LTE-FDD PF = 256 (USB disconnected)	1.6	mA
	LTE-TDD PF = 32 (USB disconnected)	4.4	mA
	LTE-TDD PF = 64 (USB disconnected)	3.1	mA
	LTE-TDD PF = 128 (USB disconnected)	2.3	mA
	LTE-TDD PF = 256 (USB disconnected)	2.0	mA
	LTE-FDD PF = 64 (USB disconnected)	10.2	mA
Idle state	LTE-FDD PF = 64 (USB 2.0 connected)	20	mA
	LTE-TDD PF = 64 (USB disconnected)	15	mA
	LTE-TDD PF = 64 (USB 2.0 connected)	22	mA
	LTE-FDD B2 CH1100 @ 23.08 dBm	749	mA
LTE data transmission (GNSS OFF)	LTE-FDD B4 CH2050 @ 22.91 dBm	757	mA
	LTE-FDD B5 CH2525 @ 23.16 dBm	598	mA
	LTE-FDD B7 CH3100 @ 22.9 dBm	815	mA
	LTE-FDD B12 CH5060 @ 22.95 dBm	634	mA
	LTE-FDD B13 CH5230 @ 22.93 dBm	608	mA
	LTE-FDD B14 CH5330 @ 23.08 dBm	568	mA
	LTE-FDD B25 CH8590 @ 23.15 dBm	752	mA
	LTE-FDD B26 CH8765 @ 23.12 dBm	644	mA

LTE-FDD B30 CH9820 @ 22.63 dBm	946	mA
LTE-TDD B41 CH40620 @ 23.07 dBm	433	mA
LTE-TDD B48 CH56640 @ 22.79 dBm	375	mA
LTE-FDD B66 CH66536 @ 23.01 dBm	770	mA
LTE-FDD B71 CH68836 @ 22.72 dBm	697	mA

6.4. Digital I/O Characteristics

Table 44: VDD_EXT I/O Requirements

Parameter	Description	Min.	Max.	Unit
V _{IH}	High-level input voltage	$0.7 \times VDD_EXT$	$VDD_EXT + 0.3$	V
V _{IL}	Low-level input voltage	-0.3	$0.3 \times VDD_EXT$	V
V _{OH}	High-level output voltage	$VDD_EXT - 0.45$	VDD_EXT	V
V _{OL}	Low-level output voltage	0	0.45	V

Table 45: USIM VDD High/Low-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
V _{IH}	High-level input voltage	$0.7 \times USIM_VDD$	$USIM_VDD + 0.3$	V
V _{IL}	Low-level input voltage	-0.3	$0.2 \times USIM_VDD$	V
V _{OH}	High-level output voltage	$0.8 \times USIM_VDD$	$USIM_VDD$	V
V _{OL}	Low-level output voltage	0	0.4	V

Table 46: SDIO VDD Low-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
V _{IH}	High-level input voltage	1.27	2.0	V
V _{IL}	Low-level input voltage	-0.3	0.58	V
V _{OH}	High-level output voltage	1.4	SDIO_VDD	V

V_{OL}	Low-level output voltage	0	0.45	V
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Table 47: SDIO_VDD High-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	$0.625 \times \text{SDIO_VDD}$	$\text{SDIO_VDD} + 0.3$	V
V_{IL}	Low-level input voltage	-0.3	$0.25 \times \text{SDIO_VDD}$	V
V_{OH}	High-level output voltage	$0.75 \times \text{SDIO_VDD}$	SDIO_VDD	V
V_{OL}	Low-level output voltage	0	$0.125 \times \text{SDIO_VDD}$	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 48: Electrostatic Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.6. Operation and Storage Temperatures

Table 49: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range ¹³	-30	+25	+75	°C

¹³ To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

Extended Operation Range ¹⁴	-40	-	+85	°C
Storage temperature range	-40	-	+90	°C

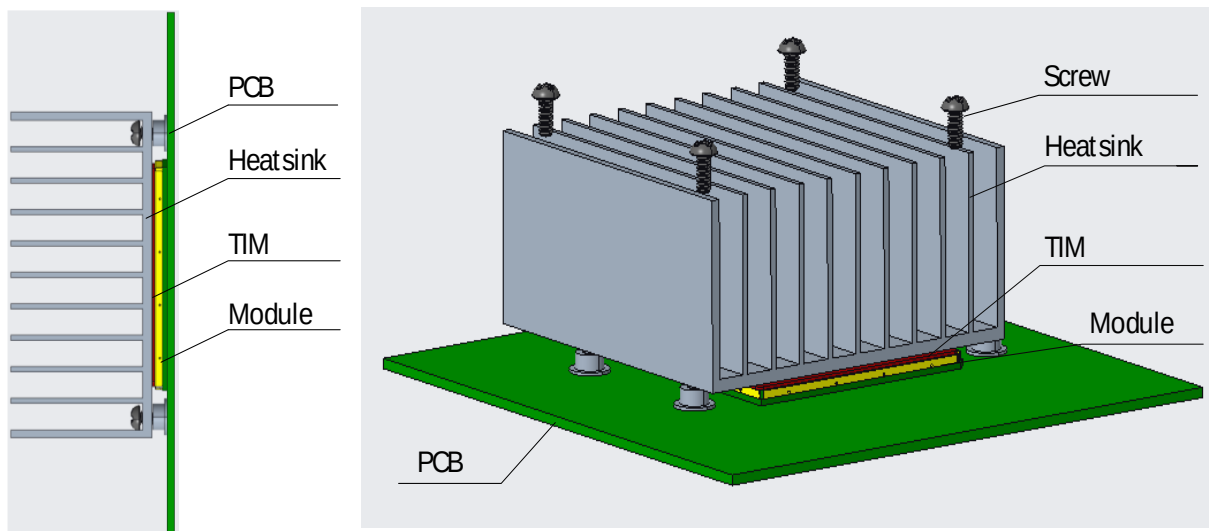
6.7. Thermal Dissipation

The module offers the best performance when all internal IC chips are working within their operating temperatures. When the IC chip reaches or exceeds the maximum junction temperature, the module may still work but the performance and function (such as RF output power, data rate.) will be affected to a certain extent. Therefore, the thermal design should be maximally optimized to ensure all internal IC chips always work within the recommended operating temperature range.

The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on your PCB, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Follow the principles below when the heatsink is necessary:
 - Do not place large size components in the area where the module is mounted on your PCB to reserve enough place for heatsink installation.
 - Attach the heatsink to the shielding cover of the module; In general, the base plate area of the heatsink should be larger than the module area to cover the module completely;
 - Choose the heatsink with adequate fins to dissipate heat;
 - Choose a TIM (Thermal Interface Material) with high thermal conductivity, good softness and good wettability and place it between the heatsink and the module;
 - Fasten the heatsink with four screws to ensure that it is in close contact with the module to prevent the heatsink from falling off during the drop, vibration test, or transportation.

Figure 40: Placement and Fixing of the Heatsink



¹⁴ To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within the range of -40 to -30 °C or 75 to 85 °C, the module retains the ability to establish and maintain functions such as voice, SMS, emergency call ^{dev}, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ± 0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

Figure 41: Module Top and Side Dimensions

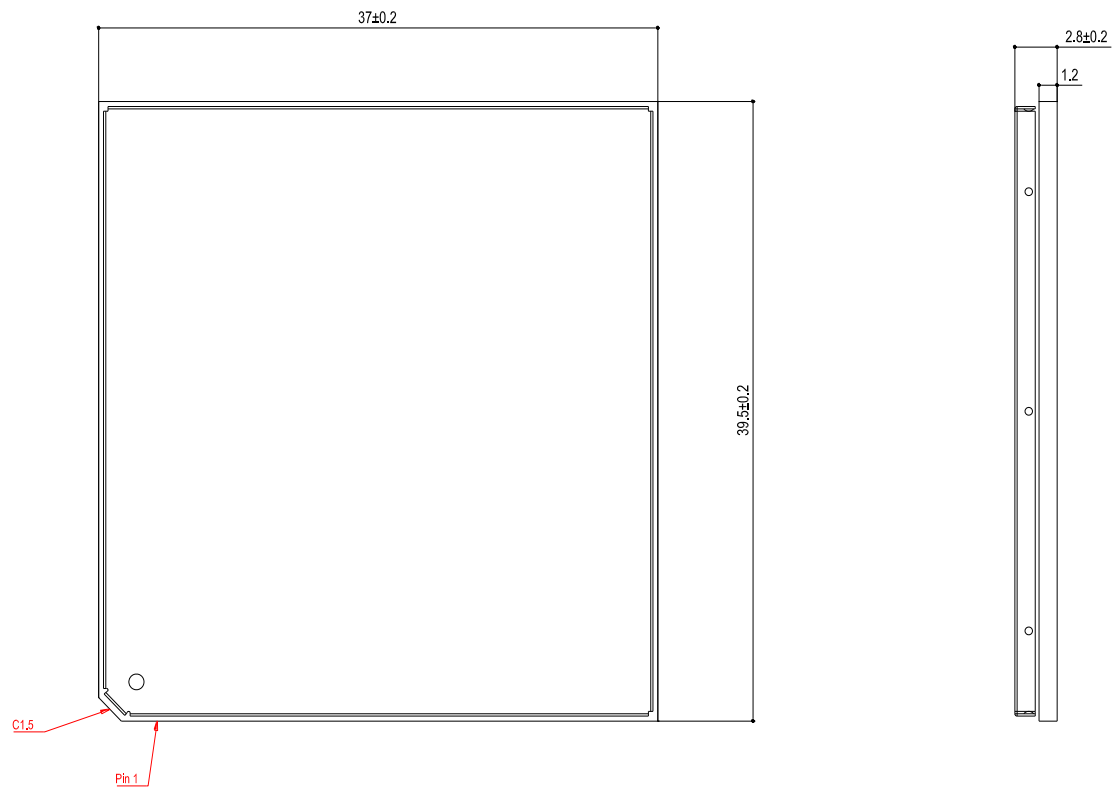
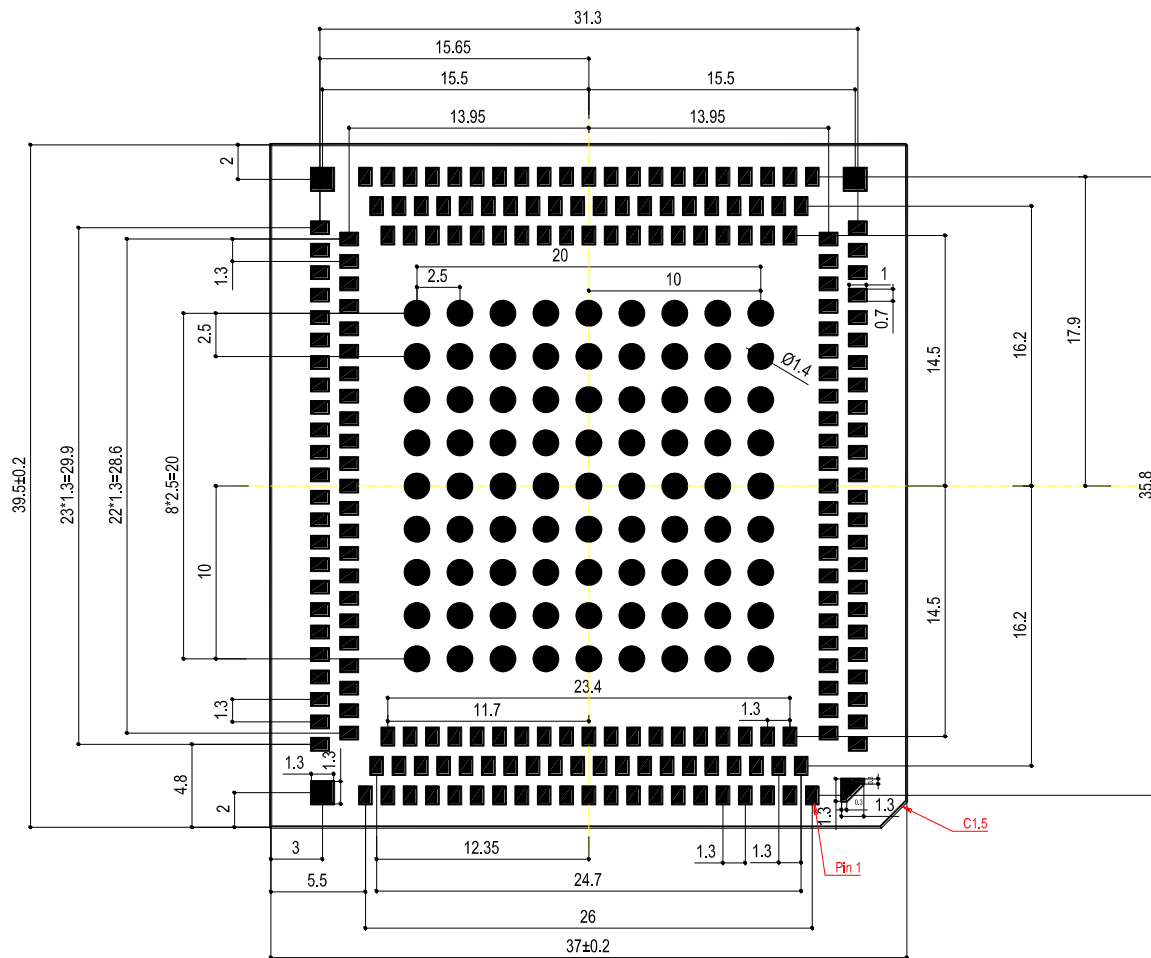


Figure 42: Module Bottom Dimensions (Bottom View)

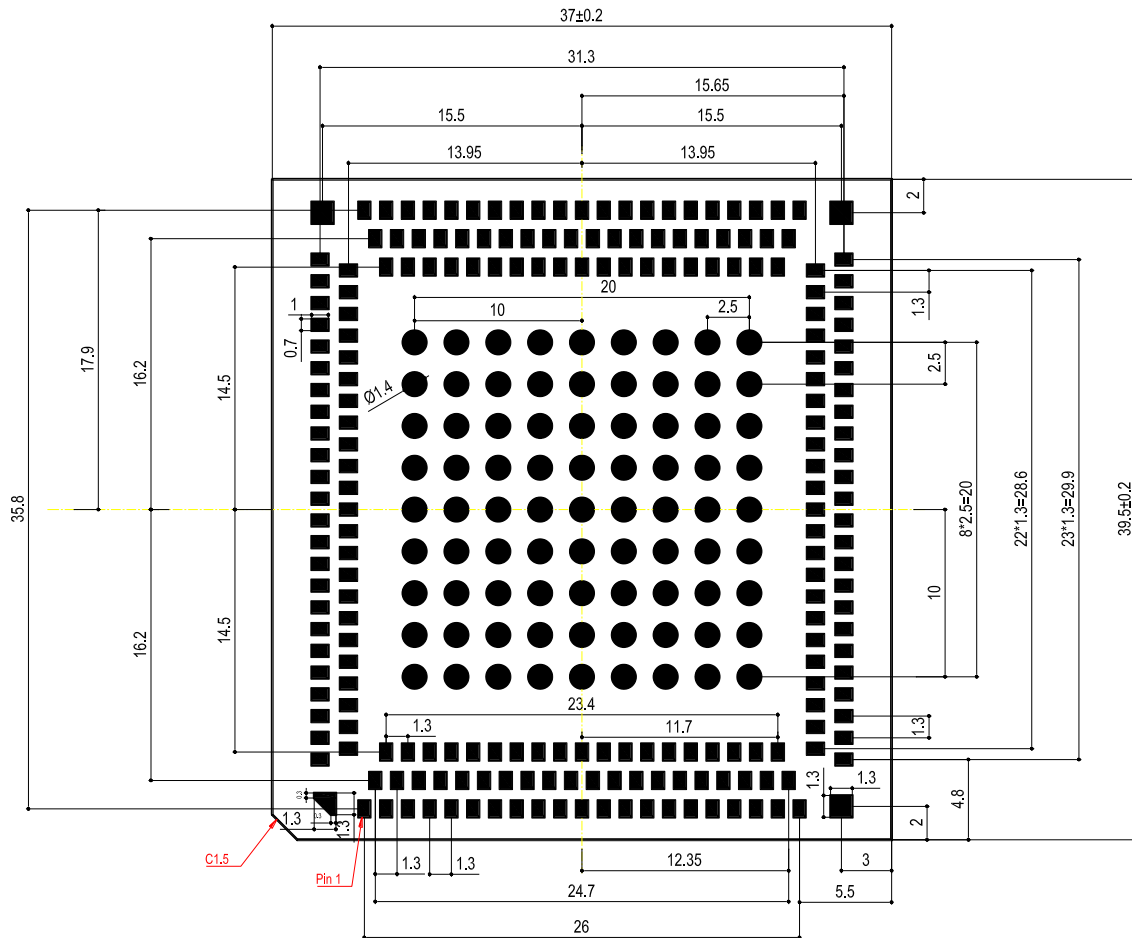


NOTE

The module's coplanarity standard: ≤ 0.13 mm.

7.2. Recommended Footprint

Figure 43: Recommended Footprint (Unit: mm)



NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

Figure 44: Top and Bottom Views of LUK64-LD

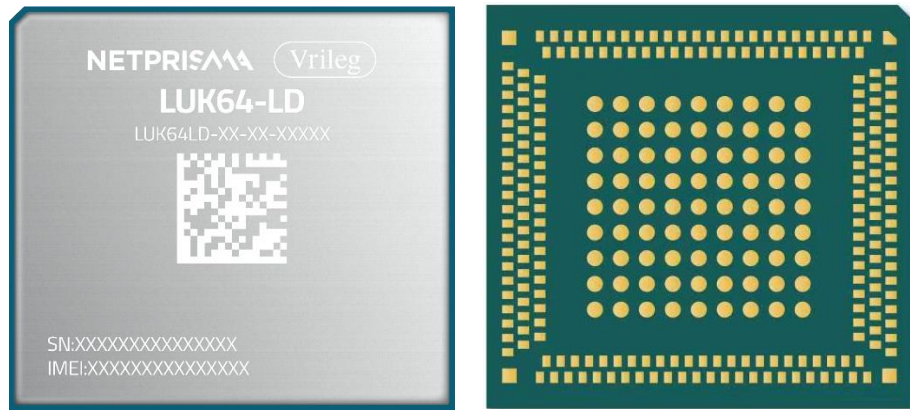
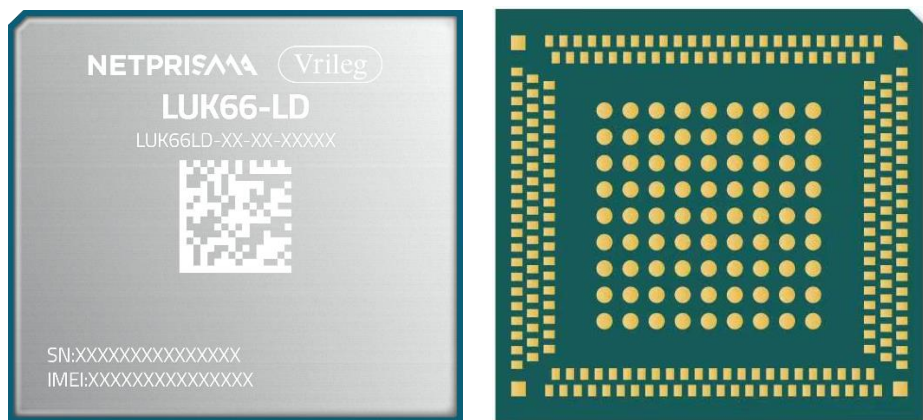


Figure 45: Top and Bottom Views of LUK64-LD



NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, see the module received from NetPrisma.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ± 5 °C and the relative humidity should be 35–60 %.
2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.
3. Floor life: 168 hours ¹⁵ in a factory where the temperature is 23 ± 5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).
4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:
 - The module is not stored in Recommended Storage Condition;
 - Violation of the third requirement mentioned above;
 - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
 - Before module repairing.
5. If needed, the pre-baking should follow the requirements below:
 - The module should be baked for 24 hours at 120 ± 5 °C;
 - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

NOTE

-
1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
 2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
 3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.
-

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.18 mm. For more details, see **document 5**.

The peak reflow temperature ranges from 235–246 °C, with 246 °C as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that

¹⁵ This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

Figure 46: Reflow Soldering Thermal Profile

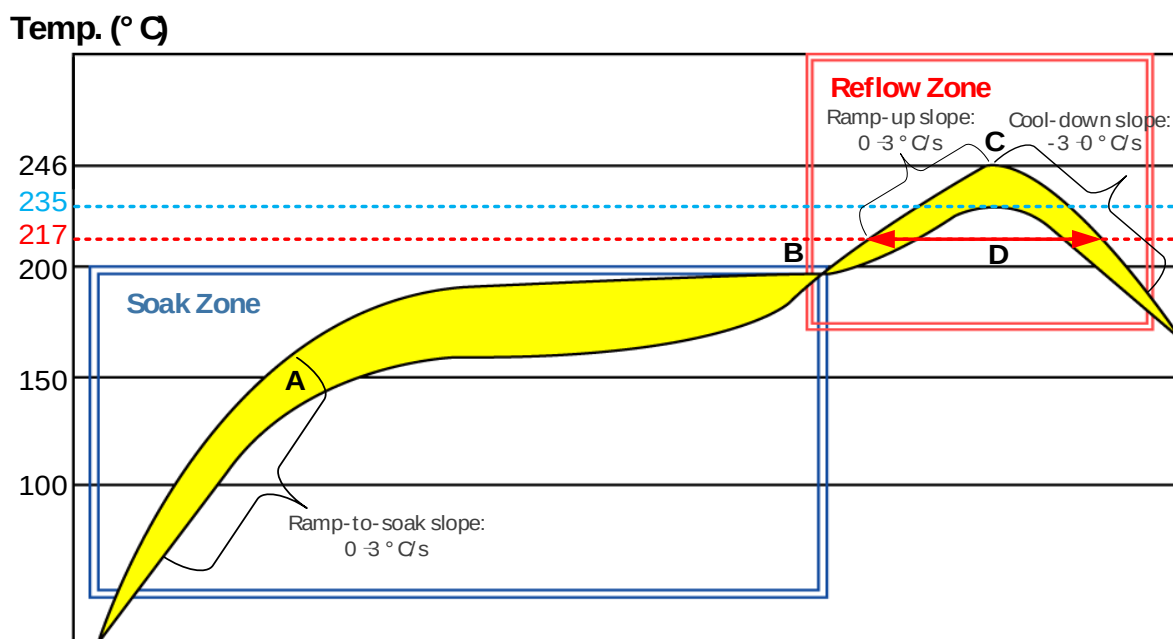


Table 50: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217°C)	40–70 s
Max Temperature	235–246 °C
Cool-down Slope	-3–0 °C/s (refer to NOTE 1 below)
Reflow Cycle	
Max Reflow Cycle	1

NOTE

1. For large-form-factor modules (that is, minimum side length ≥ 30 mm) with two-piece shielding covers, use a cool-down slope of $-1-0$ °C/s to reduce the thermal stress, preventing cover lifting. Due to the large-size form factors of such modules, an excessive temperature change may cause excessive thermal deformation of the metal shielding frame and cover. Therefore, reduce the ramp-up and cool-down slopes in the liquid phase of the solder paste to avoid excessive temperature change. If possible, choose a reflow oven with more than 10 temperature zones during production so that there are more temperature zones to set up to meet the optimal temperature curve.
2. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
6. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
7. Due to the complexity of the SMT process, contact NetPrisma Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective wave soldering, ultrasonic soldering) that is not mentioned in **document 6**.

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

Figure 47: Carrier Tape Dimension Drawing (Unit: mm)

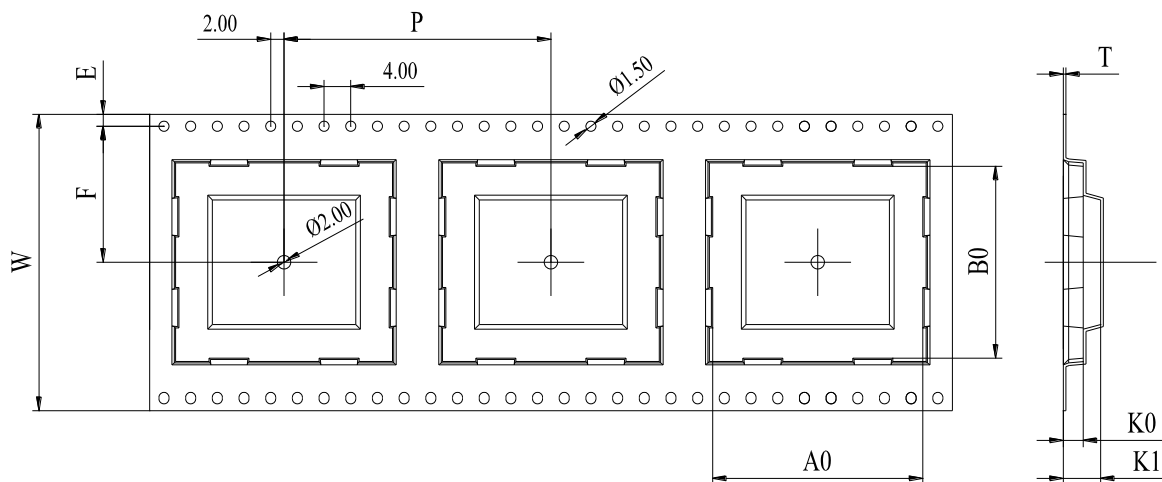


Table 51: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
56	48	0.35	40	37.5	3.9	5.3	26.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

Figure 48: Plastic Reel Dimension Drawing

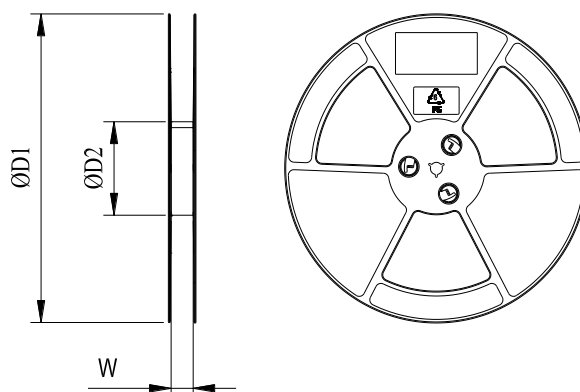
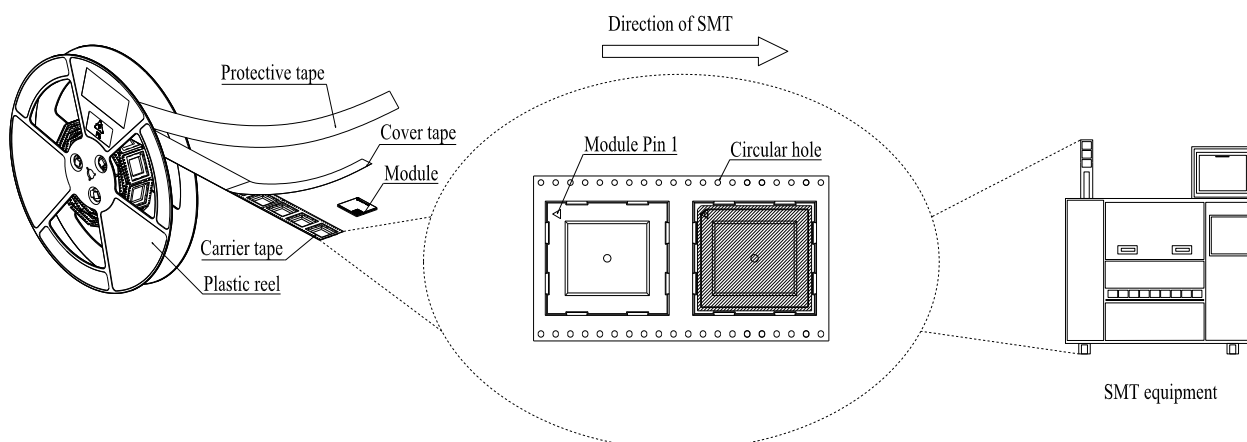


Table 52: Plastic Reel Dimension Table (Unit: mm)

ØD1	ØD2	W
330	100	56.5

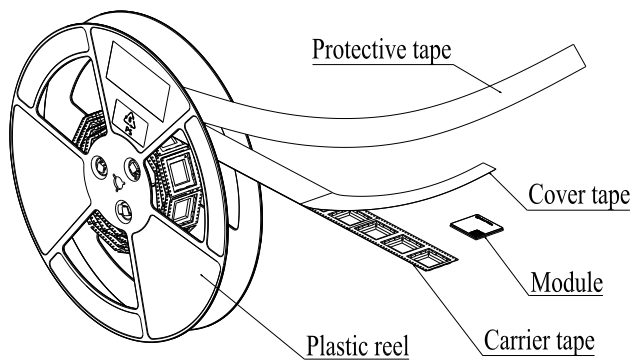
8.3.3. Mounting Direction

Figure 49: Mounting Direction



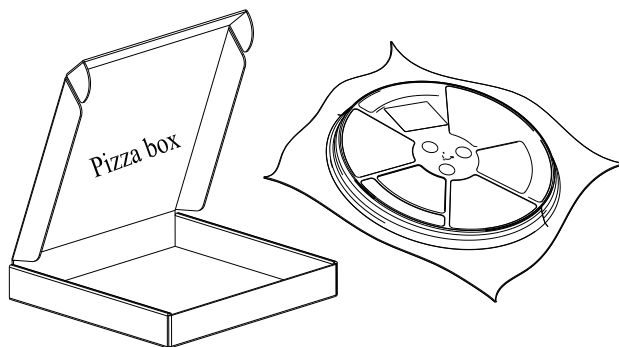
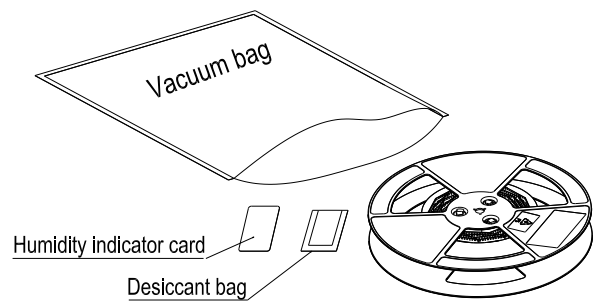
8.3.4. Packaging Process

Figure 50: Packaging Process



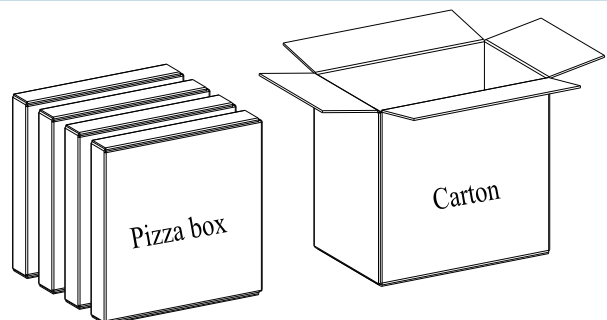
Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 200 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.



Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 800 modules.



9 Appendix References

Table 53: Related Documents

Document Name
1. NetPrisma-LUK64-LD&LUK66-LD-CA-Feature
2. NetPrisma-LUK64-LD&LUK66-LD-GNSS-Application-Note
3. NetPrisma-LUK64-LD&LUK66-LD-AT-Commands-Manual
4. NetPrisma-RF-Layout-Application-Note
5. NetPrisma-Module-Stencil-Design-Requirements
6. NetPrisma-Module-SMT-Application-Note

Table 54: Term and Abbreviation

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR	Adaptive Multi-Rate
AMR-WB	Adaptive Multi-Rate Wideband
BDS	BeiDou Navigation Satellite System
bps	bit(s) per second
CA	Carrier Aggregation
CHAP	Challenge-Handshake Authentication Protocol
C _j	Junction Capacitance
CTS	Clear To Send
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DFOTA	Delta Firmware Upgrade Over-the-Air
DL	Downlink
DRX	Discontinuous Reception
DTR	Data Terminal Ready
DTX	Discontinuous Transmission

EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
FDD	Frequency Division Duplex
FR	Full Rate
FTP	File Transfer Protocol
GLONASS	Global Navigation Satellite System (Russia)
GND	Ground
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HSPA+	Evolved High Speed Packet Access
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
I/O	Input/Output
LDO	Low-dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low-Noise Amplifier
LTE	Long-Term Evolution
LwM2M	Lightweight M2M
MBIM	Mobile Broadband Interface Model
ME	Mobile Equipment
MLCC	Multi-layer Ceramic Capacitor
MIMO	Multiple Input Multiple Output
MO	Mobile Originated

MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MS	Mobile Station
MT	Mobile Terminated
NAND	NON-AND
NITZ	Network Identity and Time Zone
NMEA	National Marine Electronics Association
OTG	On-The-Go
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QMI	Qualcomm Message Interface
QPSK	Quadrature Phase Shift Keying
RTS	Ready To Send/Request to Send
RF	Radio Frequency
RHCP	Right Hand Circular Polarization
Rx	Receive
SD Card	Secure Digital Card
SDIO	Secure Digital Input/Output
SIMO	Single Input Multiple Output
SPI	Serial Peripheral Interface
SIMO	Single Input Multiple Output
SLIC	Subscriber Line Interface Circuit
SMD	Surface Mount Device
SMS	Short Message Service
SMT	Surface Mount Technology

TCP	Transmission Control Protocol
TDD	Time Division Duplex
TIM	Thermal Interface Material
TTF	Time to First Fix
TVS	Transient Voltage Suppressor
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
VBAT	Voltage at Battery
V _{max}	Maximum Voltage
V _{nom}	Nominal Voltage
V _{min}	Minimum Voltage
V _{IHmax}	Maximum High-level Input Voltage
V _{IHmin}	Minimum High-level Input Voltage
V _{ILmax}	Maximum Low-level Input Voltage
VSWR	Voltage Standing Wave Ratio

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

Notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to NETPRISMA that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID 2BEY3LUK66LDA procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: "Contains FCC ID: 2BEY3LUK66LDA"

"Contains IC: 32052-LUK66LDA "

The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna Installation

- (1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
- (2) The transmitter module may not be co-located with any other transmitter or antenna.
- (3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Antenna Gain	LTE Band2: 1.59dBi LTE Band4: 2.0dBi LTE Band5: 2.53dBi LTE Band7: 3.00dBi LTE Band12: 3.95dBi LTE Band13: 4.45dBi LTE Band14: 3.63dBi LTE Band25: 1.59dBi LTE Band26: 3.19dBi LTE Band30: -5.70dBi LTE Band66: 2.00dBi LTE Band71: 1.66dBi	LTE Band41: 3.0dBi LTE Band48: -1.36dBi
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In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90 and part 96, requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuitry), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

- 1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
 - 2) The transmitter module may not be co-located with any other transmitter or antenna.
- As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Industry Canada Statement

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:

- (1) This device may not cause interference; and
- (2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

- (1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

- 1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
 - 2) The transmitter module may not be co-located with any other transmitter or antenna.
- As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

- 1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
- 2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains IC: 32052-LUK66LDA".

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 32052-LUK66LDA".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.

Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

Document History

Revision	Date	Changes
A	2025-05-13	The first revision.



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