

# WMC598E-GL

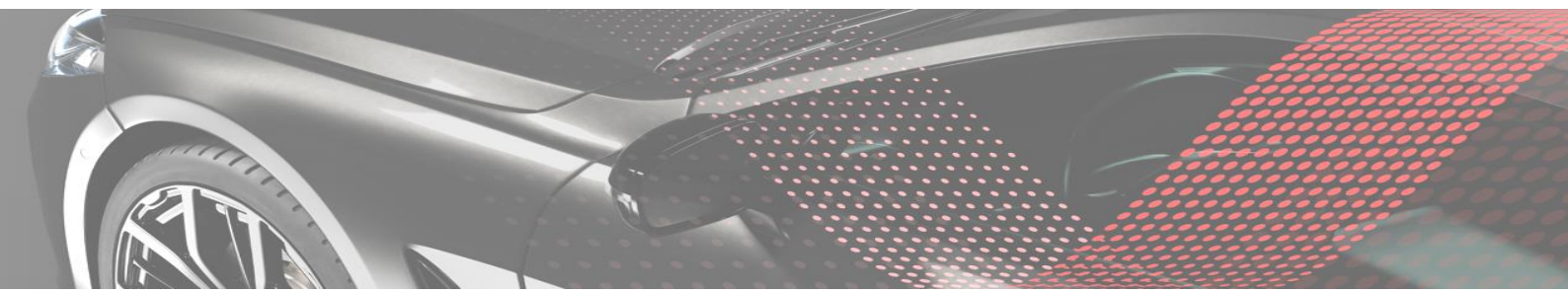
# Hardware Design

**Automotive Module Series**

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## Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Wireless Mobility assumes no liability for customers' failure to comply with these precautions.



Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.



Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.



Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.



Terminals or mobiles operating over radio signal and network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.



The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.



In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

# About the Document

This document is a preliminary version and it is highly likely that pin or interface definitions, frequency bands, functionality, features, design, or other module specifications (if any) may be modified. Some parameters have been validated, while others are still under review. Revised or additional information will be provided in subsequent official releases. This version is intended for temporary use only. In case of any discrepancies between the preliminary and official versions, the latest version takes precedence. The revision history is as follows:

## Revision History

| Version | Date       | Author                                 | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|---------|------------|----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| -       | 2024-12-06 | Scott ZHAO/<br>Snow LI/<br>Carrie PENG | Creation of the document                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 1.0.0   | 2024-12-06 | Scott ZHAO/<br>Snow LI/<br>Carrie PENG | Preliminary                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 1.0.1   | 2025-06-06 | Scott ZHAO/<br>Snow LI/<br>Carrie PENG | Preliminary<br>1. Deleted n30 of 5G SA (Table 3).<br>2. Updated the transmitting power of 5G NR and LTE (Table 4 & Chapter 5.1.3).<br>3. Added a note description that driving PWRKEY low for 1.5–2 s may result in an unexpected power-down (Chapter 3.5.1).<br>4. Updated the R11 from “0R” to “22R” in the reference design of eMMC application (Chapter 4.6.1).<br>5. Added the data of RF receiver sensitivity (Table 38).<br>6. Updated the data of power consumption (Table 45).<br>7. Updated the information of thermal dissipation (Chapter 6.7). |

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# 1 Introduction

This document helps you quickly understand the interface specifications, electrical and mechanical details, as well as other related information of the module. To facilitate application designs, it also includes some reference designs for your reference. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

## 1.1. Special Marks

**Table 1: Special Marks**

| Mark  | Definition                                                                                                                                                                                                                                                                                |
|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| *     | Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable. |
| [...] | Brackets ([...]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.                                                                          |

Hereby, WirelessMobility Automotive GmbH declares that the radio equipment type WMC598E-GL is in compliance with Directive 2014/53/EU. This product can be used across EU member states. The full text of the EU declaration of conformity is available at the following internet address:

<https://www.wirelessmobility.com/>

### Disposal of old electrical appliances



The European directive 2012/19/EU on Waste Electrical and Electronic Equipment (WEEE), requires that old household electrical appliances must not be disposed of in the normal unsorted municipal waste stream. Old appliances must be collected separately in order to optimize the recovery and recycling of the materials they contain, and reduce the impact on human health and the environment.

The crossed out “wheeled bin” symbol on the product reminds you of your obligation, that when you dispose of the appliance, it must be separately collected.

Consumers should contact their local authority or retailer for information concerning the correct disposal of their old appliance.

The device could be used with a separation distance of 20cm to the human body.

#### FCC Certification Requirements.

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.

And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based time averaging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.
2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.
3. A label with the following statements must be attached to the host end product: This device contains FCC ID: 2BH2C25WMC598EGL.
4. To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:
5. This module must not transmit simultaneously with any other antenna or transmitter
6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

For this device, OEM integrators must be provided with labeling instructions of finished products.

Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: 2BH2C25WMC598EGL" or "Contains FCC ID: 2BH2C25WMC598EGL" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier's Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.

### **Manual Information To the End User**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as shown in this manual.

### **IC Statement**

#### **IRSS-GEN**

"This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device." or "Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

1) l'appareil ne doit pas produire de brouillage; 2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

#### **Déclaration sur l'exposition aux rayonnements RF**

L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm. de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.

The host product shall be properly labeled to identify the modules within the host product.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word "Contains" or similar wording expressing the same meaning, as follows:

"Contains IC: 32403-WMC598EGL" or "where: 32403-WMC598EGL is the module's certification number".

Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte.

L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installé dans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, précédé du mot «Contient» ou d'un libellé semblable exprimant la même signification, comme suit:

"Contient IC: 32403-WMC598EGL " ou "où: 32403-WMC598EGL est le numéro de certification du module".

## 2 Product Overview

### 2.1. Frequency Bands and Functions

WMC598E-GL is an automotive-grade 5G NR Sub-6 GHz wireless communication module.

**Table 2: Basic Information**

| WMC598E-GL             |                                                                                            |
|------------------------|--------------------------------------------------------------------------------------------|
| Pin number and package | 452 LGA pins                                                                               |
| Dimensions             | (45.0 ±0.2) mm × (45.0 ±0.2) mm × (3.45 ±0.2) mm                                           |
| Weight                 | Approx.17 g                                                                                |
| Wireless technologies  | <ul style="list-style-type: none"> <li>● 5G NR, LTE, WCDMA, GSM</li> <li>● GNSS</li> </ul> |

**Table 3: Frequency Bands and Functions**

| Network Type/Function |         | WMC598E-GL                                                                                      |
|-----------------------|---------|-------------------------------------------------------------------------------------------------|
| 5G NR                 | 5G SA   | n1/n2/n3/n5/n7/n8/n12/n14/n20/n25/n26/n28(A and B)/n38/n40/n41/n48/n66/n70/n71/n77/n78/n79      |
|                       | 5G NSA  | n1/n2/n3/n5/n7/n8/n12/n14/n20/n25/n26/n28(A and B)/n38/n40/n41/n66/n71/n77/n78/n79              |
| LTE                   | LTE-FDD | B1/B2/B3/B4/B5/B7/B8/B12/B13/B14/B17/B18/B19/B20/B25/B26/B28(A and B)/B29 <sup>1</sup> /B66/B71 |
|                       | LTE-TDD | B34/B38/B39/B40/B41/B42/B43/B48                                                                 |
| WCDMA                 |         | B1/B2/B4/B5/B8/B19                                                                              |
| GSM                   |         | GSM850/EGSM900/DCS1800/PCS1900                                                                  |

<sup>1</sup> B29 supports Rx only.

|                  |                                                                                                                                                                                                         |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Dual SIM Feature | DSSA                                                                                                                                                                                                    |
| GNSS (optional)  | <ul style="list-style-type: none"> <li>● Single-band GNSS: L1</li> <li>● Dual-band GNSS: L1 + L5* (optional); L1 + L2* (optional)</li> <li>● Constellation: GPS, GLONASS, BDS, Galileo, QZSS</li> </ul> |

## 2.2. Key Features

The following table describes the detailed features of the module.

**Table 4: Key Features**

| Feature           | Details                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Power Supply      | <ul style="list-style-type: none"> <li>● VBAT_BB/VBAT_RF:</li> <li>● Supply voltage range: 3.3–4.3 V</li> <li>● Typical supply voltage: 3.8 V</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| SMS               | <ul style="list-style-type: none"> <li>● Text and PDU modes</li> <li>● Point-to-point MO and MT</li> <li>● SMS cell broadcast</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| (U)SIM Interfaces | <ul style="list-style-type: none"> <li>● Support dual (U)SIM cards, DSSA (Dual SIM Single Active)</li> <li>● (U)SIM1: 1.8/3.0 V</li> <li>● (U)SIM2: 1.8/3.0 V</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                   |
| USB Interface     | <ul style="list-style-type: none"> <li>● Compliant with USB 3.1 Gen 2 and USB 2.0 specifications, with maximum transmission rates up to 10 Gbps on USB 3.1 and 480 Mbps on USB 2.0</li> <li>● USB 2.0 and USB 3.1 are used for firmware upgrade, AT command communication, data transmission, GNSS NMEA sentences output and software debugging.</li> <li>● When USB 2.0 and USB 3.1 are connected to the same host, USB 2.0 and USB 3.1 cannot be used simultaneously, USB 3.1 takes effect by default.</li> <li>● Support USB serial drivers for Windows 10/11, Linux 2.6–6.7</li> </ul> |
| UART Interfaces   | <p><b>UART1 &amp; UART2:</b></p> <ul style="list-style-type: none"> <li>● Used for data transmission, UART2 is used for Bluetooth connection by default</li> <li>● Baud rate: up to 921600 bps, 9600 bps (default)</li> <li>● Supports RTS and CTS hardware flow control</li> </ul> <p><b>UART3 &amp; UART4:</b></p> <ul style="list-style-type: none"> <li>● Used for data transmission</li> <li>● Baud rate: up to 921600 bps, 9600 bps (default)</li> </ul>                                                                                                                             |

|                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                           | <b>Debug UART:</b> <ul style="list-style-type: none"> <li>● Used for Linux console and log output</li> <li>● 115200 bps baud rate by default</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                        |
| I2S Interfaces                            | <ul style="list-style-type: none"> <li>● Support two I2S interfaces</li> <li>● I2S1 is used for external codec by default</li> <li>● I2S2 can be used according to your application.</li> <li>● Support master and slave modes</li> </ul>                                                                                                                                                                                                                                                                                                                      |
| I2C Interfaces                            | <ul style="list-style-type: none"> <li>● Support two I2C interfaces</li> <li>● I2C1 is used for external audio codec configuration by default</li> <li>● I2C2 is used for IMU by default</li> <li>● Compliant with <i>I2C-bus Specification Version 3.0</i></li> <li>● HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported.</li> </ul>                                                                                                                                                                                             |
| PCM Interface                             | <ul style="list-style-type: none"> <li>● Used for Bluetooth audio data transmission by default</li> <li>● Supports 16-bit linear data format</li> <li>● Supports long frame synchronization and short frame synchronization</li> <li>● Supports master and slave modes</li> </ul>                                                                                                                                                                                                                                                                              |
| SDIO Interfaces                           | <b>SDIO1:</b> <ul style="list-style-type: none"> <li>● Compliant with eMMC 5.1</li> <li>● 4-bit by default, max. up to 8-bit, supports 1.8 V only</li> <li>● SDIO1 can be used for eMMC function</li> </ul> <b>SDIO2:</b> <ul style="list-style-type: none"> <li>● Compliant with SD 3.0</li> <li>● 4-bit by default, supports 1.8 V only</li> <li>● SDIO2 can be used to connect to external DSRC module if required</li> </ul>                                                                                                                               |
| PCIe Interfaces                           | <b>PCIe1:</b> <ul style="list-style-type: none"> <li>● Compliant with <i>PCI Express Base Specification Revision 3.0</i></li> <li>● Support 2 lanes, with maximum rate of 8 GT/s × 1 lane</li> <li>● Support RC and EP modes, works in RC mode by default</li> <li>● Used for WLAN function by default</li> </ul> <b>PCIe2:</b> <ul style="list-style-type: none"> <li>● Compliant with <i>PCI Express Base Specification Revision 3.0</i></li> <li>● Support 1 lane, with maximum rate of 8 GT/s × 1 lane</li> <li>● Support RC configuration only</li> </ul> |
| WLAN and Bluetooth Application Interfaces | <ul style="list-style-type: none"> <li>● Support PCIe1 (Gen 3) interface for WLAN</li> <li>● Support Bluetooth UART and PCM interfaces for Bluetooth</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                |
| SPIs                                      | <ul style="list-style-type: none"> <li>● Support 2 SPIs by default</li> <li>● Support master mode and slave mode</li> <li>● Maximum clock frequency rate: 50 MHz</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                    |
| RGMII Interface                           | <ul style="list-style-type: none"> <li>● Supports 10/100/1000 Mbps Ethernet connection <sup>2</sup></li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

<sup>2</sup> The module's RGMII/SGMII interface supports the Gigabit Ethernet protocol, while actual throughput is subject to testing.

|                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|---------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SGMII Interface                 | <ul style="list-style-type: none"> <li>Supports 1000/2500 Mbps Ethernet connection <sup>2</sup></li> </ul>                                                                                                                                                                                                                                                                                                                                                                                 |
| Antenna Interfaces <sup>3</sup> | <ul style="list-style-type: none"> <li>One main antenna interface (ANT_MAIN)</li> <li>One diversity antenna interface (ANT_DIV)</li> <li>One GNSS antenna interface (ANT_GNSS)</li> </ul>                                                                                                                                                                                                                                                                                                  |
| Temperature Range               | <ul style="list-style-type: none"> <li>Normal operating temperature range <sup>4</sup>: -40 to +85 °C</li> <li>eCall operating temperature range <sup>5</sup>: -40 to +95 °C</li> <li>Storage temperature range: -40 to +95 °C</li> </ul>                                                                                                                                                                                                                                                  |
| AT Commands                     | <ul style="list-style-type: none"> <li>3GPP TS 27.007 and 3GPP TS 27.005 AT commands</li> <li>Wireless Mobility enhanced AT commands</li> </ul>                                                                                                                                                                                                                                                                                                                                            |
| Audio Features                  | <ul style="list-style-type: none"> <li>GSM: HR/FR/EFR/AMR/AMR-WB</li> <li>WCDMA: AMR/AMR-WB</li> <li>LTE/5G: AMR/AMR-WB/EVS</li> <li>Support VoLTE (Voice over LTE)</li> <li>Support echo cancellation and noise suppression</li> </ul>                                                                                                                                                                                                                                                    |
| Transmitting Power              | <b>5G NR:</b> <ul style="list-style-type: none"> <li>5G NR TDD HPUE bands n41: Class 2 (26 dBm <math>\pm</math>2 dB);HPUE bands (n77/n78/n79) Class 2 (26 dBm +1/-2dB)</li> <li>5G NR TDD n48: Class 3 (23 dBm <math>\pm</math>2 dB)</li> <li>5G NR TDD n38/n40: Class 3 (23.5 dBm +1.5/-2 dB)</li> <li>5G NR FDD LB bands (n5/n8/n12/n14/n20/n26/n28/n71): Class 3 (23.7 dBm +1.3/-2 dB)</li> <li>5G NR FDD MHB bands (n1/n2/n3/n7/n25/n66/n70): Class 3 (23.5 dBm +1.5/-2 dB)</li> </ul> |
|                                 | <b>LTE:</b> <ul style="list-style-type: none"> <li>LTE TDD HPUE bands B40/B41: Class 2 (26 dBm <math>\pm</math>2 dB)</li> <li>LTE TDD B42/B43/B48: Class 3 (23 dBm <math>\pm</math>2 dB)</li> <li>LTE TDD B34/B38/B39: Class 3 (23.5 dBm +1.5/-2 dB)</li> <li>LTE FDD LB bands (B5/B8/B12/B13/B14/B17/B18/B19/B20/B26/B28/B71): Class 3 (23.7 dBm +1.3/-2 dB)</li> <li>LTE FDD MHB bands (B1/B2/B3/B4/B7/B25/B66): Class 3 (23.5 dBm +1.5/-2 dB)</li> </ul>                                |
|                                 | <b>WCDMA:</b> <ul style="list-style-type: none"> <li>WCDMA bands: Class 3 (23 dBm <math>\pm</math>2 dB)</li> </ul>                                                                                                                                                                                                                                                                                                                                                                         |
|                                 | <b>GSM:</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

<sup>3</sup> Antenna interfaces are supported as follow:

- 2 antennas (ANT\_MAIN & ANT\_DIV) are supported by default.
- ANT\_MIMO3, ANT\_MIMO4 and ANT\_ECALL are optional but not supported by default, if you need these 3 antennas function, please consult with Wireless Mobility Technical Support.
- GNSS is optional. L1 are supported by default. If you need GNSS dual-band function, please consult with Wireless Mobility Technical Support.

<sup>4</sup> Within the operating temperature range, the module meets 3GPP specifications.

<sup>5</sup> Within eCall temperature range, the eCall function must be functional until the module is broken. When the ambient temperature is between 75 °C and 95 °C and the module temperature has reached the threshold value, the module will trigger protective measures (such as reduce power, decrease throughput and unregister the device) to ensure the full function of eCall.

|                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                | <ul style="list-style-type: none"> <li>● GSM850: Class 4 (33 dBm <math>\pm</math>2 dB)</li> <li>● EGSM900: Class 4 (33 dBm <math>\pm</math>2 dB)</li> <li>● DCS1800: Class 1 (30 dBm <math>\pm</math>2 dB)</li> <li>● PCS1900: Class 1 (30 dBm <math>\pm</math>2 dB)</li> <li>● GSM850 8-PSK: Class E2 (27 dBm <math>\pm</math>3 dB)</li> <li>● EGSM900 8-PSK: Class E2 (27 dBm <math>\pm</math>3 dB)</li> <li>● DCS1800 8-PSK: Class E2 (26 dBm <math>\pm</math>3 dB)</li> <li>● PCS1900 8-PSK: Class E2 (26 dBm <math>\pm</math>3 dB)</li> </ul>                                         |
| 5G NR Features | <ul style="list-style-type: none"> <li>● Support 3GPP Rel-16</li> <li>● Support 5G NR CA up to 2 FR1</li> <li>● Supported modulations:<br/>Uplink: <math>\pi/2</math>-BPSK, QPSK, 16QAM, 64QAM and 256QAM<br/>Downlink: QPSK, 16QAM, 64QAM and 256QAM</li> <li>● Support SCS 15 kHz (FDD) and 30 kHz (TDD)</li> <li>● Support option 3x, 3a and option 2</li> <li>● SRS antenna rotation function can be supported <sup>6</sup></li> <li>● Support SA and NSA</li> <li>● Max. transmission data rates:<br/>NSA: 1.4 Gbps (DL)/625 Mbps (UL)<br/>SA: 1.0 Gbps (DL)/525 Mbps (UL)</li> </ul> |
| LTE Features   | <ul style="list-style-type: none"> <li>● Support LTE-FDD and TDD, up to DL 5CA Cat 16 and UL 2CA Cat 18</li> <li>● Support 1.4/3/5/10/15/20 MHz RF bandwidth</li> <li>● Support modulations:<br/>Uplink: QPSK, 16QAM, 64QAM, 256QAM<br/>Downlink: QPSK, 16QAM, 64QAM, 256QAM</li> <li>● LTE-FDD: Max. 1.0 Gbps (DL)/200 Mbps (UL)</li> <li>● LTE-TDD: Max. 700 Mbps (DL)/120 Mbps (UL)</li> </ul>                                                                                                                                                                                          |
| UMTS Features  | <ul style="list-style-type: none"> <li>● Support 3GPP Rel-9 DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA</li> <li>● Support QPSK, 16QAM and 64QAM modulation</li> <li>● DC-HSDPA: Max. 42 Mbps (DL)</li> <li>● HSUPA: Max. 5.76 Mbps (UL)</li> <li>● WCDMA: Max. 384 kbps (DL)/384 kbps (UL)</li> </ul>                                                                                                                                                                                                                                                                                            |
| GSM Features   | <p><b>GPRS:</b></p> <ul style="list-style-type: none"> <li>● Support GPRS multi-slot class 33 (33 by default)</li> <li>● Coding scheme: CS 1–4</li> <li>● Max. 107 kbps (DL)/85.6 kbps (UL)</li> </ul> <p><b>EDGE:</b></p> <ul style="list-style-type: none"> <li>● Support EDGE multi-slot class 33 (33 by default)</li> <li>● Support GMSK and 8-PSK for different MCS (Modulation and Coding Scheme)</li> <li>● Downlink coding schemes: MCS 1–9</li> <li>● Uplink coding schemes: MCS 1–9</li> </ul>                                                                                   |

<sup>6</sup> SRS function is optional, not supported by default. If you need SRS function, please consult with Wireless Mobility Technical Support.

|                  |                                                                                                                                                                                                                                                                                                                                       |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                  | <ul style="list-style-type: none"> <li>● Max. 296 kbps (DL)/236.8 kbps (UL)</li> </ul>                                                                                                                                                                                                                                                |
| Rx-diversity     | Support 5G NR, LTE and WCDMA Rx-diversity                                                                                                                                                                                                                                                                                             |
| GNSS (Optional)  | <ul style="list-style-type: none"> <li>● Constellation: GPS, GLONASS, BDS, Galileo, QZSS</li> <li>● Augmentation system: SBAS</li> <li>● Single-band GNSS: L1</li> <li>● Dual-band GNSS: L1 + L5* (optional); L1 + L2* (optional)</li> <li>● Protocol: NMEA 0183</li> <li>● Update rate: 1 Hz by default, max. up to 10 Hz</li> </ul> |
| Firmware Upgrade | <ul style="list-style-type: none"> <li>● USB 2.0 or USB 3.1 interface</li> <li>● DFOTA</li> </ul>                                                                                                                                                                                                                                     |
| RoHS             | All hardware components are fully compliant with EU RoHS directive                                                                                                                                                                                                                                                                    |

## 2.3. Pin Assignment

The following figure shows the pin assignment of the module.

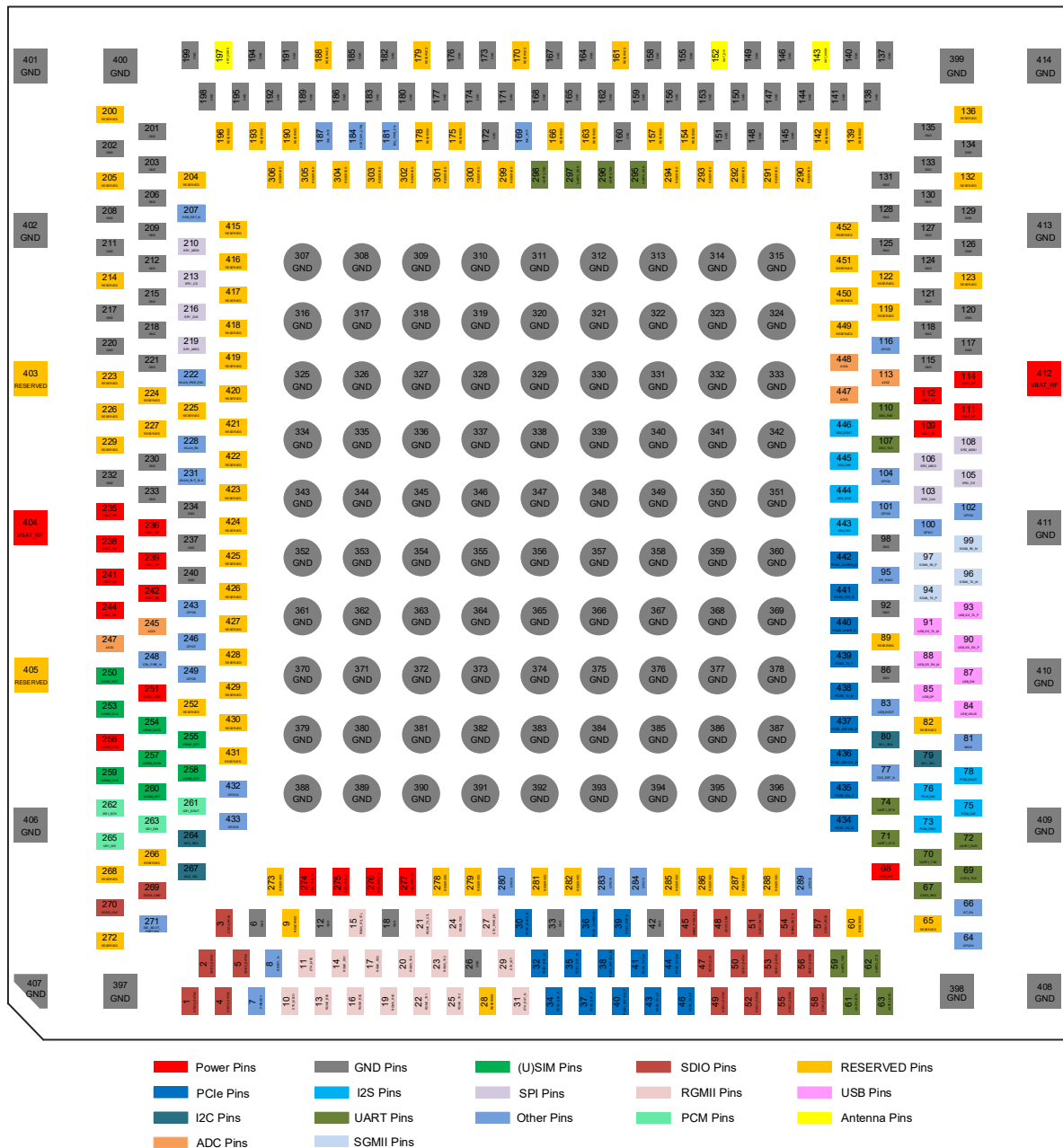


Figure 1: Pin Assignment (Top View)

#### NOTE

1. Unless otherwise specified, keep all RESERVED and unused pins unconnected.
2. GND pins should be connected to ground in the design.
3. Ensure that there is no current sink on the module's pins before the module turns on.

## 2.4. Pin Description

### 2.4.1. Pin Definition

The following tables show the pin definition of the module.

**Table 5: I/O Parameters Definition**

| Symbol | Description          |
|--------|----------------------|
| AI     | Analog Input         |
| AO     | Analog Output        |
| AIO    | Analog Input/Output  |
| DI     | Digital Input        |
| DO     | Digital Output       |
| DIO    | Digital Input/Output |
| OD     | Open Drain           |
| PI     | Power Input          |
| PO     | Power Output         |

DC characteristics include power domain and rated current.

**Table 6: Pin Description**

| Power Supply |                                              |     |                                             |                                              |         |
|--------------|----------------------------------------------|-----|---------------------------------------------|----------------------------------------------|---------|
| Pin Name     | Pin No.                                      | I/O | Description                                 | DC Characteristics                           | Comment |
| VBAT_BB      | 241,<br>242,<br>244                          | PI  | Power supply for the module's baseband part | Vmax = 4.3 V<br>Vmin = 3.3 V<br>Vnom = 3.8 V |         |
| VBAT_RF      | 109,<br>111,<br>112,<br>114,<br>235,<br>236, | PI  | Power supply for the module's RF part       | Vmax = 4.3 V<br>Vmin = 3.3 V<br>Vnom = 3.8 V |         |

|             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |    |                                                           |                                                                                                                               |                                                                                                                                                                                         |  |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|-----------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
|             | 238,<br>239,<br>404,<br>412                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |    |                                                           |                                                                                                                               |                                                                                                                                                                                         |  |
| VDD_EXT     | 68                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | PO | Provide 1.8 V for external circuits                       | Vnom = 1.8 V<br>Max. current in full functionality mode:<br>Iomax = 50 mA<br>Max. current in low power mode:<br>Iomax = 10 mA | This pin can be used to connect with VDD_IO of Wi-Fi & Bluetooth module, it also can be used as power supply for external pull up circuits. A test point is recommended to be reserved. |  |
| VDD_WIFI_VL | 274,<br>275                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | PO | Low-voltage power supply for Wi-Fi & Bluetooth modules    | Vnom = 0.976 V<br>Iomax = 1.7 A                                                                                               |                                                                                                                                                                                         |  |
| VDD_WIFI_VM | 276                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | PO | Medium-voltage power supply for Wi-Fi & Bluetooth modules | Vnom = 1.28 V<br>Iomax = 0.45 A                                                                                               |                                                                                                                                                                                         |  |
| VDD_WIFI_VH | 277                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | PO | High-voltage power supply for Wi-Fi & Bluetooth modules   | Vnom = 1.88 V<br>Iomax = 0.45 A                                                                                               |                                                                                                                                                                                         |  |
| GND         | 6, 12, 18, 26, 33, 42, 86, 92, 98, 115, 117, 118, 120, 121, 124, 125, 126, 127, 128, 129, 130, 131, 133, 134, 135, 137, 138, 140, 141, 144, 145, 146, 147, 148, 149, 150, 151, 153, 155, 156, 158, 159, 160, 162, 164, 165, 167, 168, 171, 172, 173, 174, 176, 177, 180, 182, 183, 185, 186, 189, 191, 192, 194, 195, 198, 199, 201, 202, 203, 206, 208, 209, 211, 212, 215, 217, 218, 220, 221, 230, 232, 233, 234, 237, 240, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 406, 407, 408, 409, 410, 411, 413, 414 |    |                                                           |                                                                                                                               |                                                                                                                                                                                         |  |

| Turn On/Off |         |     |                        |                              |                                                      |
|-------------|---------|-----|------------------------|------------------------------|------------------------------------------------------|
| Pin Name    | Pin No. | I/O | Description            | DC Characteristics           | Comment                                              |
| PWRKEY      | 7       | DI  | Turn on/off the module | V <sub>IL</sub> max = 0.42 V | Pulled up internally. Active low. Due to the voltage |

|           |     |    |                                                  |                                                                                          |                                                                                                                |
|-----------|-----|----|--------------------------------------------------|------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------|
|           |     |    |                                                  |                                                                                          | drop inside the chip, the pin has around 0.75 V level after the module is powered up.                          |
| RESET_N   | 8   | DI | Reset the module                                 | $V_{IHmax} = 1.5\text{ V}$<br>$V_{IHmin} = 0.78\text{ V}$<br>$V_{ILmax} = 0.42\text{ V}$ | Pulled up internally.<br>Active low.<br>A test point is recommended to be reserved if unused.                  |
| CBL_PWR_N | 248 | DI | Cable power-on; initiates power on when grounded | $V_{IHmax} = 2.1\text{ V}$<br>$V_{IHmin} = 1.17\text{ V}$<br>$V_{ILmax} = 0.63\text{ V}$ | Pulled up internally.<br>Active low.<br>Pulling it low for an extended period will not trigger hardware reset. |

#### GPIO Interfaces

| Pin Name | Pin No. | I/O | Configurable Function | DC Characteristics | Comment                                                                                                                        |
|----------|---------|-----|-----------------------|--------------------|--------------------------------------------------------------------------------------------------------------------------------|
| GPIO1    | 100     | DI  | WAKEUP_IN             | 1.8 V              | Used as WAKEUP_IN by default. If the default function is not used, it can be configured to GPIO.<br>Support wake-up interrupt. |
|          |         | DIO | GPIO                  |                    | General-purpose input/output.<br>Support wake-up interrupt.                                                                    |
| GPIO2    | 101     | DIO | GPIO                  |                    | Support wake-up interrupt.                                                                                                     |
| GPIO3    | 102     | DIO | GPIO                  |                    | General-purpose input/output.<br><b>Not</b> support wake-up interrupt.                                                         |
| GPIO4    | 104     | DO  | SLEEP_SYS_IND         |                    | Used as SLEEP_SYS_IND by default. If the default function is                                                                   |

|        |     |     |        |                                                                                                                                        |
|--------|-----|-----|--------|----------------------------------------------------------------------------------------------------------------------------------------|
|        |     |     |        |                                                                                                                                        |
|        |     | DIO | GPIO   |                                                                                                                                        |
| GPIO5  | 116 | DIO | GPIO   | General-purpose input/output.<br>Support wake-up interrupt.                                                                            |
| GPIO6  | 243 | DO  | STATUS | Used as STATUS by default. If the default function is not used, it can be configured to GPIO.<br><b>Not</b> support wake-up interrupt. |
|        |     | DIO | GPIO   | General-purpose input/output.<br><b>Not</b> support wake-up interrupt.                                                                 |
| GPIO7  | 246 | DIO | GPIO   | General-purpose input/output.<br>Support wake-up interrupt.                                                                            |
| GPIO8  | 249 | DIO | GPIO   |                                                                                                                                        |
| GPIO9  | 280 | DIO | GPIO   |                                                                                                                                        |
| GPIO10 | 283 | DIO | GPIO   |                                                                                                                                        |
| GPIO11 | 284 | DIO | GPIO   |                                                                                                                                        |
| GPIO12 | 289 | DIO | GPIO   |                                                                                                                                        |
| GPIO13 | 64  | DIO | GPIO   |                                                                                                                                        |
| GPIO14 | 432 | DIO | GPIO   |                                                                                                                                        |
| GPIO15 | 433 | DIO | GPIO   |                                                                                                                                        |

#### USB Interface

| Pin Name | Pin No. | I/O | Description | DC | Comment |
|----------|---------|-----|-------------|----|---------|
|----------|---------|-----|-------------|----|---------|

|                   |         |     |                                 |                                                                 | Characteristics                                                                                                                                                                                                                    |
|-------------------|---------|-----|---------------------------------|-----------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| USB_VBUS          | 84      | DI  | USB connection detect           | Vmax = 5.25 V<br>Vmin = 3.0 V<br>Vnom = 5.0 V                   | Maximum current: 0.1 mA.<br>A 47 kΩ resistor is connected in series inside the module.<br>If the debugging function is required, the connector cannot be occupied by other functions, otherwise, test points must be reserved.     |
| USB_DP            | 85      | AIO | USB 2.0 differential data (+)   |                                                                 | Compliant with USB 2.0 standard specifications.<br>Require differential impedance of 90 Ω.<br>If the debugging function is required, the connector cannot be occupied by other functions, otherwise, test points must be reserved. |
| USB_DM            | 87      | AIO | USB 2.0 differential data (-)   |                                                                 |                                                                                                                                                                                                                                    |
| USB_SS_TX_P       | 93      | AO  | USB 3.1 SuperSpeed transmit (+) |                                                                 | Compliant with USB 3.1 standard specifications.<br>Require differential impedance of 70–100 Ω, and 85 Ω is recommended.                                                                                                            |
| USB_SS_TX_M       | 91      | AO  | USB 3.1 SuperSpeed transmit (-) |                                                                 |                                                                                                                                                                                                                                    |
| USB_SS_RX_P       | 90      | AI  | USB 3.1 SuperSpeed receive (+)  |                                                                 |                                                                                                                                                                                                                                    |
| USB_SS_RX_M       | 88      | AI  | USB 3.1 SuperSpeed receive (-)  |                                                                 |                                                                                                                                                                                                                                    |
| (U)SIM Interfaces |         |     |                                 |                                                                 |                                                                                                                                                                                                                                    |
| Pin Name          | Pin No. | I/O | Description                     | DC Characteristics                                              | Comment                                                                                                                                                                                                                            |
| USIM1_VDD         | 251     | PO  | (U)SIM1 card power supply       | High-voltage:<br>Vmin = 2.7 V<br>Vnom = 2.95 V<br>Vmax = 3.05 V | Either 1.8 V or 3.0 V is supported by the module automatically.                                                                                                                                                                    |

|            |     |     |                              |                                                                                                                                                 |                                                                 |                            |
|------------|-----|-----|------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------|----------------------------|
|            |     |     |                              | <b>Low-voltage:</b><br>Vmin = 1.65 V<br>Vnom = 1.8 V<br>Vmax = 1.95 V                                                                           |                                                                 |                            |
| USIM1_DATA | 254 | DIO | (U)SIM1 card data            | USIM1_VDD                                                                                                                                       | Either 1.8 V or 3.0 V is supported by the module automatically. |                            |
| USIM1_RST  | 250 | DO  | (U)SIM1 card reset           |                                                                                                                                                 |                                                                 |                            |
| USIM1_CLK  | 253 | DO  | (U)SIM1 card clock           |                                                                                                                                                 |                                                                 |                            |
|            |     |     |                              | <b>High-voltage:</b><br>Vmin = 2.7 V<br>Vnom = 2.95 V<br>Vmax = 3.05 V<br><b>Low-voltage:</b><br>Vmin = 1.65 V<br>Vnom = 1.8 V<br>Vmax = 1.95 V |                                                                 |                            |
| USIM2_VDD  | 256 | PO  | (U)SIM2 card power supply    |                                                                                                                                                 |                                                                 |                            |
| USIM2_DATA | 257 | DIO | (U)SIM2 card data            | USIM2_VDD                                                                                                                                       |                                                                 |                            |
| USIM2_RST  | 260 | DO  | (U)SIM2 card reset           |                                                                                                                                                 |                                                                 |                            |
| USIM2_CLK  | 259 | DO  | (U)SIM2 card clock           |                                                                                                                                                 |                                                                 |                            |
| USIM1_DET  | 255 | DI  | (U)SIM1 card hot-plug detect | 1.8 V                                                                                                                                           |                                                                 | If unused, keep them open. |
| USIM2_DET  | 258 | DI  | (U)SIM2 card hot-plug detect |                                                                                                                                                 |                                                                 |                            |

#### UART1, UART3 and UART4 Interfaces

| Pin Name  | Pin No. | I/O | Description                          | DC Characteristics | Comment                                               |
|-----------|---------|-----|--------------------------------------|--------------------|-------------------------------------------------------|
| UART1_CTS | 71      | DO  | Clear to send signal from the module | 1.8 V              | If unused, keep it open.<br>Connect to the MCU's CTS. |
| UART1_RTS | 74      | DI  | Request to send signal to the module |                    | If unused, keep it open.<br>Connect to the MCU's RTS. |
| UART1_TXD | 70      | DO  | UART1 transmit                       |                    | If unused, keep these pins open.                      |
| UART1_RXD | 72      | DI  | UART1 receive                        |                    |                                                       |
| UART3_TXD | 298     | DO  | UART3 transmit                       |                    |                                                       |

|           |     |    |                |
|-----------|-----|----|----------------|
| UART3_RXD | 297 | DI | UART3 receive  |
| UART4_TXD | 296 | DO | UART4 transmit |
| UART4_RXD | 295 | DI | UART4 receive  |

#### UART2 (Bluetooth UART) Interface

| Pin Name  | Pin No. | I/O | Description                          | DC Characteristics | Comment                                                                        |
|-----------|---------|-----|--------------------------------------|--------------------|--------------------------------------------------------------------------------|
| UART2_TXD | 59      | DO  | Bluetooth UART transmit              | 1.8 V              | If unused, keep them open.                                                     |
| UART2_RXD | 63      | DI  | Bluetooth UART receive               |                    |                                                                                |
| UART2_RTS | 61      | DI  | Request to send signal to the module |                    | If unused, keep it open.<br>Connect to the MCU/Wi-Fi & Bluetooth module's RTS. |
| UART2_CTS | 62      | DO  | Clear to send signal from the module |                    | If unused, keep it open.<br>Connect to the MCU/Wi-Fi & Bluetooth module's CTS. |

#### Debug UART Interface

| Pin Name | Pin No. | I/O | Description         | DC Characteristics | Comment                       |
|----------|---------|-----|---------------------|--------------------|-------------------------------|
| DBG_RXD  | 110     | DI  | Debug UART receive  | 1.8 V              | Test points must be reserved. |
| DBG_TXD  | 107     | DO  | Debug UART transmit |                    |                               |

#### I2C Interface

| Pin Name | Pin No. | I/O | Description       | DC Characteristics | Comment                                                                |
|----------|---------|-----|-------------------|--------------------|------------------------------------------------------------------------|
| I2C1_SCL | 79      | OD  | I2C1 serial clock | 1.8 V              | External pull-up resistors are required.<br>If unused, keep them open. |
| I2C1_SDA | 80      | OD  | I2C1 serial data  |                    |                                                                        |
| I2C2_SCL | 267     | OD  | I2C2 serial clock |                    |                                                                        |
| I2C2_SDA | 264     | OD  | I2C2 serial data  |                    |                                                                        |

| I2S Interface   |         |     |                        |                    |                                         |
|-----------------|---------|-----|------------------------|--------------------|-----------------------------------------|
| Pin Name        | Pin No. | I/O | Description            | DC Characteristics | Comment                                 |
| CDC_RST_N       | 77      | DO  | External codec reset   | 1.8 V              |                                         |
| MCLK            | 81      | DO  | Clock output for codec |                    | 12.288 MHz clock output                 |
| I2S1_WS         | 265     | DIO | I2S1 word select       |                    | Serve as output signals in master mode. |
| I2S1_SCK        | 262     | DIO | I2S1 clock             | 1.8 V              | Serve as input signals in slave mode.   |
| I2S1_DIN        | 263     | DI  | I2S1 data in           |                    |                                         |
| I2S1_DOUT       | 261     | DO  | I2S1 data out          |                    |                                         |
| I2S2_WS         | 443     | DIO | I2S2 word select       |                    | Serve as output signals in master mode. |
| I2S2_SCK        | 444     | DIO | I2S2 clock             | 1.8 V              | Serve as input signals in slave mode.   |
| I2S2_DIN        | 445     | DI  | I2S2 data in           |                    |                                         |
| I2S2_DOUT       | 446     | DO  | I2S2 data out          |                    |                                         |
| PCM Interface   |         |     |                        |                    |                                         |
| Pin Name        | Pin No. | I/O | Description            | DC Characteristics | Comment                                 |
| PCM_SYNC        | 73      | DIO | PCM data frame sync    |                    | Serve as output signals in master mode. |
| PCM_CLK         | 75      | DIO | PCM clock              | 1.8 V              | Serve as input signals in slave mode.   |
| PCM_DIN         | 76      | DI  | PCM data input         |                    |                                         |
| PCM_DOUT        | 78      | DO  | PCM data output        |                    |                                         |
| PCIe1 Interface |         |     |                        |                    |                                         |
| Pin Name        | Pin No. | I/O | Description            | DC Characteristics | Comment                                 |

|                |    |     |                           |                                                                                                                                                            |
|----------------|----|-----|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PCIE1_REFCLK_P | 40 | AIO | PCIE1 reference clock (+) | Serve as output signals in RC mode.<br>Serve as input signals in EP mode.<br>The differential impedance should be the same as that for PCIE_TX/RX.         |
| PCIE1_REFCLK_M | 38 | AIO | PCIE1 reference clock (-) |                                                                                                                                                            |
| PCIE1_TX0_P    | 46 | AO  | PCIE1 transmit 0 (+)      | If PCIE1_TX and PCIE1_RX are unused, keep these pins unconnected.<br>Require differential impedance of 70–100 $\Omega$ , and 85 $\Omega$ is recommended.   |
| PCIE1_TX0_M    | 44 | AO  | PCIE1 transmit 0 (-)      |                                                                                                                                                            |
| PCIE1_RX0_P    | 34 | AI  | PCIE1 receive 0 (+)       |                                                                                                                                                            |
| PCIE1_RX0_M    | 32 | AI  | PCIE1 receive 0 (-)       |                                                                                                                                                            |
| PCIE1_TX1_P    | 43 | AO  | PCIE1 transmit 1 (+)      |                                                                                                                                                            |
| PCIE1_TX1_M    | 41 | AO  | PCIE1 transmit 1 (-)      |                                                                                                                                                            |
| PCIE1_RX1_P    | 37 | AI  | PCIE1 receive 1 (+)       |                                                                                                                                                            |
| PCIE1_RX1_M    | 35 | AI  | PCIE1 receive 1 (-)       |                                                                                                                                                            |
| PCIE1_CLKREQ_N | 36 | DIO | PCIE1 clock request       | Serve as input signals in RC mode.<br>Serve as output signals in EP mode.<br>Serve as an output signal in RC mode.<br>Serve as an input signal in EP mode. |
| PCIE1_WAKE_N   | 30 | DIO | PCIE1 wake up             |                                                                                                                                                            |
| PCIE1_RST_N    | 39 | DIO | PCIE1 reset               |                                                                                                                                                            |

1.8 V

#### PCIE2 Interface

| Pin Name       | Pin No. | I/O | Description               | DC Characteristics | Comment                                                                   |
|----------------|---------|-----|---------------------------|--------------------|---------------------------------------------------------------------------|
| PCIE2_REFCLK_P | 437     | AO  | PCIE2 reference clock (+) |                    | Only used in RC mode.<br>The differential impedance should be the same as |
| PCIE2_REFCLK_M | 436     | AO  | PCIE2 reference clock (-) |                    |                                                                           |

|                |     |    |                     |       |                                                                                                                                        |
|----------------|-----|----|---------------------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
|                |     |    |                     |       | that for PCIE_TX/RX.                                                                                                                   |
| PCIE2_TX_P     | 439 | AO | PCle2 transmit (+)  |       | If PCIE2_TX and PCIE2_RX are unused, keep these pins unconnected. Require differential impedance of 70–100 Ω, and 85 Ω is recommended. |
| PCIE2_TX_M     | 438 | AO | PCle2 transmit (-)  |       |                                                                                                                                        |
| PCIE2_RX_P     | 435 | AI | PCle2 receive (+)   |       |                                                                                                                                        |
| PCIE2_RX_M     | 434 | AI | PCle2 receive (-)   |       |                                                                                                                                        |
| PCIE2_CLKREQ_N | 442 | DI | PCle2 clock request |       | Only used in RC mode.                                                                                                                  |
| PCIE2_WAKE_N   | 440 | DI | PCle2 wake up       | 1.8 V |                                                                                                                                        |
| PCIE2_RST_N    | 441 | DO | PCle2 reset         |       | Only used in RC mode.                                                                                                                  |

#### WLAN and Bluetooth Application Interfaces

| Pin Name     | Pin No. | I/O | Description                                 | DC Characteristics | Comment                                          |
|--------------|---------|-----|---------------------------------------------|--------------------|--------------------------------------------------|
| WLAN_PWR_EN1 | 222     | DO  | WLAN power supply enable control 1          | 1.8 V              | Used for Wi-Fi & Bluetooth module power control. |
| BT_EN        | 66      | DO  | Bluetooth enable control                    |                    |                                                  |
| WLAN_SLP_CLK | 231     | DO  | WLAN 32 kHz sleep clock                     | 1.8 V              | If unused, keep it open.                         |
| WLAN_EN      | 228     | DO  | WLAN function enable control                |                    |                                                  |
| HOST_SW_CTRL | 184     | DI  | Switch control                              |                    | Output signal from Wi-Fi & Bluetooth module.     |
| COEX_RXD     | 67      | DI  | LTE & WLAN & Bluetooth coexistence receive  | 1.8 V              |                                                  |
| COEX_TXD     | 69      | DO  | LTE & WLAN & Bluetooth coexistence transmit |                    |                                                  |

#### Ethernet Management and Control Interfaces

| Pin Name | Pin No. | I/O | Description | DC Characteristics | Comment       |
|----------|---------|-----|-------------|--------------------|---------------|
| ETH_MDIO | 10      | DIO | Ethernet    | 1.8 V              | Add a pull-up |

|                 |         |     |                                                    |                    |                                                                                                                     |
|-----------------|---------|-----|----------------------------------------------------|--------------------|---------------------------------------------------------------------------------------------------------------------|
| management data |         |     |                                                    | 1.8 V              | resistor to this pin, and place the resistor close to the external PHY.                                             |
| ETH_MDC         | 11      | DO  | Ethernet management clock                          |                    | Do not add any pull-up resistor to this pin, otherwise it may cause higher power consumption during low power mode. |
| ETH_PWR_EN      | 27      | DO  | Enable external power supply to power Ethernet PHY |                    |                                                                                                                     |
| ETH_INT         | 29      | DI  | Ethernet PHY interrupt                             |                    |                                                                                                                     |
| ETH_RST_N       | 31      | DO  | Ethernet PHY reset                                 |                    |                                                                                                                     |
| SGMII Interface |         |     |                                                    |                    |                                                                                                                     |
| Pin Name        | Pin No. | I/O | Description                                        | DC Characteristics | Comment                                                                                                             |
| SGMII_TX_P      | 94      | AO  | SGMII transmit (+)                                 |                    | Require differential impedance of 90–110 Ω, and 100 Ω is recommended. 100 nF AC coupling capacitor is required.     |
| SGMII_TX_M      | 96      | AO  | SGMII transmit (-)                                 |                    |                                                                                                                     |
| SGMII_RX_P      | 97      | AI  | SGMII receive (+)                                  |                    |                                                                                                                     |
| SGMII_RX_M      | 99      | AI  | SGMII receive (-)                                  |                    |                                                                                                                     |
| RGMII Interface |         |     |                                                    |                    |                                                                                                                     |
| Pin Name        | Pin No. | I/O | Description                                        | DC Characteristics | Comment                                                                                                             |
| RGMII_RXC       | 19      | DI  | RGMII receive clock                                | 1.8 V              | The single-ended impedance requires 50 Ω.                                                                           |
| RGMII_RX_CTL    | 15      | DI  | RGMII receive control                              |                    |                                                                                                                     |
| RGMII_RX0       | 13      | DI  | RGMII receive data bit 0                           |                    |                                                                                                                     |
| RGMII_RX1       | 14      | DI  | RGMII receive data bit 1                           |                    |                                                                                                                     |
| RGMII_RX2       | 16      | DI  | RGMII receive data bit 2                           |                    |                                                                                                                     |

|              |    |    |                           |
|--------------|----|----|---------------------------|
| RGMII_RX3    | 17 | DI | RGMII receive data bit 3  |
| RGMII_TXC    | 24 | DO | RGMII transmit clock      |
| RGMII_TX_CTL | 21 | DO | RGMII transmit control    |
| RGMII_TX0    | 20 | DO | RGMII transmit data bit 0 |
| RGMII_TX1    | 22 | DO | RGMII transmit data bit 1 |
| RGMII_TX2    | 23 | DO | RGMII transmit data bit 2 |
| RGMII_TX3    | 25 | DO | RGMII transmit data bit 3 |

#### SDIO1 Interface

| Pin Name    | Pin No. | I/O | Description                      | DC Characteristics | Comment                               |
|-------------|---------|-----|----------------------------------|--------------------|---------------------------------------|
| SDIO1_DATA0 | 49      | DIO | SDIO1 data bit 0                 | 1.8 V              |                                       |
| SDIO1_DATA1 | 50      | DIO | SDIO1 data bit 1                 |                    |                                       |
| SDIO1_DATA2 | 51      | DIO | SDIO1 data bit 2                 |                    |                                       |
| SDIO1_DATA3 | 52      | DIO | SDIO1 data bit 3                 |                    |                                       |
| SDIO1_CMD   | 48      | DIO | SDIO1 command                    |                    |                                       |
| SDIO1_CLK   | 47      | DO  | SDIO1 clock                      |                    |                                       |
| SDIO1_RCLK  | 57      | DI  | SDIO1 return clock               |                    |                                       |
| SDIO1_DATA4 | 53      | DIO | SDIO1 data bit 4                 | 1.8 V              | This pin is not supported by default. |
| SDIO1_DATA5 | 55      | DIO | SDIO1 data bit 5                 |                    |                                       |
| SDIO1_DATA6 | 56      | DIO | SDIO1 data bit 6                 |                    |                                       |
| SDIO1_DATA7 | 58      | DIO | SDIO1 data bit 7                 |                    |                                       |
| EMMC_RST_N  | 54      | DO  | eMMC reset                       | 1.8 V              |                                       |
| EMMC_PWR_EN | 45      | DO  | eMMC power supply enable control |                    |                                       |

#### SDIO2 Interface

| Pin Name    | Pin No. | I/O | Description        | DC Characteristics | Comment |
|-------------|---------|-----|--------------------|--------------------|---------|
| SDIO2_DATA0 | 1       | DIO | SDIO2 data bit 0   | 1.8 V              |         |
| SDIO2_DATA1 | 2       | DIO | SDIO2 data bit 1   |                    |         |
| SDIO2_DATA2 | 4       | DIO | SDIO2 data bit 2   |                    |         |
| SDIO2_DATA3 | 5       | DIO | SDIO2 data bit 3   |                    |         |
| SDIO2_CMD   | 269     | DIO | SDIO2 command      |                    |         |
| SDIO2_CLK   | 270     | DO  | SDIO2 clock        |                    |         |
| SDIO2_RCLK  | 3       | DI  | SDIO2 return clock |                    |         |

#### Antenna Interfaces <sup>7</sup>

| Pin Name | Pin No. | I/O | Description                 | DC Characteristics | Comment               |
|----------|---------|-----|-----------------------------|--------------------|-----------------------|
| ANT_MAIN | 143     | AIO | Main antenna interface      |                    | 50 $\Omega$ impedance |
| ANT_DIV  | 152     | AIO | Diversity antenna interface |                    |                       |
| ANT_GNSS | 197     | AI  | GNSS antenna interface      |                    |                       |

#### SPIs

| Pin Name  | Pin No. | I/O | Description              | DC Characteristics | Comment                                                                                                               |
|-----------|---------|-----|--------------------------|--------------------|-----------------------------------------------------------------------------------------------------------------------|
| SPI1_CLK  | 216     | DO  | SPI1 clock               | 1.8 V              | SPI supports master mode by default. Contact Wireless Mobility Technical Support if slave mode needs to be supported. |
| SPI1_CS   | 213     | DO  | SPI1 chip select         |                    |                                                                                                                       |
| SPI1_MISO | 219     | DI  | SPI1 master-in slave-out |                    |                                                                                                                       |
| SPI1_MOSI | 210     | DO  | SPI1 master-out slave-in |                    |                                                                                                                       |
| SPI2_CLK  | 103     | DO  | SPI2 clock               |                    |                                                                                                                       |

<sup>7</sup> Antenna interfaces are supported as follow:

- 2 antennas (ANT\_MAIN & ANT\_DIV) are supported by default.
- ANT\_MIMO3, ANT\_MIMO4 and ANT\_ECALL are optional but not supported by default. If you need the 3 antennas function, please consult with Wireless Mobility Technical Support.
- ANT\_MIMO3 and ANT\_MIMO4 can be multiplexed from RESERVED (pin 161, pin 170) pins. ANT\_ECALL can be multiplexed from RESERVED (pin 179).
- GNSS is optional. L1 are supported by default. If you need GNSS dual-band function, please consult with Wireless Mobility Technical Support.

|           |     |    |                          |
|-----------|-----|----|--------------------------|
| SPI2_CS   | 105 | DO | SPI2 chip select         |
| SPI2_MISO | 106 | DI | SPI2 master-in slave-out |
| SPI2_MOSI | 108 | DO | SPI2 master-out slave-in |

#### ADC Interfaces

| Pin Name | Pin No. | I/O | Description                    | DC Characteristics                | Comment |
|----------|---------|-----|--------------------------------|-----------------------------------|---------|
| ADC0     | 247     | AI  | General-purpose ADC0 interface | Input voltage range:<br>0–1.875 V |         |
| ADC1     | 245     | AI  | General-purpose ADC1 interface |                                   |         |
| ADC2     | 113     | AI  | General-purpose ADC2 interface |                                   |         |
| ADC3     | 447     | AI  | General-purpose ADC3 interface |                                   |         |
| ADC4     | 448     | AI  | General-purpose ADC4 interface |                                   |         |

#### Other Interfaces

| Pin Name            | Pin No. | I/O | Description                                  | DC Characteristics | Comment                                                                                                                                                                       |
|---------------------|---------|-----|----------------------------------------------|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| USB_BOOT            | 83      | DI  | Force the module into download mode          | 1.8 V              | Active high.<br>It is recommended to reserve test points.                                                                                                                     |
| SEL_BOOT_PARTITION* | 271     | DI  | Select to boot from A or B partition address |                    | By default, the module boots from A partition address. When this pin is pulled high, the module will boot from B partition address when it restarts. If unused, keep it open. |
| DR_SYNC             | 95      | DO  | Dead reckoning sync                          |                    |                                                                                                                                                                               |
| IMU_PWR_EN          | 181     | DO  | IMU power enable control                     |                    | If unused, keep these pins open.                                                                                                                                              |
| IMU_INT1            | 169     | DI  | IMU interrupt 1                              |                    |                                                                                                                                                                               |

|           |     |    |                    |
|-----------|-----|----|--------------------|
| IMU_INT2  | 187 | DI | IMU interrupt 2    |
| HSM_RST_N | 207 | DO | External HSM reset |

#### RESERVED Pins

| Pin Name | Pin No.                                                                                                                                                                                                                                                                                                                                                                                                                          | Comment               |
|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| RESERVED | 9, 28, 60, 65, 82, 89, 119, 122, 123, 132, 136, 139, 142, 154, 157, 161, 163, 166, 170, 175, 178, 179, 188, 190, 193, 196, 200, 204, 205, 214, 223, 224, 225, 226, 227, 229, 252, 266, 268, 272, 273, 278, 279, 281, 282, 285, 286, 287, 288, 290, 291, 292, 293, 294, 299, 300, 301, 302, 303, 304, 305, 306, 403, 405, 415, 416, 417, 418, 419, 420, 421, 422, 423, 424, 425, 426, 427, 428, 429, 430, 431, 449, 450, 451, 452 | Keep these pins open. |

NOTE

1. Unless otherwise specified, keep all RESERVED and unused pins unconnected.
2. GND pins should be connected to ground in the design.
3. To reduce the probability of module damage and extend module service life, do not power up and down frequently.

## 2.4.2. Pin Multiplexing

For more details about pin multiplexing of the module, please contact Wireless Mobility Technical Support.

## 2.5. EVB Kit

Wireless Mobility supplies an evaluation board (V2X&5G EVB) with accessories to develop or test the module. For more details, please contact Wireless Mobility Technical Support.

# 3 Operating Characteristics

## 3.1. Operating Modes

The table below briefly summarizes the various operating modes of the module.

**Table 7: Overview of Operating Modes**

| Mode                       | Details                                                                                                                                                                                                                            |                                                                                                                            |
|----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------|
| Full Functionality Mode    | Idle                                                                                                                                                                                                                               | The module remains registered on the network, and is ready to send and receive data. In this mode, the software is active. |
|                            | Voice/Data                                                                                                                                                                                                                         | The module is connected to network. Its power consumption varies with the network setting and data transfer rate.          |
| Minimum Functionality Mode | <b>AT+CFUN=0</b> or device management related API function can set the module into a minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.                     |                                                                                                                            |
| Airplane Mode              | <b>AT+CFUN=4</b> or device management related API function can set the module into airplane mode where the RF function is invalid.                                                                                                 |                                                                                                                            |
| Low Power Mode             | The module remains the ability to receive paging message, SMS, voice call and TCP/UDP data from the network normally. In this mode, the power consumption of the module is reduced to a very low level.                            |                                                                                                                            |
| Power Down Mode            | The module's power supply is cut off by its power management unit. In this mode, the software is inactive, the serial interfaces are inaccessible, while the operating voltage (connected to VBAT_RF and VBAT_BB) remains applied. |                                                                                                                            |

### NOTE

For more details about device management API functions and **AT+CFUN**, please contact Wireless Mobility Technical Support.

## 3.2. Power Saving

### 3.2.1. Low Power Mode (LPM)

The module is able to reduce its power consumption to an ultra-low level during the low power mode. This chapter mainly introduces methods to enter or exit LPM. The diagram below illustrates the power consumption of the module during LPM. For more details about LPM of the module, please contact Wireless Mobility Technical Support.

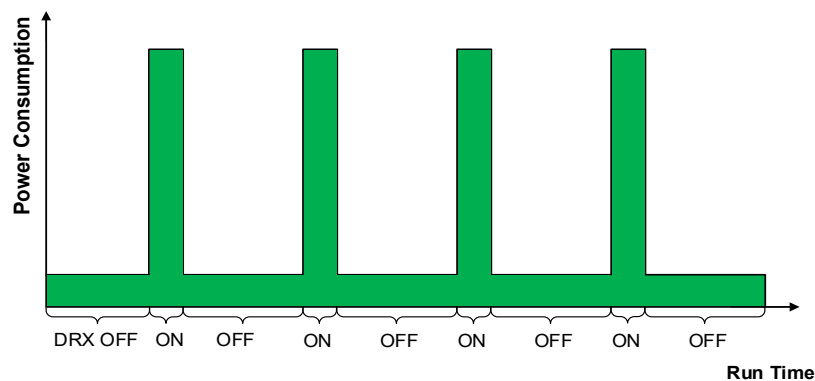


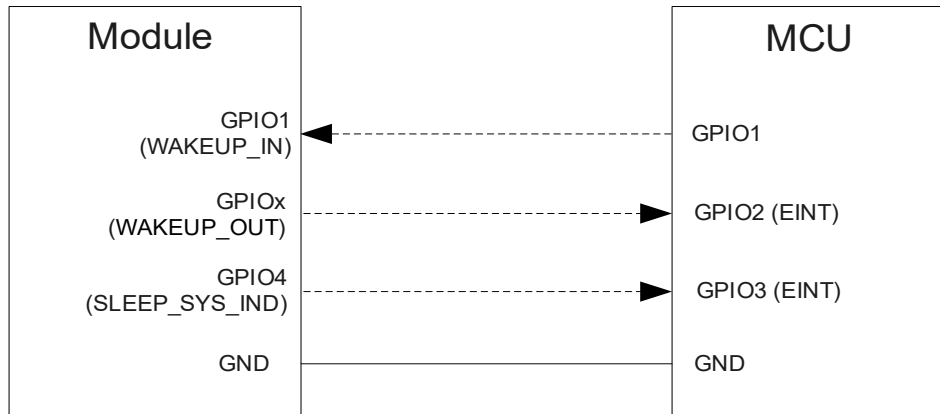
Figure 2: Module Power Consumption in Low Power Mode

#### NOTE

DRX cycle values are transmitted over the wireless network.

#### 3.2.1.1. LPM and Wakeup Functions

The module provides some specific GPIOs to implement the LPM/wakeup function between the module and the MCU.



**Figure 3: LPM/Wakeup Function Implementation Schematic Diagram**

**Table 8: GPIO Configuration Related to LPM/Wakeup Function**

| Pin Name | Pin No.        | Default Function | Status Indication                                                                                                                                                    |
|----------|----------------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO1    | 100            | WAKEUP_IN        | <ul style="list-style-type: none"> <li>Falling edge: MCU controls the module to enter LPM</li> <li>Rising edge: MCU wakes up from LPM</li> </ul>                     |
| GPIO4    | 104            | SLEEP_SYS_IND    | <ul style="list-style-type: none"> <li>Low level: the module enters LPM by default</li> <li>High level: the module exits LPM by default</li> </ul>                   |
| GPIOx    | User Specified | WAKEUP_OUT       | Recommended design: <ul style="list-style-type: none"> <li>Low level: the user application enters LPM</li> <li>High level: the user application exits LPM</li> </ul> |

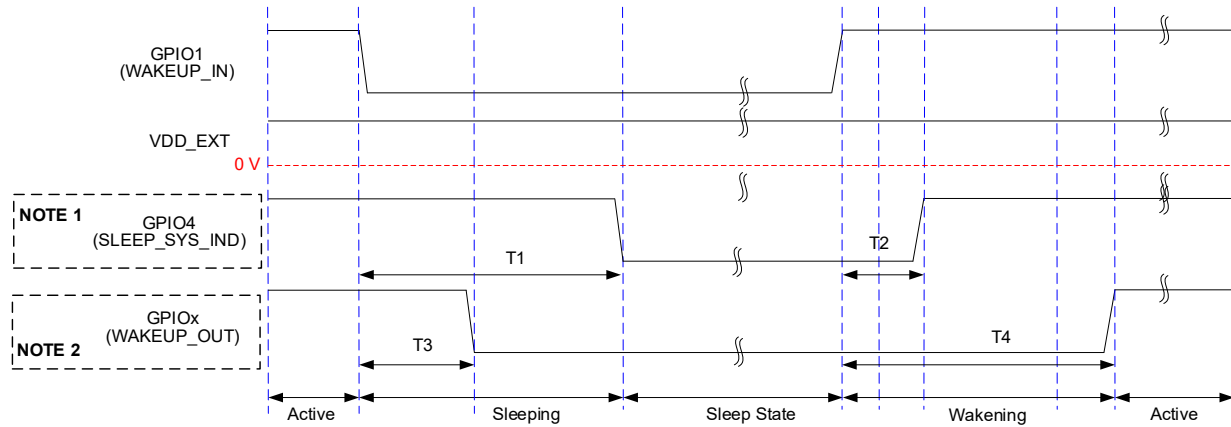
For more details about LPM of the module, please contact Wireless Mobility Technical Support.

#### NOTE

1. Pay attention to the voltage-level matching of the circuit in dotted line, when the MCU interface is not 1.8 V power domain.
2. GPIO1 of the module is used as WAKEUP\_IN (input signal) by default, through which the MCU informs the module to enter/exit LPM.
3. GPIOx can be any GPIO of the module, i.e., you can define any GPIO into WAKEUP\_OUT (output signal).

#### 3.2.1.2. LPM and Wakeup Timing

The following figure shows the LPM and wakeup timing of the module.



**Figure 4: LPM Wakeup Timing**

#### NOTE

1. The time (T1) between the falling edges of WAKEUP\_IN and SLEEP\_SYS\_IND depends on the real application scenario. If the module needs to process any task during the period, the time will be longer.
2. T3 and T4 depends on the application.

### 3.2.2. Airplane Mode

When the module enters airplane mode, the RF function does not work, all AT commands and API functions correlative with RF function will be inaccessible.

#### AT command:

The mode can be set via **AT+CFUN=<fun>**. The parameter **<fun>** of **AT+CFUN** indicates the module's functionality levels, as shown below.

- **AT+CFUN=0**: Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1**: Full functionality mode (by default).
- **AT+CFUN=4**: Airplane mode. RF function is disabled.

#### API functions:

The mode can be set via device management related API functions. For more information about device management API functions, please contact Wireless Mobility Technical Support.

#### NOTE

The execution of **AT+CFUN** or related API functions will not affect GNSS function.

### 3.3. Power Supply

#### 3.3.1. Power Supply Pins

The module provides VBAT pin for connection with external power supplies. VBAT pins are separately used to supply power for three parts of the module.

- 10 VBAT\_RF pins for module's RF part, distributed on two sides of the module.
- 3 VBAT\_BB pins for module's baseband part.

The following table shows the details of VBAT pins and ground pins.

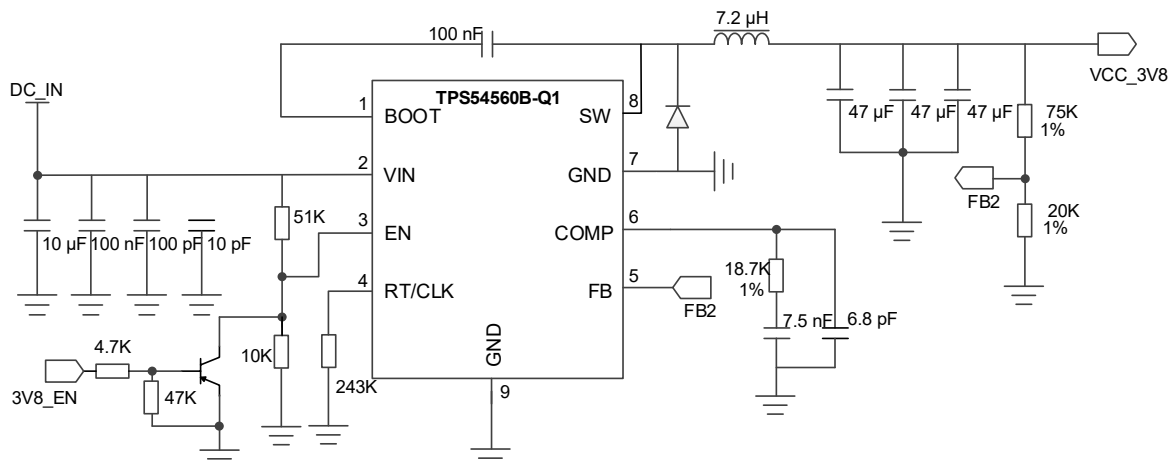
**Table 9: VBAT and GND Pins**

| Pin Name | Pin No.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Description                                 | Min. | Typ. | Max. | Unit |
|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|------|------|------|------|
| VBAT_RF  | 109, 111, 112, 114, 235, 236, 238, 239, 404, 412                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Power supply for the module's RF part       | 3.3  | 3.8  | 4.3  | V    |
| VBAT_BB  | 241, 242, 244                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Power supply for the module's baseband part | 3.3  | 3.8  | 4.3  | V    |
| GND      | 6, 12, 18, 26, 33, 42, 86, 92, 98, 115, 117, 118, 120, 121, 124, 125, 126, 127, 128, 129, 130, 131, 133, 134, 135, 137, 138, 140, 141, 144, 145, 146, 147, 148, 149, 150, 151, 153, 155, 156, 158, 159, 160, 162, 164, 165, 167, 168, 171, 172, 173, 174, 176, 177, 180, 182, 183, 185, 186, 189, 191, 192, 194, 195, 198, 199, 201, 202, 203, 206, 208, 209, 211, 212, 215, 217, 218, 220, 221, 230, 232, 233, 234, 237, 240, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 406, 407, 408, 409, 410, 411, 413, 414 |                                             |      |      |      |      |

#### 3.3.2. Reference Design for Power Supply

The performance of the module largely depends on the power source. If the voltage drop between the input and output is not too high, it is recommended to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +12/+24 V input power source when applying the module to 5G solution. The designed output is 3.8 V, and the maximum rated current of the DC-DC converter is 5 A.



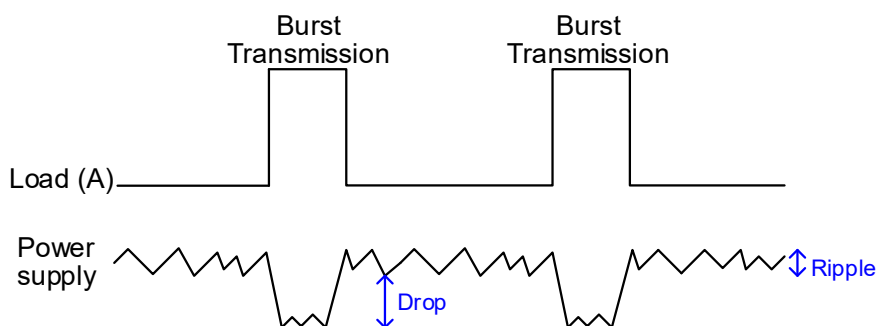
**Figure 5: Reference Design of Power Supply**

#### NOTE

1. To avoid corrupting the data of internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or Linux power off commands or API functions can you cut off the power supply.
2. It is recommended to use the default pull-down GPIO (3V8\_EN) of the MCU to control the module's power supply, otherwise the module will be abnormally turned off when the MCU updates the firmware and restarts. Only when the module crashes, the MCU's GPIO can be used to power down the module.

### 3.3.3. Voltage Stability Requirements

The power supply range of VBAT\_BB and VBAT\_RF is 3.3–4.3 V. Ensure that the input voltage of VBAT\_BB and VBAT\_RF never drops below 3.3 V. The following figure shows the voltage drop during high load (e.g. burst transmission in GSM and 5G NSA networks). The voltage drop will be less in 3G, 4G and 5G SA networks.



**Figure 6: Power Supply Limits During Burst Transmission**

To decrease voltage-drop, use bypass capacitors of at least  $100\ \mu\text{F} + 47\ \mu\text{F}$  with low ESR for each group of VBAT\_RF and VBAT\_BB, and reserve multi-layer ceramic chip capacitor (MLCC) arrays due to their low ESR. It is recommended to use at least three ceramic capacitors ( $100\ \text{nF}$ ,  $33\ \text{pF}$ ,  $10\ \text{pF}$ ) for composing the MLCC array, and place these capacitors close to VBAT pins. While connecting the module to an external  $3.8\ \text{V}$  power supply, route VBAT\_BB and VBAT\_RF traces in star structure. The width of VBAT\_BB trace should be not less than  $1.5\ \text{mm}$ . The width of VBAT\_RF trace should be not less than  $3\ \text{mm}$  for the main power trace and  $2\ \text{mm}$  for the branch power trace. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to get a stable power source, it is suggested to use TVS diodes to prevent EOS, and place them as close to the VBAT pins as possible. The recommended power supply structure is presented in the figure below.

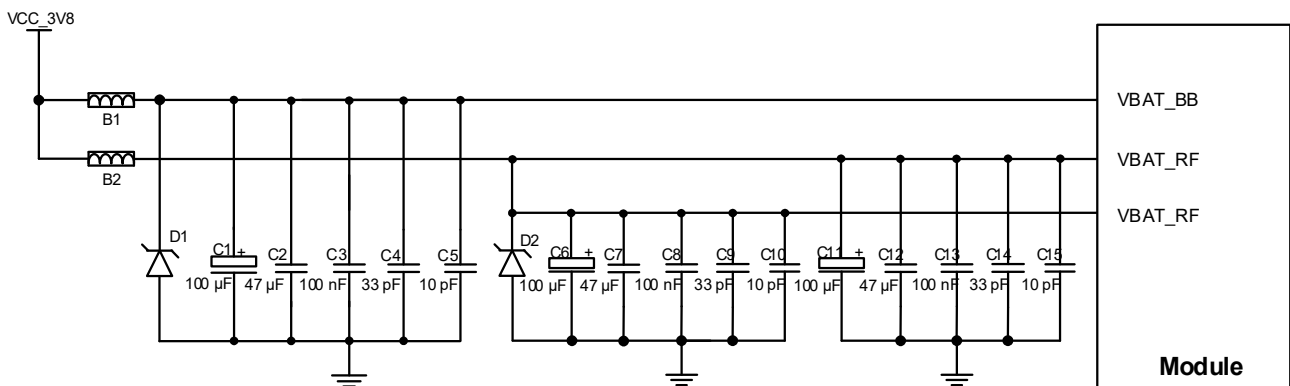


Figure 7: Power Supply Design

### 3.4. Turn-on

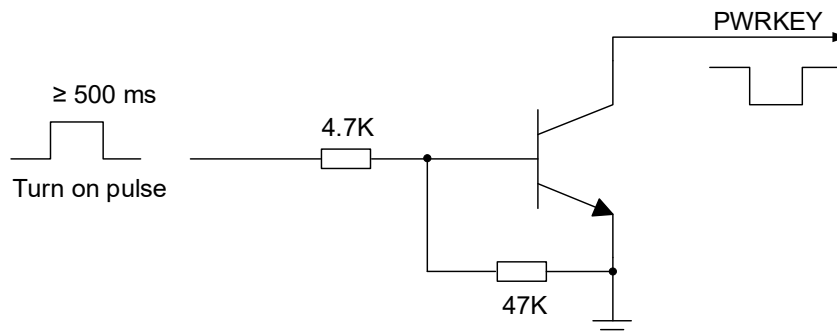
#### 3.4.1. Turn-on with PWRKEY

The following table shows the pin definition of PWRKEY.

Table 10: Pin Description of PWRKEY

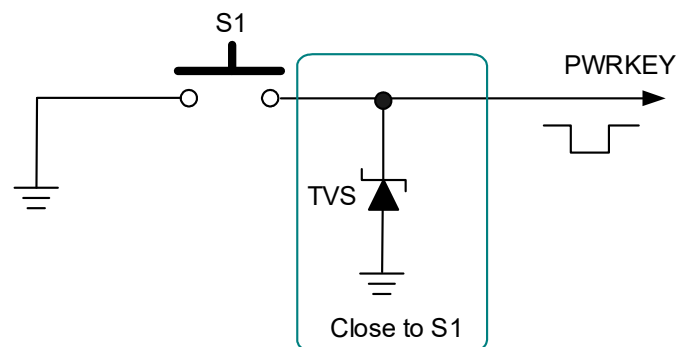
| Pin Name | Pin No. | I/O | Description            | Comment                                                                                                                                                                            |
|----------|---------|-----|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PWRKEY   | 7       | DI  | Turn on/off the module | <p>Pull-up internally.</p> <p>Active low.</p> <p>Due to the voltage drop inside the chip, the pin has around <math>0.75\ \text{V}</math> level after the module is powered up.</p> |

When the module is in power down mode, it can be turned on by driving the PWRKEY pin low for at least 500 ms and releasing it. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.



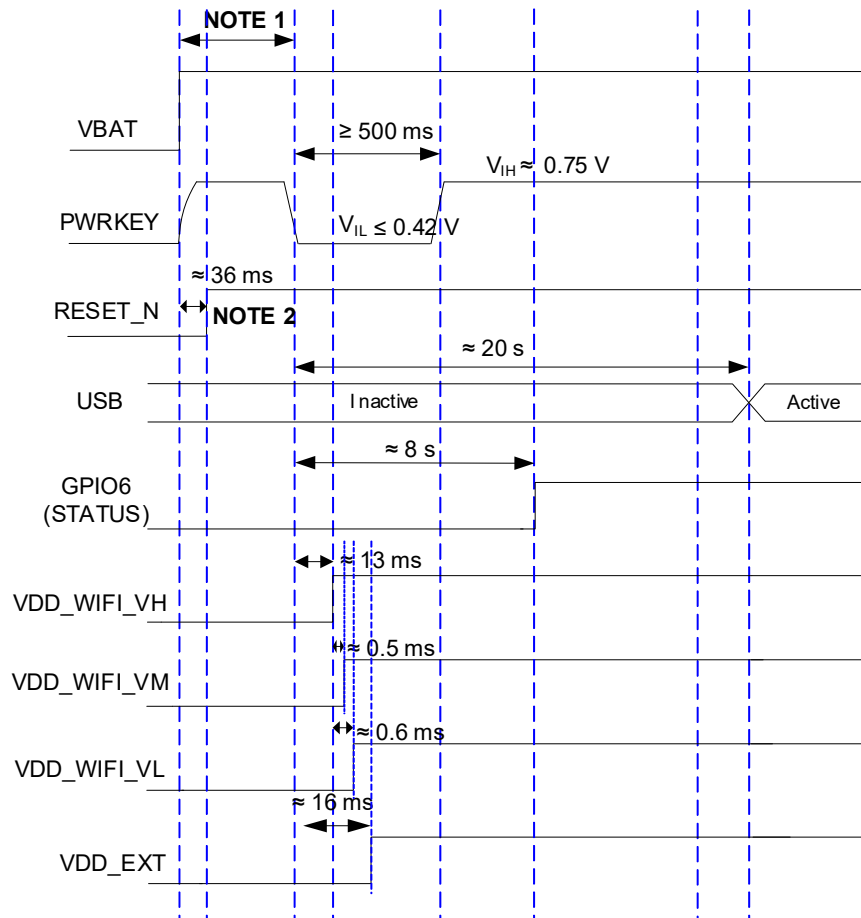
**Figure 8: Turn On the Module Using Driving Circuit**

Another way to control the PWRKEY is using a button directly. When pressing the button, electrostatic strike may generate from the finger. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.



**Figure 9: Turn On the Module Using a Button**

The turn-on timing is illustrated in the following figure.



**Figure 10: Turn-on Timing**

#### NOTE

1. Ensure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin is not less than 50 ms.
2. RESET\_N will be pulled high automatically when the voltage of VBAT is stable, therefore, MCU does not need to control RESET\_N in the power-up timing.
3. The durations listed in the turn-on timing above are for reference only. Note that there may be a few milliseconds of difference in the actual testing process, and Wireless Mobility only promises that power-on sequence is fixed.
4. The timing of GPIO6 is based on the test data of the factory version and will change accordingly when configured by application program.
5. Do not connect PWRKEY to GND. Pulling PWRKEY low for an extended period will trigger mandatory hardware reset.
6. Ensure that there is no capacitance larger than 10 nF on the PWRKEY pin.

### 3.4.2. Turn-on with CBL\_PWR\_N

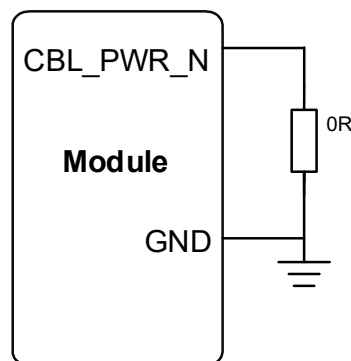
The following table shows the pin definition of CBL\_PWR\_N.

**Table 11: Pin Description of CBL\_PWR\_N**

| Pin Name  | Pin No. | I/O | Description                                      | Comment                                                                                                                       |
|-----------|---------|-----|--------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|
| CBL_PWR_N | 248     | DI  | Cable power-on; initiates power on when grounded | <p>Pulled up internally.</p> <p>Active low.</p> <p>Pulling it low for an extended period will not trigger hardware reset.</p> |

When the module is in power down mode, the module can be turned on by driving CBL\_PWR\_N low to GND. This action only triggers the module to turn on, it does not initiate power-off. After the module is turned on, the pin status of CBL\_PWR\_N can be disregard.

A simple reference circuit is illustrated in the following figure.



**Figure 11: Turn On the Module Using CBL\_PWR\_N**

#### NOTE

If the CBL\_PWR\_N pin remains low without being released, the module will turn on again after executing the module shutdown.

## 3.5. Turn-off

Any of the following methods can be used to turn off the module normally:

- Turn off the module using the PWRKEY pin.
- Turn off the module using Linux commands.
- Turn off the module using API function.

### 3.5.1. Turn-off with PWRKEY

It is recommended to drive PWRKEY low for at least 2 s and then to release it will enable the module to execute turn-off procedure. The turn-off scenario is illustrated in the following figure.

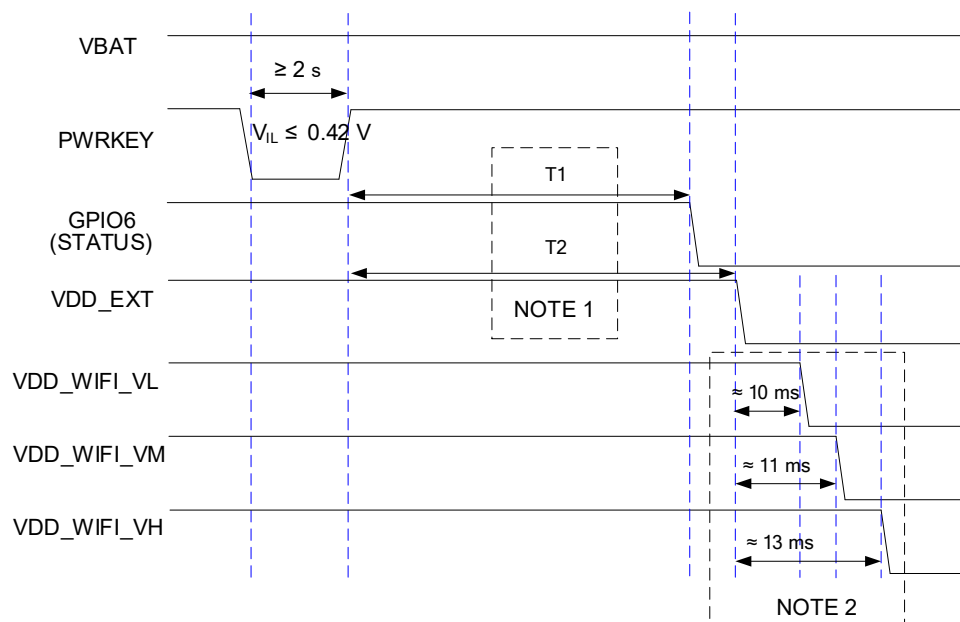


Figure 12: Turn-off Timing

#### NOTE

1. The releasing time of GPIO6 and the power-down time of the power supply (e.g VDD\_EXT) depend on the actual running business, and if the module has tasks to deal with during shutdown, the time may be longer.
2. The durations listed in turn-off timing above are for reference only. Note that there may be a few milliseconds of difference in the actual testing process, and Wireless Mobility only promises that the power-down sequence is fixed.
3. Driving PWRKEY low for 1.5–2 s may result in an unexpected power-down.

### 3.5.2. Turn-off with Linux Commands/API Function

It is also a safe way to use API functions or Linux commands, such as **shutdown** and **poweroff**, to turn off the module, which is similar to turning off the module via PWRKEY pin.

For more information about the API function for powering off the module, please contact Wireless Mobility Technical Support.

#### NOTE

1. To avoid corrupting the data of internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or Linux power off commands or API function can you cut off the power supply.
2. When you turn off module with Linux commands or API function, keep PWRKEY at high level after the execution of Linux commands or API function. Otherwise, the module will be turned on again after successful turn-off.

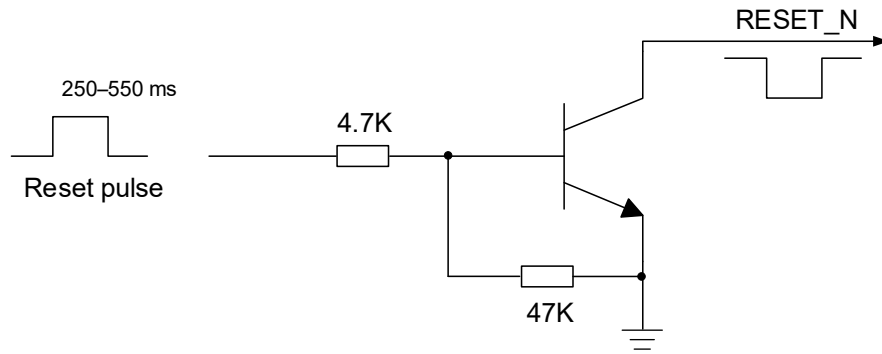
## 3.6. RESET\_N

The module can be reset by driving RESET\_N low for 250–550 ms and then releasing it. As the RESET\_N pin is sensitive to interference, the routing trace is recommended to be as short as possible and totally ground surrounded.

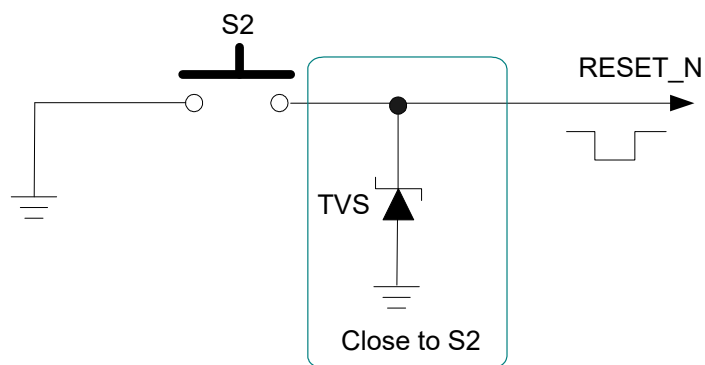
**Table 12: Pin Description of RESET\_N**

| Pin Name | Pin No. | I/O | Description      | Comment                                                                                       |
|----------|---------|-----|------------------|-----------------------------------------------------------------------------------------------|
| RESET_N  | 8       | DI  | Reset the module | Pulled up internally.<br>Active low.<br>A test point is recommended to be reserved if unused. |

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET\_N.

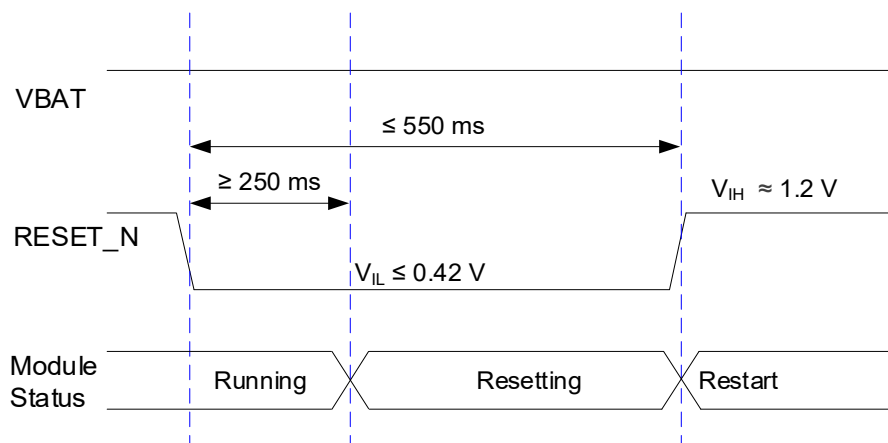


**Figure 13: Reference Circuit of RESET\_N by Using Driving Circuit**



**Figure 14: Reference Circuit of RESET\_N by Using Button**

The reset scenario is illustrated in the following figure.



**Figure 15: Reset Timing**

**NOTE**

1. RESET\_N should only be used when turning off the module by PWRKEY or Linux commands or API function all failed.
2. Ensure that there is no capacitance larger than 10 nF on RESET\_N pin.
3. Do not connect RESET\_N to GND. Pulling RESET\_N low for an extended period ( $\geq 16$  s) will trigger mandatory hardware shutdown.

# 4 Application Interfaces

## 4.1. (U)SIM Interfaces

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both (U)SIM1 and (U)SIM2 interface support 1.8/3.0 V (U)SIM card.

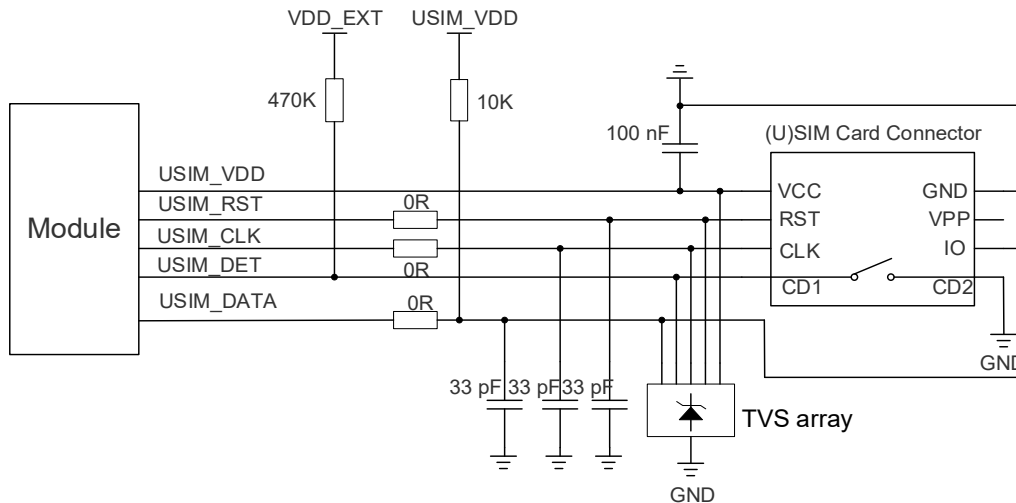
The module supports dual (U)SIM cards, and (U)SIM1 is the primary interface.

**Table 13: Pin Description of (U)SIM Interfaces**

| Pin Name   | Pin No. | I/O | Description                  | Comment                                                         |
|------------|---------|-----|------------------------------|-----------------------------------------------------------------|
| USIM1_VDD  | 251     | PO  | (U)SIM1 card power supply    |                                                                 |
| USIM1_CLK  | 253     | DO  | (U)SIM1 card clock           |                                                                 |
| USIM1_RST  | 250     | DO  | (U)SIM1 card reset           |                                                                 |
| USIM1_DATA | 254     | DIO | (U)SIM1 card data            | Either 1.8 V or 3.0 V is supported by the module automatically. |
| USIM2_VDD  | 256     | PO  | (U)SIM2 card power supply    |                                                                 |
| USIM2_CLK  | 259     | DO  | (U)SIM2 card clock           |                                                                 |
| USIM2_RST  | 260     | DO  | (U)SIM2 card reset           |                                                                 |
| USIM2_DATA | 257     | DIO | (U)SIM2 card data            |                                                                 |
| USIM1_DET  | 255     | DI  | (U)SIM1 card hot-plug detect | 1.8 V power domain.<br>If unused, keep them open.               |
| USIM2_DET  | 258     | DI  | (U)SIM2 card hot-plug detect |                                                                 |

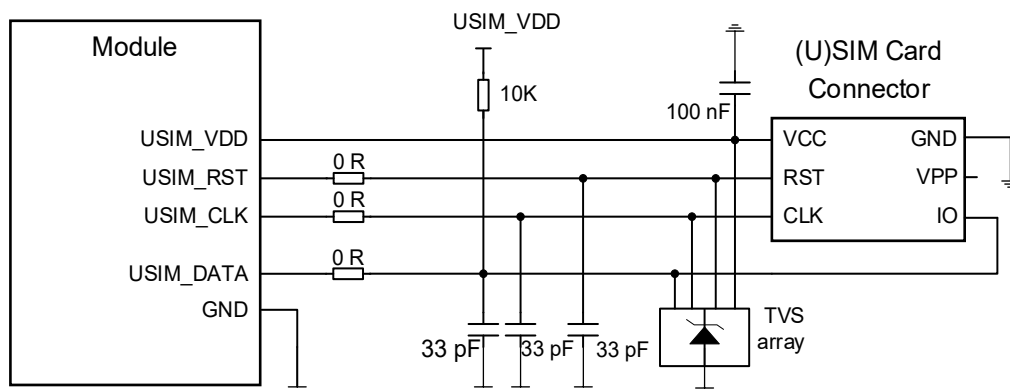
The module supports (U)SIM card hot-plug via USIM\_DET pins, and either low-level or high-level detection is supported. The function is disabled by default, and can be enabled by related software command.

The following figure shows a reference design of (U)SIM interface with an 8-pin (U)SIM card connector.



**Figure 16: Reference Design of (U)SIM Interface with an 8-Pin (U)SIM Card Connector**

If (U)SIM card detection function is not needed, keep USIM\_DET unconnected. A reference design of (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.



**Figure 17: Reference Design of (U)SIM Interface with a 6-Pin (U)SIM Card Connector**

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in the (U)SIM circuit design:

- Keep the placement of (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and power supply traces.
- Ensure the tracing between the ground of (U)SIM card connector and the module is short and wide. To maintain the same electrical potential, the trace width for USIM\_VDD must be at least 0.5 mm.
- To avoid cross talk between USIM\_DATA and USIM\_CLK, keep them away from each other and shield them with surrounded ground.
- To offer better ESD protection, you can add a TVS array of which the parasitic capacitance should be less than 10 pF. Add 0  $\Omega$  resistors in series between the module and the (U)SIM card connector to

suppress EMI and enhance ESD protection. Additionally, add 33 pF capacitors in parallel among USIM\_DATA, USIM\_CLK and USIM\_RST signal traces to filter out RF interference.

- USIM\_DATA must be connected to USIM\_VDD with a 10 kΩ pull-up resistor. The pull-up resistor can improve anti-jamming capability and should be placed close to the (U)SIM card connector.

## 4.2. USB Interface

The module provides one USB interface. The USB interface complies with the USB 3.1 Gen 2 and USB 2.0 specifications, and supports SuperSpeed (10 Gbps) on USB 3.1, high-speed (480 Mbps) and full-speed (12 Mbps) on USB 2.0.

Both USB 2.0 interface and USB 3.1 interface can be used for firmware upgrade, AT command communication, data transmission, GNSS NMEA sentences output and software debugging.

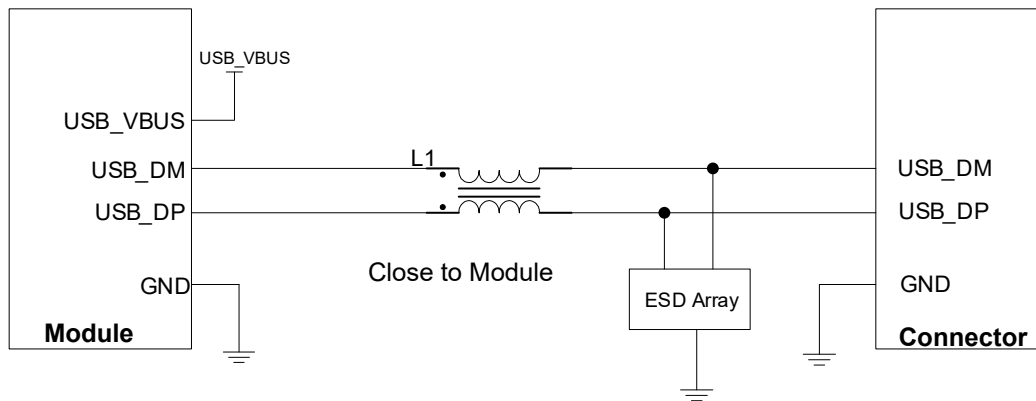
The following table shows the pin definition of USB interface.

**Table 14: Pin Description of USB Interface**

| Pin Name    | Pin No. | I/O | Description                     | Comment                                                                                                                                                                                                                                         |
|-------------|---------|-----|---------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| USB_VBUS    | 84      | DI  | USB connection detect           | Maximum current: 0.1 mA<br>Typical 5.0 V.<br>A 47 kΩ resistor is connected in series inside the module.<br>If the debugging function is required, the connector cannot be occupied by other functions, otherwise, test points must be reserved. |
| USB_DP      | 85      | AIO | USB 2.0 differential data (+)   | Compliant with USB 2.0 standard specifications.<br>Require differential impedance of 90 Ω.                                                                                                                                                      |
| USB_DM      | 87      | AIO | USB 2.0 differential data (-)   | If the debugging function is required, the connector cannot be occupied by other functions, otherwise, test points must be reserved.                                                                                                            |
| USB_SS_TX_P | 93      | AO  | USB 3.1 SuperSpeed transmit (+) | Compliant with USB 3.1 standard specifications.                                                                                                                                                                                                 |
| USB_SS_TX_M | 91      | AO  | USB 3.1 SuperSpeed transmit (-) | Require differential                                                                                                                                                                                                                            |

|             |    |    |                                |                                                                    |
|-------------|----|----|--------------------------------|--------------------------------------------------------------------|
| USB_SS_RX_P | 90 | AI | USB 3.1 SuperSpeed receive (+) | impedance range of 70–100 $\Omega$ and 85 $\Omega$ is recommended. |
| USB_SS_RX_M | 88 | AI | USB 3.1 SuperSpeed receive (-) |                                                                    |

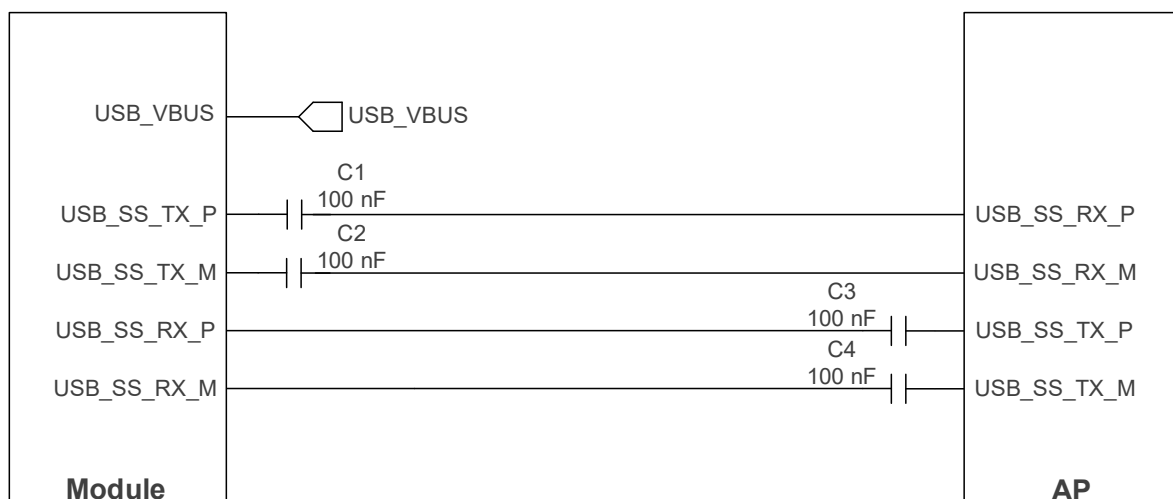
It is recommended to use USB 2.0 for firmware upgrading in application designs. USB 2.0 interface reference circuit is presented below.



**Figure 18: Reference Design of USB 2.0 Application**

In USB 2.0 applications, it is recommended to add a common mode choke L1 in series between the module and the connector to suppress EMI.

USB 3.1 interface reference circuit is presented below.



**Figure 19: Reference Design of USB 3.1 Application**

In USB 3.1 applications, place C1 and C2 near the module, and place C3 and C4 near the AP. The extra stubs of trace must be as short as possible.

To meet USB 2.0 and USB 3.1 specifications, the following principles of USB interface should be complied with.

- It is important to route the USB 2.0 and 3.1 signal traces as differential pairs with total grounding. The recommended differential impedance is 90  $\Omega$  for USB 2.0 and 85  $\Omega$  for USB 3.1.
- The intra-lane length match should be less than 2.0 mm for USB 2.0 and 0.7 mm for USB 3.1.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below. Route the RF signals operating at a 2.4 GHz frequency with the highest isolation possible from the USB\_SS\_TX/RX traces.
- If a USB connector is used, keep the ESD protection components as close to the USB connector as possible. Junction capacitance of the ESD protection device might cause influences on USB data traces, so pay attention to the selection of the device. Typically, the parasitic capacitance should be less than 2.0 pF for USB 2.0 and less than 0.3 pF for USB 3.1.
- Keep isolation between the USB\_SS\_TX pair, USB\_SS\_RX pair, and USB\_DP/USB\_DM to avoid crosstalk.
- USB\_SS\_TX AC coupling capacitors can be anywhere along the trace, but it is better to place them close to the source or the ESD/connector side to keep good signal integrity of the main route on the PCB.

For more details about the USB 2.0 and USB 3.1 specifications, visit <http://www.usb.org/home>.

#### NOTE

1. The module supports master mode, but works in slave mode by default.
2. The high-speed PHY and SuperSpeed PHY share the same USB 3.1 Gen 2 controller inside baseband chipset, so USB 2.0 and USB 3.1 cannot be used simultaneously. When USB 2.0 and USB 3.1 are connected to the same host, USB 3.1 takes effect by default.
3. As for the AC coupling capacitors C1–C4, the recommended value is 220 nF for USB 3.1 Gen 2 and 100 nF for USB 3.1 Gen 1.

## 4.3. UART Interfaces

The module provides five UART interfaces: UART1, UART2, UART3, UART4 and debug UART. The following are the features of these UART interfaces.

**Table 15: Basic Information of UART Interfaces**

| UART Type                              | Supported Baud Rate (bps)                   | Default Baud Rate (bps) | Description                                 |
|----------------------------------------|---------------------------------------------|-------------------------|---------------------------------------------|
| UART1                                  |                                             | 9600                    | ● Data transmission                         |
| UART2 <sup>8</sup><br>(Bluetooth UART) | 4800, 9600, 19200,<br>38400, 57600, 115200, | 9600                    | ● Support RTS and CTS hardware flow control |
| UART3                                  | 230400, 460800,<br>921600                   | 9600                    | Data transmission                           |
| UART4                                  |                                             | 9600                    |                                             |
| Debug UART <sup>9</sup>                | 115200                                      | 115200                  | Used for Linux console and log output       |

For more details about baud rate and hardware flow control, please contact Wireless Mobility Technical Support. The following tables show the pin definition of the UART interfaces.

**Table 16: Pin Description of UART Interfaces**

| Pin Name  | Pin No. | I/O | Description                          | Comment                                                                           |
|-----------|---------|-----|--------------------------------------|-----------------------------------------------------------------------------------|
| UART1_TXD | 70      | DO  | UART1 transmit                       | 1.8 V power domain.<br>If unused, keep these pins open.                           |
| UART1_RXD | 72      | DI  | UART1 receive                        |                                                                                   |
| UART1_CTS | 71      | DO  | Clear to send signal from the module | Connect to the MCU's CTS.<br>1.8 V power domain.<br>If unused, keep the pin open. |
| UART1_RTS | 74      | DI  | Request to send signal to the module | Connect to the MCU's RTS.<br>1.8 V power domain.<br>If unused, keep the pin open. |
| UART2_TXD | 59      | DO  | UART2 transmit                       | 1.8 V power domain.<br>If unused, keep these pins open.                           |
| UART2_RXD | 63      | DI  | UART2 receive                        |                                                                                   |
| UART2_CTS | 62      | DO  | Clear to send signal from the module | If unused, keep it open.<br>Connect to the MCU/Wi-Fi & Bluetooth module's CTS.    |
| UART2_RTS | 61      | DI  | Request to send signal to the module | If unused, keep it open.<br>Connect to the MCU/Wi-Fi & Bluetooth module's RTS.    |

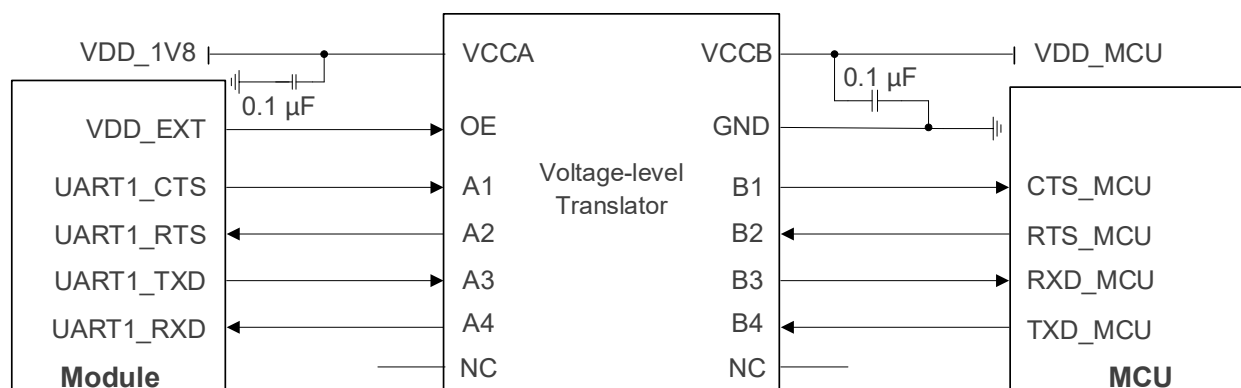
<sup>8</sup> UART2 is used for Bluetooth application by default, but also can be connected to other peripherals. For more details about Bluetooth application, see **Chapter 4.8**.

<sup>9</sup> The debug UART pins are dedicated ones and cannot be multiplexed into other functions.

|           |     |    |                     |                                                                     |
|-----------|-----|----|---------------------|---------------------------------------------------------------------|
| UART3_TXD | 298 | DO | UART3 transmit      | 1.8 V power domain.<br>If unused, keep these pins open.             |
| UART3_RXD | 297 | DI | UART3 receive       |                                                                     |
| UART4_TXD | 296 | DO | UART4 transmit      |                                                                     |
| UART4_RXD | 295 | DI | UART4 receive       |                                                                     |
| DBG_TXD   | 107 | DO | Debug UART transmit | 1.8 V power domain.<br>Test points must be reserved for debug UART. |
| DBG_RXD   | 110 | DI | Debug UART receive  |                                                                     |

The module provides 1.8 V UART interfaces. Use a voltage-level translator if your application is equipped with a 3.3 V UART interface. It is recommended that the enable pin of the voltage-level translator is controlled by VDD\_EXT to eliminate the possible influence of current sinking from its internal circuits (e.g. pull-ups) into the module.

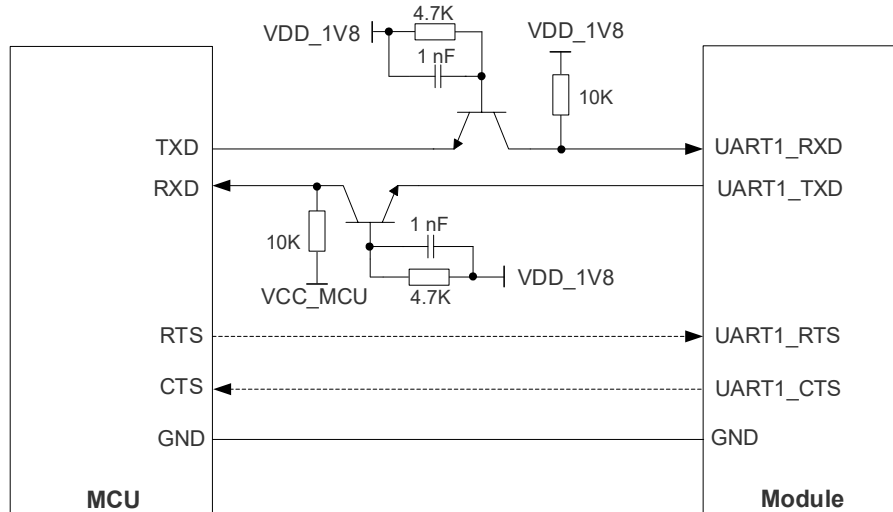
The following figure shows a reference design.



**Figure 20: Reference Design of UART Interface with Translator Chip (UART1)**

Another example with transistor translation circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

Ensure the VDD\_1V8 are not powered on before VDD\_EXT, otherwise its pull-up may affect the normal startup of the module.



**Figure 21: Reference Circuit with Transistor Circuit (UART1)**

#### NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. To increase the stability of UART communication, it is recommended to add UART hardware flow control design. If hardware flow control is intended to be used, then CTS and RTS should also be designed with the level shifting circuit.
3. Please note that the module's CTS is connected to the MCU/Wi-Fi & Bluetooth module's CTS, and the module's RTS is connected to the MCU/Wi-Fi & Bluetooth module's RTS.
4. When the module enters LPM, it is recommended to switch off the power supply for VDD\_1V8 to reduce power consumption.
5. The level-shifting circuits (**Figure 20 & Figure 21**) are illustrated using UART1 as an example. The circuits of the debug UART and the UART2/UART3/UART4 are connected in the same way as the UART1.

## 4.4. I2S and I2C Interfaces

The module provides two I2S interfaces and two I2C interfaces.

### I2S:

- I2S1 is used for external audio codec by default.
- I2S2 can be used according to your application.

## I2C:

- I2C1 is used for external audio codec by default.
- I2C2 is used for IMU (inertial measurement unit) by default.

The following table shows the pin definition of I2S and I2C interfaces.

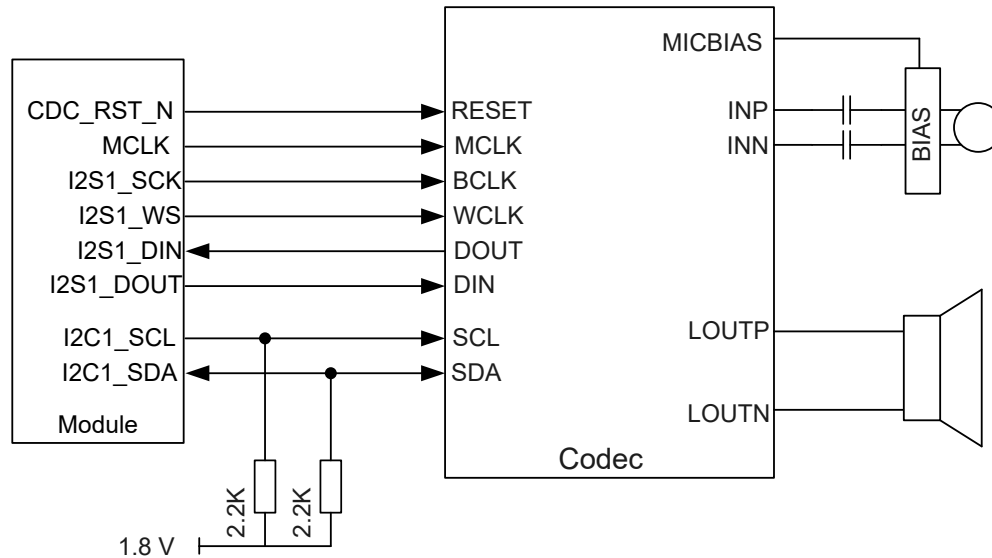
**Table 17: Pin Description of I2S Interfaces**

| Pin Name  | Pin No. | I/O | Description            | Comment                                                                                                 |
|-----------|---------|-----|------------------------|---------------------------------------------------------------------------------------------------------|
| MCLK      | 81      | DO  | Clock output for codec | 12.288 MHz clock output                                                                                 |
| I2S1_WS   | 265     | DIO | I2S1 word select       | 1.8 V power domain.<br>Serve as output signals in master mode.<br>Serve as input signals in slave mode. |
| I2S1_SCK  | 262     | DIO | I2S1 clock             |                                                                                                         |
| I2S1_DIN  | 263     | DI  | I2S1 data in           | 1.8 V power domain.                                                                                     |
| I2S1_DOUT | 261     | DO  | I2S1 data out          |                                                                                                         |
| CDC_RST_N | 77      | DO  | External codec reset   |                                                                                                         |
| I2S2_WS   | 443     | DIO | I2S2 word select       | 1.8 V power domain.<br>Serve as output signals in master mode.<br>Serve as input signals in slave mode. |
| I2S2_SCK  | 444     | DIO | I2S2 clock             |                                                                                                         |
| I2S2_DIN  | 445     | DI  | I2S2 data in           | 1.8 V power domain.                                                                                     |
| I2S2_DOUT | 446     | DO  | I2S2 data out          |                                                                                                         |

**Table 18: Pin Description of I2C Interfaces**

| Pin Name | Pin No. | I/O | Description       | Comment                                                                |
|----------|---------|-----|-------------------|------------------------------------------------------------------------|
| I2C1_SDA | 80      | OD  | I2C1 serial data  | Require external pull-up to 1.8 V.<br>If unused, keep these pins open. |
| I2C1_SCL | 79      | OD  | I2C1 serial clock |                                                                        |
| I2C2_SDA | 264     | OD  | I2C2 serial data  |                                                                        |
| I2C2_SCL | 267     | OD  | I2C2 serial clock |                                                                        |

The following figure shows a reference design of I2S and I2C interfaces with an external codec IC.



**Figure 22: Reference Design of I2S1 and I2C1 Interfaces with External Audio Codec**

**NOTE**

1. It is recommended to reserve an RC circuit on the I2S1 signal traces, especially for I2S1\_SCK and MCLK.
2. The module works as a master device in I2C applications.

## 4.5. PCM Interface

The module provides one PCM interface for Bluetooth audio transmission by default. See **Chapter 4.8** for details. The PCM interface supports primary (short frame sync) and auxiliary (long frame sync) modes.

**Table 19: Pin Description of PCM Interface**

| Pin Name | Pin No. | I/O | Description         | Comment                                                        |
|----------|---------|-----|---------------------|----------------------------------------------------------------|
| PCM_SYNC | 73      | DIO | PCM data frame sync | 1.8 V power domain.<br>Serve as output signals in master mode. |
| PCM_CLK  | 75      | DIO | PCM clock           | Serve as input signals in slave mode.                          |
| PCM_DIN  | 76      | DI  | PCM data input      | 1.8 V power domain.                                            |
| PCM_DOUT | 78      | DO  | PCM data output     |                                                                |

The module supports 16-bit linear data format. Clock and mode can be configured, and the default configuration is primary mode using short frame sync format with 1536 kHz PCM\_CLK and 48 kHz PCM\_SYNC. For more details, please contact Wireless Mobility Technical Support.

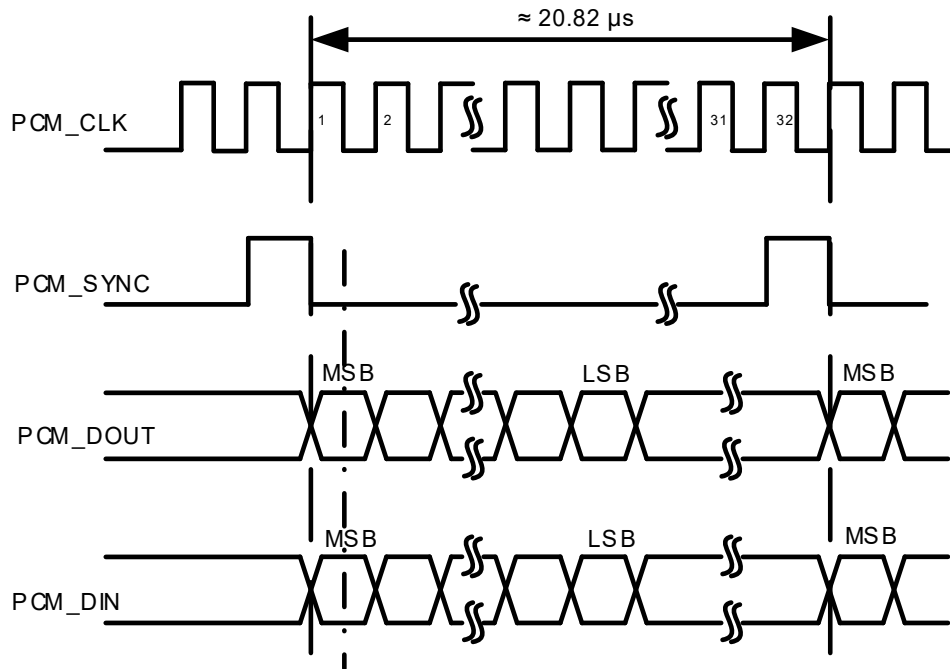


Figure 23: PCM Timing (Short Frame Sync)

#### NOTE

When using Bluetooth function, PCM\_SYNC and PCM\_CLK can only be used as output signals.

## 4.6. SDIO Interfaces

The module provides two SDIO interface:

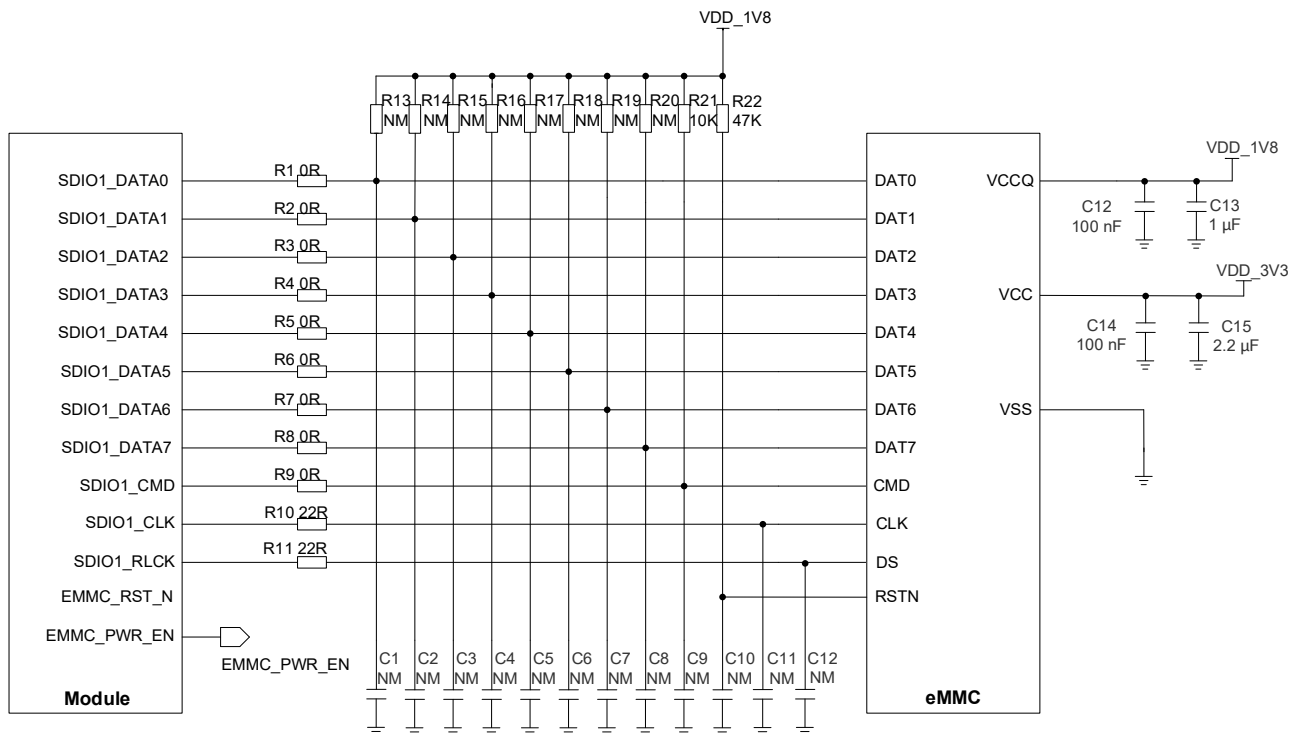
- SDIO1 can be used for eMMC function. 4-bit by default, max. up to 8-bit, supports 1.8 V only.
- SDIO2 can be used to connect to external DSRC module if required. 4-bit by default, supports 1.8 V only.

The following tables show the pin definition of SDIO interface.

**Table 20: Pin Description of SDIO Interface**

| Pin Name    | Pin No. | I/O | Description                      | Comment                                                           |
|-------------|---------|-----|----------------------------------|-------------------------------------------------------------------|
| SDIO1_DATA0 | 49      | DIO | SDIO1 data bit 0                 |                                                                   |
| SDIO1_DATA1 | 50      | DIO | SDIO1 data bit 1                 |                                                                   |
| SDIO1_DATA2 | 51      | DIO | SDIO1 data bit 2                 |                                                                   |
| SDIO1_DATA3 | 52      | DIO | SDIO1 data bit 3                 |                                                                   |
| SDIO1_CMD   | 48      | DIO | SDIO1 command                    |                                                                   |
| SDIO1_CLK   | 47      | DO  | SDIO1 clock                      | 1.8 V power domain.<br>The single-ended impedance requires 50 Ω.  |
| SDIO1_RCLK  | 57      | DI  | SDIO1 return clock               |                                                                   |
| SDIO1_DATA4 | 53      | DIO | SDIO1 data bit 4                 |                                                                   |
| SDIO1_DATA5 | 55      | DIO | SDIO1 data bit 5                 |                                                                   |
| SDIO1_DATA6 | 56      | DIO | SDIO1 data bit 6                 |                                                                   |
| SDIO1_DATA7 | 58      | DIO | SDIO1 data bit 7                 |                                                                   |
| EMMC_RST_N  | 54      | DO  | eMMC reset                       | 1.8 V power domain. The pin function is not supported by default. |
| EMMC_PWR_EN | 45      | DO  | eMMC power supply enable control | 1.8 V power domain.                                               |
| SDIO2_DATA0 | 1       | DIO | SDIO2 data bit 0                 |                                                                   |
| SDIO2_DATA1 | 2       | DIO | SDIO2 data bit 1                 |                                                                   |
| SDIO2_DATA2 | 4       | DIO | SDIO2 data bit 2                 |                                                                   |
| SDIO2_DATA3 | 5       | DIO | SDIO2 data bit 3                 | 1.8 V power domain.<br>The single-ended impedance requires 50 Ω.  |
| SDIO2_CMD   | 269     | DIO | SDIO2 command                    |                                                                   |
| SDIO2_CLK   | 270     | DO  | SDIO2 clock                      |                                                                   |
| SDIO2_RCLK  | 3       | DI  | SDIO2 return clock               |                                                                   |

#### 4.6.1. Reference Design for eMMC Application



**Figure 24: Reference Design for eMMC Application**

Follow the principles below in eMMC circuit design:

- To avoid jitter of bus, it is recommended to reserve R13–R20 (10–100 k $\Omega$ ) to pull up SDIO signals to an external 1.8 V VDD. The resistors are not mounted by default, and the recommended value is 100 k $\Omega$ .
- To improve signal quality, it is recommended to add resistors R1–R11 in series between the module and eMMC. Resistor R10, R11 should be 20–30  $\Omega$  and the other resistors are 0  $\Omega$  by default. The bypass capacitors C1–C12 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50  $\Omega$  ( $\pm 10\%$ ).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is recommended to keep the trace length difference between SDIO\_CLK and SDIO\_DATA[0:7]/SDIO\_CMD/SDIO\_RCLK less than 1 mm and the total routing length less than 60 mm. The total trace length for SDIO1 inside the module is 38 mm, so the exterior total trace length should be less than 22 mm. For SDIO2, the total trace length inside the module is 14 mm, so the exterior total length can be 46 mm.
- Keep the spacing between SDIO and other signal traces at least 2.5 times the trace width.

## 4.7. PCIe Interfaces

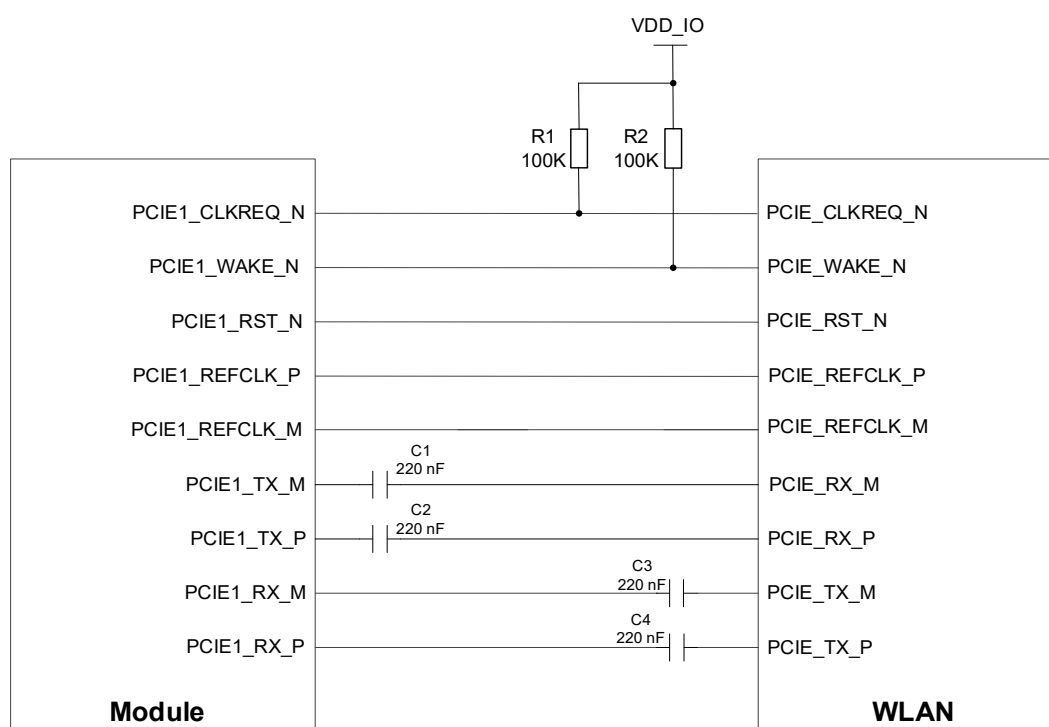
The module provides two PCIe 3.0 interface.

- PCIe1:
  - Supports RC and EP modes, and works in RC mode by default.
  - Supports 2 lanes.
  - Can be used to connect to an external WLAN chip or application processor.
- PCIe2:
  - Supports RC mode only.
  - Supports 1 lane
- Compliant with *PCI Express Base Specification Revision 3.0*
- Maximum rate: 8 GT/s × 1 lane
- Backward compatible

**Table 21: Pin Description of PCIe Interface**

| Pin Name       | Pin No. | I/O | Description               | Comment                                                                                                                                   |
|----------------|---------|-----|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| PCIE1_REFCLK_P | 40      | AIO | PCIe1 reference clock (+) | Serve as output signals in RC mode.                                                                                                       |
| PCIE1_REFCLK_M | 38      | AIO | PCIe1 reference clock (-) | Serve as input signals in EP mode.<br>The differential impedance should be the same as that for PCIE_TX/RX.                               |
| PCIE1_TX0_M    | 44      | AO  | PCIe1 transmit 0 (-)      | If PCIE1_TX and PCIE1_RX are unused, keep these pins unconnected.<br>Require differential impedance of 70–100 Ω, and 85 Ω is recommended. |
| PCIE1_TX0_P    | 46      | AO  | PCIe1 transmit 0 (+)      |                                                                                                                                           |
| PCIE1_TX1_M    | 41      | AO  | PCIe1 transmit 1 (-)      |                                                                                                                                           |
| PCIE1_TX1_P    | 43      | AO  | PCIe1 transmit 1 (+)      |                                                                                                                                           |
| PCIE1_RX0_M    | 32      | AI  | PCIe1 receive 0 (-)       |                                                                                                                                           |
| PCIE1_RX0_P    | 34      | AI  | PCIe1 receive 0 (+)       |                                                                                                                                           |
| PCIE1_RX1_M    | 35      | AI  | PCIe1 receive 1 (-)       |                                                                                                                                           |
| PCIE1_RX1_P    | 37      | AI  | PCIe1 receive 1 (+)       |                                                                                                                                           |
| PCIE1_CLKREQ_N | 36      | DIO | PCIe1 clock request       | Serve as input signals in RC mode.                                                                                                        |
| PCIE1_WAKE_N   | 30      | DIO | PCIe1 wake up             | Serve as output signals in EP mode.                                                                                                       |

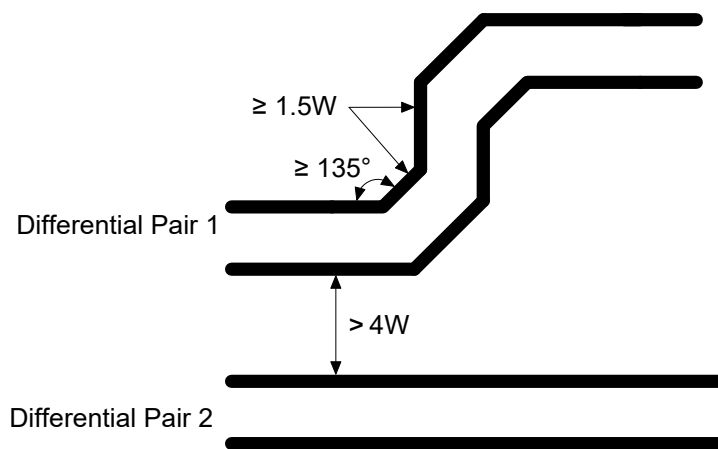
|                |     |     |                           |                                                                                                        |
|----------------|-----|-----|---------------------------|--------------------------------------------------------------------------------------------------------|
|                |     |     |                           | 1.8 V power domain.                                                                                    |
| PCIE1_RST_N    | 39  | DIO | PCle1 reset               | Serves as an output signal in RC mode.<br>Serves as an input signal in EP mode.<br>1.8 V power domain. |
| PCIE2_REFCLK_P | 437 | AO  | PCle2 reference clock (+) | Only supports RC mode.                                                                                 |
| PCIE2_REFCLK_M | 436 | AO  | PCle2 reference clock (-) | The differential impedance should be the same as that for PCIE_TX/RX.                                  |
| PCIE2_TX_P     | 439 | AO  | PCle2 transmit (+)        | If PCIE2_TX and PCIE2_RX are unused, keep these pins unconnected.                                      |
| PCIE2_TX_M     | 438 | AO  | PCle2 transmit (-)        |                                                                                                        |
| PCIE2_RX_P     | 435 | AI  | PCle2 receive (+)         | Require differential impedance of 70–100 $\Omega$ , and 85 $\Omega$ is recommended.                    |
| PCIE2_RX_M     | 434 | AI  | PCle2 receive (-)         |                                                                                                        |
| PCIE2_CLKREQ_N | 442 | DI  | PCle2 clock request       | Only supports RC mode.                                                                                 |
| PCIE2_WAKE_N   | 440 | DI  | PCle2 wakeup              |                                                                                                        |
| PCIE2_RST_N    | 441 | DO  | PCle2 reset               | Only supports RC mode.                                                                                 |



**Figure 25: Reference Design of PCIe Interface**

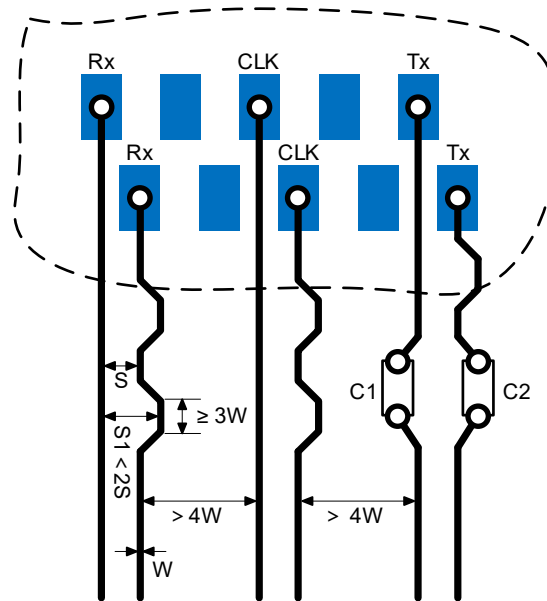
To meet PCIe specifications and enhance the reliability of applications, follow the criteria below in the PCIe interface circuit design:

- It is important to route the PCIe signal traces as differential pairs with ground surrounded. The differential impedance is 70–100  $\Omega$  and 85  $\Omega$  is recommended for PCIe Tx/Rx/REFCLK traces.
- PCIe signals must be protected from noisy signals (clocks, DC-DC, RF and so forth). All other sensitive/high-speed signals and circuits must be routed far away from PCIe traces.
- For each differential pair, the intra-lane length match should be less than 0.7 mm, while the inter-lane length match, that is, the trace length matching between the Tx, Rx and reference clock pairs is not required.
- Do not stagger the capacitors, as this can affect the differential integrity of the design and can create EMI.
- To reduce the probability for layer-to-layer manufacturing variation, minimize layer transitions for the main route on the PCB (that is, apply layer transitions only at break in and break out regions). When the differential signal traces changes layers, create ground vias near signal vias, and create at least 1–3 ground vias for each differential pair.
- Avoid bending of the traces to avoid common mode noise to the system. When bending is required, maintain a bend angle greater than  $135^\circ$  as shown in the figure below, and the shortest trace caused by bending should be at least 1.5 times the trace width (1.5W). The spacing between Tx and Rx pairs, and the spacing between PCIe lanes and all other signals, should exceed 4 times the trace width (4W).



**Figure 26: Curved Trace of Differential Pair**

- PCIe Tx AC coupling capacitors can be anywhere along the line, but better to be placed close to the source or the receiver side to keep good signal integrity of main route on PCB. Use a serpentine to keep the difference pairs equal in the break out region as much as possible, to ensure that the traces stay differential thereafter. The length of each serpentine section should be at least 3 times the trace width ( $\geq 3W$ ), and the maximum spacing between the serpentine section and the other differential trace should be less than twice of the normal differential trace spacing ( $S1 < 2S$ ).



**Figure 27: PCIe Trace Requirements**

- PCIe Tx AC coupling capacitors should be 220 nF for PCIe Gen 3 applications, and 100 nF for PCIe Gen 2 applications.
- The maximum trace length of each differential pair for PCIe Gen 3 applications should be less than 300 mm, and that for PCIe Gen 2 applications less than 250 mm.

## 4.8. WLAN and Bluetooth Application Interfaces

The module provides one PCIe1 interface for WLAN function (see **Chapter 4.7** for more details), Bluetooth UART and PCM interfaces for Bluetooth function (see **Chapter 4.3** and **Chapter 4.5** for more details), as well as 4 power supply pins, a coexistence interface and other interfaces for Wi-Fi & Bluetooth.

The following table shows the pin definition of WLAN and Bluetooth application interfaces.

**Table 22: Pin Description of WLAN and Bluetooth Application Interfaces**

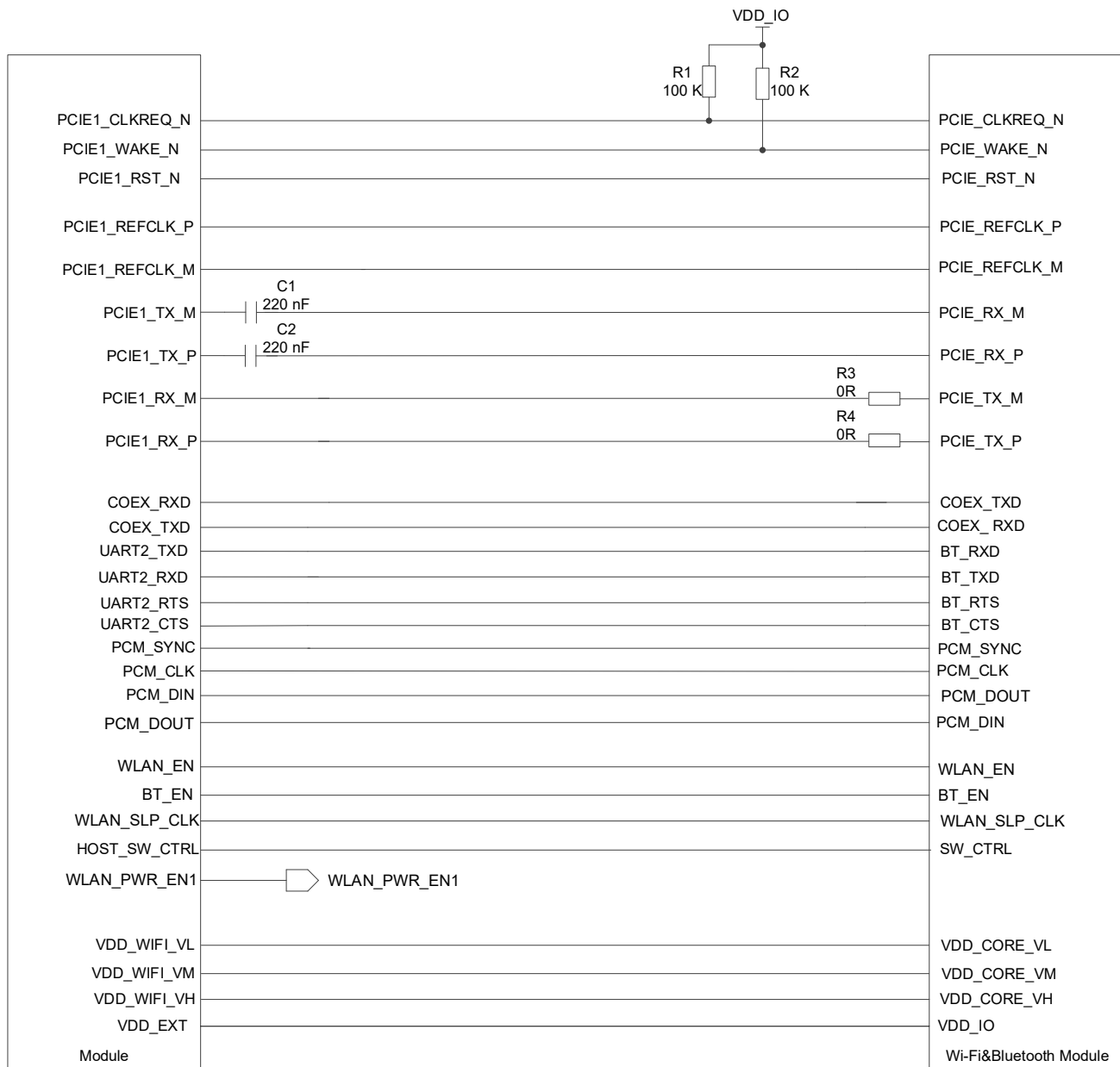
| Pin Name                      | Pin No. | I/O | Description                         | Comment                                                                                               |
|-------------------------------|---------|-----|-------------------------------------|-------------------------------------------------------------------------------------------------------|
| <b>Power Supply Interface</b> |         |     |                                     |                                                                                                       |
| VDD_EXT                       | 68      | PO  | Provide 1.8 V for external circuits | This pin can be used to connect with VDD_IO of Wi-Fi & Bluetooth module, it also can be used as power |

|                               |          |    |                                                           |                                                                                                                                         |
|-------------------------------|----------|----|-----------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
|                               |          |    |                                                           | supply for external pull up circuits.<br>A test point is recommended to be reserved.                                                    |
| VDD_WIFI_VL                   | 274, 275 | PO | Low-voltage power supply for Wi-Fi & Bluetooth modules    | After the Wi-Fi driver is loaded, the output voltage of these pins will be adjusted automatically to adapt to Wi-Fi & Bluetooth module. |
| VDD_WIFI_VM                   | 276      | PO | Medium-voltage power supply for Wi-Fi & Bluetooth modules |                                                                                                                                         |
| VDD_WIFI_VH                   | 277      | PO | High-voltage power supply for Wi-Fi & Bluetooth modules   |                                                                                                                                         |
| Coexistence Control Interface |          |    |                                                           |                                                                                                                                         |
| COEX_TXD                      | 69       | DO | LTE & WLAN & Bluetooth coexistence transmit               | 1.8 V power domain.                                                                                                                     |
| COEX_RXD                      | 67       | DI | LTE & WLAN & Bluetooth coexistence receive                |                                                                                                                                         |
| Others Interfaces             |          |    |                                                           |                                                                                                                                         |
| WLAN_PWR_EN1                  | 222      | DO | WLAN power supply enable control 1                        | Used for Wi-Fi & Bluetooth module power control.                                                                                        |
| WLAN_EN                       | 228      | DO | WLAN function enable control                              |                                                                                                                                         |
| BT_EN                         | 66       | DO | Bluetooth enable control                                  |                                                                                                                                         |
| HOST_SW_CTRL                  | 184      | DI | Switch control                                            | Output signal from Wi-Fi & Bluetooth module.                                                                                            |
| WLAN_SLP_CLK                  | 231      | DO | WLAN 32 kHz sleep clock                                   | If unused, keep it open.                                                                                                                |

#### NOTE

When WLAN or Bluetooth function is intended to be used, the coexistence interface must be used simultaneously. The coexistence interface cannot be used as general-purpose UART interface.

The following figure shows the application of the module with Wi-Fi & Bluetooth module.



**Figure 28: Reference Design of WLAN & Bluetooth Application Interfaces**

**NOTE**

When using Bluetooth function, PCM\_SYNC and PCM\_CLK can only be used as output signals.

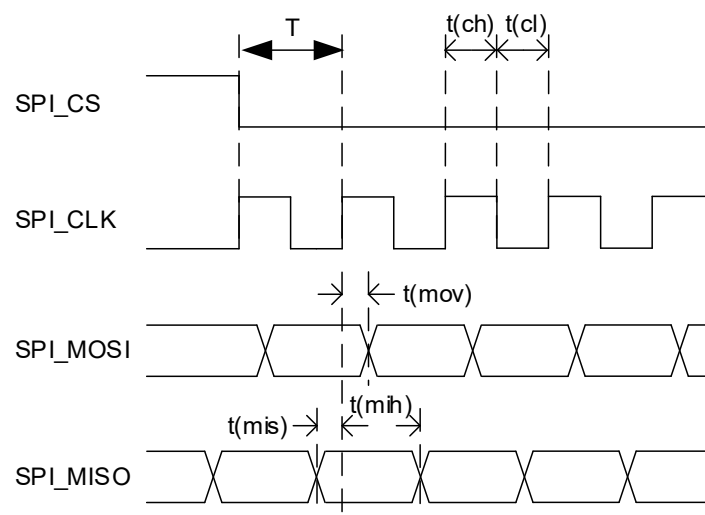
## 4.9. SPIs

The module provides two SPIs by default, which support master and slave\* modes. The maximum clock frequency rate is up to 50 MHz. The following tables show the pin definition of SPIs.

**Table 23: Pin Description of SPIs**

| Pin Name  | Pin No. | I/O | Description              | Comment                                                                          |
|-----------|---------|-----|--------------------------|----------------------------------------------------------------------------------|
| SPI1_CLK  | 216     | DO  | SPI1 clock               | 1.8 V power domain.                                                              |
| SPI1_CS   | 213     | DO  | SPI1 chip select         | SPI1 supports master mode by default.                                            |
| SPI1_MISO | 219     | DI  | SPI1 master-in slave-out | Contact Wireless Mobility Technical Support if slave mode needs to be supported. |
| SPI1_MOSI | 210     | DO  | SPI1 master-out slave-in |                                                                                  |
| SPI2_CLK  | 103     | DO  | SPI2 clock               | 1.8 V power domain.                                                              |
| SPI2_CS   | 105     | DO  | SPI2 chip select         | SPI2 supports master mode by default.                                            |
| SPI2_MISO | 106     | DI  | SPI2 master-in slave-out | Contact Wireless Mobility Technical Support if slave mode needs to be supported. |
| SPI2_MOSI | 108     | DO  | SPI2 master-out slave-in |                                                                                  |

The following figure shows the timing relationship of SPIs.



**Figure 29: SPI Timing**

The related parameters of SPI timing are shown in the table below.

**Table 24: Parameters of SPI Timing**

| Parameter | Description                       | Min. | Typ. | Max. | Unit |
|-----------|-----------------------------------|------|------|------|------|
| T         | SPI clock period                  | 20.0 | -    | -    | ns   |
| t(ch)     | SPI clock high-level time         | 8.0  | -    | -    | ns   |
| t(cl)     | SPI clock low-level time          | 8.0  | -    | -    | ns   |
| t(mov)    | SPI master data output valid time | -5.0 | -    | 5.0  | ns   |
| t(mis)    | SPI master data input setup time  | 5.0  | -    | -    | ns   |
| t(mih)    | SPI master data input hold time   | 1.0  | -    | -    | ns   |

#### NOTE

The module provides 1.8 V SPIs. A voltage-level translator should be used between the module and the host if the application is equipped with a 3.3 V processor or device interface.

## 4.10. RGMII Interface

The module includes an integrated Ethernet MAC with a RGMII interface which also supports EAVB. Key features of the RGMII interface are shown below:

- IEEE 802.3 compliant
- Supports 10/100/1000 Mbps operation <sup>10</sup>
- Supports protocols such as IEEE 1722.A (AVTP), 802.1Qav (FQTSS), 802.1Qat (SRP), 802.1AS (gPTP)
- Support connecting to an external Ethernet PHY or switch
- Support 1.8 V I/O standards

The following table shows the pin definition of RGMII interface.

<sup>10</sup> The module's RGMII interface supports the Gigabit Ethernet protocol, while actual throughput is subject to testing.

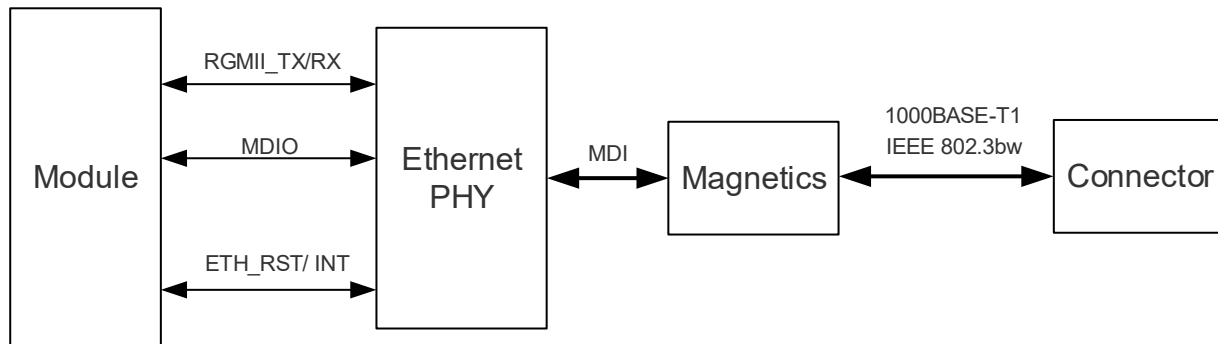
**Table 25: Pin Description of Ethernet Management and Control Interfaces**

| Pin Name   | Pin No. | I/O | Description                                        | Comment                                                                                                             |
|------------|---------|-----|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|
| ETH_MDIO   | 10      | DIO | Ethernet management data                           | Add a pull-up resistor to this pin, and place the resistor close to the external PHY.                               |
| ETH_MDC    | 11      | DO  | Ethernet management clock                          | Do not add any pull-up resistor to this pin, otherwise it may cause higher power consumption during low power mode. |
| ETH_PWR_EN | 27      | DO  | Enable external power supply to power Ethernet PHY | 1.8 V power domain.                                                                                                 |
| ETH_INT    | 29      | DI  | Ethernet PHY interrupt                             |                                                                                                                     |
| ETH_RST_N  | 31      | DO  | Ethernet PHY reset                                 |                                                                                                                     |

**Table 26: Pin Description of RGMII Interface**

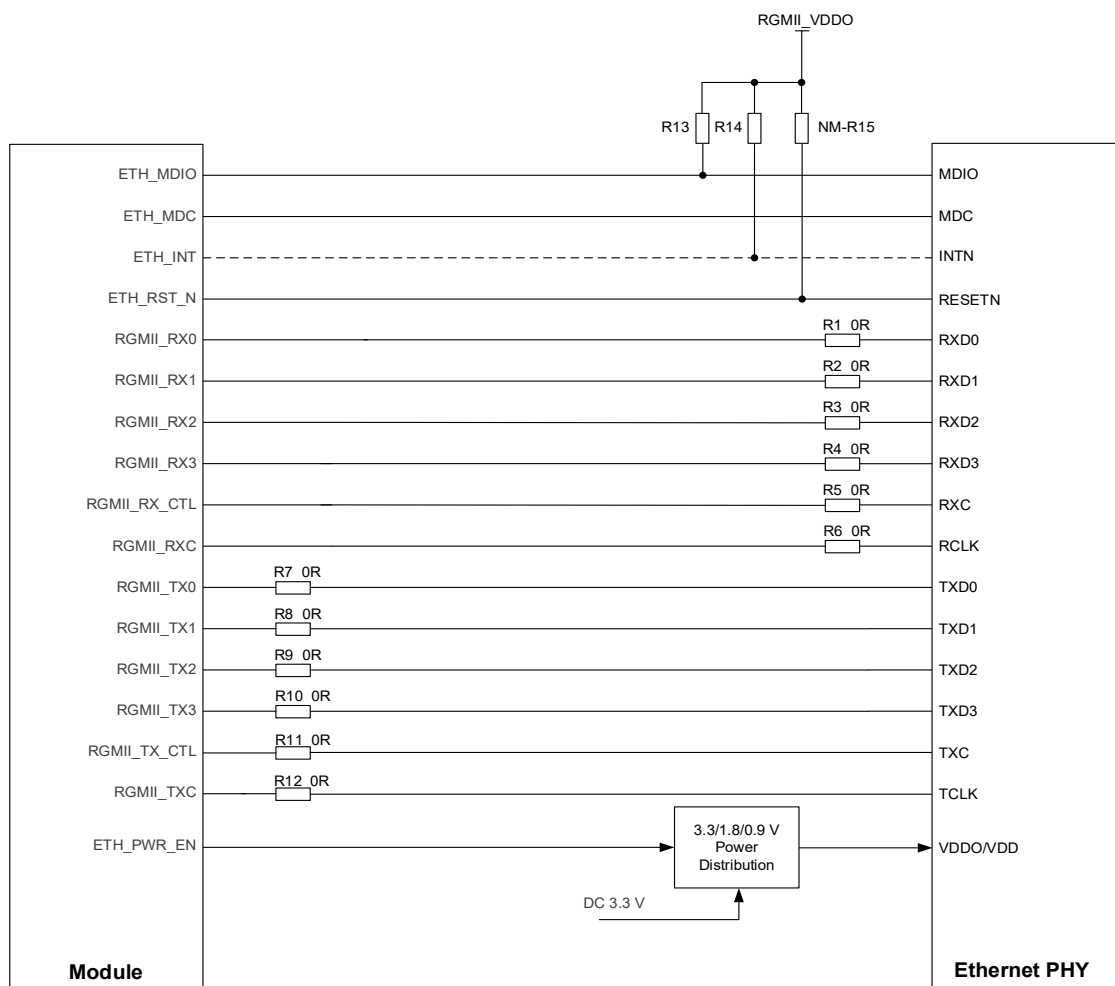
| Pin Name     | Pin No. | I/O | Description               | Comment                                           |
|--------------|---------|-----|---------------------------|---------------------------------------------------|
| RGMII_RXC    | 19      | DI  | RGMII receive clock       | The single-ended impedance requires 50 $\Omega$ . |
| RGMII_RX_CTL | 15      | DI  | RGMII receive control     |                                                   |
| RGMII_RX0    | 13      | DI  | RGMII receive data bit 0  |                                                   |
| RGMII_RX1    | 14      | DI  | RGMII receive data bit 1  |                                                   |
| RGMII_RX2    | 16      | DI  | RGMII receive data bit 2  |                                                   |
| RGMII_RX3    | 17      | DI  | RGMII receive data bit 3  |                                                   |
| RGMII_TXC    | 24      | DO  | RGMII transmit clock      |                                                   |
| RGMII_TX_CTL | 21      | DO  | RGMII transmit control    |                                                   |
| RGMII_TX0    | 20      | DO  | RGMII transmit data bit 0 |                                                   |
| RGMII_TX1    | 22      | DO  | RGMII transmit data bit 1 |                                                   |
| RGMII_TX2    | 23      | DO  | RGMII transmit data bit 2 |                                                   |
| RGMII_TX3    | 25      | DO  | RGMII transmit data bit 3 |                                                   |

The following figure shows the simplified block diagram for Ethernet application.



**Figure 30: Simplified Block Diagram for Automotive Ethernet Application**

The following figure shows a reference design of RGMII interface with PHY application. For more details, please contact Wireless Mobility Technical Support.



**Figure 31: Reference Circuit of RGMII Interface with PHY Application**

To enhance the reliability and availability of application designs, follow the criteria below in the Ethernet PHY circuit design:

- Keep RGMII data and control signals away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- The single-ended impedance of RGMII data traces is  $50\ \Omega \pm 20\%$ .
- The length matching between Tx signals (RGMII\_TXC, RGMII\_TX\_CTL and RGMII\_TX[0:3]) or Rx signals (RGMII\_RXC, RGMII\_RX\_CTL and RGMII\_RX[0:3]) is less than 2 mm.
- Keep the spacing between Tx bus traces (RGMII\_TXC to RGMII\_TX[0:3]/RGMII\_TX\_CTL) or that between Rx bus traces (RGMII\_RXC to RGMII\_RX[0:3]/RGMII\_RX\_CTL) at least 2 times the trace width.
- Keep the spacing between Tx bus and Rx bus traces at least 2.5 times trace width. Keep the spacing between RGMII and other signal traces at least 3 times trace width. If the PCB space is enough, it is recommended to shield with ground for each signal trace.
- Resistors R7–R12 should be placed near the module. Resistors R1–R6 should be placed near the Ethernet PHY. The value of R1–R15 varies with the selection of PHY.
- ETH\_INT and ETH\_RST\_N are always 1.8 V power domain. A voltage-level translator should be used when the module I/O level does not match with PHY.

#### NOTE

RGMII and SGMII interfaces cannot be used simultaneously. RGMII is supported by default.

## 4.11. SGMII Interface

The module includes an integrated Ethernet MAC with a SGMII interface, which supports EAVB. Key features of the SGMII interface are shown below:

- Supports 1000/2500 Mbps operation <sup>11</sup>
- Supports protocols such as IEEE 1722.A (AVTP), 802.1Qav (FQTSS), 802.1Qat (SRP), 802.1AS (gPTP)
- Support connecting to an external Ethernet PHY or switch

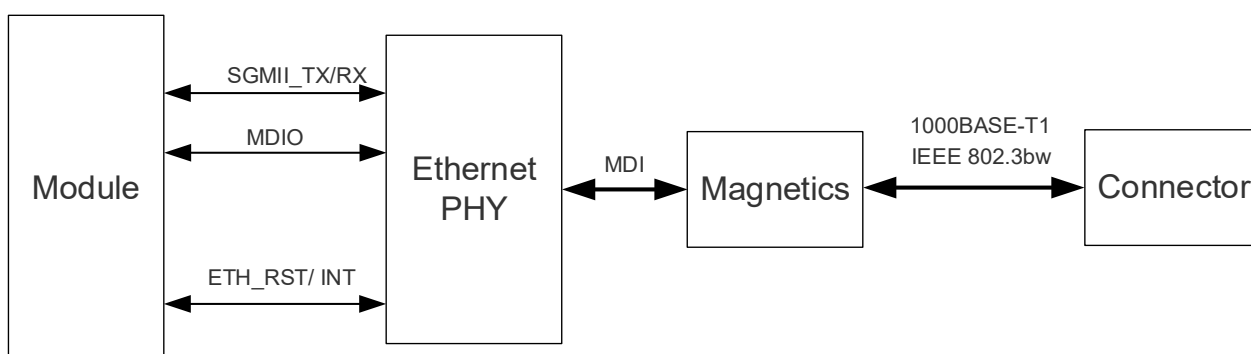
For the information about the pin definition of Ethernet management and control interfaces, see **Table 25**.

<sup>11</sup> The module's SGMII interface supports the Gigabit Ethernet protocol, while actual throughput is subject to testing.

**Table 27: Pin Description of SGMII Interface**

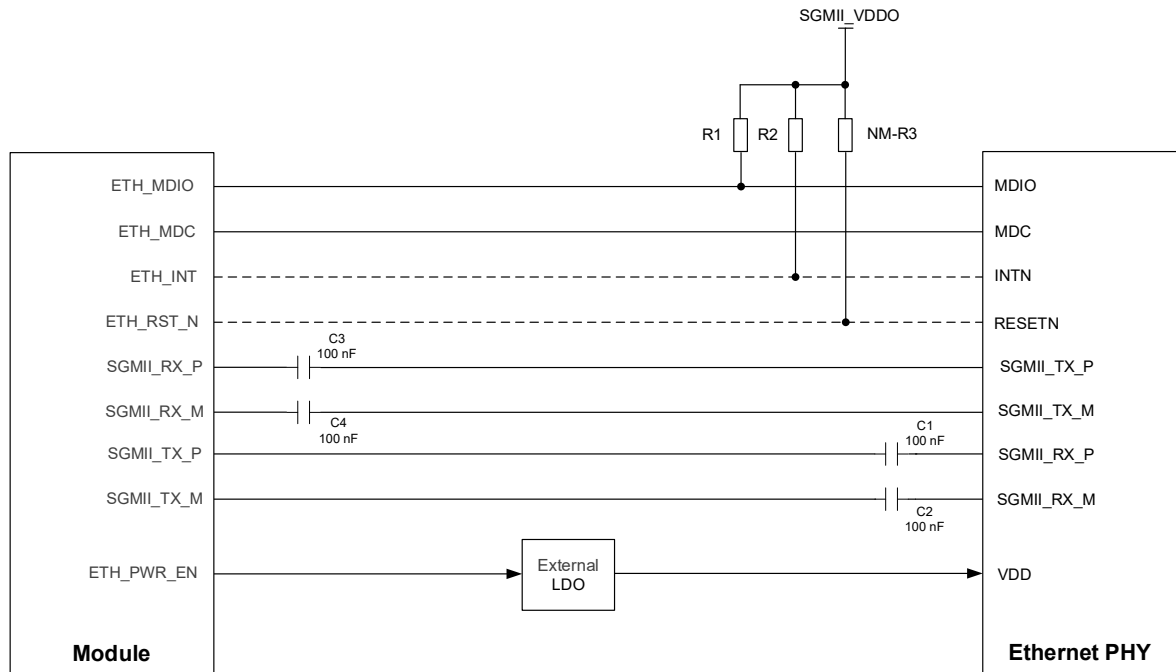
| Pin Name   | Pin No. | I/O | Description        | Comment                                                                                                                           |
|------------|---------|-----|--------------------|-----------------------------------------------------------------------------------------------------------------------------------|
| SGMII_TX_P | 94      | AO  | SGMII transmit (+) | Require differential impedance of 90–110 $\Omega$ , and 100 $\Omega$ is recommended.<br>100 nF AC coupling capacitor is required. |
| SGMII_TX_M | 96      | AO  | SGMII transmit (-) |                                                                                                                                   |
| SGMII_RX_P | 97      | AI  | SGMII receive (+)  |                                                                                                                                   |
| SGMII_RX_M | 99      | AI  | SGMII receive (-)  |                                                                                                                                   |

The following figure shows the simplified block diagram for Ethernet application.



**Figure 32: Simplified Block Diagram for Automotive Ethernet Application**

The following figure shows a reference design of SGMII interface with PHY application. For more details, please contact Wireless Mobility Technical Support.



**Figure 33: Reference Circuit of SGMII Interface with PHY Application**

To enhance the reliability and availability of application designs, follow the criteria below in the Ethernet PHY circuit design:

- It is important to route the SGMII signal traces as differential pairs with ground surrounded. The differential impedance is 90–110  $\Omega$  and 100  $\Omega$  is recommended for SGMII Tx/Rx traces.
- SGMII signals must be protected from noisy signals (clocks, DC-DC, RF and so forth). All other sensitive/high-speed signals and circuits must be routed far away from SGMII traces.
- For each differential pair, the intra-lane length match should be less than 0.7 mm, while the inter-lane length match, that is, the trace length matching between the Tx, Rx and reference clock pairs is not required.
- The spacing between Tx and Rx pairs, and the spacing between SGMII lanes and all other signals, should exceed 4 times the trace width (4W).
- ETH\_INT and ETH\_RST\_N are always 1.8 V power domain. A voltage-level translator should be used when module I/O level does not match with PHY.

**NOTE**

RGMII and SGMII interfaces cannot be used simultaneously. RGMII is supported by default.

## 4.12. GPIO Interfaces

The module provides 15 GPIOs for application designs. More GPIOs are available through pin multiplexing, for more details, please contact Wireless Mobility Technical Support.

**Table 28: Pin Description of GPIO Interfaces**

| Pin Name | Pin No. | I/O | Configurable Function | Comment                                                                                                                                   |
|----------|---------|-----|-----------------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| GPIO1    | 100     | DI  | WAKEUP_IN             | Used as WAKEUP_IN by default.<br>If the default function is not used, it can be configured to GPIO.<br>Support wake-up interrupt.         |
|          |         | DIO | GPIO                  | General-purpose input/output.<br>Support wake-up interrupt.                                                                               |
| GPIO2    | 101     | DIO | GPIO                  | General-purpose input/output.<br>Support wake-up interrupt.                                                                               |
| GPIO3    | 102     | DIO | GPIO                  | General-purpose input/output<br><b>Not</b> support wake-up interrupt.                                                                     |
| GPIO4    | 104     | DO  | SLEEP_SYS_IND         | Used as SLEEP_SYS_IND by default.<br>If the default function is not used, it can be configured to GPIO.<br>Support wake-up interrupt.     |
|          |         | DIO | GPIO                  | General-purpose input/output.<br>Support wake-up interrupt.                                                                               |
| GPIO5    | 116     | DIO | GPIO                  | General-purpose input/output.<br>Support wake-up interrupt.                                                                               |
| GPIO6    | 243     | DO  | STATUS                | Used as STATUS by default.<br>If the default function is not used, it can be configured to GPIO.<br><b>Not</b> support wake-up interrupt. |
|          |         | DIO | GPIO                  | General-purpose input/output.<br><b>Not</b> support wake-up interrupt.                                                                    |
| GPIO7    | 246     | DIO | GPIO                  | General-purpose input/output.<br>Support wake-up interrupt.                                                                               |
| GPIO8    | 249     | DIO |                       |                                                                                                                                           |
| GPIO9    | 280     | DIO |                       |                                                                                                                                           |
| GPIO10   | 283     | DIO |                       |                                                                                                                                           |
| GPIO11   | 284     | DIO |                       |                                                                                                                                           |

|        |     |     |
|--------|-----|-----|
| GPIO12 | 289 | DIO |
| GPIO13 | 64  | DIO |
| GPIO14 | 432 | DIO |
| GPIO15 | 433 | DIO |

#### NOTE

1. GPIO1 is used as WAKEUP\_IN by default. GPIO4 is used as SLEEP\_SYS\_IND by default. For more details about WAKEUP\_IN and SLEEP\_SYS\_IND, please contact Wireless Mobility Technical Support.
2. GPIO6 is used as STATUS by default. This pin is recommended to be used as an output signal.
3. If you intend to use GPIO1, GPIO4 and/or GPIO6 for other purposes, disable the corresponding default function first through software configuration.

## 4.13. ADC Interfaces

The module provides five analog-to-digital converter (ADC) interfaces. The voltage value on ADC pins can be read with related API. For more details, please contact Wireless Mobility Technical Support.

To improve the accuracy of ADC, the traces of ADC interfaces should be surrounded by ground.

**Table 29: Pin Description of ADC Interfaces**

| Pin Name | Pin No. | I/O | Description                    | Comment                     |
|----------|---------|-----|--------------------------------|-----------------------------|
| ADC0     | 247     | AI  | General-purpose ADC0 interface | Voltage range:<br>0–1.875 V |
| ADC1     | 245     | AI  | General-purpose ADC1 interface |                             |
| ADC2     | 113     | AI  | General-purpose ADC2 interface |                             |
| ADC3     | 447     | AI  | General-purpose ADC3 interface |                             |
| ADC4     | 448     | AI  | General-purpose ADC4 interface |                             |

The following table describes the characteristic of ADC interfaces.

**Table 30: Characteristic of ADC Interface**

| Parameter                | Min. | Typ. | Max.  | Unit |
|--------------------------|------|------|-------|------|
| ADC0 Input Voltage Range | 0    | -    | 1.875 | V    |
| ADC1 Input Voltage Range | 0    | -    | 1.875 | V    |
| ADC2 Input Voltage Range | 0    | -    | 1.875 | V    |
| ADC3 Input Voltage Range | 0    | -    | 1.875 | V    |
| ADC4 Input Voltage Range | 0    | -    | 1.875 | V    |
| ADC Resolution           | -    | 15   | -     | bits |
| ADC Sample Rate          | -    | 4.8  | -     | MHz  |

**NOTE**

1. The input voltage for each ADC interface must not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application.

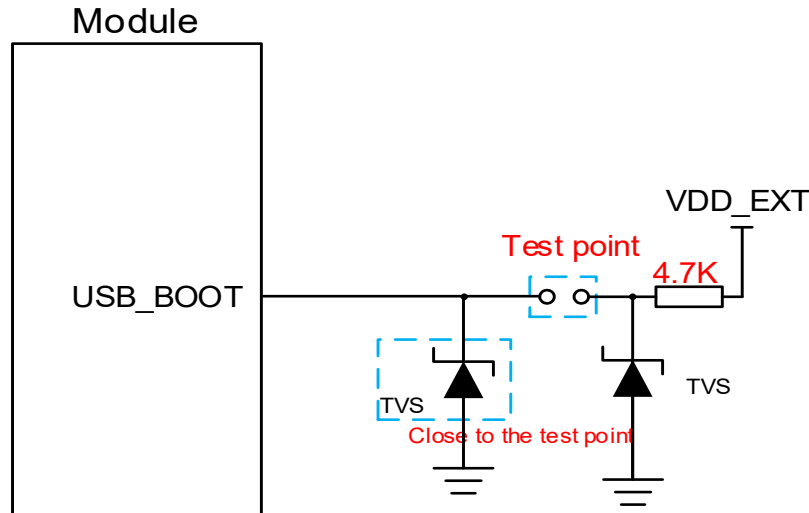
## 4.14. Forced Download Interface

The module provides a USB\_BOOT pin. Pull up USB\_BOOT to VDD\_EXT before turning on the module, and then the module will enter forced download mode. In this mode, the module supports firmware upgrade over USB interface.

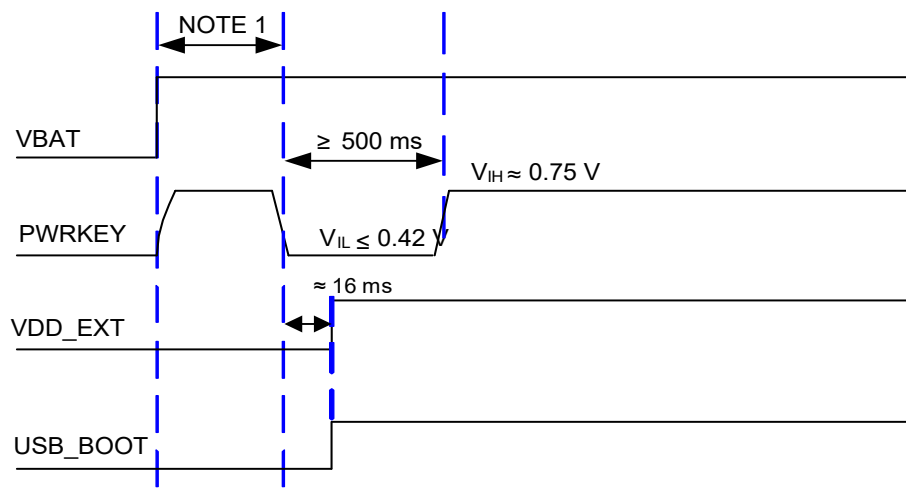
**Table 31: Pin Description of USB\_BOOT Interface**

| Pin Name | Pin No. | I/O | Description                         | Comment                                                                          |
|----------|---------|-----|-------------------------------------|----------------------------------------------------------------------------------|
| USB_BOOT | 83      | DI  | Force the module into download mode | 1.8 V power domain.<br>Active high.<br>It is recommended to reserve test points. |

The following figure shows a reference design of USB\_BOOT interface.



**Figure 34: Reference Design of USB\_BOOT Interface**



**Figure 35: Forced Download Mode Timing**

**NOTE**

1. Ensure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin is not less than 50 ms.
2. When using MCU to control the module entering forced download mode, follow the above timing. It is not recommended to pull up USB\_BOOT to VDD\_EXT before VBAT powers up. Connecting the test points as shown in **Figure 34** can manually force the module into download mode.
3. Ensure that the RESET\_N cannot be pulled up or down externally when the module enters forced download mode.

## 4.15. RTC

The module has a real time clock within the PMIC, but has no dedicated RTC power supply pin. The RTC is powered by VBAT\_BB. If VBAT\_BB is removed, the RTC will not maintain. If RTC is needed, then VBAT\_BB must be powered. For more details, please contact Wireless Mobility Technical Support.

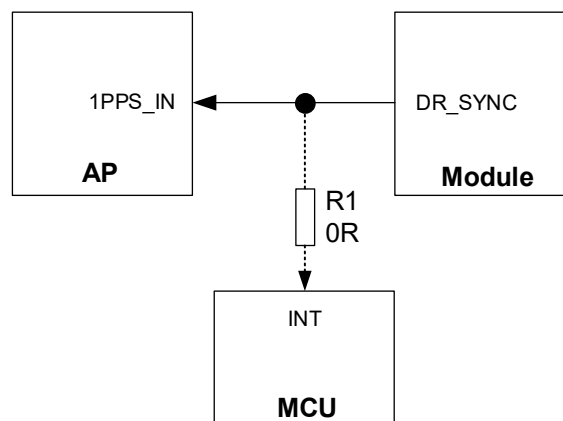
## 4.16. DR\_SYNC

The module obtains time through GNSS positioning and outputs 1PPS signal for clock synchronization. The DR\_SYNC pin usually connects to an external AP and a MCU to maintain the time consistency between the three.

**Table 32: Pin Description of DR\_SYNC**

| Pin Name | Pin No. | I/O | Description         |
|----------|---------|-----|---------------------|
| DR_SYNC  | 95      | DO  | Dead reckoning sync |

A reference design of DR\_SYNC interface for clock synchronization application is shown as below:



**Figure 36: Reference Design of DR\_SYNC for Clock Synchronization Application**

### NOTE

Pay attention to the level matching of the signal shown in dotted line between the module and the MCU.

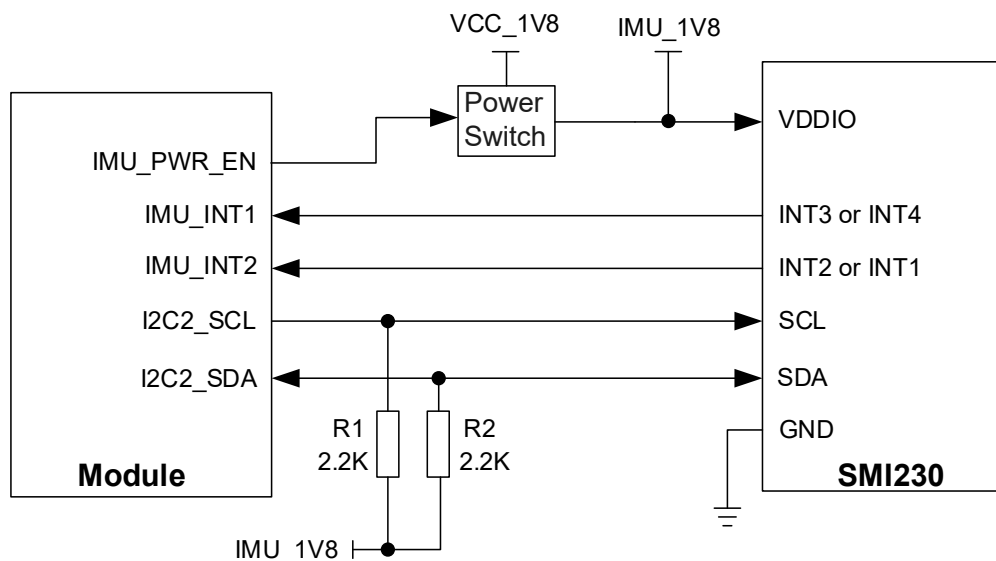
## 4.17. IMU Interrupt Interface

The module realizes DR (dead-reckoning) function through an external IMU. For more details about IMU, please contact Wireless Mobility Technical Support.

**Table 33: Pin Description of IMU Interrupt Interface**

| Pin Name   | Pin No. | I/O | Description              | Comment                                                 |
|------------|---------|-----|--------------------------|---------------------------------------------------------|
| IMU_PWR_EN | 181     | DO  | IMU power enable control |                                                         |
| IMU_INT1   | 169     | DI  | IMU interrupt 1          | 1.8 V power domain.<br>If unused, keep these pins open. |
| IMU_INT2   | 187     | DI  | IMU interrupt 2          |                                                         |

A reference design of IMU interrupt interface is shown as below:



**Figure 37: IMU Reference Design Circuit**

### NOTE

The module also supports TDK IAM-20680 and ST ASM330LHH sensors.

## 4.18. SEL\_BOOT\_PARTITION\*

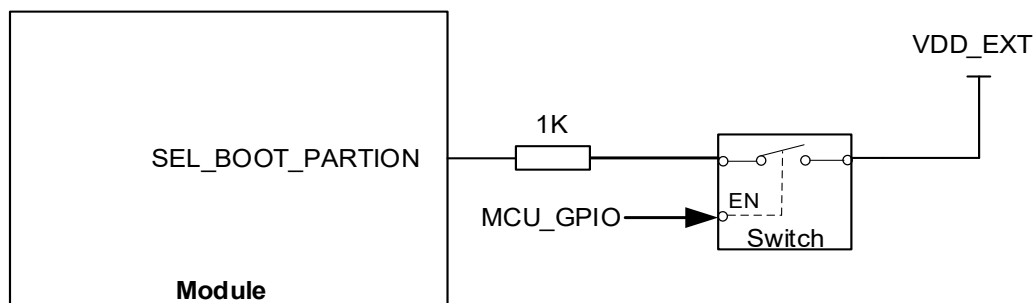
The module sets the partitions involved in startup into two sets, namely, A system and B system. The two systems burn the same image and back up each other. The A/B system is switched by software by default. The module also supports switching A/B partition address through SEL\_BOOT\_PARTITION in hardware. Partition address switching in hardware is disabled by default, if this function is required, please contact Wireless Mobility Technical Support.

For more details of A/B partition address, please contact Wireless Mobility Technical Support.

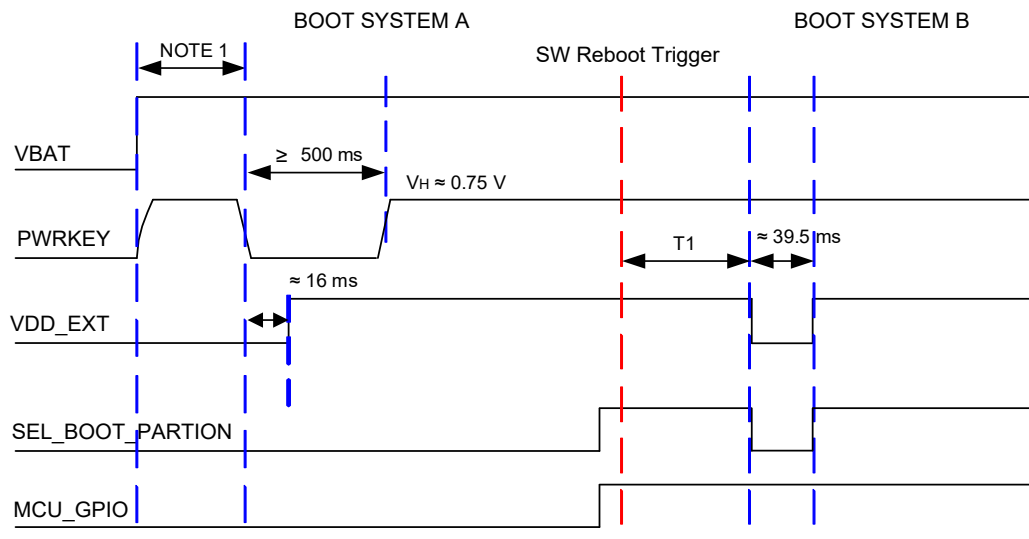
**Table 34: Pin Description of SEL\_BOOT\_PARTITION**

| Pin Name           | Pin No. | I/O | Description                                  | Comment                                                                                                                                                                       |
|--------------------|---------|-----|----------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SEL_BOOT_PARTITION | 271     | DI  | Select to boot from A or B partition address | By default, the module boots from A partition address. When this pin is pulled high, the module will boot from B partition address when it restarts. If unused, keep it open. |

A reference design of SEL\_BOOT\_PARTITION interrupt interface is shown as below:



**Figure 38: Reference Design of SEL\_BOOT\_PARTITION**



**Figure 39: Timing of Switching A/B System**

**NOTE**

1. Ensure that VBAT is stable before pulling down the PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down the PWRKEY pin is not less than 50 ms.
2. The shutdown time ( $T_1$ ) of the power supply depend on the actual running business, and if the module has tasks to deal with during shutdown, the time may be longer.
3. It is recommended to restart the module by software mechanisms.

# 5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module supports main antenna interface, diversity antenna interface <sup>12</sup> and GNSS antenna interface, and the impedance of antenna ports is 50  $\Omega$ .

## NOTE

1. The module supports 2 × 2 MIMO antennas configuration (ANT\_MAIN & ANT\_DIV) by default, 4 × 4 MIMO antennas configuration (ANT\_MAIN, ANT\_DIV, ANT\_MIMO3 and ANT\_MIMO4) is optional but not supported by default. If you need 4 × 4 MIMO antenna function, please consult with Wireless Mobility Technical Support.
2. ANT\_ECALL is optional but not supported by default. If ANT\_ECALL is supported, it only takes effect in eCall switching mode.
3. GNSS is optional. L1 are supported by default. If you need GNSS dual-band function, please consult with Wireless Mobility Technical Support.

<sup>12</sup> Diversity antenna interface is used to resist the fall of signals caused by high-speed movement and multipath effect.

## 5.1. Cellular Antenna Interfaces

### 5.1.1. Pin Definition <sup>13</sup>

The pin definition of cellular antenna interfaces is shown below.

**Table 35: Pin Description of Cellular Antenna Interfaces – WMC598E-GL**

| Pin Name | Pin No. | I/O | Description                                                                                                                                                                                                                   | LB (MHz) | MHB (MHz) | UHB (MHz) |
|----------|---------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-----------|-----------|
| ANT_MAIN | 143     | AIO | <ul style="list-style-type: none"> <li>● GSM DCS1800/PCS1900 Tx &amp; PRx</li> <li>● WCDMA MHB Tx &amp; PRx</li> <li>● LTE MHB Tx &amp; PRx</li> <li>● LTE UHB Tx &amp; PRx</li> <li>● 5G NR MHB (SA) Tx &amp; PRx</li> </ul> | 617–960  | 1695–2690 | 3300–5000 |
|          |         |     | 5G NR n41/n77/n78/n79 (SA) Tx & PRx                                                                                                                                                                                           |          |           |           |
|          |         |     | 5G NR MHB (NSA) Tx @ LTE LB + 5G NR MHB EN-DC Combos                                                                                                                                                                          |          |           |           |
|          |         |     | 5G NR n41 (NSA) Tx @ LTE LB + n41 EN-DC Combos                                                                                                                                                                                |          |           |           |
|          |         |     | 5G NR n77/n78/n79 (NSA) Tx @ LTE LB + n77/n78/n79 EN-DC Combos                                                                                                                                                                |          |           |           |
|          |         |     |                                                                                                                                                                                                                               |          |           |           |
|          |         |     |                                                                                                                                                                                                                               |          |           |           |

<sup>13</sup> Frequency range of LB, MB, HB and UHB:  
 LB: < 1 GHz;  
 MB: 1–2.3 GHz;  
 HB: 2.3–2.7 GHz;  
 UHB: 3.3–6.0 GHz.

|         |     |     |                                                                                                                                                                                                                                                                                                                                                                           |         |           |           |
|---------|-----|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----------|-----------|
|         |     |     | <ul style="list-style-type: none"> <li>● WCDMA LB DRx</li> <li>● LTE LB DRx</li> <li>● 5G NR (SA) LB DRx</li> </ul>                                                                                                                                                                                                                                                       |         |           |           |
|         |     |     | <ul style="list-style-type: none"> <li>● <b>GSM GSM850/EGSM900 Tx &amp; PRx</b></li> <li>● <b>WCDMA LB Tx &amp; PRx</b></li> <li>● <b>LTE LB Tx &amp; PRx</b></li> <li>● <b>5G NR LB (SA) Tx &amp; PRx</b></li> <li><b>5G NR LB (NSA) Tx @ LTE MHB + 5G NR LB EN-DC Combos</b></li> <li><b>5G NR n77/n78/n79 (NSA) Tx @ LTE MHB + n77/n78/n79 EN-DC Combos</b></li> </ul> |         |           |           |
| ANT_DIV | 152 | AIO |                                                                                                                                                                                                                                                                                                                                                                           | 617–960 | 1695–2690 | 3300–5000 |
|         |     |     | <ul style="list-style-type: none"> <li>● WCDMA MHB DRx</li> <li>● LTE MHB DRx</li> <li>● LTE UHB DRx</li> <li>● 5G NR (SA) MHB DRx</li> <li>5G NR n41/n77/n78/n79 (SA) DRx</li> </ul>                                                                                                                                                                                     |         |           |           |

#### NOTE

1. The frequency bands in bold in the table above support both transmission and reception.
2. The module supports the two cellular antennas (ANT\_MAIN and ANT\_DIV) by default. The lack of any one antenna may cause the loss of performance and function.
3. Before designing and evaluating, for more information on CA & EN-DC features, please contact Wireless Mobility Technical Support.

## 5.1.2. Operating Frequencies

**Table 36: WMC598E-GL Operating Frequencies**

| 3GPP Band   | Transmit  | Receive   | Unit |
|-------------|-----------|-----------|------|
| GSM850      | 824–849   | 869–894   | MHz  |
| EGSM900     | 880–915   | 925–960   | MHz  |
| DCS1800     | 1710–1785 | 1805–1880 | MHz  |
| DCS1900     | 1850–1910 | 1930–1990 | MHz  |
| WCDMA B1    | 1920–1980 | 2110–2170 | MHz  |
| WCDMA B2    | 1850–1910 | 1930–1990 | MHz  |
| WCDMA B4    | 1710–1755 | 2110–2155 | MHz  |
| WCDMA B5    | 824–849   | 869–894   | MHz  |
| WCDMA B8    | 880–915   | 925–960   | MHz  |
| WCDMA B19   | 830-845   | 875-890   | MHz  |
| LTE-FDD B1  | 1920–1980 | 2110–2170 | MHz  |
| LTE-FDD B2  | 1850–1910 | 1930–1990 | MHz  |
| LTE-FDD B3  | 1710–1785 | 1805–1880 | MHz  |
| LTE-FDD B4  | 1710–1755 | 2110–2155 | MHz  |
| LTE-FDD B5  | 824–849   | 869–894   | MHz  |
| LTE-FDD B7  | 2500–2570 | 2620–2690 | MHz  |
| LTE-FDD B8  | 880–915   | 925–960   | MHz  |
| LTE-FDD B12 | 699–716   | 729–746   | MHz  |
| LTE-FDD B13 | 777–787   | 746–756   | MHz  |
| LTE-FDD B14 | 788–798   | 758–768   | MHz  |
| LTE-FDD B17 | 704–716   | 734–746   | MHz  |
| LTE-FDD B18 | 815-830   | 860-875   | MHz  |

|                           |           |           |     |
|---------------------------|-----------|-----------|-----|
| LTE-FDD B19               | 830-845   | 875-890   | MHz |
| LTE-FDD B20               | 832-862   | 791-821   | MHz |
| LTE-FDD B25               | 1850-1915 | 1930-1995 | MHz |
| LTE-FDD B26               | 814-849   | 859-894   | MHz |
| LTE-FDD B28               | 703-748   | 758-803   | MHz |
| LTE-FDD B29 <sup>14</sup> | -         | 717-728   | MHz |
| LTE-TDD B34               | 2010-2025 | 2010-2025 | MHz |
| LTE-TDD B38               | 2570-2620 | 2570-2620 | MHz |
| LTE-TDD B39               | 1880-1920 | 1880-1920 | MHz |
| LTE-TDD B40               | 2300-2400 | 2300-2400 | MHz |
| LTE-TDD B41               | 2496-2690 | 2496-2690 | MHz |
| LTE-TDD B42               | 3400-3600 | 3400-3600 | MHz |
| LTE-TDD B43               | 3600-3800 | 3600-3800 | MHz |
| LTE-TDD B48               | 3550-3700 | 3550-3700 | MHz |
| LTE-FDD B66               | 1710-1780 | 2110-2200 | MHz |
| LTE-FDD B71               | 663-698   | 617-652   | MHz |
| 5G NR FDD n1              | 1920-1980 | 2110-2170 | MHz |
| 5G NR FDD n2              | 1850-1910 | 1930-1990 | MHz |
| 5G NR FDD n3              | 1710-1785 | 1805-1880 | MHz |
| 5G NR FDD n5              | 824-849   | 869-894   | MHz |
| 5G NR FDD n7              | 2500-2570 | 2620-2690 | MHz |
| 5G NR FDD n8              | 880-915   | 925-960   | MHz |
| 5G NR FDD n12             | 699-716   | 729-746   | MHz |
| 5G NR FDD n14             | 788-798   | 758-768   | MHz |

<sup>14</sup> B29 supports Rx only.

|               |           |           |     |
|---------------|-----------|-----------|-----|
| 5G NR FDD n20 | 832–862   | 791–821   | MHz |
| 5G NR FDD n25 | 1850–1915 | 1930–1995 | MHz |
| 5G NR FDD n26 | 814–849   | 859–894   | MHz |
| 5G NR FDD n28 | 703–748   | 758–803   | MHz |
| 5G NR TDD n38 | 2570–2620 | 2570–2620 | MHz |
| 5G NR TDD n40 | 2300–2400 | 2300–2400 | MHz |
| 5G NR TDD n41 | 2496–2690 | 2496–2690 | MHz |
| 5G NR TDD n48 | 3550–3700 | 3550–3700 | MHz |
| 5G NR FDD n66 | 1710–1780 | 2110–2200 | MHz |
| 5G NR FDD n70 | 1695–1710 | 1995–2020 | MHz |
| 5G NR FDD n71 | 663–698   | 617–652   | MHz |
| 5G NR TDD n77 | 3300–4200 | 3300–4200 | MHz |
| 5G NR TDD n78 | 3300–3800 | 3300–3800 | MHz |
| 5G NR TDD n79 | 4400–5000 | 4400–5000 | MHz |

### 5.1.3. Transmitting Power

The following table shows the transmitting power of the module.

**Table 37: Transmitting Power (25 °C, 3.8 V Power Supply)**

| Type  | Frequency Band | Max. Transmitting Power     | Min. Transmitting Power |
|-------|----------------|-----------------------------|-------------------------|
| GSM   | GSM850         | Class 4 (33 dBm $\pm$ 2 dB) | 5 dBm $\pm$ 5 dB        |
|       | EGSM900        | Class 4 (33 dBm $\pm$ 2 dB) | 5 dBm $\pm$ 5 dB        |
|       | DCS1800        | Class 1 (30 dBm $\pm$ 2 dB) | 0 dBm $\pm$ 5 dB        |
|       | PCS1900        | Class 1 (30 dBm $\pm$ 2 dB) | 0 dBm $\pm$ 5 dB        |
| WCDMA | WCDMA bands    | Class 3 (23 dBm $\pm$ 2 dB) | < -50 dBm               |

|       |                                                                         |                               |           |
|-------|-------------------------------------------------------------------------|-------------------------------|-----------|
| LTE   | LTE FDD MHB bands<br>(B1/B2/B3/B4/B7/B25/B66)                           | Class 3 (23.5 dBm +1.5/-2 dB) | < -40 dBm |
|       | LTE FDD LB bands<br>(B5/B8/B12/B13/B14/B17/B18/<br>B19/B20/B26/B28/B71) | Class 3 (23.7 dBm +1.3/-2 dB) | < -40 dBm |
|       | LTE TDD B34/B38/B39                                                     | Class 3 (23.5 dBm +1.5/-2 dB) | < -40 dBm |
|       | LTE TDD B42/B43/B48                                                     | Class 3 (23 dBm $\pm$ 2 dB)   | < -40 dBm |
|       | LTE TDD HPUE bands B40/B41                                              | Class 2 (26 dBm $\pm$ 2 dB)   | < -40 dBm |
| 5G NR | 5G NR FDD MHB bands<br>(n1/n2/n3/n7/n25/n66/n70)                        | Class 3 (23.5 dBm +1.5/-2 dB) | < -40 dBm |
|       | 5G NR FDD LB bands<br>(n5/n8/n12/n14/n20/n26/n28/n71)                   | Class 3 (23.7 dBm +1.3/-2 dB) | < -40 dBm |
|       | 5G NR TDD n38/n40                                                       | Class 3 (23.5 dBm +1.5/-2 dB) | < -40 dBm |
|       | 5G NR TDD n48                                                           | Class 3 (23 dBm $\pm$ 2 dB)   | < -40 dBm |
|       | 5G NR TDD HPUE bands<br>(n41/n77/n78/n79)                               | Class 2 (26 dBm $\pm$ 2 dB)   | < -40 dBm |

#### NOTE

1. For GPRS/EDGE transmissions on four uplink timeslots, the maximum transmitting power reduction is 4.0 dB. The design complies with *3GPP TS 51.010-1*: GPRS complies with **subclause 13.16**, and EDGE complies with **subclause 13.17**.
2. WCDMA maximum transmitting power meets *3GPP TS 34.121-1* requirements.
3. LTE maximum transmitting power meets *3GPP TS 36.521-1* requirements and it is tested @ BW = 10 MHz, 1 RB.
4. 5G NR maximum transmitting power meets *3GPP TS 38.521-1* requirements.

### 5.1.4. Receiver Sensitivity

**Table 38: WMC598E-GL RF Receiver Sensitivity (3.8 V, Room Temperature)**

| Frequency Band | SIMO <sup>15</sup>  |        |                      | 3GPP SIMO |
|----------------|---------------------|--------|----------------------|-----------|
|                | Min.<br>(Best Case) | Typ.   | Max.<br>(Worst Case) |           |
| GSM850         | -113.5              | -107.5 | -102                 | -102      |

<sup>15</sup> Test conditions for the receiver sensitivity of WMC598E-GL:

- GSM bands: tested with 1 antenna (1Rx);
- WCDMA/LTE/5G NR bands: tested with 2 antennas (2Rx);

|                      |        |        |        |        |
|----------------------|--------|--------|--------|--------|
| EGSM900              | -113.2 | -107.5 | -102   | -102   |
| DCS1800              | -112.8 | -107   | -102   | -102   |
| PCS1900              | -112.4 | -107   | -102   | -102   |
| WCDMA B1             | -113.5 | -111   | -106.7 | -106.7 |
| WCDMA B2             | -113.4 | -111   | -104.7 | -104.7 |
| WCDMA B4             | -113.5 | -111   | -106.7 | -106.7 |
| WCDMA B5             | -115.2 | -111   | -104.7 | -104.7 |
| WCDMA B8             | -115   | -111   | -103.7 | -103.7 |
| WCDMA B19            | -115.7 | -111   | -106.7 | -106.7 |
| LTE-FDD B1 (10 MHz)  | -101.3 | -100.3 | -96.3  | -96.3  |
| LTE-FDD B2 (10 MHz)  | -101.2 | -98.3  | -94.3  | -94.3  |
| LTE-FDD B3 (10 MHz)  | -101.4 | -97.3  | -93.3  | -93.3  |
| LTE-FDD B4 (10 MHz)  | -101.2 | -100.3 | -96.3  | -96.3  |
| LTE-FDD B5 (10 MHz)  | -103   | -98.3  | -94.3  | -94.3  |
| LTE-FDD B7 (10 MHz)  | -101   | -98.3  | -94.3  | -94.3  |
| LTE-FDD B8 (10 MHz)  | -102.6 | -97.3  | -93.3  | -93.3  |
| LTE-FDD B12 (10 MHz) | -102.8 | -97.3  | -93.3  | -93.3  |
| LTE-FDD B13 (10 MHz) | -102.5 | -97.3  | -93.3  | -93.3  |
| LTE-FDD B14 (10 MHz) | -102.5 | -97.3  | -93.3  | -93.3  |
| LTE-FDD B17 (10 MHz) | -103.1 | -97.3  | -93.3  | -93.3  |
| LTE-FDD B18 (10 MHz) | -102.9 | -100.3 | -96.3  | -96.3  |
| LTE-FDD B19 (10 MHz) | -102.9 | -100.3 | -96.3  | -96.3  |
| LTE-FDD B20 (10 MHz) | -102.8 | -97.3  | -93.3  | -93.3  |
| LTE-FDD B25 (10 MHz) | -101.2 | -96.8  | -92.8  | -92.8  |
| LTE-FDD B26 (10 MHz) | -102.8 | -97.8  | -93.8  | -93.8  |
| LTE-FDD B28 (10 MHz) | -102.6 | -98.8  | -94.8  | -94.8  |

|                                    |        |       |       |       |
|------------------------------------|--------|-------|-------|-------|
| LTE-FDD B29 (10 MHz) <sup>16</sup> | -102.3 | -97.3 | -93.3 | -93.3 |
| LTE-TDD B34 (10 MHz)               | -101.5 | -99.3 | -96.3 | -96.3 |
| LTE-TDD B38 (10 MHz)               | -100.4 | -99.3 | -96.3 | -96.3 |
| LTE-TDD B39 (10 MHz)               | -100.6 | -99.3 | -96.3 | -96.3 |
| LTE-TDD B40 (10 MHz)               | -100.4 | -99.3 | -96.3 | -96.3 |
| LTE-TDD B41 (10 MHz)               | -99.4  | -97.3 | -94.3 | -94.3 |
| LTE-TDD B42 (10 MHz)               | -99.3  | -98   | -95.0 | -95.0 |
| LTE-TDD B43 (10 MHz)               | -99.6  | -98   | -95.0 | -95.0 |
| LTE-TDD B48 (10 MHz)               | -99.7  | -98   | -95.0 | -95.0 |
| LTE-FDD B66 (10 MHz)               | -100.9 | -99.8 | -95.8 | -95.8 |
| LTE-FDD B71 (10 MHz)               | -102.8 | -97.5 | -93.5 | -93.5 |
| 5G NR FDD n1 (20 MHz)              | -99.6  | -97.1 | -93.1 | -93.1 |
| 5G NR FDD n2 (20 MHz)              | -99.5  | -95.1 | -91.1 | -91.1 |
| 5G NR FDD n3 (20 MHz)              | -100   | -94.1 | -90.1 | -90.1 |
| 5G NR FDD n5 (20 MHz)              | -100.6 | -92.1 | -86.1 | -86.1 |
| 5G NR FDD n7 (20 MHz)              | -99.5  | -95.1 | -91.1 | -91.1 |
| 5G NR FDD n8 (20 MHz)              | -100.2 | -89.1 | -85.1 | -85.1 |
| 5G NR FDD B12 (10 MHz)             | -103.6 | -97.1 | -93.1 | -93.1 |
| 5G NR FDD B14 (10 MHz)             | -103.4 | -97.1 | -93.1 | -93.1 |
| 5G NR FDD n20 (10 MHz)             | -103.7 | -97.1 | -93.1 | -93.1 |
| 5G NR FDD n25 (20 MHz)             | -99.5  | -93.6 | -89.6 | -89.6 |
| 5G NR FDD n26 (20 MHz)             | -99.9  | -90.9 | -86.9 | -86.9 |
| 5G NR FDD n28 (20 MHz)             | -100.6 | -94.1 | -90.1 | -90.1 |
| 5G NR TDD n38 (20 MHz)             | -99.5  | -97.1 | -93.1 | -93.1 |
| 5G NR TDD n40 (20 MHz)             | -99.1  | -97.1 | -93.1 | -93.1 |

<sup>16</sup> LTE-FDD B29 supports Rx only, so the sensitivity of the bands is tested with CA combination, in which B29 is tested with 2 antennas (2Rx).

|                         |        |       |       |       |
|-------------------------|--------|-------|-------|-------|
| 5G NR TDD n41 (100 MHz) | -92    | -87.8 | -83.8 | -83.8 |
| 5G NR TDD n48 (20 MHz)  | -99.3  | -95.8 | -91.8 | -91.8 |
| 5G NR FDD n66 (20 MHz)  | -99.2  | -96.6 | -92.6 | -92.6 |
| 5G NR FDD n70 (15 MHz)  | -100.9 | -97.1 | -93.1 | -93.1 |
| 5G NR FDD n71 (20 MHz)  | -100.8 | -89.3 | -85.3 | -85.3 |
| 5G NR TDD n77 (100 MHz) | -91.7  | -88.5 | -84.5 | -84.5 |
| 5G NR TDD n78 (100 MHz) | -91.7  | -88.5 | -84.5 | -84.5 |
| 5G NR TDD n79 (100 MHz) | -90.5  | -88.5 | -84.5 | -84.5 |

#### NOTE

1. GSM receiver sensitivity values meet 3GPP TS 51.010-1 requirements.
2. WCDMA receiver sensitivity values meet 3GPP TS 34.121-1 requirements.
3. LTE receiver sensitivity values meet 3GPP TS 36.521-1 requirements and it is tested under BW = 10 MHz according to 3GPP RB configuration.
4. 5G NR receiver sensitivity values meet 3GPP TS 38.521-1 requirements, FDD test @ SCS 15 kHz, TDD test @ SCS 30 kHz.

### 5.1.5. Reference Design

A reference design of main and diversity antenna interfaces is shown as below. Use a dual L-type matching circuit for the antenna interfaces for better RF performance and for the ease of debugging.

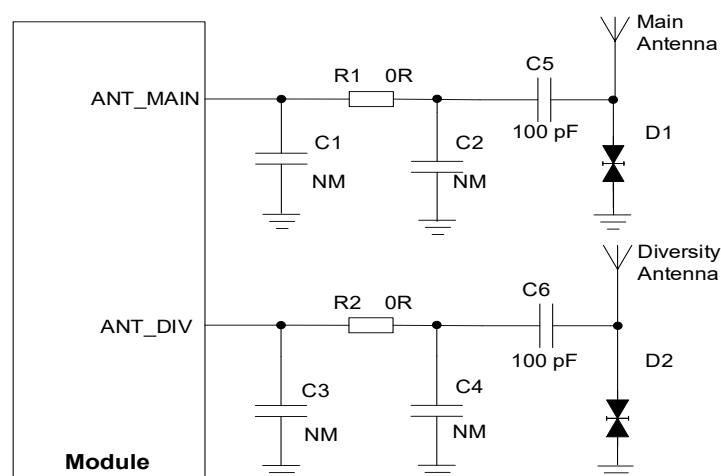


Figure 40: Reference Design of Main and Diversity Antenna Interfaces

#### NOTE

1. Keep a proper distance between each antenna to improve receiving sensitivity.
2. Place the dual L-type matching components (R1/C1/C2/C5, R2/C3/C4/C6) to antennas as close as possible.
3. Capacitors (C1–C4) are not mounted by default.
4. C5 and C6 are used for DC-blocking and the capacitance value is recommended to be 100 pF.
5. ESD protection components need to be added close to the antenna to effectively prevent static electricity. Junction capacitance of ESD protection components on the antenna interfaces is recommended to be 0.05 pF.

## 5.2. GNSS Antenna Interface (Optional)

The module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, Galileo and QZSS positioning system and SBAS augmentation system, and supports L1 (default).

The module supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1–10 Hz (1 Hz by default) data update rate via USB interface.

By default, GNSS engine of the module is switched off. It has to be switched on via an API function. For more details about GNSS engine technology and configurations, please contact Wireless Mobility Technical Support.

### 5.2.1. Pin Definition

The following tables show the pin definition of GNSS antenna interface.

**Table 39: Pin Description of GNSS Antenna Interface**

| Pin Name | Pin No. | I/O | Description            | GNSS L1 (MHz) | Comment                |
|----------|---------|-----|------------------------|---------------|------------------------|
| ANT_GNSS | 197     | AI  | GNSS antenna interface | 1559–1606     | 50 $\Omega$ impedance. |

## 5.2.2. Operating Frequency

**Table 40: GNSS Operating Frequency**

| Type    | Frequency Band                                           | Unit |
|---------|----------------------------------------------------------|------|
| GPS     | 1575.42 $\pm$ 1.023 (L1)                                 | MHz  |
| GLONASS | 1601.7 $\pm$ 4.2 (L1)                                    | MHz  |
| Galileo | 1575.42 $\pm$ 2.046 (E1)                                 | MHz  |
| BDS     | 1561.098 $\pm$ 2.046 (B1I)<br>1575.42 $\pm$ 16.368 (B1C) | MHz  |
| QZSS    | 1575.42 $\pm$ 1.023 (L1)                                 | MHz  |

## 5.2.3. GNSS Performance

The module's internal GNSS path does not include an external LNA (eLNA), so an active antenna with an LNA must be used. The GNSS performance of the module is shown in the table below. The sensitivity test environment: an eLNA with approximately 18 dB gain is used outside the test instrument.

**Table 41: GNSS Performance**

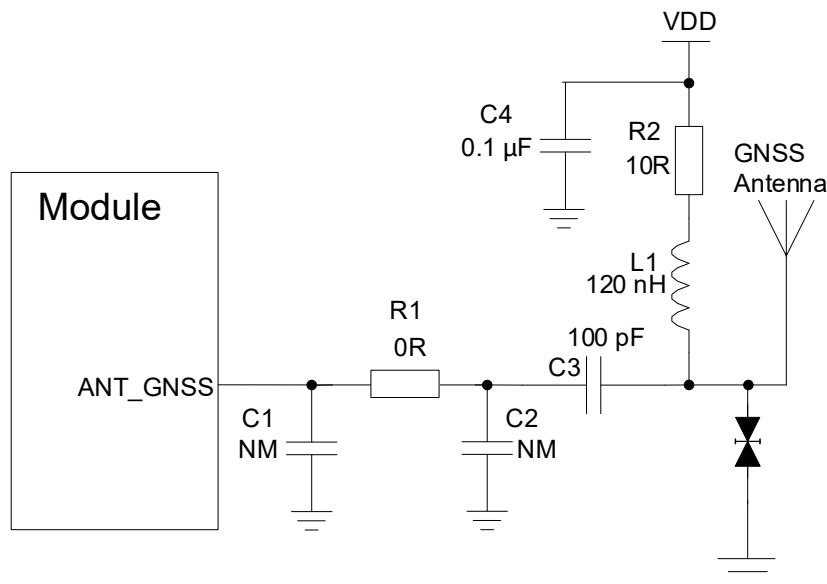
| Parameter   | Description           | Conditions            | Typ. | Unit |
|-------------|-----------------------|-----------------------|------|------|
| Sensitivity | Acquisition           | Autonomous            | TBD  | dBm  |
|             | Reacquisition         | Autonomous            | TBD  | dBm  |
|             | Tracking              | Autonomous            | TBD  | dBm  |
| TTFF        | Cold start @ open sky | Autonomous            | TBD  | s    |
|             |                       | XTRA start            | TBD  | s    |
|             | Warm start @ open sky | Autonomous            | TBD  | s    |
|             |                       | XTRA start            | TBD  | s    |
|             | Hot start @ open sky  | Autonomous            | TBD  | s    |
|             |                       | XTRA start            | TBD  | s    |
| Accuracy    | CEP-50                | Autonomous @ open sky | TBD  | m    |

**NOTE**

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (within 5 minutes, the GNSS signal lost lock times  $\leq 3$ , and GNSS signal lost lock time cannot exceed 10 seconds each time).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 5 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

### 5.2.4. Reference Design

A reference design of GNSS antenna is shown as below.



**Figure 41: Reference Circuit of GNSS Antenna**

**NOTE**

1. GNSS is an optional function. If unused, keep ANT\_GNSS open.
2. An external LDO can be selected to supply power according to the active antenna requirement.
3. An ESD protection component need to be added close to the antenna to effectively prevent static electricity. Junction capacitance of ESD protection component on the antenna interface is recommended to be 0.05 pF.
4. C3 is used for DC-blocking and the capacitance value is recommended to be 100 pF.
5. When LTE B13 or B14 is supported, it is recommended to add a 25 dB notch circuit at the LNA input end of the active antenna to filter the frequency of LTE B13 or B14.

### 5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to  $50\ \Omega$ . The impedance of the RF traces is usually determined by the trace width ( $W$ ), the materials' dielectric constant, the height from the reference ground to the signal layer ( $H$ ), and the spacing between RF traces and grounds ( $S$ ). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

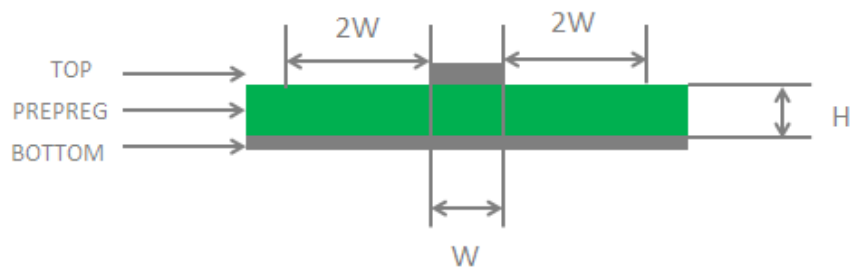


Figure 42: Microstrip Design on a 2-layer PCB

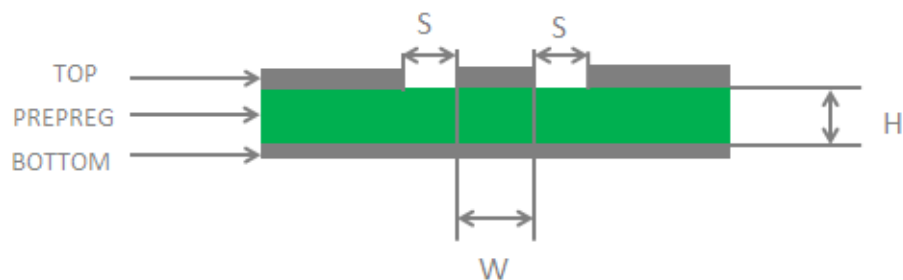


Figure 43: Coplanar Waveguide Design on a 2-layer PCB

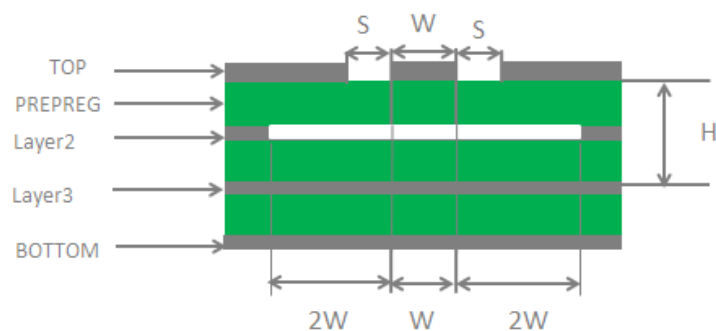
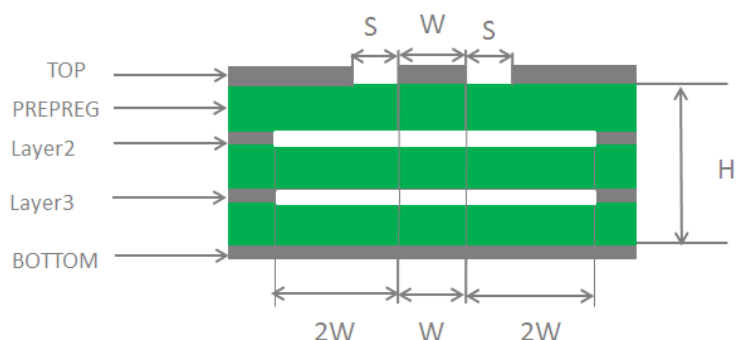


Figure 44: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)



**Figure 45: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)**

To ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50  $\Omega$ .
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces ( $2 \times W$ ).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, please contact Wireless Mobility Technical Support.

## 5.4. Antenna Design Requirements

The following table shows the requirements on RF antenna design.

**Table 42: Antenna Design Requirements**

| Type | Requirements                          |
|------|---------------------------------------|
| GNSS | Frequency range:<br>L1: 1559–1606 MHz |

|          |                                                                                                                                                                                                                                                                                    |
|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          | Polarization: RHCP<br>VSWR: $\leq 2$ (Typ.)<br>Antenna gain: $> 0$ dBi<br>Active antenna embedded LNA noise figure: $< 1.5$ dB<br>Active antenna embedded LNA gain: see <b>NOTE 4</b> & <b>NOTE 5</b> below<br>for design considerations                                           |
| Cellular | VSWR: $\leq 2$<br>Efficiency: $> 30$ %<br>Input impedance: $50 \Omega$<br>Polarization: Vertical<br>Cable insertion loss:<br><b><math>&lt; 1</math> dB:</b> LB ( $< 1$ GHz)<br><b><math>&lt; 1.5</math> dB:</b> MB (1–2.3 GHz)<br><b><math>&lt; 2</math> dB:</b> HB ( $> 2.3$ GHz) |

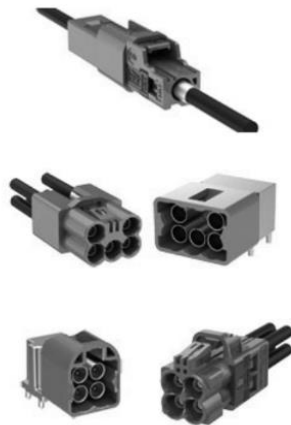
#### NOTE

1. Maximize the distance among main antenna, diversity antenna and GNSS antenna.
2. Antenna isolation:  
 $> 20$  dB @ above 1000 MHz;  
 $> 15$  dB @ 600–1000 MHz;  
 $> 10$  dB @ 400–600 MHz.
3. The isolation between each antenna traces on PCB is recommended to be over 75 dB.
4. GNSS receiver is designed to work with an external LNA (eLNA) in range of 15–20 dB. That is, ensure that the total gain from eLNA to GNSS receiver (including external active antenna, cable loss, connectors, PCB traces, and attenuator) meets 15–20 dB.
5. Attenuator ( $\pi$ -type attenuation circuit) can be used when the total gain exceeds 20 dB.

## 5.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the HFM connector provided by Rosenberger.

## HFM - Products



### Products

- HFM Cable plugs and jacks  
single, double, quad, quint  
straight and right angle  
Cable diameter: 1.2 mm; 2.9 mm; 3.6 mm
- HFM PCB connectors  
single, double, quad, quint
- HFM Cable connectors waterproof  
under development

### Features

- Frequency up to 15 GHz
- High data rates up to 20 Gbit/s
- Optimized used of space
- Saving up of installation space up to 80%
- Cost optimized

**Figure 46: Feature of the HFM Connector**

For more details, visit <https://www.rosenbergerap.com>.

# 6 Electrical Characteristics and Reliability

## 6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

**Table 43: Absolute Maximum Ratings**

| Parameter               | Min. | Max. | Unit |
|-------------------------|------|------|------|
| VBAT_RF/VBAT_BB         | -0.3 | 6.0  | V    |
| USB_VBUS                | -0.3 | 5.5  | V    |
| Voltage at Digital Pins | -0.3 | 2.13 | V    |
| ADC Input Voltage       | 0    | 2.2  | V    |

### NOTE

Exceeding the conditions of use as shown above may cause permanent damage to the module.

## 6.2. Power Supply Ratings

**Table 44: Power Supply Ratings**

| Parameter                                      | Description                                               | Conditions                                                                     | Min. | Typ.  | Max. | Unit |
|------------------------------------------------|-----------------------------------------------------------|--------------------------------------------------------------------------------|------|-------|------|------|
| VBAT_BB,<br>VBAT_RF                            | VBAT_BB and VBAT_RF                                       | The actual input voltages must be kept between the minimum and maximum values. | 3.3  | 3.8   | 4.3  | V    |
| I <sub>VBAT_BB</sub> ,<br>I <sub>VBAT_RF</sub> | Peak supply current under BB and RF application scenarios | -                                                                              | -    | -     | 4.0  | A    |
| USB_VBUS                                       | USB connection detect                                     | -                                                                              | 3.0  | 5.0   | 5.25 | V    |
| VDD_EXT                                        | Provide 1.8 V for external circuits                       | -                                                                              | -    | 1.8   | -    | V    |
|                                                |                                                           |                                                                                | -    | -     | 50   | mA   |
| VDD_WIFI_VL                                    | Low-voltage power supply for Wi-Fi & Bluetooth module     | -                                                                              | -    | 0.976 | -    | V    |
|                                                |                                                           |                                                                                | -    | -     | 1.7  | A    |
| VDD_WIFI_VM                                    | Medium-voltage power supply for Wi-Fi & Bluetooth module  | -                                                                              | -    | 1.28  | -    | V    |
|                                                |                                                           |                                                                                | -    | -     | 0.45 | A    |
| VDD_WIFI_VH                                    | High-voltage power supply for Wi-Fi & Bluetooth module    | -                                                                              | -    | 1.88  | -    | V    |
|                                                |                                                           |                                                                                | -    | -     | 0.45 | A    |
| USIM_VDD                                       | (U)SIM card power supply                                  | 1.8 V application                                                              | 1.65 | 1.8   | 1.95 | V    |
|                                                |                                                           | 3.0 V application                                                              | 2.7  | 2.95  | 3.05 | V    |

## 6.3. Power Consumption

Table 45: WMC598E-GL Power Consumption (25 °C, 3.8 V Power Supply)

| Test Mode   | Test Condition                       | Typ.  | Unit |
|-------------|--------------------------------------|-------|------|
| OFF state   | Power down                           | 0.164 | mA   |
|             | <b>AT+CFUN=0</b> (USB disconnected)  | 1.192 | mA   |
|             | <b>AT+CFUN=4</b> (USB disconnected)  | 1.273 | mA   |
|             | EGSM900 @ DRX = 2                    | 3.212 | mA   |
|             | EGSM900 @ DRX = 5                    | 2.498 | mA   |
|             | EGSM900 @ DRX = 5 (USB Suspend)      | -     | mA   |
|             | EGSM900 @ DRX = 9                    | 2.021 | mA   |
|             | DCS1800 @ DRX = 2                    | 3.288 | mA   |
|             | DCS1800 @ DRX = 5                    | 2.272 | mA   |
|             | DCS1800 @ DRX = 5 (USB Suspend)      | -     | mA   |
|             | DCS1800 @ DRX = 9                    | 1.988 | mA   |
| Sleep state | WCDMA @ DRX = 0.64 s                 | 2.89  | mA   |
|             | WCDMA @ DRX = 0.64 s (USB Suspend)   | -     | mA   |
|             | WCDMA @ DRX = 1.28 s                 | 2.139 | mA   |
|             | WCDMA @ DRX = 2.56 s                 | 1.709 | mA   |
|             | WCDMA @ DRX = 5.12 s                 | 1.559 | mA   |
|             | LTE-FDD @ DRX = 0.32 s               | 4.146 | mA   |
|             | LTE-FDD @ DRX = 0.64 s               | 2.711 | mA   |
|             | LTE-FDD @ DRX = 0.64 s (USB Suspend) | -     | mA   |
|             | LTE-FDD @ DRX = 1.28 s               | 2.013 | mA   |
|             | LTE-FDD @ DRX = 2.56 s               | 1.681 | mA   |
|             | LTE-TDD @ DRX = 0.32 s               | 4.17  | mA   |

|            |                                        |       |    |
|------------|----------------------------------------|-------|----|
| Idle state | LTE-TDD @ DRX = 0.64 s                 | 2.722 | mA |
|            | LTE-TDD @ DRX = 0.64 s (USB Suspend)   | -     | mA |
|            | LTE-TDD @ DRX = 1.28 s                 | 2.017 | mA |
|            | LTE-TDD @ DRX = 2.56 s                 | 1.722 | mA |
|            | 5G NR FDD @ DRX = 0.32 s               | 4.735 | mA |
|            | 5G NR FDD @ DRX = 0.64 s               | 3.068 | mA |
|            | 5G NR FDD @ DRX = 0.64 s (USB Suspend) | -     | mA |
|            | 5G NR FDD @ DRX = 1.28 s               | 2.249 | mA |
|            | 5G NR FDD @ DRX = 2.56 s               | 1.725 | mA |
|            | 5G NR TDD @ DRX = 0.32 s               | 4.597 | mA |
|            | 5G NR TDD @ DRX = 0.64 s               | 2.928 | mA |
|            | 5G NR TDD @ DRX = 0.64 s (USB Suspend) | -     | mA |
|            | 5G NR TDD @ DRX = 1.28 s               | 2.121 | mA |
|            | 5G NR TDD @ DRX = 2.56 s               | 1.695 | mA |
|            | EGSM900 CH62 @ DRX = 2                 | 17.24 | mA |
|            | EGSM900 CH62 @ DRX = 2 (USB Active)    | 41.39 | mA |
|            | WCDMA @ DRX = 0.64 s                   | 17.51 | mA |
|            | WCDMA @ DRX = 0.64 s (USB Active)      | 41.14 | mA |
|            | LTE-FDD @ DRX = 0.64 s                 | 17.43 | mA |
|            | LTE-FDD @ DRX = 0.64 s (USB Active)    | 41.54 | mA |
|            | LTE-TDD @ DRX = 0.64 s                 | 17.49 | mA |
|            | LTE-TDD @ DRX = 0.64 s (USB Active)    | 41.97 | mA |
|            | 5G NR FDD @ DRX = 0.64 s               | 18.05 | mA |
|            | 5G NR FDD @ DRX = 0.64 s (USB Active)  | 42.22 | mA |
|            | 5G NR TDD @ DRX = 0.64 s               | 17.95 | mA |
|            | 5G NR TDD @ DRX = 0.64 s (USB Active)  | 41.65 | mA |

|                       |                        |        |    |
|-----------------------|------------------------|--------|----|
| GSM max. power        | GSM850 CH188 PCL = 5   | 395    | mA |
|                       | EGSM900 CH62 PCL = 5   | 427    | mA |
|                       | DCS1800 CH698 PCL = 0  | 267    | mA |
|                       | PCS1900 CH661 PCL = 0  | 284    | mA |
| GPRS max. throughput  | GSM850 CH188 4DL/1UL   | 379    | mA |
|                       | EGSM900 CH62 4DL/1UL   | 416    | mA |
|                       | DCS1800 CH698 4DL/1UL  | 267    | mA |
|                       | PCS1900 CH661 4DL/1UL  | 262    | mA |
| EDGE max. throughput  | GSM850 CH188 4DL/1UL   | 226    | mA |
|                       | EGSM900 CH62 4DL/1UL   | 236    | mA |
|                       | DCS1800 CH698 4DL/1UL  | 203    | mA |
|                       | PCS1900 CH661 4DL/1UL  | 206    | mA |
| WCDMA max. power      | WCDMA B1 CH10700       | 571    | mA |
|                       | WCDMA B2 CH9800        | 518.37 | mA |
|                       | WCDMA B4 CH1638        | 507.72 | mA |
|                       | WCDMA B5 CH4408        | 558.95 | mA |
|                       | WCDMA B8 CH3012        | 640.09 | mA |
|                       | WCDMA B19 CH412        | 574.38 | mA |
| WCDMA max. throughput | WCDMA B1 HSDPA CH10700 | 552    | mA |
|                       | WCDMA B1 HSUPA CH10700 | 556    | mA |
|                       | WCDMA B2 HSDPA CH9800  | 504.14 | mA |
|                       | WCDMA B2 HSUPA CH9800  | 504.59 | mA |
|                       | WCDMA B4 HSDPA CH1638  | 492.36 | mA |
|                       | WCDMA B4 HSUPA CH1638  | 493.31 | mA |
|                       | WCDMA B5 HSDPA CH4408  | 551.23 | mA |
|                       | WCDMA B5 HSUPA CH4408  | 553.99 | mA |

|                |                       |        |    |
|----------------|-----------------------|--------|----|
| LTE max. power | WCDMA B8 HSDPA CH3012 | 616.73 | mA |
|                | WCDMA B8 HSUPA CH3012 | 621.98 | mA |
|                | WCDMA B19 HSDPA CH738 | 559.87 | mA |
|                | WCDMA B19 HSUPA CH738 | 562.78 | mA |
|                | LTE-FDD B1 CH300      | 649.54 | mA |
|                | LTE-FDD B2 CH900      | 620.75 | mA |
|                | LTE-FDD B3 CH1575     | 643.13 | mA |
|                | LTE-FDD B4 CH2175     | 671.35 | mA |
|                | LTE-FDD B5 CH2525     | 532.38 | mA |
|                | LTE-FDD B7 CH3100     | 645.8  | mA |
|                | LTE-FDD B8 CH3625     | 664.05 | mA |
|                | LTE-FDD B12 CH5095    | 569.14 | mA |
|                | LTE-FDD B13 CH5230    | 676.77 | mA |
|                | LTE-FDD B14 CH5330    | 556.49 | mA |
|                | LTE-FDD B17 CH5790    | 548.35 | mA |
|                | LTE-FDD B18 CH5920    | 585.97 | mA |
|                | LTE-FDD B19 CH6075    | 546.94 | mA |
|                | LTE-FDD B20 CH6300    | 556.39 | mA |
|                | LTE-FDD B25 CH8365    | 625.11 | mA |
|                | LTE-FDD B26 CH8665    | 563.68 | mA |
|                | LTE-FDD B28 CH9435    | 602.82 | mA |
|                | LTE-TDD B34 CH36275   | 298.57 | mA |
|                | LTE-TDD B38 CH38000   | 362.65 | mA |
|                | LTE-TDD B39 CH38450   | 302.65 | mA |
|                | LTE-TDD B40 CH39150   | 399.29 | mA |
|                | LTE-TDD B41 CH40620   | 487.35 | mA |

|                     |                     |        |    |
|---------------------|---------------------|--------|----|
| LTE max. throughput | LTE-TDD B42 CH42590 | 399.42 | mA |
|                     | LTE-TDD B43 CH44590 | 336.02 | mA |
|                     | LTE-TDD B48 CH55990 | 334.12 | mA |
|                     | LTE-FDD B66 CH66886 | 685.02 | mA |
|                     | LTE-FDD B71 CH68761 | 758.6  | mA |
|                     | LTE-FDD B1 CH300    | 421.49 | mA |
|                     | LTE-FDD B2 CH900    | 437.18 | mA |
|                     | LTE-FDD B3 CH1575   | 425.91 | mA |
|                     | LTE-FDD B4 CH2175   | 432.57 | mA |
|                     | LTE-FDD B5 CH2525   | 406.4  | mA |
|                     | LTE-FDD B7 CH3100   | 404.75 | mA |
|                     | LTE-FDD B8 CH3625   | 492.11 | mA |
|                     | LTE-FDD B12 CH5095  | 424.57 | mA |
|                     | LTE-FDD B13 CH5230  | 439.53 | mA |
|                     | LTE-FDD B14 CH5330  | 424.45 | mA |
|                     | LTE-FDD B17 CH5790  | 424.26 | mA |
|                     | LTE-FDD B18 CH5920  | 420.65 | mA |
|                     | LTE-FDD B19 CH6075  | 417.52 | mA |
|                     | LTE-FDD B20 CH6300  | 414.62 | mA |
|                     | LTE-FDD B25 CH8365  | 422.52 | mA |
|                     | LTE-FDD B26 CH8665  | 431.26 | mA |
|                     | LTE-FDD B28 CH9435  | 462.17 | mA |
|                     | LTE-TDD B34 CH36275 | 265.15 | mA |
|                     | LTE-TDD B38 CH38000 | 301.31 | mA |
|                     | LTE-TDD B39 CH38450 | 266.29 | mA |
|                     | LTE-TDD B40 CH39150 | 273.77 | mA |

|                     |                     |        |    |
|---------------------|---------------------|--------|----|
| 5G NR SA max. power | LTE-TDD B41 CH40620 | 297.81 | mA |
|                     | LTE-TDD B42 CH42590 | 368.73 | mA |
|                     | LTE-TDD B43 CH44590 | 285.52 | mA |
|                     | LTE-TDD B48 CH55990 | 284.61 | mA |
|                     | LTE-FDD B66 CH66886 | 496.41 | mA |
|                     | LTE-FDD B71 CH68761 | 528.11 | mA |
|                     | n1A CH428000        | 752.17 | mA |
|                     | n2A CH392000        | 682.72 | mA |
|                     | n3A CH368500        | 683.51 | mA |
|                     | n5A CH176300        | 554.19 | mA |
|                     | n7A CH531000        | 743.04 | mA |
|                     | n8A CH188500        | 631.78 | mA |
|                     | n12A CH147500       | 521.1  | mA |
|                     | n14A CH152600       | 563.45 | mA |
|                     | n20A CH161200       | 510.21 | mA |
|                     | n25A CH392500       | 722.58 | mA |
|                     | n26A CH175300       | 491.44 | mA |
|                     | n28A CH156100       | 587.71 | mA |
|                     | n38A CH519000       | 235.98 | mA |
|                     | n40A CH470000       | 236.53 | mA |
|                     | n41A CH518598       | 324.13 | mA |
|                     | n48A CH641666       | 223.39 | mA |
|                     | n66A CH429000       | 681.42 | mA |
|                     | n70A CH400500       | 785.13 | mA |
|                     | n71A CH126900       | 729.86 | mA |
|                     | n77A CH650000       | 310.48 | mA |

|                          |                  |        |    |
|--------------------------|------------------|--------|----|
|                          | n78A CH636666    | 346.13 | mA |
|                          | n79A CH713334    | 318.09 | mA |
| 5G NR SA max. throughput | n1A CH428000     | 458    | mA |
|                          | n2A CH392000     | 421    | mA |
|                          | n3A CH368500     | 437    | mA |
|                          | n5A CH176300     | 420    | mA |
|                          | n7A CH531000     | 461    | mA |
|                          | n8A CH188500     | 467    | mA |
|                          | n12A CH147500    | 413    | mA |
|                          | n14A CH152600    | 397    | mA |
|                          | n20A CH161200    | 420    | mA |
|                          | n25A CH392500    | 468    | mA |
|                          | n26A CH175300    | 395    | mA |
|                          | n28A CH156100    | 402    | mA |
|                          | n38A CH519000    | 208    | mA |
|                          | n40A CH470000    | 273    | mA |
|                          | n41A CH518598    | 197    | mA |
|                          | n48A CH641666    | 180    | mA |
|                          | n66A CH429000    | 435    | mA |
|                          | n70A CH400500    | 460    | mA |
|                          | n71A CH126900    | 465    | mA |
|                          | n77A CH650000    | 260    | mA |
|                          | n78A CH636666    | 324    | mA |
|                          | n79A CH713522    | 289    | mA |
| 5G NR NSA max. power     | 1A_n71A CH126900 | 875.39 | mA |
|                          | 1A_n77A CH650000 | 773.93 | mA |

|                           |                   |        |    |
|---------------------------|-------------------|--------|----|
| 5G NR NSA max. throughput | 41A_n77A CH650000 | 419.42 | mA |
|                           | 7A_n20A CH161200  | 726.94 | mA |
|                           | 3A_n79A CH713334  | 770.3  | mA |
|                           | 40A_n79A CH713334 | 338.77 | mA |
|                           | 48A_n5A CH176300  | 524.09 | mA |
|                           | 48A_n66A CH429000 | 625.62 | mA |
|                           | 5A_n40A CH470000  | 541.18 | mA |
|                           | 12A_n7A CH531000  | 876.88 | mA |
|                           | 28A_n2A CH392000  | 875.56 | mA |
|                           | 28A_n79A CH713334 | 622.29 | mA |
|                           | 71A_n77A CH650000 | 643.65 | mA |
|                           | 71A_n41A CH518598 | 638.37 | mA |
|                           | 1A_n71A CH126900  | 890    | mA |
|                           | 1A_n77A CH650000  | 744    | mA |
|                           | 41A_n77A CH650000 | 369    | mA |
|                           | 7A_n20A CH161200  | 785    | mA |
|                           | 3A_n79A CH713334  | 694    | mA |
|                           | 40A_n79A CH713334 | 426    | mA |
|                           | 48A_n5A CH176300  | 553    | mA |
|                           | 48A_n66A CH429000 | 671    | mA |
|                           | 5A_n40A CH470000  | 592    | mA |
|                           | 12A_n7A CH531000  | 891    | mA |
|                           | 28A_n2A CH392000  | 809    | mA |
|                           | 28A_n79A CH713334 | 699    | mA |
|                           | 71A_n77A CH650000 | 743    | mA |
|                           | 71A_n41A CH518598 | 693    | mA |

#### NOTE

1. The above power consumption data are all tested with the GNSS OFF by default.
2. The data of maximum throughput are tested at the condition of maximum power.
3. The above power consumption data are tested under 50  $\Omega$  impedance.
4. The above power consumption data is the typical value for your reference only. Actual values may vary among different modules due to differences in internal components, software versions and test ambient temperatures. For more details, please contact Wireless Mobility Technical Support.

## 6.4. Digital I/O Characteristics

**Table 46: 1.8 V I/O Requirements**

| Parameter       | Description               | Min. | Max. | Unit |
|-----------------|---------------------------|------|------|------|
| V <sub>IH</sub> | High-level input voltage  | 1.26 | 2.1  | V    |
| V <sub>IL</sub> | Low-level input voltage   | -0.3 | 0.54 | V    |
| V <sub>OH</sub> | High-level output voltage | 1.35 | 1.8  | V    |
| V <sub>OL</sub> | Low-level output voltage  | 0    | 0.45 | V    |

**Table 47: (U)SIM High-voltage/Low-voltage I/O Requirements**

| Parameter       | Description               | Min.                          | Max.                          | Unit |
|-----------------|---------------------------|-------------------------------|-------------------------------|------|
| V <sub>IH</sub> | High-level input voltage  | $0.7 \times \text{USIM\_VDD}$ | $\text{USIM\_VDD} + 0.3$      | V    |
| V <sub>IL</sub> | Low-level input voltage   | -0.3                          | $0.2 \times \text{USIM\_VDD}$ | V    |
| V <sub>OH</sub> | High-level output voltage | $0.8 \times \text{USIM\_VDD}$ | -                             | V    |
| V <sub>OL</sub> | Low-level output voltage  | -                             | 0.4                           | V    |

## 6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

The following table shows the module electrostatic discharge characteristics.

**Table 48: Electrostatic Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)**

| Tested Interfaces  | Contact Discharge | Air Discharge | Unit |
|--------------------|-------------------|---------------|------|
| VBAT, GND          | ±6                | ±10           | kV   |
| Antenna Interfaces | ±6                | ±10           | kV   |
| Other Interfaces   | ±0.5              | ±1            | kV   |

## 6.6. Operating and Storage Temperatures

**Table 49: Operating and Storage Temperatures**

| Parameter                                        | Min. | Typ. | Max. | Unit |
|--------------------------------------------------|------|------|------|------|
| Normal Operating Temperature Range <sup>17</sup> | -40  | +25  | +85  | °C   |
| eCall Operating Temperature Range <sup>18</sup>  | -40  | -    | +95  | °C   |
| Storage Temperature Range                        | -40  | -    | +95  | °C   |

<sup>17</sup> Within the operating temperature range, the module meets 3GPP specifications.

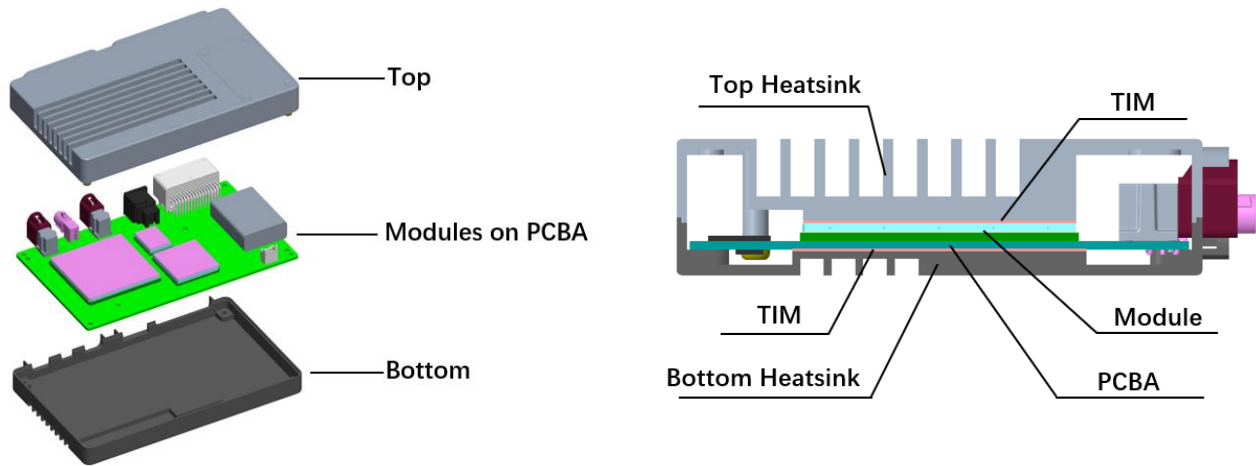
<sup>18</sup> Within eCall temperature range, the eCall function must be functional until the module is broken. When the ambient temperature is between 75 °C and 95 °C and the module temperature has reached the threshold value, the module will trigger protective measures (such as reduce power, decrease throughput and unregister the device) to ensure the full function of eCall.

## 6.7. Thermal Dissipation

The module exhibits the best performance when all internal chips are working within their designated operating temperature ranges. However, if any chip reaches or exceeds its maximum temperature, the module may still work but its performance and functionalities (such as RF output power and data rate) will be compromised. Therefore, the thermal design should be maximally optimized to ensure that all internal chips consistently remain within their recommended operating temperature ranges.

The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on the PCBA main board, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Expose the copper on the backside of the PCB where the module is mounted.
- Follow the principles below when designing the heatsink:
  - 1) It is recommended to integrate the heatsink with the outer shell of the device according to the module's application scenario. This allows for rapid transfer of the heat generated by the module to the outer shell, thus enhancing heat dissipation efficiency and eliminating the need for fixing the heatsink.
  - 2) The entire shell of the device or the shell of the area where the module is located must be made of materials with excellent heat dissipation properties. It is recommended to use die-cast aluminum with higher thermal conductivity.
  - 3) Based on the heat dissipation direction of the module, you can choose any of the following optional heatsink installation positions:
    - a) The top surface of the module shielding cover;
    - b) The bottom surface of the PCBA under the module;
    - c) Both the top surface of the module shielding cover and the bottom surface of the PCBA under the module.If the situation allows, option c) is recommended; if the heatsink is located only on one side, option a) is recommended.
  - 4) The heatsink must meet the following requirements:
    - a) The base plate area of the heatsink should be larger than the module area for full coverage;
    - b) Choose a heatsink with adequate fins to ensure effective heat dissipation. The fins should be located within the area where the module is mounted.
  - 5) Since the heatsink is in contact with either the top surface of the shielding cover or the bottom surface of the PCBA under the module through the thermal interface material (TIM), it is necessary to choose a TIM with high thermal conductivity, good flexibility, and good wettability.
  - 6) Fasten the shell (heatsink) with screws around the device to prevent the heatsink from falling off during the drop tests, shock and vibration tests, or transportation.
- Implement other auxiliary cooling methods, such as air cooling or liquid cooling.



**Figure 47: Heatsink Design Example**

**NOTE**

1. When the maximum temperature of the baseband chip reaches or exceeds specified temperature threshold, the module will adopt different thermal management policies by default (such as speed reduction, power reduction and entering Limited Service Mode) to protect the module. When the maximum temperature of the baseband chip exceeds 120 °C, the module will enter Limited Service Mode (such as eCall). Therefore, the thermal dissipation design should be added as much as possible to maximize the module performance. For details about software thermal management, please contact Wireless Mobility Technical Support.
2. For details about the hardware heat dissipation design, please contact Wireless Mobility Technical Support.

# 7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are  $\pm 0.2$  mm unless otherwise specified.

## 7.1. Mechanical Dimensions

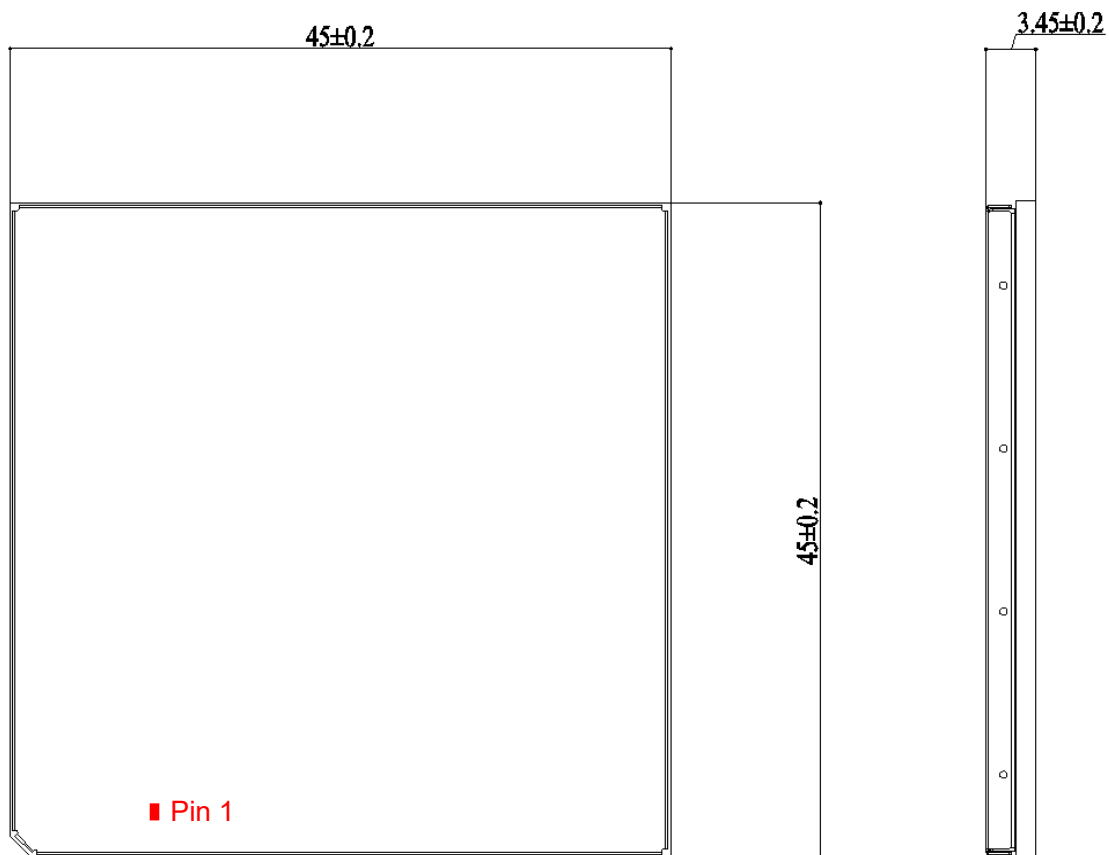


Figure 48: Module Top and Side Dimensions



**Figure 49: Module Bottom Dimensions (Unit: mm)**

## NOTE

1. The module's coplanarity standard:  $\leq 0.13$  mm.
2. Please note that the positions shown by the arrows in the above figure are the mark points of the module, and no additional design is required.



### 7.3. Top and Bottom Views

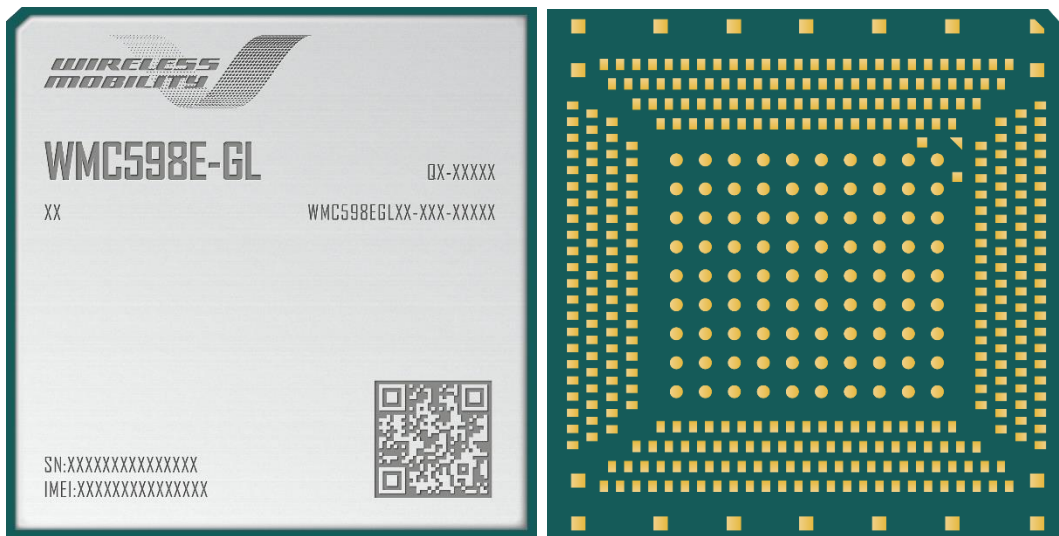


Figure 51: Top and Bottom Views of the Module

#### NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, refer to the module received from Wireless Mobility.

# 8 Storage, Manufacturing and Packaging

## 8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be  $23 \pm 5$  °C and the relative humidity should be 35–60 %.
2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.
3. The floor life of the module is 168 hours<sup>19</sup> in a plant where the temperature is  $23 \pm 5$  °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).
4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:
  - The module is not stored in Recommended Storage Condition;
  - Violation of the third requirement above occurs;
  - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
5. If needed, the pre-baking should follow the requirements below:
  - The module should be baked for 24 hours at  $120 \pm 5$  °C;
  - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

---

<sup>19</sup> This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

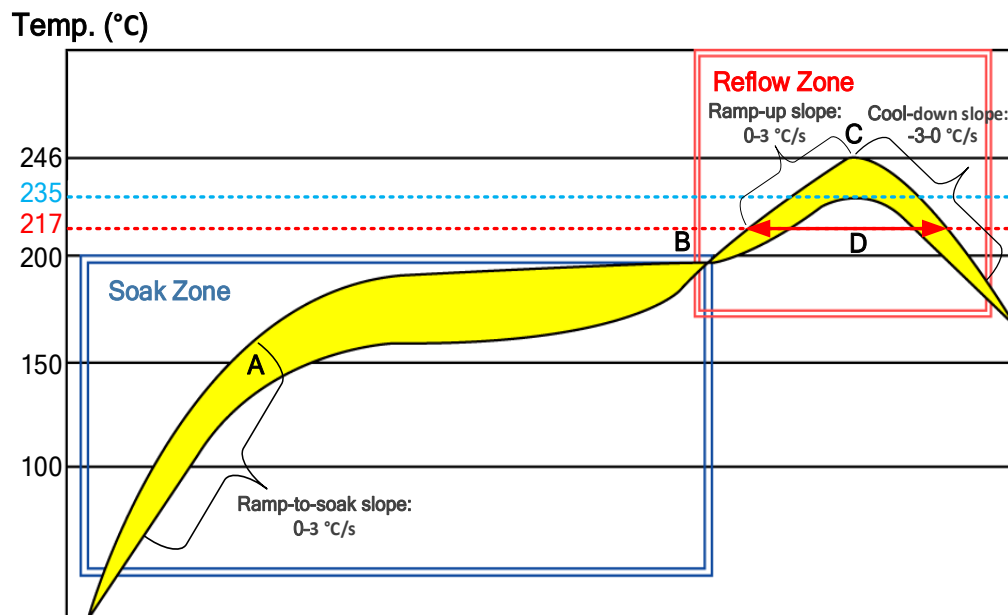
**NOTE**

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

## 8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, please contact Wireless Mobility Technical Support.

The peak reflow temperature should be 235–246 °C, with 246 °C as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.



**Figure 52: Recommended Reflow Soldering Thermal Profile**

**Table 50: Recommended Thermal Profile Parameters**

| Factor                                         | Recommended Value                 |
|------------------------------------------------|-----------------------------------|
| <b>Soak Zone</b>                               |                                   |
| Ramp-to-soak slope                             | 0–3 °C/s                          |
| Soak time (between A and B: 150 °C and 200 °C) | 70–120 s                          |
| <b>Reflow Zone</b>                             |                                   |
| Ramp-up slope                                  | 0–3 °C/s                          |
| Reflow time (D: over 217°C)                    | 40–70 s                           |
| Max temperature                                | 235–246 °C                        |
| Cool-down slope                                | -3–0 °C/s (refer to NOTE 1 below) |
| <b>Reflow Cycle</b>                            |                                   |
| Max reflow cycle                               | 1                                 |

**NOTE**

1. For large-form-factor modules (that is, minimum side length  $\geq 30$  mm) with two-piece shielding covers, use a cool-down slope of -1~0 °C/s to reduce the thermal stress, preventing cover lifting. Due to the large-size factors of such modules, an excessive temperature change may cause excessive thermal deformation of the metal shielding frame and cover. Therefore, reduce the ramp-up and cool-down slopes in the liquid phase of the solder paste to avoid excessive temperature change. If possible, choose a reflow oven with more than 10 temperature zones during production so that there are more temperature zones to set up to meet the optimal temperature curve.
2. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
6. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
7. Due to the complexity of the SMT process, please contact Wireless Mobility Technical Supports in

advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering).

### 8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

#### 8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

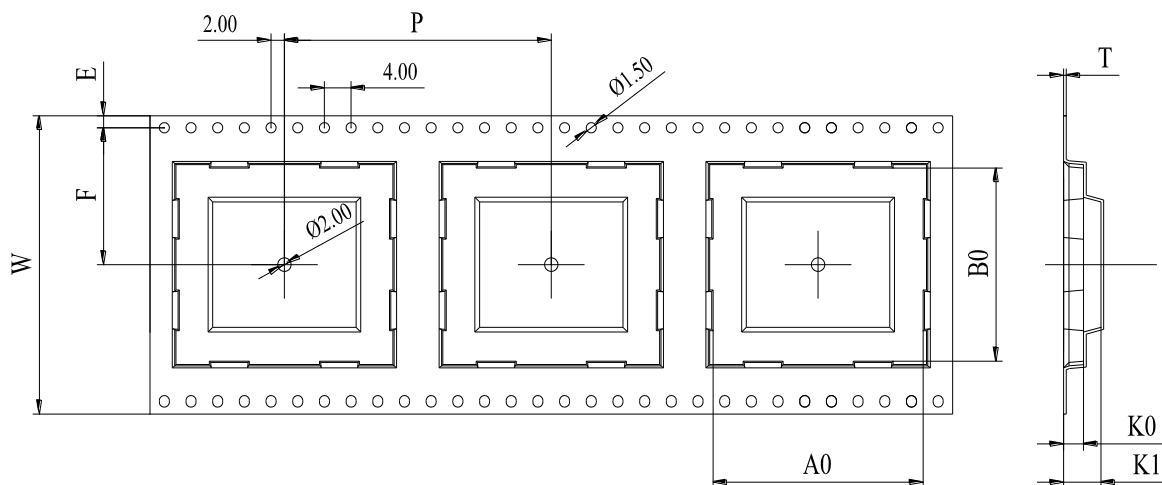


Figure 53: Carrier Tape Dimension Drawing (Unit: mm)

Table 51: Carrier Tape Dimension Table (Unit: mm)

| W  | P  | T   | A0   | B0   | K0  | K1 | F    | E    |
|----|----|-----|------|------|-----|----|------|------|
| 72 | 64 | 0.4 | 45.8 | 45.8 | 4.7 | 6  | 34.2 | 1.75 |

#### 8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

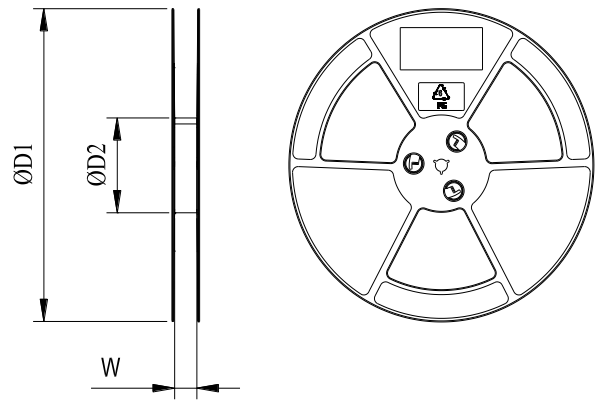


Figure 54: Plastic Reel Dimension Drawing

Table 52: Plastic Reel Dimension Table (Unit: mm)

| øD1 | øD2 | W    |
|-----|-----|------|
| 380 | 180 | 72.5 |

### 8.3.3. Mounting Direction

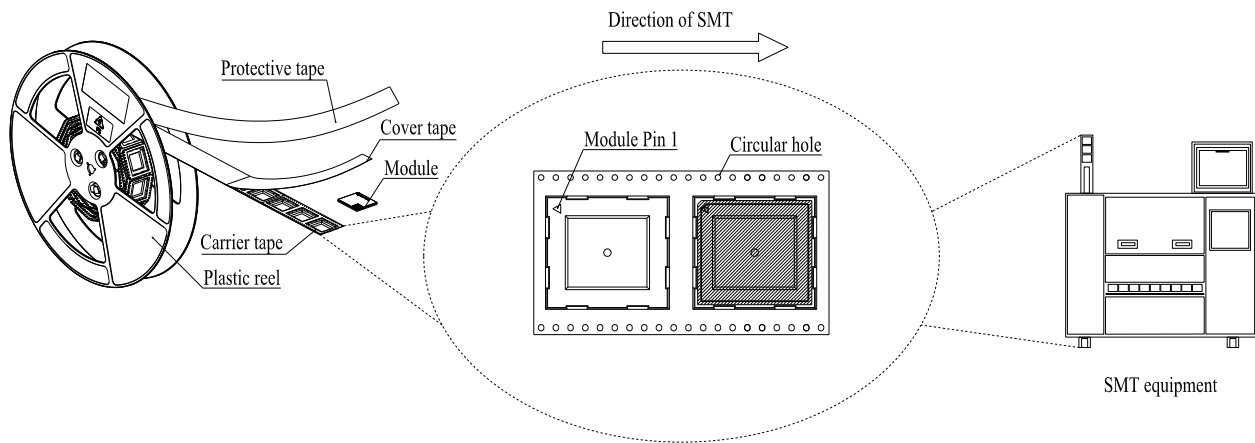
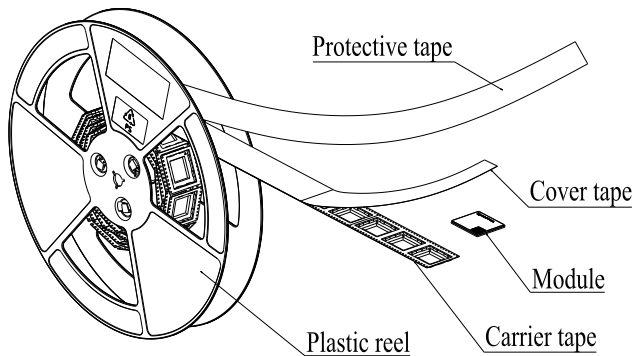


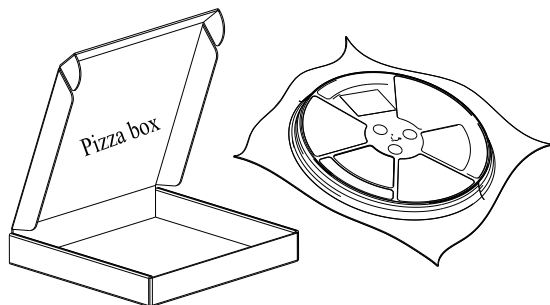
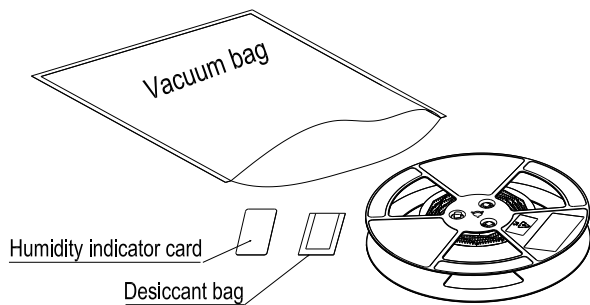
Figure 55: Mounting Direction

### 8.3.4. Packaging Process



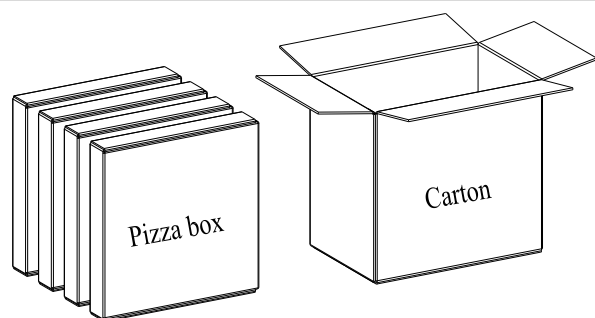
Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 150 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.



Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 600 modules.



Pizza box Size: 405\*390\*83mm

Carton Size: 425\*358\*410mm

**Figure 56: Packaging Process**

# 9 Appendix Reference

**Table 53: Terms and Abbreviations**

| Abbreviation | Description                                |
|--------------|--------------------------------------------|
| 3GPP         | 3rd Generation Partnership Project         |
| 5G NR        | 5G New Radio                               |
| AC           | Alternating Current                        |
| ADC          | Analog-to-Digital Converter                |
| AMR          | Adaptive Multi-rate                        |
| AP           | Application Processor                      |
| API          | Application Program Interface              |
| AVTP         | Audio/Video Transport Protocol             |
| bps          | Bits Per Second                            |
| BPSK         | Binary Phase Shift Keying                  |
| BT           | Bluetooth                                  |
| CS           | Coding Scheme                              |
| CTS          | Clear to Send                              |
| DCE          | Data Communications Equipment              |
| DC-HSDPA     | Dual Carrier High Speed Packet Access Plus |
| DCS          | Data Communications Equipment              |
| DFOTA        | Delta Firmware Upgrade Over the Air        |
| DL           | Downlink                                   |
| DR           | Dead Reckoning                             |

|         |                                                       |
|---------|-------------------------------------------------------|
| DRX     | Discontinuous Reception                               |
| DSSA    | Dual SIM Single Active                                |
| DTE     | Data Terminal Equipment                               |
| DTR     | Data Terminal Ready                                   |
| EAVB    | Ethernet Audio Video Bridging                         |
| EDGE    | Enhanced Data Rates for GSM Evolution                 |
| EFR     | Enhanced Full Rate                                    |
| EGSM    | Extended GSM900 Band (including standard GSM900 band) |
| EMI     | Electromagnetic Interference                          |
| eMMC    | Embedded Multimedia Card                              |
| EN-DC   | E-UTRA-NR Dual Connectivity                           |
| EP      | PCIe Endpoint                                         |
| ESD     | Electrostatic Discharge                               |
| EVB     | Evaluation Board                                      |
| EOS     | Electrical Over Stress                                |
| FDD     | Frequency Division Duplex                             |
| FEM     | Front-End Module                                      |
| FR      | Full Rate                                             |
| FQTSS   | Forwarding and Queuing of Time Sensitive Streams      |
| Galileo | Galileo Satellite Navigation System                   |
| GLONASS | Russian Global Navigation Satellite System            |
| GMSK    | Gaussian Minimum Shift Keying                         |
| GNSS    | Global Navigation Satellite System                    |
| GPIO    | General-purpose Input/Output                          |
| GPRS    | General Packet Radio Service                          |

|                  |                                         |
|------------------|-----------------------------------------|
| GPS              | Global Positioning System               |
| GSM              | Global System for Mobile Communications |
| gPTP             | General Precise Time Protocol           |
| HPUE             | High Power User Equipment               |
| HR               | Half Rate                               |
| HSDPA            | High Speed Down Link Packet Access      |
| HSPA             | High Speed Packet Access                |
| HSUPA            | High Speed Uplink Packet Access         |
| I <sub>max</sub> | Maximum Load Current                    |
| IMU              | Inertial Measurement Unit               |
| I/O              | Input/Output                            |
| ITS              | Intelligent Transportation System       |
| I <sub>nom</sub> | Normal Current                          |
| LDO              | Low-dropout Regulator                   |
| LGA              | Land Grid Array                         |
| LNA              | Low Noise Amplifier                     |
| LPM              | Low Power Mode                          |
| LTE              | Long Term Evolution                     |
| MAC              | Medium Access Control                   |
| MCS              | Modulation and Coding Scheme            |
| MDIO             | Management Data Input/Output            |
| ME               | Mobile Equipment                        |
| MIMO             | Multiple Input Multiple Output          |
| MHB              | Middle/High Band                        |
| MO               | Mobile Originated                       |

|       |                                                                        |
|-------|------------------------------------------------------------------------|
| MLCC  | Multi-layer Ceramic Chip Capacitor                                     |
| MT    | Mobile Terminated                                                      |
| NMEA  | NMEA (National Marine Electronics Association) 0183 Interface Standard |
| NSA   | Non-Standalone                                                         |
| PA    | Power Amplifier                                                        |
| PCB   | Printed Circuit Board                                                  |
| PCIe  | Peripheral Component Interconnect Express                              |
| PCM   | Pulse Code Modulation                                                  |
| PDU   | Protocol Data Unit                                                     |
| PMIC  | Power Management IC                                                    |
| PPP   | Point-to-Point Protocol                                                |
| PSK   | Phase Shift Keying                                                     |
| QAM   | Quadrature Amplitude Modulation                                        |
| QPSK  | Quadrature Phase Shift Keying                                          |
| QZSS  | Quasi-Zenith Satellite System                                          |
| RC    | PCIe Root Complex                                                      |
| RF    | Radio Frequency                                                        |
| RGMII | Reduced Gigabit Media Independent Interface                            |
| RSU   | Roadside Units                                                         |
| RTC   | Real-Time Clock                                                        |
| RTS   | Ready To Send/Request to Send                                          |
| RoHS  | Restriction of Hazardous Substances                                    |
| Rx    | Receive                                                                |
| SA    | Standalone                                                             |
| SCS   | Sub-Carrier Space                                                      |

|                    |                                               |
|--------------------|-----------------------------------------------|
| SDIO               | Secure Digital Input/Output                   |
| SIM                | Subscriber Identity Module                    |
| SMD                | Surface Mount Device                          |
| SMS                | Short Message Service                         |
| SPI                | Serial Peripheral Interface                   |
| TCU                | Telematics Control Units                      |
| TDD                | Time Division Duplexing                       |
| Tx                 | Transmitting Direction                        |
| XFEM               | Extended Finite Element Method                |
| t(ch)              | Clock high                                    |
| t(cl)              | Clock low                                     |
| t(mov)             | Master Output Valid                           |
| t(mis)             | Master Input Setup                            |
| t(mih)             | Master Input Hold                             |
| UART               | Universal Asynchronous Receiver & Transmitter |
| UL                 | Uplink                                        |
| UMTS               | Universal Mobile Telecommunications System    |
| URC                | Unsolicited Result Code                       |
| USB                | Universal Serial Bus                          |
| (U)SIM             | (Universal) Subscriber Identity Module        |
| V <sub>max</sub>   | Maximum Voltage                               |
| V <sub>nom</sub>   | Nominal Voltage                               |
| V <sub>min</sub>   | Minimum Voltage                               |
| V <sub>IHmax</sub> | Maximum High-level Input Voltage              |
| V <sub>IHmin</sub> | Minimum High-level Input Voltage              |

|             |                                        |
|-------------|----------------------------------------|
| $V_{ILmax}$ | Maximum Low-level Input Voltage        |
| $V_{ILmin}$ | Minimum Low-level Input Voltage        |
| $V_{Imax}$  | Absolute Maximum Input Voltage         |
| $V_{Imin}$  | Absolute Minimum Input Voltage         |
| $V_{OHmax}$ | Maximum High-level Output Voltage      |
| $V_{OHmin}$ | Minimum High-level Output Voltage      |
| $V_{OLmax}$ | Maximum Low-level Output Voltage       |
| $V_{OLmin}$ | Minimum Low-level Output Voltage       |
| VSWR        | Voltage Standing Wave Ratio            |
| WCDMA       | Wideband Code Division Multiple Access |
| Wi-Fi       | Wireless Fidelity                      |
| WLAN        | Wireless Local Area Network            |