

User Manual (LGSRFT3 / LGSRFR3W)

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User Manual

SoC Center / CTO
LG Electronics, Inc.

Contents

1 Introduction	3
1.1 Overview and Feature of 'LG2832 Board'	4
1.2 Feature of 'LG2851 Module'	7
1.3 Application Example	8
2. Electrical Specifications	9
2.1 Absolute Maximum Rating for 'LG2851 Module'	10
2.2 Operating Conditions for 'LG2832 IC'	11
2.3 Operating Conditions for 'LG2851 Module'	12
3. Pin Descriptions	13
3.1 Pin Descriptions for 'LG2832 IC'	14
3.2 Pin Descriptions for 'LG2851 Module'	24
4. RF Specifications	25
4.1 Receiver and Transmitter for 'LG2832 Board'	26
4.2 Receiver and Transmitter for 'LG2851 Module'	27
5. Regulatory Statement	29
5.1 FCC	30
5.2 ISSED	31
5.3 CE	32
5.4 UKCA	32

1 Introduction

This document describes functionality and electrical specification of LGSRT3 and LGSRT3W. LGSRT3 together with LGSRT3W can transmit and receive 9.2 Gbps data through 60 GHz ISM band wirelessly. With this ultra-high throughput, it can implement 4K wireless video transfer between main SoC and display panel. It is possible to remove every wire attached to TV display and to make customer use living space more freely.

1.1 Overview and Feature of 'LG2832 Board'

LG wireless AV transfer solution (LGSRT3 + LGSFR3W) consists of 'LG2832 board' and 'LG2851 module'. It implements wireless data transaction between main SoC and T-Con instead of Vx1 wired connection. LG2832 is responsible for video/audio data reception from main SoC and regeneration of received data through wireless channel to T-Con. In case of LG2851, it receives data through 10 GHz wired connection from LG2832 and transmits data through 60GHz wireless channel in box side. In case of display panel, it will do the reverse function of box side.

The main functions of LG2832 are audio/video data reception from main SoC and regeneration to T-Con, video data compression/decompression with visually lossless quality, making-up wireless transaction protocol and analog-to/from digital conversion to communicate with LG2851.

It supports 4K60p, 4K120p up to 4K165p video frame through Vx1 interface. It also supports variable refresh rate of video frame. It supports 16-lane Vx1 interface for 4K video transaction. In case of audio, it supports 7.1 channels up to 96 kHz sampling data.

In a view point of data stream, main SoC located at box side processes audio/video data from external input and provide it to LG2832. After receiving video data, LG2832 compresses it with ratio from 7:1 to 30:1. Up to 10:1 compression rate, it can achieve visually lossless image and provide better quality of video to customer. The compressed data is handled by wireless protocol IP, packetized and formatted for wireless transmission through LG2851. To communicate with LG2851, LG2832 has analog interface which can convert digital signal to 10 GHz analog signal.

At the other end, i.e, display side, LG2851 receives 60 GHz radio signal and converts to 10 GHz analog signal to LG2832. After receiving analog signal from LG2851, LG2832 do reverse functions as described above.

For unpredicted radio condition during transmission, the modem protocol IP measures radio quality and control MCS for each packet. In addition, LG2832 will control compression rate of video data for more reliable wireless communication.

'LG2832 board' provides the following key features:

• CPU Subsystem

- Processor (CPU)
 - CPU Core: ARM Cortex-R5
 - Core Clock Frequency: 480 MHz
 - Cache: I-cache: 32 KB, D-cache: 32 KB, I-TCM: 32 KB, D-TCM: 32 KB
 - SRAM : 1088 KB
- Peripherals
 - USB2.0
 - Memory Interface: Quad-SPI (up to 60 MHz)
 - GPIO: Dedicated 10 ports, Shared 49 ports
 - UART: Dedicated 1 ports (up to 921.6 Kbps)
 - I2C: 5 Master/Slave 5, 1 Slave
 - SPI: 1 Master/Slave

- System DMA
- Security Peripheral
 - Security Core IP: Supported (for USB camera content protection)
- USB Camera Data Transfer
 - Resolution Support: up to 4K30p, 200 Mbps
 - Feature: Encryption for privacy protection
- **Display**
 - Display Resolution
 - Supported Resolutions: 4K, 2K, QHD (2560x1440), WQHD (3440x1440)
 - Bit Depth
 - Supported Bit Depths: RGB 39-bit, 36-bit, 33-bit, 30-bit
 - Color Space
 - Color Space: RGB444
 - Frame Rate
 - 4K Frame Rates: 40 ~ 165 Hz
 - Input / Output Interfaces
 - Video Interface: 16 lanes (Vx1)
 - Customized packet data interface via Vx1 control channels
 - 8K Functionality
 - Not supported
 - Local Dimming
 - SPI data transmission and generation logic embedded
 - Backlight functionality for LD inspection to be added in separate production
 - Guide UI
 - Resolution: 768x384 (8 bpp), Scalable to 1536x768 with 2x scaling and sharpness enhancement
 - White Balance Adjustment
 - Support: Embedded with OIF support
- **Wireless Codec (WCOD)**
 - Main Video
 - Engine: IntoPIX FIP
 - Color Format: RGB only (YUV CSC removed)
 - Visual seamless : 1/7 ~ 1/10
 - Latency: 16H (1H: 3.7 us at 4K 120Hz), End-to-End: 32H
 - Sub Video
 - Engine: Single-core TICO-XS
 - Latency: 16H (1H: 3.7 us at 4K 120Hz)
- **Content Protection (HDCP)**
 - Content Protection
 - HDCP 2.3 for LG Interface
- **Audio**
 - Audio Formats
 - Sampling Rates: 48, 96 kHz
 - Bit Depth: 32 bit
 - Channels: Up to 7.1 ch I2S (L/R, Sub L/R, Center/LF, Reverse L/R)
 - Microphone (MIC)
 - Support: PDM data transmission
 - Noise Reduction
 - Support: AEC (Acoustic Echo Cancellation) I2S data transmission

• MODEM / RF IP

- Frequency Range: 57.24 ~ 65.88 GHz
- Bandwidth: 4.32 GHz
- Access Mode: TDD
- Antenna configuration: SISO
- Protocol: Proprietary STD based on 802.11 ay
- PHY Throughput: Max. Throughput 9.2 Gbps, Effective Throughput 6.5 Gbps
- Modulation: Single carrier-BPSK, QPSK, 16-QAM
- Latency: < 4 ms
- RF Ports: Up to 4 ports supported with integrated triplexer circuits

• Mixed IP

- RX Display (Vx1) Interface
 - Data Rate: 2.6 ~ 4.0 Gbps
 - 16 Lane. 10-12bit, 4/5 Byte
- TX Display (Vx1) Interface
 - 16 lane Vx1 TX mode only
 - 120 Hz panel: 3.71 Gbps (74.25 MHz), 5 Byte
 - 144 Hz panel: 3.37 Gbps (84.24 MHz), 4 Byte
 - 165 Hz panel: 3.80 Gbps (95 MHz), 4 Byte
- Clock Tracking PLL
 - Input: 10 ~ 25 kHz Input
 - Output: 10 ~ 25 MHz Output for AIOPLL
- AIOPLL (All-In-One PLL)
 - Input : 24 MHz Crystal
 - Output: CPU: 1920 MHz ($\pm 1\%$, ~ 100 kHz tolerance)
Modem (with/without Spread Spectrum): 880 MHz ($\pm 2\%$, ~100 kHz tolerance)
Display: 594 MHz ($\pm 2\%$, ~100 kHz tolerance)
Wireless Codec: 624/672 MHz ($\pm 2\%$, ~100 kHz tolerance)
- Thermal Sensor
 - Temperature Range: -40°C ~ 125°C (Accuracy improves with calibration within typical usage temperature range)

• Package

- fcBGA: 388 balls
- Ball pitch/size: 0.75/0.45 mm
- Body size: 17x17 mm²

• Clock

- Requires external 24 MHz Crystal, 48 MHz TCXO

• Power

- 3.3V/1.8V/1.2V/0.9V

1.2 Feature of 'LG2851 Module'

LG2851 module is 60GHz mmWave RF front-end module using mmWave RFIC and is supporting the 57.24 – 65.88GHz frequency range and supports 4.32 GHz channel bandwidth. The module includes RX and TX functions needed for signal conversion between the intermediate 10.56GHz frequency and mmWave frequency. Patch, dipole and monopole antennas for the air interface and antenna control functions to form and steer the antenna beam. LG2851 has been designed to be used with LG2832 base-band chip for main application being 4k wireless TVs.

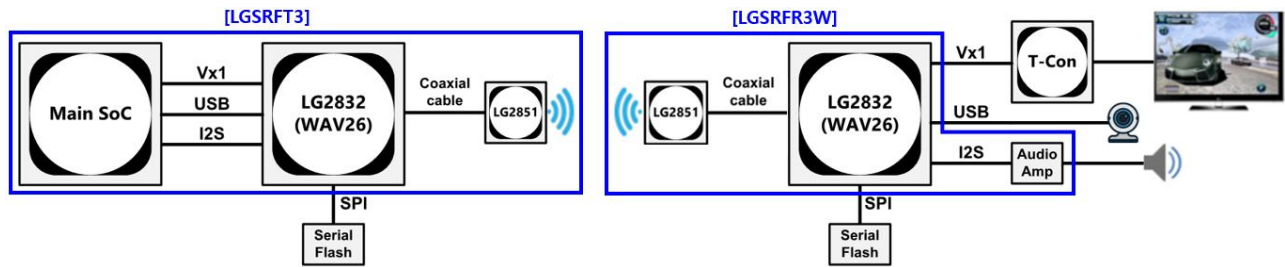
Main features for the LG2851 module are:

- RF frequency range from 57.24 to 65.88 GHz
- Support for 4.32 GHz bandwidth
- Support of BPSK, QPSK and 16-QAM modulations
- COAX-interface between LG2851 and LG2832 combining
 - 330 MHz reference clock
 - 2.64 GHz KIF-control interface for 220 Mbps control data rate
 - 10.56 GHz IF data frequency
- 32 RF inputs and outputs with configurable phase and on-chip combining network to operate beam-forming in RX and TX direction.
- Independent power up/down and bias control for each line-up to support multiple difference module configurations with different antenna arrangements.
- On-chip power detectors and configurable biasing to sense and accurately control the output power of the device
- Simple and fast chip control through programmable trigger commands, both for mode changes and beam steering.

Module is operated from single 5V supply and contains two DCDC converters and two linear regulators to generate power supplies for the LG2851 RFIC.

1.3 Application Example

The figure below shows an example of 4K 165Hz wireless TV application of LGSRT3 and LGSRFR3W.



[Figure 1-1] 'LGSRT3' and 'LGSRFR3W' Use Case for 4K 165Hz Wireless TV System

It shows that 4K 120Hz wireless TV System with LG2832 and LG2851. Main SoC receives all external inputs and send video/osd to LG2832. LG2832 sends manipulated data to LG2851. LG2851 transmits data through wireless channel and receives it at LGSRFR3W. At the other end, i.e., LGSRFR3W, LG2832 processes and regenerates video and audio data, sending them to T-Con.

2 Electrical Specifications

This chapter describes the electrical specifications of LG2832 and LG2851 module, including recommended operating power conditions, recommended operating power ripple conditions, and system power-up sequence.

2.1 Absolute Maximum Ratings for 'LG2851 Module'

The absolute maximum ratings describe the maximum conditions in which the device can be operated without risk of temporary or unrecoverable failure of the device. Compliancy with the electrical specifications or reliability requirements is not guaranteed if any of these conditions are violated.

[Table 2-1] Absolute maximum ratings for supply pins

Parameter	Description	Min	Typ	Max	Unit
	Maximum voltage VDD pins (5.0V)			5.5	V
	Maximum Junction temperature	0		105	deg
	Maximum current draw (32TX)			1.5	A

[Table 2-2] Absolute maximum ratings for signal pins

Parameter	Description	Min	Typ	Max	Unit
	Maximum RF input power without breaking device			+10	dBm

[Table 2-3] ESD maximum ratings

Parameter	Description	Min	Typ	Max	Unit
	All pins except RF pins (HBM)	2000			V
	RF pins (HBM)	1000			V

[Table 2-4] Storage conditions maximum ratings

Parameter	Description	Min	Typ	Max	Unit
	Storage Temperature	-55		125	°C
	Humidity	5		95	%

2.2 Operating Conditions for 'LG2832 IC'

Followings are recommended operating power conditions and temperature conditions for 'LG2832 IC'.

[Table 2-5] Recommended Operating Power Conditions

Parameters		Min.	Typ.	Max.	Units
DVDD33_XTAL DVDD33 AVDD33_USB20	3.3V Digital/XTAL Power Supply	3.14	3.30	3.47	V
AVDD18_C4TX AVDD18_VRX VQPS	1.8V Vx1 Power Supply	1.71	1.80	1.89	V
AVDD18_PLL	1.8V AIO/CTPLL Vx1 Power Supply	1.71	1.80	1.89	V
AVDDT_C4TX	C4TX Termination Supply	1.71	1.80	1.89	V
AVDD18_RF_COM AVDD18_RF AVDD18_RF_TPX	1.8V RF Power Supply	1.75	1.80	1.90	V
AVDD18_RF_PLL	1.8V RF PLL Power Supply	1.75	1.80	1.90	V
AVDD12_RF_COM AVDD12_RF_RXDAC AVDD12_RF_TXADC AVDD12_RF AVDD12_RF_TPX	1.2V RF Power Supply	1.15	1.20	1.26	V
DVDD09	V3	0.90	0.93	0.96	V
	V2	0.85	0.88	0.91	
	V1	0.80	0.83	0.86	
DVDD09_XTAL	0.9V XTAL Power	0.86	0.90	0.95	V
ADVDD09_PLL ADVDD09_VRX	0.9V C4TX PLL Power Supply 0.9V VRX Equalizer Power Supply	0.85	0.90	0.95	V

[Table 2-6] Recommended Operating Temperature Conditions

	Parameters	Min.	Typ.	Max.	Units
	Ambient Temperature	-10		+50	°C

2.3 Operating Conditions for 'LG2851 Module'

When the device is operated within these conditions the full functionality is guaranteed and electrical specifications and reliability targets are met. Unless otherwise noted in subsequent sections.

[Table 2-7] Supply voltages

Parameter	Description	Min	Typ	Max	Unit
	VDD supply (5.0V)	5		5.5	V

[Table 2-8] Normal Operating Temperature Conditions

Parameter	Description	Min	Typ	Max	Unit
	Ambient Temperature	-10		+50	°C

3 Pin Descriptions

LG2832 and LG2851 module includes many digital / mixed IPs. This chapter describes ball map, power supply pins, and functional pins of the chip.

3.1 Pin Description for 'LG2832 IC'

3.1.1 Power Supply Pins

Power types can be categorized as follows.

- Normal Power for Active mode operation
 - DVDD33 → 3.3V Power Supply for I/O
 - DVDD33_XTAL → 3.3V Power Supply for Crystal Oscillator
 - AVDD33_USB20 → 3.3V Power Supply for USB 2.0
 - AVDD18_* → 1.8V Power Supply for Mixed-IP
 - AVDDT_C4TX → 1.8V Power Supply for Vx1-Tx(C4TX) Termination
 - VQPS → 1.8V Power Supply for eFuse
 - AVDD12_* → 1.2V Power Supply for RF-IP
 - DVDD09 → 0.9V Power Supply for Digital Core
 - AVDD09_* → 0.9V Power Supply for Mixed IP
 - DVDD09_XTAL → 0.9V Power Supply for Crystal Oscillator
- GND → Ground

The following tables provide detailed pin descriptions.

1. Digital Power Supply (3.3V)

Type	Counts	Ball No.	Description
DVDD33	4	E13,E14,T13,T14	Digital 3.3V Power Supply for I/O
DVDD33_XTAL	1	E9	Digital 3.3V Power Supply for Crystal Oscillator

2. Analog Power Supply (3.3V)

Type	Counts	Ball No.	Description
AVDD33_USB20	1	E16	3.3V Power Supply for USB 2.0

3. Digital Power Supply (1.8V)

Type	Counts	Ball No.	Description
VQPS	1	L17	1.8V Power for eFuse OTP Programming (secure boot)

4. Analog Power Supply (1.8V)

Type	Counts	Ball No.	Description
AVDD18_C4TX	3	H6,J6,K6	Analog 1.8V Power for C4TX
AVDDT_C4TX	3	H7,J7,K7	1.8V Power Supply for Vx1-Tx(C4TX) Termination
AVDD18_RF_PLL	1	T10	Analog 1.8V Power for RF-IP
AVDD18_RF	1	M8	Analog 1.8V Power for RF-IP
AVDD18_RF_COM	1	T8	Analog 1.8V Power for RF-IP
AVDD18_RF_TPX	1	T7	Analog 1.8V Power for RF-IP
AVDD18_VRX	4	M19,N19,P19,R19	Analog 1.8V Power for Vx1-RX
AVDD18_PLL	1	H9	Analog 1.8V Power for PLL

5. Analog Power Supply (1.2V)

Type	Counts	Ball No.	Description
AVDD12_RF_RXADC	1	N9	Analog 1.2V Power for RF-IP
AVDD12_RF_TXDAC	1	P9	Analog 1.2V Power for RF-IP
AVDD12_RF_COM	1	P10	Analog 1.2V Power for RF-IP
AVDD12_RF	1	P8	Analog 1.2V Power for RF-IP
AVDD12_RF_TPX	2	N6,P6	Analog 1.2V Power for RF-IP

6. Digital Power Supply (0.9V)

Type	Counts	Ball No.	Description
DVDD09	28	H11,H13,H15,H17,J9,J11,J13,J15,J17,K9,K11,K13,K15,K17,L9,L11,L13,L15,M11	Digital 0.9V Power for CORE
DVDD09_XTAL	1	F16	Digital 0.9V Power for Crystal Oscillator

7. Analog Power Supply (0.9V)

Type	Counts	Ball No.	Description
AVDD09_PLL	1	H10	Analog 0.9V Power for PLL
AVDD09_VRX	4	M17,N17,P17,R17	Analog 0.9V Power for Vx1-RX

8. Ground (0V)

Type	Counts	Ball No.	Description
GND	147	B17,C3,C7,C8,C13,C19,D3,D7,D13,D19,E3,E4,E5,E6,E7,E12,E17,E19,E20,F3,F19,F20,G3,G4,G19,G20,H3,H4,H8,H12,H14,H16,H19,H20,J3,J4,J8,J10,J12,J14,J16,J19,J20,K3,K4,K8,K10,K12,K16,K19,K20,L3,L4,L6,L7,L8,L12,L16,L19,L20,M1,M2,M3,M4,M6,M9,M14,M20,N2,N3,N4,N8,N10,N14,N20,P1,P2,P3,P4,P12,P14,P16,P20,R2,R3,R4,R6,R13,R14,R15,R16,R20,T1,T2,T3,T4,T6,T9,T11,T12,T15,T16,T17,T19,T20,T21,T22,U2,U3,U4,V1,V2,V3,V4,V5,V6,V7,V8,V9,V10,V11,W2,W3,W4,W5,W6,W7,W8,W	Analog / Digital Ground for All Power Domain.

3.1.2 Functional Pins

Pin types can be categorized as follows.

- I → Input. Must be applied as required.
- I,0 → Input. If not used, needs to be pulled-down.
- I,1 → Input. If not used, needs to be pulled-up.
- IS → Input with Schmitt triggered.
- IU → Input with internal pull-up resistor. Do not need external pull-up or down.
- ID → Input with internal pull-down resistor. Do not need external pull-up or down.
- IDS → Input with internal pull-down resistor and Schmitt triggered. Do not need external pull-up or down.
- O → Output
- OZ → Tri-state Output
- IO → Bidirectional. Must be applied as required.
- IO(I) → Bidirectional. The default value is input.
- IO(O) → Bidirectional. The default value is output.
- IOU → Bidirectional, input with internal pull-up resistor.
- IO,0 → Bidirectional. If not used, pull-down may be required.
- IO,1 → Bidirectional. If not used, pull-up may be required.
- OZD → Tri-state Output with input and internal pull-down resistor.
- OD → Open Drain.
- AI → Analog Input.
- AO → Analog Output.
- AIO → Analog Input/Output.

Note

When you do not use any pins in your applications, the input and bi-directional pins which do not have an internal pull-up or down resistor should be implemented by external pull-up or down resistor.

- Here are some information for designing test / evaluation boards.
- Pull-up and pull-down resistors are used to retain unused or un-driven inputs in an appropriate state. The recommended pull-up value of 4.7 kΩ to VDD33 (+3.3V) or VDD18 (+1.8V) and pull-down value of same value, applies only to individually terminated signals.
- To prevent possible damage to the device, I/Os capable of becoming outputs must never be tied together and terminated through a common resistor.
- The GPIO shared pins are all 'Bidirectional pin' and possible to control Input / Output polarities.

Pin lists are described by classifying into categories. Those are digital interface pins, analog interface pins. Following sections provide detailed pin descriptions.

3.1.2.1 Digital Interface Pins

Digital pins include categories as below (Total 91 pins):

- System Clock (2 balls)
- IC Operational Mode Signal (7 balls)

- Power-ON Reset (1 ball)
- SPI (Serial Peripheral Interface) – 3 ports (14 balls) / GPIO shared (8 balls)
- UART Interface -- 1 ports (2 balls)
- JTAG Interface -- 2 ports (10 balls) / GPIO shared (8 balls)
- I2C Interface -- 8 ports (16 balls) / GPIO shared (8 balls)
- PWM Interface for LCD Backlight Control (2 balls) / GPIO (2 balls)
- Local Dimming Control (12 balls) / GPIO shared (12 balls)
- Digital Audio Input/Output Interface (7 balls) / GPIO shared (2 balls)
- HDCP Interface (8 balls) / GPIO shared (8 balls)
- GPIO Interface -- Dedicated (10 balls)

The following tables provide detailed pin descriptions.

System Clock (2 balls)

Name	Pin(s)	Type	Description
Xin	B8	I	Input (24MHz) This should comprise the RC network externally. It provides the clock source for internal System PLL and Core.
Xout	A8	O	

* Crystal Specification

Parameter	Value	Unit
Nominal Frequency	24	MHz
Oscillation Mode	Fundamental	
Load Capacitance (CL)	8	pF
LG2832 Frequency Tolerance (25°C)	±30	ppm
Effective Series Resistance	40Ω Max	ohm
Operation Temperature Range	-20~+95	°C
Crystal input swing	> 800	mV

IC Operational Mode Signal (7 balls) / GPIO shared (1 ball)

Name	Pin(s)	Type	Description
opm	C17	I	This signal is for selecting operation mode of the device. This pin should be tied to GND in operation mode.
wakeup_reset_n	D17	I	Wake Up Reset for Non Always On Block (Active Low)
tvon_out	D18	O	TV On Mode Operation Indication
tvon_in	E18	I	TV On Mode or TV OFF Mode Selection
tx0rx1	D8	I	TX Mode or RX Mode Selection
tx_start_tick	AA7	IO	TX Operation Start
hdcv_statvector_sel	W18	I	Setting the boot mode 0 : Serial Flash Boot (Rom Boot) 1 : IRMA/DRMA Boot

Power-ON Reset (1 ball)

Name	Pin(s)	Type	Description
pores_n	C18	I	Power-On Reset (Active Low)

SPI (Serial Peripheral Interface) – 3 ports (14 balls) / GPIO shared (8 balls)

Name	Pin(s)	Type	Description
spi_clk_ms	C16	IO	SPI Slave Interface (Clock)
spi_cs_ms	B16	IO	SPI Slave Interface (Chip Select)
spi_di_ms	B15	IO	SPI Slave Interface (Data Input)
spi_do_ms	A16	IO	SPI Slave Interface (Data Output)
spi_clk_mf	B13	O	SPI Master Flash Memory Interface (Clock)
spi_cs_mf	C15	O	SPI Master Flash Memory Interface (Chip Select)
spi_d0_mf	B14	IO	SPI Master Flash Memory Interface (Data Input/Output)
spi_d1_mf	A14	IO	SPI Master Flash Memory Interface (Data Input/Output)
spi_d2_mf	A13	IO	SPI Master Flash Memory Interface (Data Input/Output)
spi_d3_mf	C14	IO	SPI Master Flash Memory Interface (Data Input/Output)
spi_clk_mf_hdcp	A10	IO	SPI Master HDCP Interface (Clock)
spi_cs_mf_hdcp	C10	IO	SPI Master HDCP Interface (Chip Select)
spi_di_mf_hdcp	B10	IO	SPI Master HDCP Interface (Data Input)
spi_do_mf_hdcp	C11	IO	SPI Master HDCP Interface (Data Output)

UART Interface -- 1 ports (2 balls)

Name	Pin(s)	Type	Description
uart0_rxd	Y13	I	UART0 Interface Receive Data
uart0_txd	AA13	O	UART0 Interface Transmit Data

JTAG Interface -- 2 ports (10 balls) / GPIO shared (8 balls)

Name	Pin(s)	Type	Description
jtag_tck_hdcp	Y22	I	JTAG Interface Test Clock for HDCP
jtag_tms_hdcp	AA22	IO	JTAG Interface Test MODE Select for HDCP
jtag_trst_hdcp	AA21	IO	JTAG Interface Test Reset for HDCP
jtag_tdi_hdcp	Y21	IO	JTAG Interface Test Data In for HDCP
jtag_tdo_hdcp	AB21	IO	JTAG Interface Test Data Out for HDCP
jtag_tck_cpu	W16	I	JTAG Interface Test Clock for CPU
jtag_tms_cpu	V17	IO	JTAG Interface Test MODE Select for CPU
jtag_trst_cpu	V16	IO	JTAG Interface Test Reset for CPU
jtag_tdi_cpu	V18	IO	JTAG Interface Test Data In for CPU
jtag_tdo_cpu	W17	IO	JTAG Interface Test Data Out for CPU

I2C Interface -- 8 ports (16 balls) / GPIO shared (8 balls)

Name	Pin(s)	Type	Description
sda0_ms	D16	IO	I2C Interface Data must be Pull-Up
scl0_ms	D15	IO	I2C Interface Clock must be Pull-Up
sda1_ms	AA18	IO	I2C Interface Data must be Pull-Up
scl1_ms	AB18	IO	I2C Interface Clock must be Pull-Up
sda2_ms	AA19	IO	I2C Interface Data must be Pull-Up
scl2_ms	Y18	IO	I2C Interface Clock must be Pull-Up
sda3_ms	AA20	IO	I2C Interface Data must be Pull-Up
scl3_ms	Y19	IO	I2C Interface Clock must be Pull-Up
sda4_ms	Y20	IO	I2C Interface Data must be Pull-Up
scl4_ms	AB20	IO	I2C Interface Clock must be Pull-Up
sda_s	D14	IO	I2C Interface Data must be Pull-Up
scl_s	E15	IO	I2C Interface Clock must be Pull-Up
sda_ms_hdcp	B12	IO	I2C Interface Data must be Pull-Up
scl_ms_hdcp	C12	IO	I2C Interface Clock must be Pull-Up
sda_s_hdcp	A11	IO	I2C Interface Data must be Pull-Up
scl_s_hdcp	B11	IO	I2C Interface Clock must be Pull-Up

PWM Interface for LCD Backlight Control (2 balls) / GPIO (2 balls)

Name	Pin(s)	Type	Description
pwm0	AB14	IO	PWM0 (Pulse Width Modulation) Output for LED Backlight Control
pwm1	AA14	IO	PWM1 (Pulse Width Modulation) Output for LED Backlight Control

Local Dimming Control (12 balls) / GPIO shared (12 balls)

Name	Pin(s)	Type	Description
m1_sclk	Y15	IO	Clock for Local Dimming Control 1(SPI Interface)
m1_mosi	Y14	IO	Data for Local Dimming Control 1 (SPI Interface)
m2_sclk	AB17	IO	Clock for Local Dimming Control 2 (SPI Interface)
m2_mosi	AA16	IO	Data for Local Dimming Control 2 (SPI Interface)
m3_sclk	AA17	IO	Clock for Local Dimming Control 3 (SPI Interface)
m3_mosi	Y16	IO	Data for Local Dimming Control 3 (SPI Interface)
ld_vs_out0	V14	IO	Vsync Output for Local Dimming Control 0
ld_vs_out1	W14	IO	Vsync Output for Local Dimming Control 1
ld_vs_out2	V15	IO	Vsync Output for Local Dimming Control 2
ld_vs_out3	W15	IO	Vsync Output for Local Dimming Control 3
m1_sclk	Y15	IO	Clock for Local Dimming Control 1(SPI Interface)
m1_mosi	Y14	IO	Data for Local Dimming Control 1 (SPI Interface)

Digital Audio Input/Output Interface (7 balls) / GPIO shared (2 balls)

Name	Pin(s)	Type	Description
audclk	Y11	IO	Clock Input/Output for Digital Audio AMP
daclrch	Y10	IO	L/R Output (Front)
dacslrch	Y9	IO	Surround L/R Output
dacclfch	W11	IO	Center and Low Frequency Output
dacsck	AB11	IO	PCM Bit Clock Output (Input) to (from) External Audio DAC
daclrck	AA10	IO	Sampling Clock Output (Input) to (from) External Audio DAC
dacrlrch	AA11	IO	Rear L/R Output

GPIO Interface for HDCP (8 balls) / GPIO shared (8 balls)

Name	Pin(s)	Type	Description
hdcg_gpio0	D12	IO	General Purpose IO for HDCP
hdcg_gpio1	E11	IO	General Purpose IO for HDCP
hdcg_gpio2	D11	IO	General Purpose IO for HDCP
hdcg_gpio3	D10	IO	General Purpose IO for HDCP
hdcg_gpio4	B9	IO	General Purpose IO for HDCP
hdcg_gpio5	C9	IO	General Purpose IO for HDCP
hdcg_gpio6	E10	IO	General Purpose IO for HDCP
hdcg_gpio7	D9	IO	General Purpose IO for HDCP

GPIO Interface GPIO Interface -- Dedicated (10 balls)

Name	Pin(s)	Type	Description
gpio0	W20	IO	General Purpose IO
gpio1	W21	IO	General Purpose IO
gpio2	V19	IO	General Purpose IO
gpio3	W22	IO	General Purpose IO
gpio4	V20	IO	General Purpose IO
gpio5	V21	IO	General Purpose IO
gpio6	U19	IO	General Purpose IO
gpio7	U20	IO	General Purpose IO
gpio8	U21	IO	General Purpose IO
gpio9	U22	IO	General Purpose IO

GPIO Interface -- RFIP(RAUTA) (4 Balls) / GPIO Shared (4 Balls)

Name	Pin(s)	Type	Description
rf5v_0_on1off0	AA9	IO	RAUTA General Purpose IO
rf5v_1_on1off0	AB8	IO	RAUTA General Purpose IO
rf5v_2_on1off0	AB9	IO	RAUTA General Purpose IO
rf5v_3_on1off0	AA8	IO	RAUTA General Purpose IO

3.1.2.2 Analog Interface Pins

LG2832 has analog interfaces. Those are:

- Vx1-Rx Interface (33 balls)
- Vx1-Tx Interface (33 balls)
- RFIP(RAUTA) Interface (9 balls)
- USB 2.0 Host Interface -- 1 port (3 balls)

The following tables provide detailed pin descriptions.

Vx1-Rx Interface (33 balls)

Name	Pin(s)	Type	Description
VRX0P	R22	AI	Vx1 Serial Data Input
VRX0N	R21	AI	Vx1 Serial Data Input
VRX1N	P21	AI	Vx1 Serial Data Input
VRX1P	P22	AI	Vx1 Serial Data Input
VRX2P	N22	AI	Vx1 Serial Data Input
VRX2N	N21	AI	Vx1 Serial Data Input
VRX3N	M21	AI	Vx1 Serial Data Input
VRX3P	M22	AI	Vx1 Serial Data Input
VRX4P	L22	AI	Vx1 Serial Data Input
VRX4N	L21	AI	Vx1 Serial Data Input
VRX5N	K21	AI	Vx1 Serial Data Input
VRX5P	K22	AI	Vx1 Serial Data Input
VRX6P	J22	AI	Vx1 Serial Data Input
VRX6N	J21	AI	Vx1 Serial Data Input
VRX7N	H21	AI	Vx1 Serial Data Input
VRX7P	H22	AI	Vx1 Serial Data Input
VRX8P	G22	AI	Vx1 Serial Data Input
VRX8N	G21	AI	Vx1 Serial Data Input
VRX9N	F21	AI	Vx1 Serial Data Input
VRX9P	F22	AI	Vx1 Serial Data Input
VRX10P	E22	AI	Vx1 Serial Data Input
VRX10N	E21	AI	Vx1 Serial Data Input
VRX11N	D21	AI	Vx1 Serial Data Input
VRX11P	D22	AI	Vx1 Serial Data Input
VRX12P	C22	AI	Vx1 Serial Data Input
VRX12N	C21	AI	Vx1 Serial Data Input
VRX13N	B21	AI	Vx1 Serial Data Input
VRX13P	B22	AI	Vx1 Serial Data Input
VRX14P	A20	AI	Vx1 Serial Data Input
VRX14N	B20	AI	Vx1 Serial Data Input
VRX15N	C20	AI	Vx1 Serial Data Input
VRX15P	D20	AI	Vx1 Serial Data Input
vrx_lock_n	Y17	OD	Vx1 Lock (Active Low). Must be external Pull-Up.

Vx1-Tx Interface (33 balls)

Name	Pin(s)	Type	Description
C4TX_0N	L1	AO	Vx1 Serial Data Output
C4TX_0P	L2	AO	Vx1 Serial Data Output
C4TX_1N	K1	AO	Vx1 Serial Data Output
C4TX_1P	K2	AO	Vx1 Serial Data Output
C4TX_2N	J1	AO	Vx1 Serial Data Output
C4TX_2P	J2	AO	Vx1 Serial Data Output
C4TX_3N	H1	AO	Vx1 Serial Data Output
C4TX_3P	H2	AO	Vx1 Serial Data Output
C4TX_4N	G1	AO	Vx1 Serial Data Output
C4TX_4P	G2	AO	Vx1 Serial Data Output
C4TX_5N	F1	AO	Vx1 Serial Data Output
C4TX_5P	F2	AO	Vx1 Serial Data Output
C4TX_6N	E1	AO	Vx1 Serial Data Output
C4TX_6P	E2	AO	Vx1 Serial Data Output
C4TX_7N	D1	AO	Vx1 Serial Data Output
C4TX_7P	D2	AO	Vx1 Serial Data Output
C4TX_8N	C1	AO	Vx1 Serial Data Output
C4TX_8P	C2	AO	Vx1 Serial Data Output
C4TX_9N	B1	AO	Vx1 Serial Data Output
C4TX_9P	B2	AO	Vx1 Serial Data Output
C4TX_10N	B3	AO	Vx1 Serial Data Output
C4TX_10P	A3	AO	Vx1 Serial Data Output
C4TX_11N	B4	AO	Vx1 Serial Data Output
C4TX_11P	A4	AO	Vx1 Serial Data Output
C4TX_12N	C4	AO	Vx1 Serial Data Output
C4TX_12P	D4	AO	Vx1 Serial Data Output
C4TX_13N	C5	AO	Vx1 Serial Data Output
C4TX_13P	D5	AO	Vx1 Serial Data Output
C4TX_14N	A6	AO	Vx1 Serial Data Output
C4TX_14P	B6	AO	Vx1 Serial Data Output
C4TX_15N	C6	AO	Vx1 Serial Data Output
C4TX_15P	D6	AO	Vx1 Serial Data Output
TX_LOCKN	F4	AI	Vx1 Locking Check Pin

RFIP(RAUTA) Interface (9 balls)

Name	Pin(s)	Type	Description
RF0_10G_CTRL_CLK	N1	AIO	10 GHz RF0-port, 330MHz RF0 reference clock for KASI, RF0
RF1_10G_CTRL_CLK	R1	AO	10 GHz RF1-port, 330MHz RF1 reference clock for KASI, RF1
RF2_10G_CTRL_CLK	U1	AIO	10 GHz RF2-port, 330MHz RF2 reference clock for KASI, RF2
RF3_10G_CTRL_CLK	W1	AIO	10 GHz RF3-port, 330MHz RF3 reference clock for KASI, RF3
RF_REFCLK_IN	AB6	AI	48 MHz reference clock input
RF_AFCDAC	AB2	AO	AFCDAC output for VCTCXO control
RF_VREF_CAP	AA1	AO	External filtering capacitor pin for the reference voltage
RF_TP_P	AA4	AIO	Testpoint (Positive)
RF_TP_N	AA3	AIO	Testpoint (Negative)

USB 2.0 Host Interface -- 1 port (3 balls)

Name	Pin(s)	Type	Description
USB20_TXRTUNE	A17	AIO	USB 2.0 Transmitter Resistor Tune & voltage probe. External Resistor value is (200 ohm $\pm$ 1%) to GND.
USB20_DM	B18	AIO	USB 2.0 port D-. If not used, must be floated.
USB20_DP	A18	AIO	USB 2.0 port D+. If not used, must be floated.

3.2 Pin Description for 'LG2851 Module'

'LG2851 module' connections and testpoints are listed in the table below.

Module Interface (8 pins and testpoints)

Name	Pin(s)	Type	Description
COAX			Triplexer connector
+5.0V			5V external supply DC connector
TP100			Testpoint for VQPS
TP103			Testpoint for GPIO0
TP107			Testpoint for VREF_CAP
TP108			Testpoint for +5.0V
TP109			Testpoint for GND
TP110			Testpoint for +1.8V

4 RF Specifications

RF specifications are defined in typical conditions and room temperature only (ambient). Performance may vary due to variations in IC manufacturing process.

4.1 Receiver and Transmitter for 'LG2832 Board'

Receiver and transmitter specifications are defined below.

[Table 4-1] Transceiver specifications

Parameter	Description	Min	Typ	Max	Unit
RF_COAX*	DATA-path Frequency channel	8800	10560	12320	MHz
	CTRL-path Frequency channel		2640		MHz
	CLOCK-path Frequency channel		330		MHz
	Impedance		50		Ohm
	S11 for each Frequency channel range			-10	dB
	PIN DC-level		0		V
RF_COAX* DATA Transmitter-path	Pout (scaler value 256)	-11	-7.5		dBm
	OIP3-Linearity (Ptot-IM3/2)	9			dBm
	<u>Calibrated</u> Image LO leakage			-40 -40	dBc dBc
	<u>Band flatness</u> DMG EDMG		< +/-1 < +/-2		dB dB
	<u>EVM</u> DMG EDMG			-27 -27	dB dB
RF_COAX* DATA Receiver-path	Noise figure (ADC included, max gain)			20	dB
	Analog gain range 0 ... 24dB				
	Analog gain max	24			dB
	Analog gain step		3		dB
	<u>Calibrated</u> Image			-40	dBc
	IM3-Linearity Pin=-10dBm (freq1 & freq2, Pin=-13dBm per tone)			-40	dBc
	<u>EVM</u> DMG EDMG			-27 -27	dB dB
RF_COAX* CTRL KIF-interface	Frequency channel		2640		MHz
	TX Signal amplitude tune range	25		150	mV
	RX Signal amplitude min detection	30			mV
RF_COAX* CLOCK REF330-path	Frequency		330		MHz
	Signal amplitude		150		mV
RF_REFCLK_IN	Frequency		48		MHz
	Frequency accuracy			20	ppm
	Clock input level requirement (from VC		0.8		Vpp
	Port DC-level (internal)		450		mV

*=0, 1, 2 or 3 depending on the path, specified at RAUTA RF_COAX-pin

4.2 Receiver and Transmitter for 'LG2851 Module'

Receiver and transmitter specifications are defined for 32 or 14 line-up unless otherwise stated. RX and TX can also be operated with fewer line-ups enabled.

[Table 4-2] Receiver specifications for 'LG2851 Box Module'

Parameter	Description	Min	Typ	Max	Unit
	Operating frequency	57.24		65.88	GHz
	Gain (with 32RX)	36	42		dB
	Gain (with 16RX)	32	38		dB
	Sensitivity (1.76GHz band width, 15db SNR)		-70		dBm EIRS
	Sensitivity (3.52GHz band width, 15db SNR)		-67		dBm EIRS
	Maximum input power		-52		dBm EIRS
	IIP3 (with 32RX)	-38	-30		dBm EIRS
	IIP3 (with 16RX)	-34	-26		dBm EIRS
	RX EVM (with phase tracking)		-30		dB
	RX phase control step size		45		deg
	COAX-port frequency range			12.32	GHz
	Maximum COAX-port output power		-13		dBm
	COAX-port output impedance		50		Ω
	COAX-port return loss (S11)		-10		dB

Conditions: $T_A = 25^\circ\text{C}$, supply VDD= 5V

[Table 4-3] Transmitter specifications for 'LG2851 Box Module'

Parameter	Description	Min	Typ	Max	Unit
	Operating frequency	57.24		65.88	GHz
	Maximum output power		37		dBm EIRP
	OIP3	44	48		dBm EIRP
	Gain (nominal input power -20dBm)	44	52		dB
	TX EVM (with phase tracking)		-30		dB
	TX phase control step size		45		deg
	COAX port frequency range			12.32	GHz
	COAX-port input power		-20		dBm
	COAX-port input impedance		50		Ω
	COAX-port return loss (S11)			-10	dB

Conditions: $T_A = 25^\circ\text{C}$, supply VDD= 5V

[Table 4-4] Receiver specifications for 'LG2851 Slim-Right Display Module'

Parameter	Description	Min	Typ	Max	Unit
	Operating frequency	57.24		65.88	GHz
	Gain (with 14RX)	29	35		dB
	Sensitivity (1.76GHz band width, 15db SNR)		-65		dBm EIRS
	Sensitivity (3.52GHz band width, 15db SNR)		-62		dBm EIRS
	Maximum input power		-45		dBm EIRS
	IIP3 (with 14RX)	-31	-23		dBm EIRS
	RX EVM (with phase tracking)	-28	-30		dB
	RX phase control step size		45		deg
	COAX-port frequency range			12.32	GHz
	Maximum COAX-port output power		-13		dBm
	COAX-port output impedance		50		Ω
	COAX-port return loss (S11)		-10		dB

Conditions: T_A= 25°C, supply VDD= 5V

[Table 4-5] Transmitter specifications for 'LG2851 Slim-Right Display Module'

Parameter	Description	Min	Typ	Max	Unit
	Operating frequency	57.24		65.88	GHz
	Maximum output power	21	23		dBm EIRP
	OIP3	35	39		dBm EIRP
	Gain (nominal input power -20dBm)	35	43		dB
	TX EVM (with phase tracking)	-28	-30		dB
	TX phase control step size		45		deg
	COAX port frequency range			12.32	GHz
	COAX-port input power		-20		dBm
	COAX-port input impedance		50		Ω
	COAX-port return loss (S11)			-10	dB

Conditions: T_A= 25°C, supply VDD= 5V

5 Regulatory Statement

This chapter describes the regulatory statement for FCC, ISED, CE and UKCA.

5.1 FCC

FCC Part 15.19 Statements:

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Part 15.21 statement

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

Regulatory notice to host manufacturer according to KDB 996369 D03 OEM Manual v01

This module has been granted modular approval as below listed FCC rule parts.

- FCC Rule parts 15C(15.255)

Summarize the specific operational use conditions

- The OEM integrator should use equivalent antennas which is the same type and equal or less gain than an antenna listed below this instruction manual.

RF exposure considerations

- The module has been certified for integration into products only by OEM integrators under the following condition:
- The antenna(s) must be installed such that a minimum separation distance of at least 20 cm is maintained between the radiator (antenna) and all persons at all times.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

Mobile use

As long as the three conditions above are met, further transmitter testing will not be required.

OEM integrators should provide the minimum separation distance to end users in their end-product manuals.

Antennas list

This module is certified with the following integrated antenna.

1. LGSRFT3 : Patch Array Antenna, (peak antenna gain: 20 dBi)
2. LGSRFR3W :

Antenna No.	Antenna type	Peak Antenna gain (dBi)
ANT0	Dipole Array Antenna	14.6
ANT1	Patch Array Antenna	15.2
ANT2	Dipole Array Antenna	7.5
ANT2	Dipole Array Antenna	7.5

Any new antenna type, higher gain than listed antenna should be met the requirements of FCC rule 15.203 and 2.1043 as permissive change procedure.

Label and compliance information

End Product Labeling

The module is labeled with its own FCC ID and IC Certification Number. If the FCC ID and IC Certification Number are not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final end product must be labeled in a visible area with the following:

"Contains FCC ID : 2B03LLGSRFT3 / 2B03LLGSRFR3W

"Contains IC : 2703H-LGSRFT3 / 2703H-LGSRFR3W

Information on test modes and additional testing requirements

OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, additional transmitter in the host, etc.).

Additional testing, Part 15 Subpart B disclaimer

The final host product also requires Part 15 subpart B compliance testing with the modular transmitter installed to be properly authorized for operation as a Part 15 digital device.

Note EMI Considerations

Note that a host manufacture is recommended to use D04 Module Integration Guide recommending as "best practice" RF design engineering testing and evaluation in case non-linear interactions generate additional non-compliant limits due to module placement to host components or properties.

For standalone mode, reference the guidance in D04 Module Integration Guide and for simultaneous mode⁷; see D02 Module Q&A Question 12, which permits the host manufacturer to confirm compliance.

How to make changes

Since only Grantees are permitted to make permissive changes, when the module will be used differently than granted, please contact the module manufacture on below contact information.

- Contact information: younguk.nam@lge.com / Tel: 82-31-8066-5543.

5.2 ISED

RSS-GEN, Sec. 7.1.3–(licence-exempt radio apparatus)

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions:

- (1) this device may not cause interference, and
- (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

- (1) l'appareil ne doit pas produire de brouillage, et
- (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

RF Exposure

The antenna (or antennas) must be installed so as to maintain at all times a distance minimum of at least 20 cm between the radiation source (antenna) and any individual. This device may not be installed or used in conjunction with any other antenna or transmitter.

L'exposition aux RF L'antenne (ou les antennes) doit être installée de façon à maintenir à tout instant une distance minimum de au moins 20 cm entre la source de radiation (l'antenne) et toute personne physique.

Caution: Any changes or modifications to this device not explicitly approved by manufacturer could void your authority to operate this equipment. Attention:

Les changements ou modifications de cet appareil non expressément approuvé par le fabricant peuvent annuler votre droit à utiliser cet équipement.

Étiquetage du produit final (IC)

Le module est étiqueté avec sa propre identification FCC et son propre numéro de certification IC. Si l'identification FCC et le numéro de certification IC ne sont pas visibles lorsque le module est installé à l'intérieur d'un autre dispositif, la partie externe du dispositif dans lequel le module est installé devra également présenter une étiquette faisant référence au module inclus. Dans ce cas, le produit final devra être étiqueté sur une zone visible avec les informations suivantes :

« Contient module émetteur IC : **2703H-LGSRFT3 / 2703H-LGSRFR3W**

5.3 CE

Simplified EU Declaration of Conformity

Hereby, LG Electronics Inc. declares that the radio equipment type **[LGSRFT3, LGSRFR3W]** is in compliance with Directive 2014/53/EU. The full text of the EU declaration of conformity is available at the following internet address: <http://www.lg.com/global/support/cedoc/cedoc#>

RF Exposure

The antenna (or antennas) must be installed so as to maintain at all times a distance minimum of at least 20 cm between the radiation source (antenna) and any individual. This device may not be installed or used in conjunction with any other antenna or transmitter

EU Importer : LG Electronics European Shared Service Center B.V.

Address : Krijgsman 1, 1186 DM Amstelveen, The Netherlands

The host manufacturer has the responsibility that the host device should be compliance with all essential requirement of RED.

5.4 UKCA

Simplified UKCA Declaration of Conformity

Hereby, LG Electronics Inc. declares that the radio equipment type **[LGSRFT3, LGSRFR3W]** is in compliance with the Radio Equipment Regulations 2017(SI 2017 No.1206). The full text of the UK declaration of conformity is available at the following internet address: <http://www.lg.com/global/support/cedoc/cedoc#>

UK Importer : LG Electronics U.K. Ltd

Address : Velocity 2, Brooklands Drive, Weybridge, KT13 0SL

The host manufacturer has the responsibility that the host device should be compliance with all essential requirement of the Radio Equipment Regulations 2017.