

ATWINC15x0-MR210xB IEEE® 802.11 b/g/n SmartConnect IoT Module

Introduction

The ATWINC15x0-MR210xB is a low power consumption 802.11 b/g/n IoT (Internet of Things) module, specifically optimized for low power IoT applications. The module integrates Power Amplifier (PA), Low-Noise Amplifier (LNA), Switch, Power Management, and a printed antenna or a micro co-ax (u.FL) connector for an external antenna resulting in a small form factor (21.7 x 14.7 x 2.1 mm) design. It is interoperable with various vendors' 802.11 b/g/n access points. This module provides SPI ports to interface with a host controller.

The references to the ATWINC1510-MR210UB module include the module devices listed in the following:

- ATWINC1510-MR210UB

Features

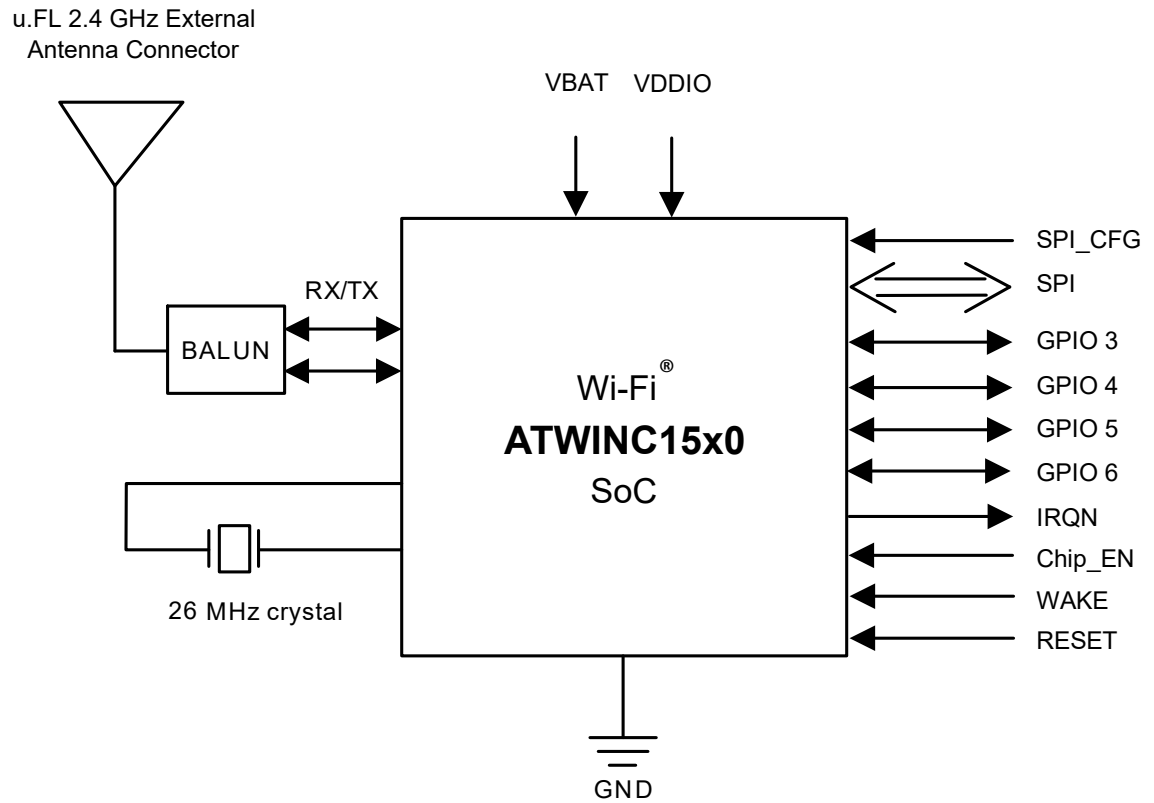
- IEEE® 802.11 b/g/n 20 MHz (1x1) solution
- Single spatial stream in 2.4 GHz ISM band
- Integrated Transmit/Receive switch
- Integrated PCB antenna or u.FL micro co-ax connector for external antenna
- Superior sensitivity and range via advanced PHY signal processing
- Advanced equalization and channel estimation
- Advanced carrier and timing synchronization
- Wi-Fi® Direct (supported till firmware release 19.5.2)
- Soft-AP support
- Supports IEEE 802.11 WEP, WPA, WPA2 security
- Support Enterprise security with WPA/WPA2 (802.1X)⁽¹⁾
 - EAP-TLS
 - EAP-PEAPv0/1 with TLS
 - EAP-TTLSv0 with MSCHAPv2
 - EAP-PEAPv0/1 with MSCHAPv2
- Superior MAC throughput via hardware accelerated two-level A-MSDU/A-MPDU frame aggregation and block acknowledgment
- On-chip memory management engine to reduce host load
- SPI host interface

- Operating temperature range from -40°C to +85°C. RF performance at room temperature of 25°C with a 2-3 db change at boundary conditions
- I/O operating voltage of 2.7V to 3.6V
- Built-in 26 MHz crystal
- Integrated Flash memory for system software
- Power Save modes
 - 4 µA Power-Down mode typical at 3.3V I/O
 - 380 µA Doze mode with chip settings preserved (used for beacon monitoring)⁽²⁾
 - On-chip low power sleep oscillator
 - Fast host wake-up from Doze mode by a pin or SPI transaction
- Fast Boot options
 - On-chip boot ROM (Firmware instant boot)
 - SPI flash boot
 - Low-leakage on-chip memory for state variables
 - Fast AP re-association (150 ms)
- On-chip Network stack to offload MCU
 - Integrated Network IP stack to minimize host CPU requirements
 - Network features TCP, UDP, DHCP, ARP, HTTP, TLS, and DNS
 - Hardware accelerators for Wi-Fi and TLS security to improve connection time
- Hardware accelerator for IP checksum
- Hardware accelerators for OTA security
- Small footprint host driver
- Wi-Fi Alliance® certifications for Connectivity and Optimizations
 - ID: [WFA61069](#)

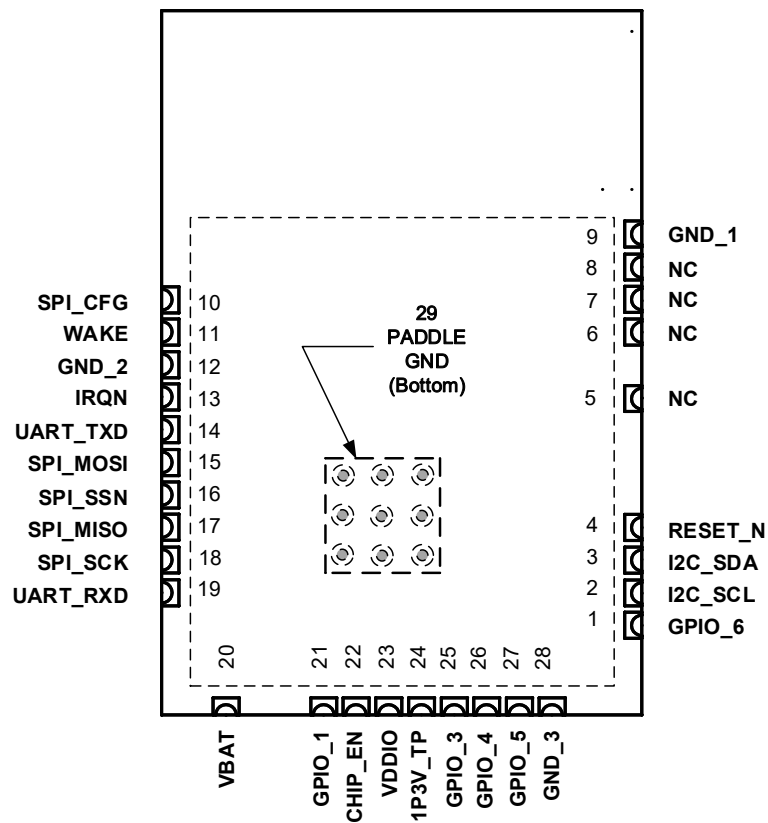
Note:

1. For more information on software feature, refer to Wi-Fi Network Controller Software Design Guide (DS00002389).
2. For information on module power modes, refer to [Power Consumption](#).

Block Diagram



Pin Description



Pin #	Name	Type	Description	Programmable Pull Up Resistor
1	GPIO_6	I/O	General purpose I/O.	Yes
2	I2C_SCL	I/O	I2C Slave Clock. Currently used only for development debug. Leave unconnected.	Yes
3	I2C_SDA	I/O	I2C Slave Data. Currently used only for development debug. Leave unconnected.	Yes
4	RESET_N	I	Active-Low Hard Reset. When this pin is asserted low, the module will be placed in the reset state. When this pin is asserted high, the module will be out of reset and will function normally. Connect to a host output that defaults low at power up. If the host output is tri-stated, add a 1 MΩ pull down resistor to ensure a low level at power-up.	No
5	NC	-	No connect.	-

Pin #	Name	Type	Description	Programmable Pull Up Resistor
6	NC	-	No connect.	-
7	NC	-	No connect.	-
8	NC	-	No connect.	-
9	GND_1	-	GND.	-
10	SPI_CFG	I	Tie to VDDIO through a 1 MΩ resistor to enable the SPI interface.	No
11	WAKE	I	Host Wake control. Can be used to wake-up the module from Doze mode. Connect to a host GPIO.	Yes
12	GND_2	-	GND.	-
13	IRQN	O	ATWINC15x0-MR210xB Device Interrupt output. Connect to host interrupt input pin.	Yes
14	UART_TXD	O	UART Transmit Output from ATWINC15x0-MR210xB Added debug.	Yes
15	SPI_RXD	I	SPI MOSI (Master Out, Slave In) pin.	Yes
16	SPI_SSN	I	SPI Slave Select. Active-low.	Yes
17	SPI_TXD	O	SPI MISO (Master In, Slave Out) pin.	Yes
18	SPI_SCK	I	SPI Clock.	Yes
19	UART_RXD	I	UART Receive input to ATWINC15x0-MR210xB. Added debug.	Yes
20	VBATT	-	Battery power supply.	-
21	GPIO_1/RTC	I	General Purpose I/O / RTC.	Yes
22	CHIP_EN	I	Module enable. High level enables the module; low level places module in Power-Down mode. Connect to a host output that defaults low at power-up. If the host output is tri-stated, add a 1 MΩ pull down resistor to ensure a low level at power-up.	No
23	VDDIO	-	I/O Power Supply. Must match host I/O voltage.	-
24	1P3V_TP	-	1.3V VDD Core Test Point. Decouple with 10 μF, and 0.01 μF to GND.	-
25	GPIO_3	I/O	General purpose I/O.	Yes
26	GPIO_4	I/O	General purpose I/O.	Yes
27	GPIO_5	I/O	General purpose I/O.	Yes
28	GND_3	-	GND.	-
29	PADDLE GND	-	GND.	-

Electrical Specifications

Absolute Maximum Ratings

Absolute maximum ratings for the modules are listed below.

Symbol	Description	Min.	Max.	Unit
VBATT	Input supply voltage	-0.3	5.0	V
VDDIO	I/O voltage	-0.3	4.2	V
Operating Temperature		-40	+85	°C

	Stresses listed under " Absolute Maximum Ratings " may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect the device reliability.
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Recommended Operating Conditions

Recommended Operating Conditions

Symbol	Min.	Typ.	Max.	Unit
VBATT	3.0	3.3	4.2	V
VDDIO	2.7	3.3	3.6	V

CPU and Memory Subsystems

Processor

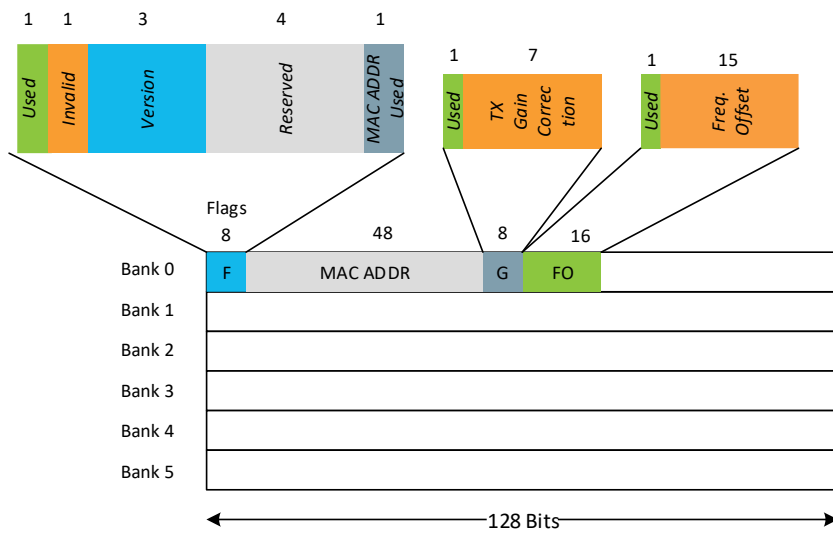
The ATWINC1510-MR210UB modules have a Cortus APS3 32-bit processor. This processor performs many of the MAC functions, including but not limited to the association, authentication, power management, security key management, and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes.

Memory Subsystem

The APS3 core uses a 128KB instruction/boot ROM along with a 160KB instruction RAM and a 64KB data RAM. The ATWINC1510-MR210UB modules come populated with either 4Mb or 8Mb of Flash memory depending on the module model that is ordered. This memory can be used for system software. See [Table 1-1](#) for more information. In addition, the device uses a 128KB shared RAM, accessible by the processor and MAC, which allows the APS3 core to perform various data management tasks on the TX and RX data packets.

Non-volatile Memory (eFuse)

The ATWINC1510-MR210UB modules have 768 bits of non-volatile eFuse memory that can be read by the CPU after device reset. This non-volatile one-time-programmable (OTP) memory can be used to store customer-specific parameters, such as MAC address; various calibration information, such as TX power, crystal frequency offset, etc.; and other software-specific configuration parameters. The eFuse is partitioned into six 128-bit banks. Each bank has the same bitmap (see following figure). The purpose of the first 80 bits in each bank is fixed, and the remaining 48 bits are general-purpose software dependent bits, or reserved for future use. Since each bank can be programmed independently, this allows for several updates of the device parameters following the initial programming; for example, if the MAC address has to be changed, Bank 1 has to be programmed with the new MAC address along with the values of TX gain correction and frequency offset if they are used and programmed in Bank 0. The contents of Bank 0 have to be invalidated in this case by programming the invalid bit in the Bank 0. This will allow the firmware to use the MAC address. By default, all the ATWINC15x0-MR210xB modules are programmed with the MAC address and the frequency offset bits of Bank 0.



WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC) and the Physical Layer (PHY). The following two subsections describe the MAC and PHY in detail.

MAC

Description

The ATWINC1510-MR210UB MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

Dedicated datapath engines are used to implement datapath functions with heavy computational requirements. For example, an FCS engine checks the CRC of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, and WPA2 CCMP-AES.

Control functions which have real-time requirements are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability via the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon TX control, interframe spacing, etc.), protocol timer module (responsible for the Network Access Vector, back-off timing, timing synchronization function, and slot management), MPDU handling module, aggregation/de-aggregation module, block ACK controller (implements the protocol requirements for burst block communication), and TX/RX control FSMs (coordinate data movement between PHY-MAC interface, cipher engine, and the DMA interface to the TX/RX FIFOs).

The MAC functions implemented solely in software on the microprocessor have the following characteristics:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real-time requirements. Examples are authentication and association.
- Functions which need flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

Features

The ATWINC15x0-MR210xB IEEE802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
 - Transmission and reception of aggregated MPDUs (A-MPDU) – Transmission and reception of aggregated MSDUs (A-MSDU) – Immediate Block Acknowledgment
 - Reduced Interframe Spacing (RIFS)

- Support for IEEE802.11i and WPA security with key management:
 - WEP 64/128
 - WPA-TKIP
 - 128-bit WPA2 CCMP (AES)
- Advanced power management:
 - Standard 802.11 Power Save Mode
- RTS-CTS and CTS-self support
- Supports either STA or AP mode in the infrastructure basic service set mode

PHY

Description

The ATWINC1510-MR210UB WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in single stream mode with 20MHz bandwidth. Advanced algorithms have been employed to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions that include FFT, filtering, FEC (Viterbi decoder), frequency, timing acquisition and tracking, channel estimation and equalization, carrier sensing, clear channel assessment, and automatic gain control.

Features

The ATWINC1510-MR210UB IEEE802.11 PHY supports the following functions:

- Single antenna 1x1 stream in 20MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, 11Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12, 18, 24, 36, 48, 54Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20MHz, 800 and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, 72.2Mbps
- IEEE 802.11n mixed mode operation
- Per packet TX power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery, and frame detection

Radio

This section presents information describing the properties and characteristics of the ATWINC15x0-MR210xB and Wi-Fi radio transmit and receive performance capabilities of the device.

The performance measurements are taken at the RF pin assuming 50Ω impedance; the RF performance is guaranteed for room temperature of 25 °C with a derating of 2-3dB at boundary conditions.

Measurements were taken under typical conditions: VBATT=3.3V; VDDIO=3.3V; temperature: +25°C

Features and Properties

Feature	Description
Part Number	ATWINC1510-MR210UB
WLAN Standard	IEEE 802.11 b/g/n, Wi-Fi compliant

Feature	Description
Host Interface	SPI
Dimension	21.7 x 14.7 x 2.1 mm
Frequency Range	2.412GHz ~ 2.472GHz (2.4GHz ISM Band)
Number of Channels	11 for North America, and 13 for Europe
Modulation	802.11b: DQPSK, DBPSK, CCK 802.11g/n: OFDM /64-QAM, 16-QAM, QPSK, BPSK
Data Rate	802.11b: 1, 2, 5.5, 11Mbps
	802.11g: 6, 9, 12, 18, 24, 36, 48, 54Mbps
Data Rate (20MHz, normal GI, 800ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps
Data Rate (20MHz, short GI, 400ns)	802.11n: 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65, 72.2Mbps
Operating temperature	-40 to +85°C
Storage temperature	-40 to +125 °C
Humidity	Operating Humidity 10% to 95% Non-Condensing Storage Humidity 5% to 95% Non-Condensing

Receiver Performance

Receiver Performance

Parameter	Description	Minimum	Typical	Maximum	Unit
Frequency		2,412		2,472	MHz

Parameter	Description	Minimum	Typical	Maximum	Unit
Sensitivity 802.11b	1Mbps DSS		-95		dBm
	2Mbps DSS		-90		
	5.5Mbps DSS		-92		
	11Mbps DSS		-86		
Sensitivity 802.11g	6Mbps OFDM		-90		
	9Mbps OFDM		-89		
	12Mbps OFDM		-88		
	18Mbps OFDM		-85		
	24Mbps OFDM		-83		
	36Mbps OFDM		-80		
	48Mbps OFDM		-76		
	54Mbps OFDM		-74		
Sensitivity 802.11n (BW=20MHz)	MCS 0		-89		
	MCS 1		-87		
	MCS 2		-85		
	MCS 3		-82		
	MCS 4		-77		
	MCS 5		-74		
	MCS 6		-72		
	MCS 7		-70.5		
Maximum Receive Signal Level	1-11Mbps DSS		0		
	6-54Mbps OFDM		0		
	MCS 0 – 7		0		
Adjacent Channel Rejection	1Mbps DSS (30MHz offset)		50		dB
	11Mbps DSS (25MHz offset)		43		
	6Mbps OFDM (25MHz offset)		40		
	54Mbps OFDM (25MHz offset)		25		
	MCS 0 – 20MHz BW (25MHz offset)		40		
	MCS 7 – 20MHz BW (25MHz offset)		20		

Parameter	Description	Minimum	Typical	Maximum	Unit
Cellular Blocker Immunity	776-794MHz CDMA		-14		dBm
	824-849MHz GSM		-10		
	880-915MHz GSM		-10		
	1710-1785MHz GSM		-15		
	1850-1910MHz GSM		-15		
	1850-1910MHz WCDMA		-24		
	1920-1980MHz WCDMA		-24		

Transmitter Performance

Transmitter Performance

Parameter	Description	Minimum	Typical	Maximum	Unit
Frequency	—	2,412	—	2,472	MHz
Output Power ¹⁻² ON_Transmit	802.11b 1Mbps	—	17.5	—	dBm
	802.11b 11Mbps	—	18.5	—	
	802.11g 6Mbps	—	17.5	—	
	802.11g 54Mbps	—	16	—	
	802.11n MCS 0	—	17.0	—	
	802.11n MCS 7	—	14.5	—	
TX Power Accuracy	—	—	±1.5 ²	—	dB
Carrier Suppression	—	—	30.0	—	dBc
Harmonic Output Power	2nd	—		-41	dBm/MHz
	3rd	—	—	-41	

Note:

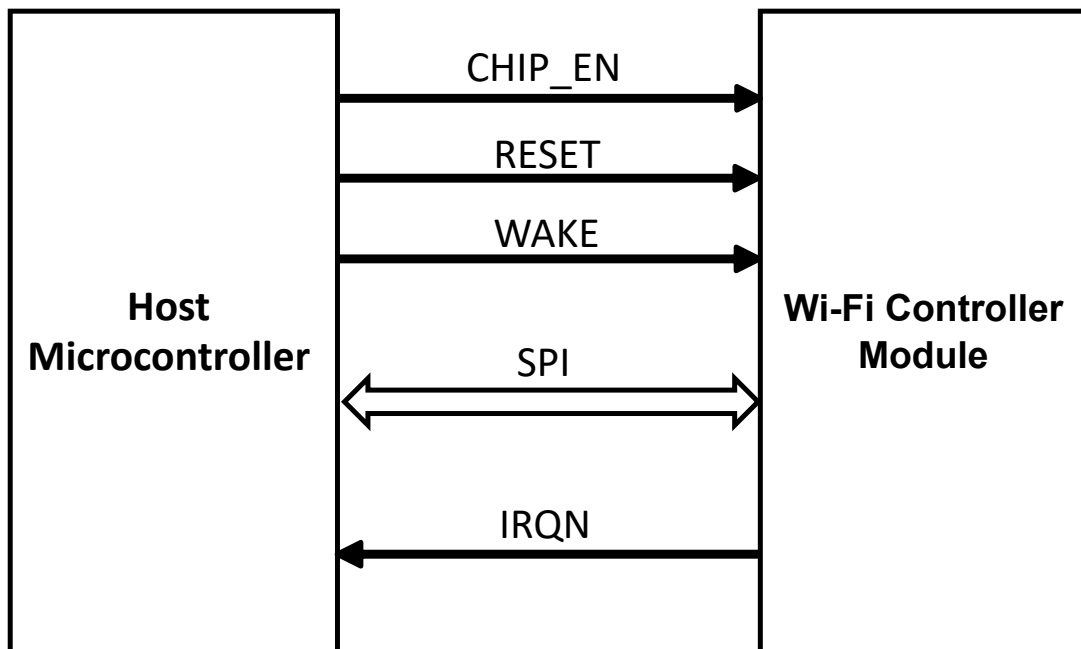
1. Measured at 802.11 spec compliant EVM/Spectral Mask.
2. Measured after RF matching network.
3. Operating temperature range is -40°C to +85°C. RF performance guaranteed at room temperature of 25°C with a 2-3dB change at boundary conditions.
4. With respect to TX power, different (higher/lower) RF output power settings may be used for specific antennas and/or enclosures, in which case recertification may be required.
5. The availability of some specific channels and/or operational frequency bands are country dependent and should be programmed at the Host product factory to match the intended destination. Regulatory bodies prohibit exposing the settings to the end user. This requirement needs to be taken care of via Host implementation.

External Interfaces

Interfacing with the Host Microcontroller

This section describes interfacing the ATWINC1510-MR210UB module with the host microcontroller. The interface is comprised of a slave SPI and additional control signals, as shown in the following figure . For more information on SPI interface specification and timing, refer to the SPI Interface. Additional control signals are connected to the GPIO/IRQ interface of the microcontroller.

Interfacing with Host Microcontroller



Host Microcontroller Interface Pins

Pin Number	Function
4	RESET_N
11	WAKE
13	IRQ_N
22	CHIP_EN
16	SPI_SSN
15	SPI_MOSI
17	SPI_MISO
18	SPI_SCK

SPI Interface

Overview

The ATWINC1510-MR210UB has a Serial Peripheral Interface (SPI) that operates as an SPI slave. The SPI interface can be used for control and for serial I/O of 802.11 data. The SPI pins are mapped as shown in the following table. The SPI is a full-duplex slave-synchronous serial interface that is available immediately following reset when pin 10 (SPI_CFG) is tied to VDDIO.

SPI Interface Pin Mapping

Pin #	SPI function
10	CFG: Must be tied to VDDIO
16	SSN: Active-Low Slave Select
15	MOSI(RXD): Serial Data Receive
18	SCK: Serial Clock
17	MISO(TXD): Serial Data Transmit

When the SPI is not selected, that is, when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the MISO line.

The SPI interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers.

The SPI SSN, MOSI, MISO, and SCK pins of the ATWINC1510-MR210UB have internal programmable pull-up resistors. These resistors should be programmed to be disabled; otherwise, if any of the SPI pins are driven to a low level while the ATWINC1510-MR210UB is in the low power sleep state, the current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module.

Related Links

SPI Timing

The SPI Slave interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in the following table and figure.

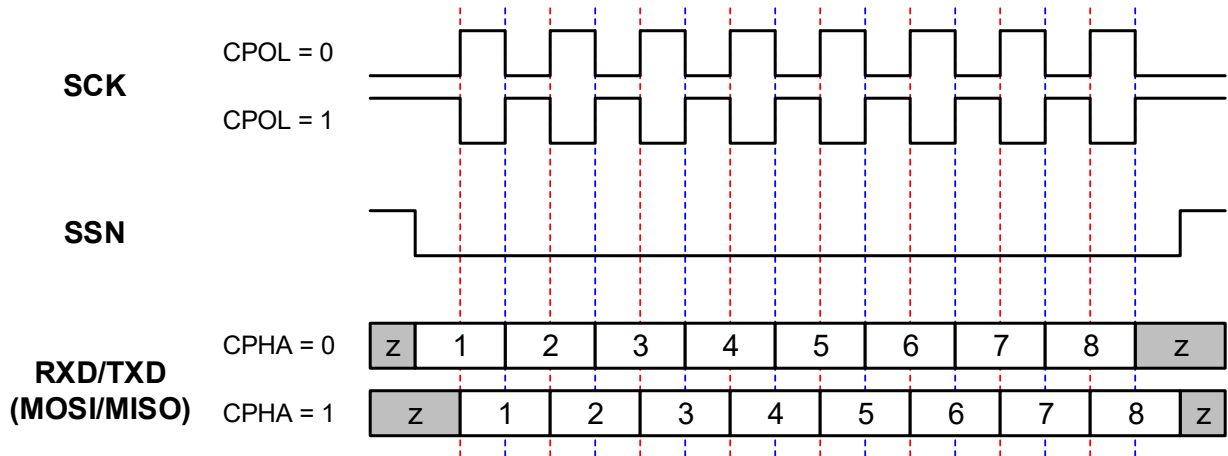
SPI Slave Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

Note: The ATWINC1510-MR210UB firmware uses “SPI MODE 0” to communicate with the host.

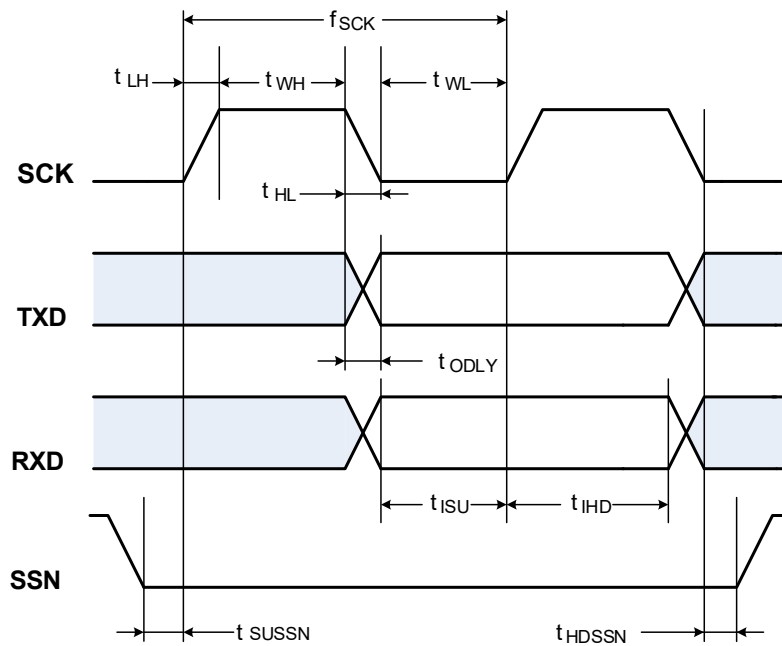
The red lines in the following figure correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

SPI Slave Clock Polarity and Clock Phase Timing



The SPI timing is provided in the following figure and table.

SPI Timing Diagram (SPI Mode CPOL=0, CPHA=0)



SPI Slave Timing Parameters¹

Parameter	Symbol	Min.	Max.	Units
Clock Input Frequency ²	f_{SCK}	—	48	MHz

Parameter	Symbol	Min.	Max.	Units
Clock Low Pulse Width	t_{WL}	4	—	ns
Clock High Pulse Width	t_{WH}	5	—	
Clock Rise Time	t_{LH}	0	7	
Clock Fall Time	t_{HL}	0	7	
TXD Output Delay ³	t_{ODLY}	4	9 from SCK fall 12.5 from SCK rise	
RXD Input Setup Time	t_{ISU}	1	—	
RXD Input Hold Time	t_{IHD}	5	—	
SSN Input Setup Time	t_{SUSSN}	3	—	
SSN Input Hold Time	t_{HDSSN}	5.5	—	

Note:

1. Timing is applicable to all SPI modes
2. Maximum clock frequency specified is limited by the SPI Slave interface internal design, actual maximum clock frequency can be lower and depends on the specific PCB layout
3. Timing based on 15pF output loading

UART Interface

The ATWINC1510-MR210UB supports the Universal Asynchronous Receiver/Transmitter (UART) interface. This interface should be used for debug purposes only. The UART is available on pins 14 and 19. The UART is compatible with the RS-232 standard, and the ATWINC1510-MR210UB operates as Data Terminal Equipment (DTE). It has a two-pin RXD/TXD interface.

The default configuration for accessing the UART interface of ATWINC1510-MR210UB is mentioned below:

- Baud rate: 115200
- Data: 8 bit
- Parity: None
- Stop bit: 1 bit
- Flow control: None

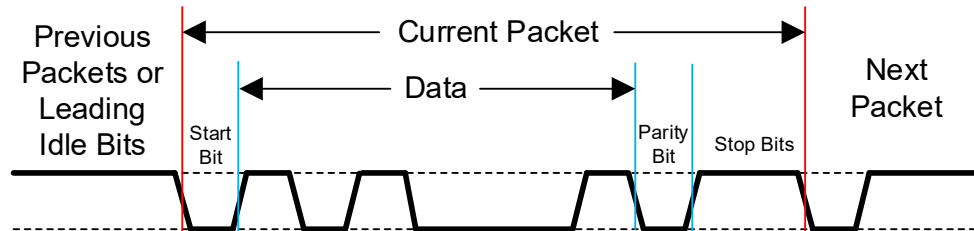
It also has RX and TX FIFOs, which ensure reliable high-speed reception and low software overhead transmission. FIFO size is 4 x 8 for both RX and TX direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well the ability to generate interrupts based on these status bits.

An example of the UART receiving or transmitting a single packet is shown in the following figure. This example shows 7-bit data (0x45), odd parity, and two stop bits.



Important: UART2 supports RTS and CTS flow control. The UART RTS and UART CTS MUST be connected to the host MCU UART and enabled for the UART interface to be functional.

Example of UART RX of TX Packet



Power Consumption

Description of Device States

The ATWINC1510-MR210UB has several device states:

- ON_Transmit – Device is actively transmitting an 802.11 signal. Highest output power and nominal current consumption.
- ON_Receive – Device is actively receiving an 802.11 signal. Lowest sensitivity and nominal current consumption.
- ON_Doze – Device is ON but is neither transmitting nor receiving
- Power_Down – Device core supply off (Leakage)
- IDLE connect – Device is connected with 1 DTIM beacon interval

The following pins are used to switch between the ON and Power_Down states:

- CHIP_EN – Device pin (pin #22) used to enable DC/DC Converter
 - VDDIO – I/O supply voltage from external supply
- In the ON states, VDDIO is on and CHIP_EN is high (at VDDIO voltage level). To switch between the ON states and Power_Down state CHIP_EN has to change between high and low (GND) voltage. When VDDIO is off and CHIP_EN is low, the chip is powered off with no leakage (also see [Restrictions for Power States](#)).

Current Consumption in Various Device States

Current Consumption

Device State	Code Rate	Output power, dBm	Current Consumption ¹	
			IVBATT	IVDDIO
ON_Transmit	802.11b 1Mbps	17.5	268mA	22mA
	802.11b 11Mbps	18.5	264mA	22mA
	802.11g 6Mbps	17.5	269mA	22mA
	802.11g 54Mbps	16.0	266mA	22mA
	802.11n MCS 0	17.0	268mA	22mA
	802.11n MCS 7	14.5	265mA	22mA
ON_Receive	802.11b 1Mbps	N/A	61mA	22mA
	802.11b 11Mbps	N/A	61mA	22mA
	802.11g 6Mbps	N/A	61mA	22mA
	802.11g 54Mbps	N/A	61mA	22mA
	802.11n MCS 0	N/A	61mA	22mA
	802.11n MCS 7	N/A	61mA	22mA

Device State	Code Rate	Output power, dBm	Current Consumption ¹	
			IVBATT	IVDDIO
ON_Doze	N/A	N/A	380μA	<10μA
Power_Down	N/A	N/A	<0.5μA	<3.5μA

Note:

1. Measured conditions: VBATT @ 3.3V, VDDIO@ 3.3V, temp. 25°C.

Restrictions for Power States

When no power is supplied to the device, for example, the DC/DC Converter output and VDDIO are both off (at ground potential), a voltage cannot be applied to the device pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when a voltage higher than one diode drop is supplied to the pin.

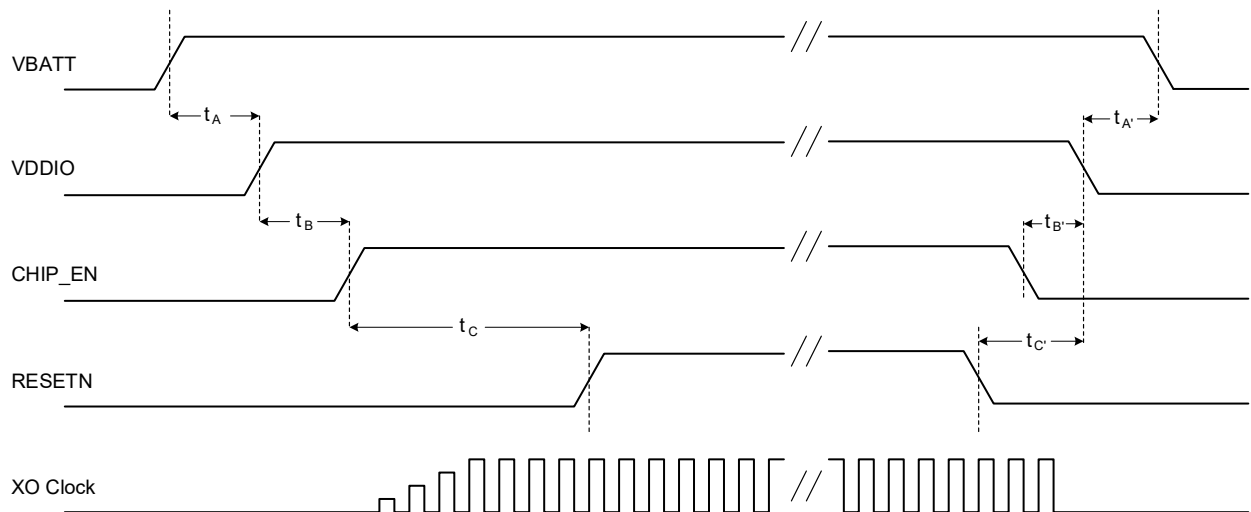
If a voltage must be applied to the signal pads while the chip is in a low-power state, the VDDIO supply must be on, so the SLEEP or Power_Down state must be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode drop below ground to any pin.

Power-up/down Sequence

The power-up/down sequence for ATWINC1510-MR210UB is shown in the Following Figure. The timing parameters are provided in following the table.

Power Up/Down Sequence



Power-up/down Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t_A	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied together. VDDIO must not rise before VBATT.
t_B	0		ms	VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating.
t_C	5		ms	CHIP_EN rise to RESETN rise	This delay is needed because the XO clock must stabilize before RESETN removal. RESETN must be driven high or low, not left floating.
$t_{A'}$	0		ms	VDDIO fall to VBATT fall	VBATT and VDDIO can fall simultaneously or can be tied together. VBATT must not fall before VDDIO.
$t_{B'}$	0		ms	CHIP_EN fall to VDDIO fall	VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN can fall simultaneously.
$t_{C'}$	0		ms	RESETN fall to VDDIO fall	VDDIO must not fall before RESETN. RESETN and CHIP_EN can fall simultaneously.

Digital I/O Pin Behavior During Power-up Sequences

The following table represents digital I/O Pin states corresponding to device power modes

.Digital I/O Pin Behavior in Different Device States

Device state	VDDIO	CHIP_EN	RESETN	Output driver	Input driver	Pull up/down resistor (96kΩ)
Power-Down: core supply off	High	Low	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-on Reset: core supply on, hard reset on	High	High	Low	Disabled (Hi-Z)	Disabled	Enabled
Power-On Default: core supply on, the device is out of reset but not programmed yet	High	High	High	Disabled (Hi-Z)	Enabled	Enabled

Device state	VDDIO	CHIP_EN	RESETN	Output driver	Input driver	Pull up/down resistor (96kΩ)
On Sleep/ On Transmit/ On Receive: core supply on, device programmed by firmware	High	High	High	Programmed by firmware for each pin: Enabled or Disabled	Opposite of Output Driver state	Programmed by firmware for each pin: Enabled or Disabled

Module Reset

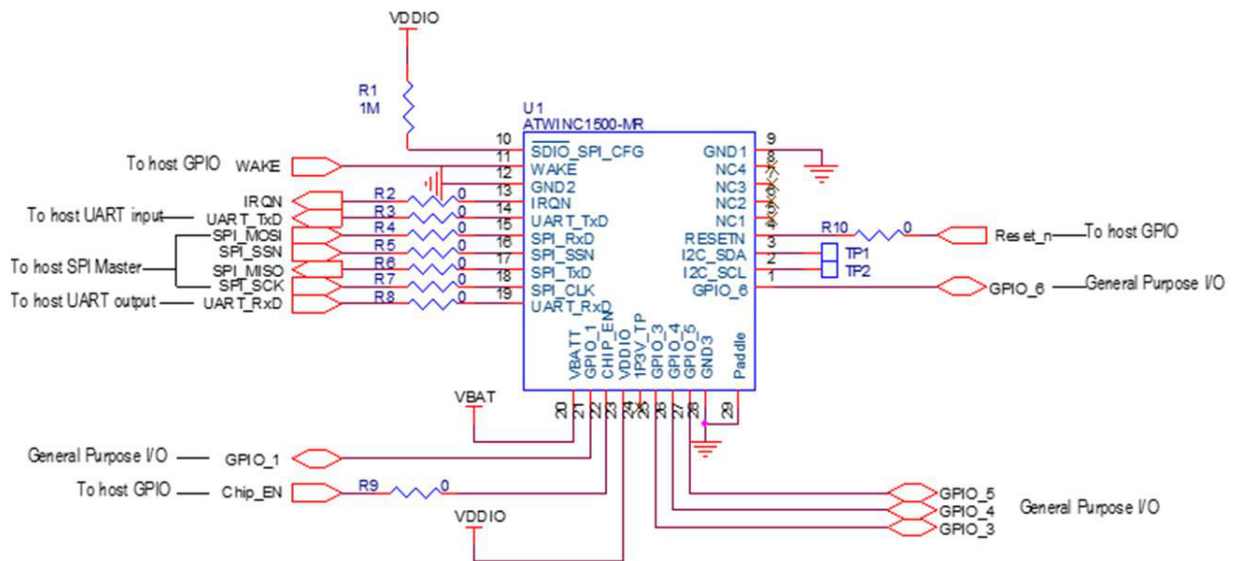
If a module reset is performed, the RESETN pin must be pulsed low for a minimum of 1μ second.

Schematic Design Information

This section provides schematic information for reference. Application schematics for SPI are provided in the following figure. Module design information such as module schematics can be obtained under an NDA from Microchip. These schematics are applicable to the ATWINC1510-MR210UB modules.

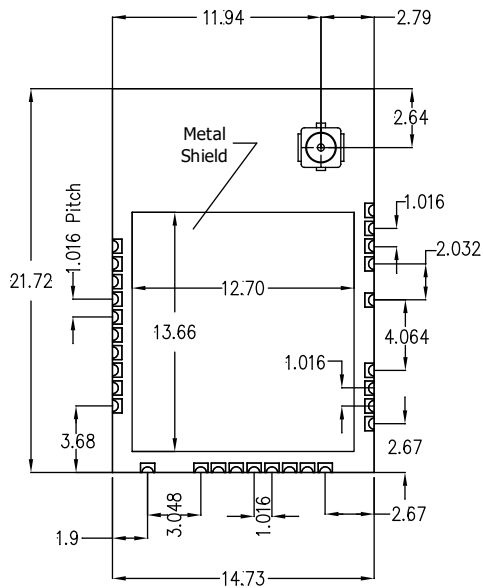
Application Schematic

SPI Application Schematic

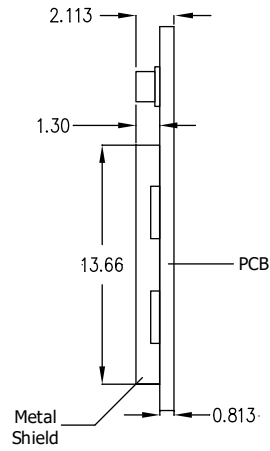


Resistors R2-R1 are recommended
As placeholders in case filtering
of noisy signals is required. They
also allow disconnecting of module
For debug purposes.

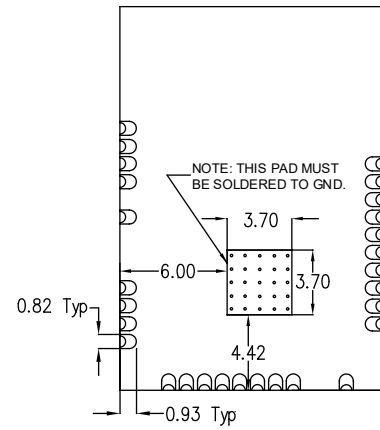
Note: Add 10uF and 0.01uF decoupling capacitors between the pin 24 (1P3V_TP) and GND.



MODULE TOP VIEW



MODULE SIDE VIEW



MODULE BOTTOM VIEW

SCALE: NOT TO SCALE	DATE: 12/04/15	Rev. 2	TITLE:
DIMENSIONAL UNIT: MM	UNTOLERANCED DIMENSIONS		WIFI MODULE uFL ANTENNA WITH LOW PROFILE SHIELD
PROJECTION UNLESS SPECIFIED			

11.1 Module Footprint

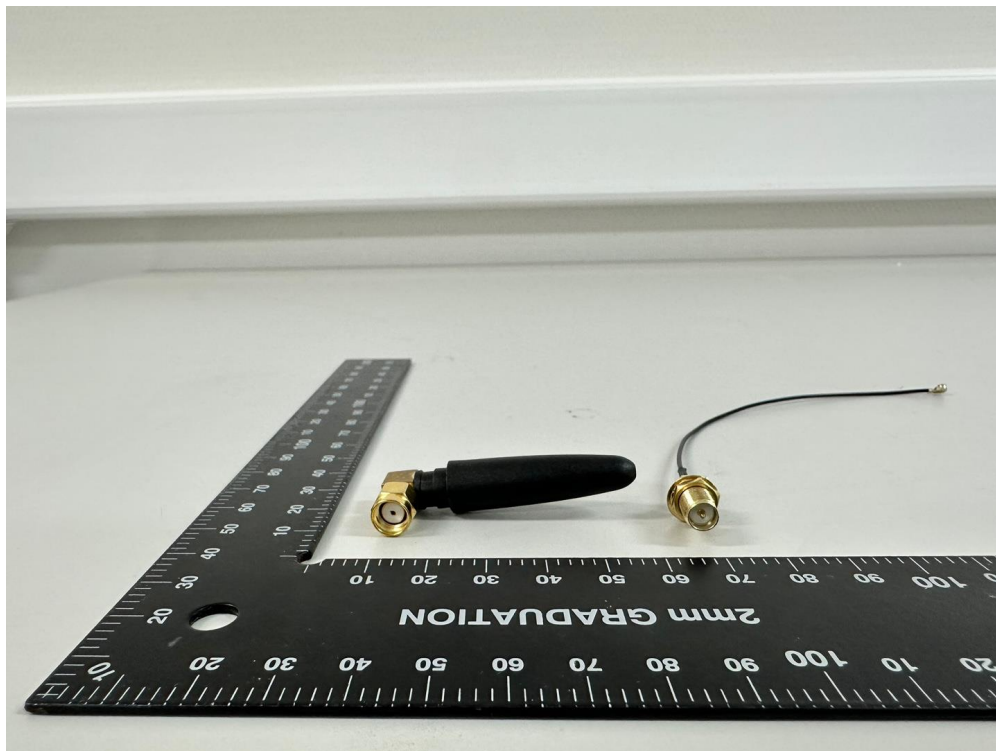
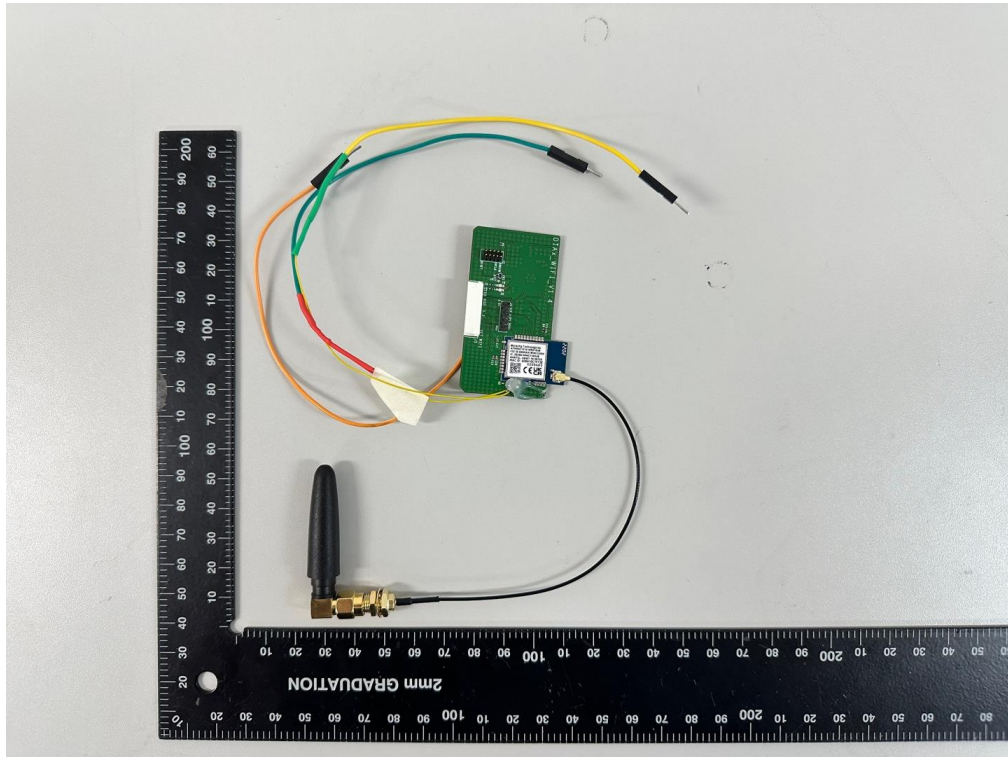
This section provides the outline drawing for the recommended footprint for the ATWINC1510-MR210UB module. It is imperative that the center Ground Pad is provided, with an array of vias to provide for a good ground and thermal transfer for the ATWINC1510-MR210UB module.

This footprint is applicable to the ATWINC1510-MR210UB module devices.

Antenna details

Dipole Antenna (Part No. TE-2402TO-C3)

The dipole antenna uses a fixed RP-SMA connector, which is considered a unique coupling method. The RP-SMA connector prevents substitution with standard SMA antennas. The antenna is not intended for user replacement.



United States

The ATWINC1510-MR210UB modules have received Federal Communications Commission (FCC) CFR 47 Telecommunications, Part 15 Subpart C “Intentional Radiators” single-modular approval in accordance with Part 15.212 Modular Transmitter approval. Single-modular transmitter approval is defined as a complete RF transmission sub-assembly, designed to be incorporated into another device, that must demonstrate compliance with FCC rules and policies independent of any host. A transmitter with a modular grant can be installed in different end-use products (referred to as a host, host product, or host device) by the grantee or other equipment manufacturer, then the host product may not require additional testing or equipment authorization for the transmitter function provided by that specific module or limited module device.

The user must comply with all of the instructions provided by the Grantee, which indicate installation and/or operating conditions necessary for compliance.

A host product itself is required to comply with all other applicable FCC equipment authorization regulations, requirements, and equipment functions that are not associated with the transmitter module portion. For example, compliance must be demonstrated: to regulations for other transmitter components within a host product; to requirements for unintentional radiators (Part 15 Subpart B), such as digital devices, computer peripherals, radio receivers, etc.; and to additional authorization requirements for the non-transmitter functions on the transmitter module (i.e., Suppliers Declaration of Conformity (SDoC) or certification) as appropriate (e.g., Bluetooth and Wi-Fi transmitter modules may also contain digital logic functions).

Labeling And User Information Requirements

The ATWINC1510- MR210UB modules have been labeled with its own FCC ID number, and if the FCC ID is not visible when the module is installed inside another device, then the outside of the finished product into which the module is installed must display a label referring to the enclosed module. This exterior label should use the following wording:
For the ATWINC1510-MR210UB

For the ATWINC1510-MR210UB:

Contains Transmitter Module FCC ID: 2BO6O-MR210UB

or

Contains FCC ID: 2BO6O-MR210UB

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

The user's manual for the finished product should include the following statement:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

Additional information on labeling and user information requirements for Part 15 devices can be found in KDB Publication 784748, which is available at the FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB) <https://apps.fcc.gov/oetcf/kdb/index.cfm>.

RF Exposure

All transmitters regulated by FCC must comply with RF exposure requirements. KDB 447498 General RF Exposure Guidance provides guidance in determining whether proposed or existing transmitting facilities, operations or devices comply with limits for human exposure to Radio Frequency (RF) fields adopted by the Federal Communications Commission (FCC).

From the FCC Grant: Output power listed is conducted. This transmitter is restricted for use with the specific antenna(s) tested in this application for Certification.

In the end product, the antenna(s) used with this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operation in conjunction with any other antenna or transmitter. User and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying the RF exposure compliance.

Helpful Web Sites

Federal Communications Commission (FCC): <http://www.fcc.gov>

FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB)
<https://apps.fcc.gov/oetcf/kdb/index.cfm>

Canada

The ATWINC1510- MR210UB modules have been certified for use in Canada under Innovation, Science, and Economic Development Canada (ISED, formerly Industry Canada) Radio Standards Procedure (RSP) RSP-100, Radio Standards Specification (RSS) RSS-Gen and RSS-247. Modular approval permits the installation of a module in a host device without the need to recertify the device.

Labeling and User Information Requirements

Labeling Requirements (from RSP-100 - Issue 11, Section 3): The host product shall be properly labeled to identify the module within the host device.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host device; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number of the module,

preceded by the word "Contains" or similar wording expressing the same meaning, as follows:

Contains IC: 33929-MR210UB

User Manual Notice for License-Exempt Radio Apparatus (from Section 8.4 RSS-Gen, Issue 4, November 2014): User manuals for license-exempt radio apparatus shall contain the following or equivalent notice in a conspicuous location in the user manual or alternatively on the device or both:

This device complies with Industry Canada's license exempt RSS standard(s). Operation is subject to the following two conditions:

- (1) This device may not cause interference, and**
- (2) This device must accept any interference, including interference that may cause undesired operation of the device.**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

- (1) l'appareil ne doit pas produire de brouillage, et**
- (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.**

Guidelines on Transmitter Antenna for License Exempt Radio Apparatus:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

This radio transmitter (identify the device by certification number, or model number if Category II) has been approved by Industry Canada to operate with the antenna types listed below with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Le présent émetteur radio (identifier le dispositif par son numéro de certification) a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés ci-dessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

RF Exposure

All transmitters regulated by Innovation, Science and Economic Development Canada (ISED) must comply with RF exposure requirements listed in RSS-102 - Radio Frequency (RF) Exposure Compliance of Radiocommunication Apparatus (All Frequency Bands).

This transmitter is restricted for use with a specific antenna tested in this application for certification, and must not be co-located or operating in conjunction with any other antenna or transmitters within a host device, except in accordance with Canada multi-transmitter product procedures.

The installation of the transmitter must ensure that the antenna has a separation distance of at least 20 cm from all persons or compliance must be demonstrated according to the ISED SAR procedures.

Helpful Web Sites

Innovation, Science and Economic Development Canada (ISED): <http://www.ic.gc.ca/>



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모델명 : WINC1510MR210UB
제조년월 : 별도표기
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