
FX095 Series Module Hardware Design

Versioning History

Version	Date	Descriptions
V1.0	2025-05-13	Initial version

XINXINZHIHUO

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution:

- Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.
- This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This device is intended only for OEM integrators under the following conditions:

- 1) The antenna must be installed such that 20 cm is maintained between the antenna and user.
- 2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed

IMPORTANT NOTE: In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “**Contains FCC ID: 2BQML2025FX095G1**”. The grantee's FCC ID can be used only when all FCC compliance requirements are met.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is authorized by the Federal Communications Commission (FCC) only for the specific rule parts (i.e., FCC transmitter rules) listed in the grant. The host product manufacturer is responsible for ensuring the host complies with any other applicable FCC rules not covered by the modular transmitter certification. If the grantee markets its product as compliant with Part 15, Subpart B (while the product also contains digital circuitry operating as unintentional radiators), the grantee must state that the final host product incorporating the modular transmitter still requires Part 15, Subpart B compliance testing.

► EU Regulatory Conformance

Hereby, We, Jiangyin Xinxinzhijie Technology Co., Ltd. declares that the radio equipment type FX095-G1 is in compliance with the Directive 2014/53/EU.

► RF exposure

A minimum separation distance of 20 cm must be maintained between the user's body and the device, including the antenna during body-worn operation to comply with the RF exposure requirements in Europe.

► Technical & accessories information

Including operating frequency band(s) and transmitting power (conducted power or limit for licensed bands and EIRP for un-licensed bands);

► Contact information (manufacturer& postal address, importer & address)

Location to indicate: on the radio equipment or its packaging or manual.

Industry Canada statement

- ❶ This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions:
 - 1) this device may not cause interference, and
 - 2) this device must accept any interference, including interference that may cause undesired operation of the device.
- ❶ Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
 - 1) l'appareil ne doit pas produire de brouillage, et
 - 2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.
- ❷ This Class B digital apparatus complies with Canadian ICES-003.
- ❷ Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.
- ❸ This device complies with RSS-310 of Industry Canada. Operation is subject to the condition that this device does not cause harmful interference.
- ❸ Cet appareil est conforme à la norme RSS-310 d'Industrie Canada. L'opération est soumise à la condition que cet appareil ne provoque aucune interférence nuisible.
- ❹ This device and its antenna(s) must not be co-located or operating in conjunction with any other antenna or transmitter, except tested built-in radios.
- ❹ Cet appareil et son antenne ne doivent pas être situés ou fonctionner en conjonction avec une autre antenne ou un autre émetteur, exception faites des radios intégrées qui ont été testées.
- ❺ The County Code Selection feature is disabled for products marketed in the US/ Canada.
- ❺ La fonction de sélection de l'indicatif du pays est désactivée pour les produits commercialisés aux États-Unis et au Canada.

Radiation Exposure Statement:

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

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1 Introduction

This document defines FX095 series module and describes its air and hardware interfaces which connect to your applications.

This document helps you quickly understand the interface specifications, electrical and mechanical details, as well as other related information of FX095 series. To facilitate application designs, it also includes some reference designs. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

2 Product Overview

2.1 General Description

FX095 is a series of embedded IoT (LTE Cat.1bis R14) wireless communication modules. It provides data connectivity on LTE Cat.1bis R14 networks.

FX095 series is an industrial-grade module for industrial and commercial applications only.

2.2 Key Features

Table 1 : Key Features of FX095 Series Module

Features	Details
Power Supply	Supply voltage: 3.4V – 4.5V Typical supply voltage: 3.8V
Support bands	LTE -FDD B1/B2/B3/B4/B5/B7/B8/B12/B13/B18/ B19/B20/B25/B26/B28/B66 LTE -TDD B34/B38/B39/B40/B41
Transmitting Power	Class 3 (23dBm $\pm$ 2dB)
Features	3GPP: Cat.1bis R14, FDD & TDD Up to: 10Mbps DL / 5Mbps UL LTE BW: 1.4/3/5/10/15/20MHz Supports Transmission Mode: 1~8 Positioning: ECID, Wi-Fi scan PSM, eDRX, CP/UP Optimization TTI Bundling, Special Subframe 9/10
Protocol	IPv4, IPv6, IPv4v6 TCP, UDP, TLS/DTLS MQTT(S), FTP(S), DHCPv4/v6, HTTP(S), DNS, NDP, CoAP, SLAAC, SNTP, LWM2M RNDIS, ECM, PPP FOTA
SMS	Text and PDU mode SMS cell broadcast SMS storage: ME by default
(U)SIM Interface	Supports 1.8 V /3V USIM/SIM card
PCM interface	PCM Interface Supports one digital audio interface
USB interface	Compliant with USB 2.0 specification (slave only)

	Supports operations at high-speed, full-speed and low-speed modes Used for AT command communication, data transmission, software debugging and firmware upgrade Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–6.5, Android 4.x–13.x
UART	Used for data transmission and AT command communication 115200 bps by default The default frame format is 8N1 (8 data bits, no parity, 1 stop bit) Supports RTS and CTS hardware flow control Debug UART: Used for software debugging and log output Supports 2880000 bps
AT commands	3GPP TS 27.007 and 3GPP TS 27.005 AT commands. Xinxinzhijie enhanced AT commands
Antenna interface	Main antenna interface (ANT_MAIN)
Physical characteristics	Dimensions: (23.6±0.2) mm x (19.9±0.2) mm x (2.6±0.2) mm
Temperature Range	Operation temperature: -35 to +75 °C Extended temperature: -40 to +85 °C Storage temperature: -40 to +90 °C
Firmware Upgrade	USB interface, FOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3 Functional Diagram

The following figures show the block diagram of FX095 series and the major functional parts.

- Power management
- Baseband
- Radio frequency
- Peripheral interfaces

NOTE:

eSIM function is optional. If eSIM is selected, then any external (U)SIM card cannot be used simultaneously.*

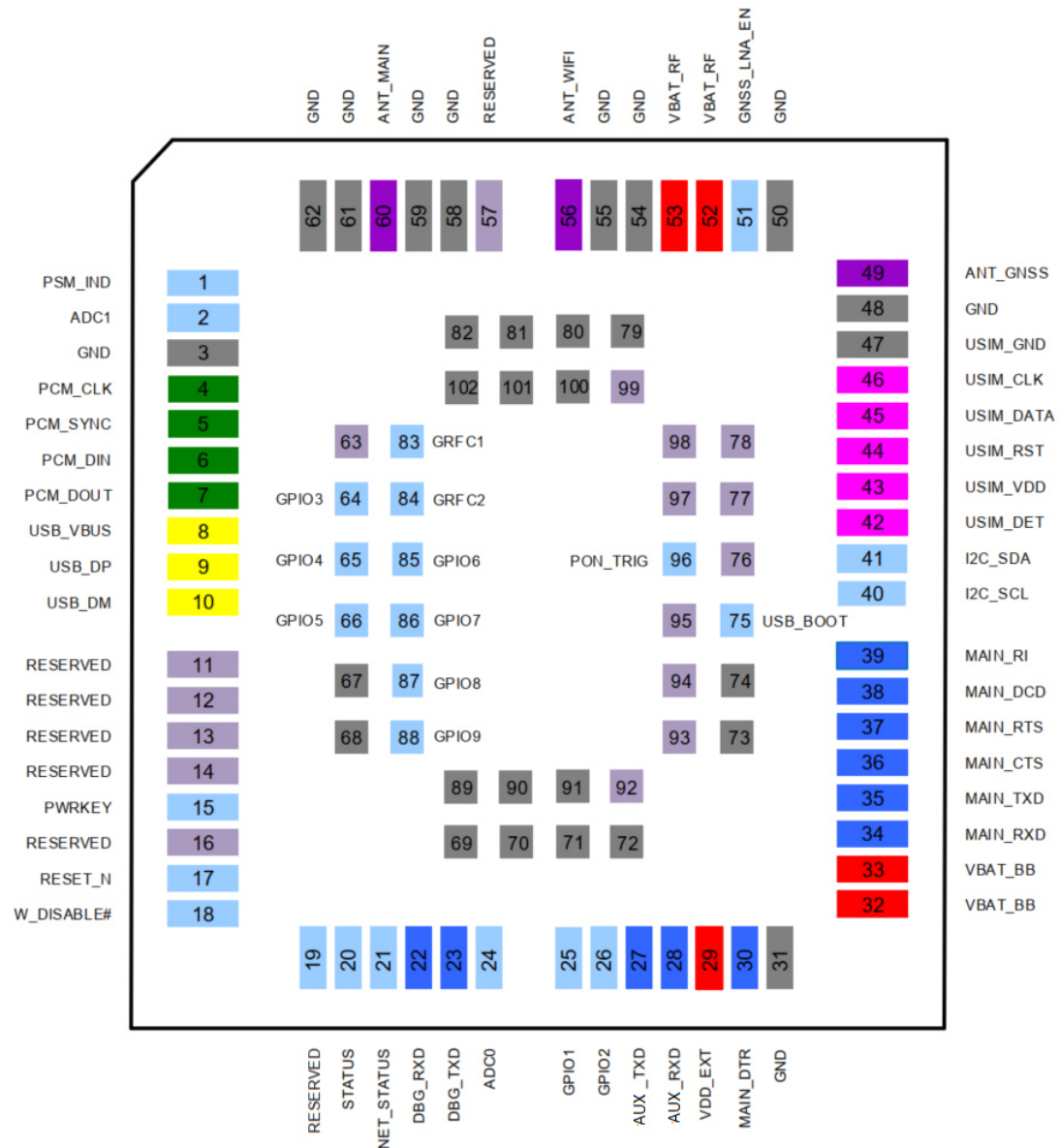
The output voltage of PWRKEY is 2.2 V because of the voltage drop inside the chipset.

3 Application Interfaces

FX095 series is designed with 102 LGA pins for connection to various cellular application platforms. The subsequent chapters describe the interfaces listed below in detail:

- Power supply
- PON_TRIG Interface
- (U)SIM interface
- USB interface
- UART
- PCM and I2C interfaces
- Status indication interfaces
- MAIN_RI
- USB_BOOT
- ADC interfaces
- GPIO interfaces
- GRFC interfaces

3.1 Pin Assignment



NOTE

- The output voltage of PWRKEY is 2.2 V because of the voltage drop inside the chipset.
- Keep all RESERVED and unused pins unconnected.
- Connect GND pins to the ground in the design.

3.2 Pin Description

Table 2: Definition of I/O Parameters

Type	Description
AI	Analog Input
AO	Analog Output

AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

Table 3: Pin Description

Power Supply					
Pin Name	Pin No.	I/O	Description	DC	Comment
VBAT_BB	32,33	PI	Power supply for the module's baseband part.	Vmax=4.5V Vmin=3.4V Vnom=3.8V	
VDD_EXT	29	PO	Provides 1.9V for external circuits.	Vnom=1.9V Iomax=50mA	If not used, keep this pin open.
GND	3,31,47,48,50,54,55,58,59,61,62,67-74,79-82,89-91,100-102				
Turn-on/Turn-off the Module					
Pin Name	Pin No.	I/O	Description	DC	Comment
PWRKEY	15	DI	Turn on/off the module.	Vnom=2.2V Vilmax=0.38V	Never pull down PWRKEY to GND permanently. The output voltage is 1.5V because of the voltage drop inside the chipset.
Reset the Module					
Pin Name	Pin No.	I/O	Description	DC	Comment
RESET_N	17	DI	Reset the module	Vnom=1.4V Vilmax=0.38V	Multiplexed from PWRKEY(connects directly to PWRKEY inside the module). If not used, keep this pin open.
Status Indication Interface					
Pin Name	Pin No.	I/O	Description	DC	Comment
PSM_IND	1	DO	Indicate the module's power saving	Vohmin=1.35V Volmax=0.45V	1.8V power domain. If not used, keep

			mode.		these pins open.
STATUS	20	DO	Indicate the module's operation status.		
NET_STATUS	21	DO	Indicate the module's network activity status.		
PON_TRIG Interface					
Pin Name	Pin No.	I/O	Description	DC	Comment
PON_TRIG	96	DI	Wake up the module from PSM.		1.8V power domain. Rising edge triggered. Pulled-down by default. If not used, keep it open.
USB Interface					
Pin Name	Pin No.	I/O	Description	DC	Comment
USB_VBUS	8	AI	USB connention detect.	Vmax=5.25V Vmin=4.0V Vnom=5.0V	Typical 5.0V
USB_DP	9	AIO	USB differential data (+).		Compliant with USB 2.0 standard specification. Require differential impedance of 90 Ω
USB_DM	10	AIO	USB differential data (-).		
(U)SIM Interface					
Pin Name	Pin No.	I/O	Description	DC	Comment
USIM_DET	42	DI	(U)SIM card hot-plug detect.	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	1.8V/3.0V power domain. If not used, keep open.
USIM_VDD	43	PO	(U)SIM card power supply.	1.8V/3.0V	
USIM_RST	44	DO	(U)SIM card reset	VOLmax=0.45V VOHmin=0.8*USIM_VDD	
USIM_DATA	45	DIO	(U)SIM card data.	VILmin=-0.3V VILmax=0.6V VIHmin=0.7*USIM_VDD VIHmax=USIM_VDD	

				VOLmax=0.45V VOHmin=0.8*USIM_VDD	
USIM_CLK	46	DO	(U)SIM card clock	VOLmax=0.45V VOHmin=0.8*USIM_VDD	
Main UART					
Pin Name	Pin No.	I/O	Description	DC	Comment
MAIN_DTR	30	DI	Main UART data terminal ready	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	1.8V power domain. If not used, keep open.
MAIN_RXD	34	DI	Main UART receive		
MAIN_TXD	35	DO	Main UART transmit	VOLmax=0.45V VOHmin=1.35V	1.8V power domain. If not used, keep open.
MAIN_CTS	36	DO	Clear to send signal from the module.		Connect to the MCU's CTS. 1.8V power domain. If not used, keep open.
MAIN_RTS	37	DI	Request to send signal to the module.	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	Connect to the MCU's RTS. 1.8V power domain. If not used, keep open.
MAIN_DCD	38	DO	Main UART data carrier detect.	VOLmax=0.45V VOHmin=1.35V	1.8V power domain. If not used, keep open.
MAIN_RI	39	DO	Main UART ring indication.		
Debug UART					
Pin Name	Pin No.	I/O	Description	DC	Comment
DBG_RXD	22	DI	Debug UART receive.	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	1.8V power domain. If not used, keep open.
DBG_TXD	23	DO	Debug UART transmit.	VOLmax=0.45V VOHmin=1.35V	
Aux UART					
Pin Name	Pin No.	I/O	Description	DC	Comment
AUX_TXD	27	DO	Aux UART transmit.	VOLmax=0.45V VOHmin=1.35V	1.8V power domain. If not used, keep open.
AUX_RXD	28	DI	Aux UART receive.	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	

PCM Interface					
Pin Name	Pin No.	I/O	Description	DC	Comment
PCM_CLK	4	DO	PCM clock	VOLmax=0.45V VOHmin=1.35V	1.8V power domain. If not used, keep these pins open.
PCM_SYNC	5	DO	PCM data frame sync		
PCM_DIN	6	DI	PCM data input	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	
PCM_DOUT	7	DO	PCM data output	VOLmax=0.45V VOHmin=1.35V	
I2C Interface					
Pin Name	Pin No.	I/O	Description	DC	Comment
I2C_SCL	40	OD	I2C serial clock (for external codec)		External pull-up resistor is required. 1.8V only.
I2C_SDA	41	OD	I2C serial data (for external codec)		If not used, keep this pin open.
Antenna Interface					
Pin Name	Pin No.	I/O	Description	DC	Comment
ANT_MAIN	60	AIO	Main antenna interface.		50Ω impedance
GPIO Interface					
Pin Name	Pin No.	I/O	Description	DC	Comment
GPIO1	25	DIO	General purpose input/output	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V VOLmax=0.45V VOHmin=1.35V	1.8V power domain. If not used, keep these pins open.
GPIO2	26				
GPIO3	64				
GPIO4	65				
GPIO5	66				
GPIO6	85				
GPIO7	86				
GPIO8	87				
GPIO9	88				
ADC Interface					
Pin Name	Pin No.	I/O	Description	DC	Comment
ADC0	24	AI	General purpose ADC interface.	Voltage range: 0 – 1.5V	If not used, keep these pins open.
ADC1	2	AI			

Other Interface					
Pin Name	Pin No.	I/O	Description	DC	Comment
W_DISABLE#	18	DI	Airplane mode control.	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	1.8V power domain. Pulled up by default. When it is in low voltage level, the module can enter airplane mode. If unused, keep this pin open.
USB_BOOT	75	DI	Force the module into emergency download mode.		1.8V power domain
GRFC Interface					
Pin Name	Pin No.	I/O	Description	DC	Comment
GRFC1	83	DO			
GRFC2	84	DO			
RESERVED Pins					
Pin Name	Pin No.				Comment
RESERVED	11-14,16,19,49,56,57, 63, 76-78, 92-95, 97-99				Keep these pins open.

3.3 Operating Modes

Table 4: Operating Modes of FX095 Series Module

Mode	Details
Full Functionality Mode	Connected: The module connects to network. Its power consumption varies with the network setting and data transfer rate.
	Idle: The module remains registered on network, and is ready to send and receive data. In this mode, the software is active.
Airplane Mode	AT+CFUN=4 or W_DISABLE# pin can set the module into airplane mode where the RF function is invalid
Minimum Functionality Mode	AT+CFUN=0 can set the module into a minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.
Sleep Mode	The module remains the ability to receive paging message, SMS and TCP/UDP data from the network normally. In this mode, the power consumption reduces to a low level
Power OFF Mode	The module's power supply is shut down by its power management unit. In this mode, the software is inactive, the serial interfaces are inaccessible, while the operating voltage (connected to VBAT) remains applied
Power Saving	PSM is similar to power-off, but the module remains registered on the

Mode (PSM)	network and there is no need to re-attach or re-establish PDN connections. The power consumption reduces to a minimized level
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NOTE: During e-I-DRX, it is recommended to use UART for data communication, as the use of USB interface increases power consumption

3.4 Power Saving

3.4.1 Airplane Mode

When the module enters airplane mode, the RF function does not work, and all AT commands correlative with RF function are inaccessible. This mode can be set via the following methods.

Software:

AT+CFUN=<fun> provides choice of the functionality level via setting <fun> to 0, 1 or 4.

AT+CFUN=0: Minimum functionality mode. Both (U)SIM and RF functions are disabled.

AT+CFUN=1: Full functionality mode (by default).

AT+CFUN=4: Airplane mode. RF function is disabled.

3.4.2 Power Saving Mode (PSM)

The module minimizes its power consumption through entering PSM. PSM mode is similar to power-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections. Therefore, the module in PSM cannot immediately respond to your requests.

When the module wants to use the PSM, it shall request an Active Time value during every Attach and TAU procedures. If the network supports PSM and accepts that the module uses PSM, the network confirms usage of PSM by allocating an Active Time value to the module. If the module wants to change the Active Time value, e.g., the module requests the value it wants in the TAU procedure.

If PSM is supported by the network, then it can be enabled via **AT+CPSMS**.

Any of the following methods can wake up the module from PSM:

- Wake up the module from PSM through a rising edge on PON_TRIG. (Recommended)
- Wake up the module by driving PWRKEY low.
- When the TAU timer expires, the module wakes up from PSM automatically.

3.4.3 Sleep Mode

The module reduces its current consumption to a low level during sleep mode. The following sub-chapters describe the power saving procedure of the module.

UART Application

If the MCU communicates with the module via UART, the following preconditions enable the module to enter sleep mode.

- Execute 'AT+QSClk=1' to enable sleep mode.
- Drive MAIN_DTR high.
- When the module has a URC to report, MAIN_RI will wake up the MCU.
- Driving MAIN_DTR low will wake up the module.

The following figure shows the connection between the module and the MCU.

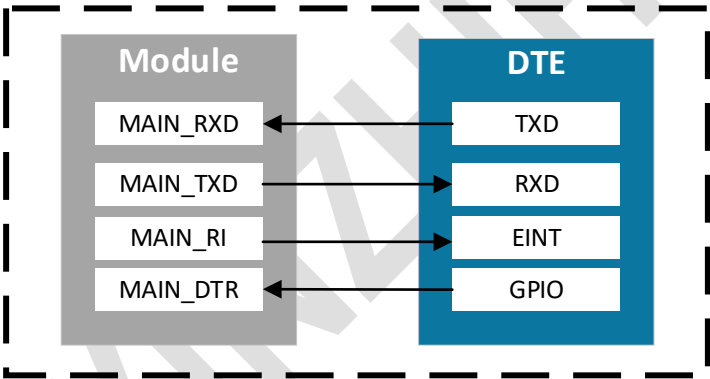


Figure 1: Sleep Mode Application via UART

3.5 Power Supply

3.5.1 Power Supply Pins

FX095 series provides the following four VBAT pins for connection with an external power supply.

Two VBAT pins for the module's baseband part.

Table 5: VBAT and GND Pins

Pin Name	Pin No.	IO	Description	Min.	Typ.	Max.	Unit
VBAT	32,33	PI	Power supply for the module's baseband part,	3.4	3.8	4.5	V
GND	3,31,47,48,50,54,55,58,59,61,62,67-74,79-82,89-91,100-102						

3.5.2 Voltage Stability Requirements

The power supply range of FX095 is 3.4–4.5 V. For every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should be higher than 3.4 V. After the module starts up normally, the minimum safety voltage is 3.4V. To ensure full functionality mode, the minimum power supply voltage should be higher than 3.4V. Make sure that the input voltage never drops below 3.4 V.

To decrease voltage-drop, bypass capacitors of about 100 μF with low ESR should be used, and multi-layer ceramic chip capacitor (MLCC) arrays should also be reserved due to their low ESR. Use five ceramic capacitors (220uF, 220uF, 10uF, 100nF, 33pF) to compose the MLCC array for VBAT, and place these capacitors close to VBAT pins. The main power supply from an external application has to be a single voltage source. The width of VBAT trace should be not less than 2.0 mm. The longer the VBAT trace is, the wider it should be.

To get a stable power source, it is suggested to use one TVS components with low leakage current and suitable reverse stand-off voltage, and it is recommended to place them as close as possible to the VBAT pins.

In addition, route VBAT in inner-layer of the PCB, and place a ferrite bead as close to VBAT_BB as possible. Follow the criteria below for ferrite bead selection:

- Current rating ≥ 600 mA and low DC resistance to avoid voltage drop during instantaneous high power consumption.
- $\geq 800 \Omega$ impedance @ 700–960 MHz.

The following figure shows the star structure of the power supply.

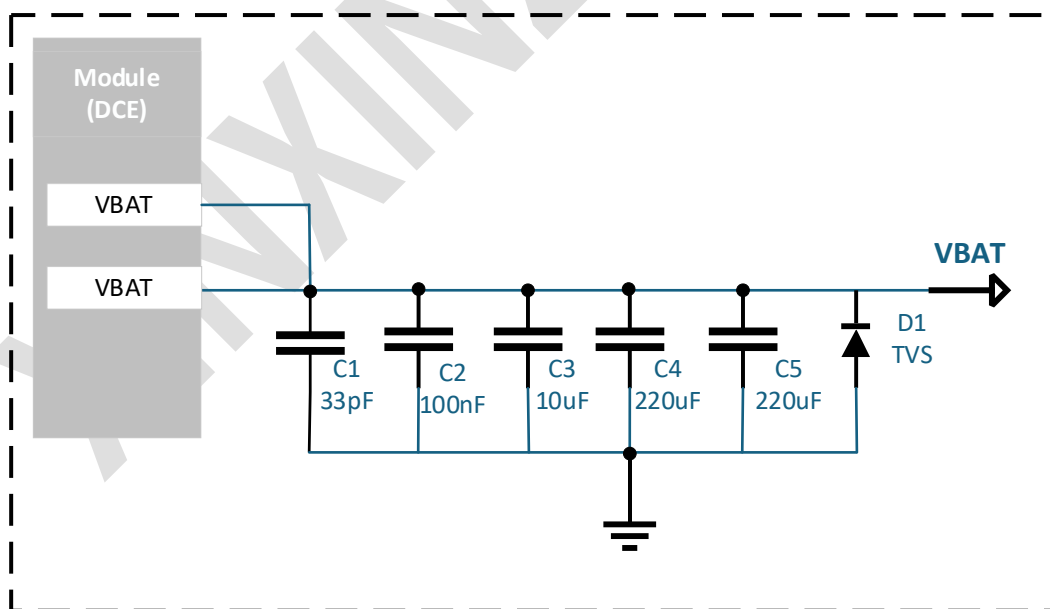


Figure 2: Star Structure of the Power Supply

If LTE Cat 1 networks are all used, the current output of DC-DC converter chip or LDO chip should exceed 2.0 A and power supply chips with low leakage current should be adopted because the module needs higher current in LTE CAT1 network data transmission.

3.6 Turn On and Turn Off

3.6.1 Turn On with PWRKEY

Table 6 : Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turn on/off the module	Never pull down PWRKY to GND permanently. The output voltage is 2.2V because of the voltage drop inside the chipset.

The module can be turned on by driving PWRKEY low for 520–3520 ms, and default time is 520 ms. It is recommended to use an open drain/collector driver to control the PWRKEY.

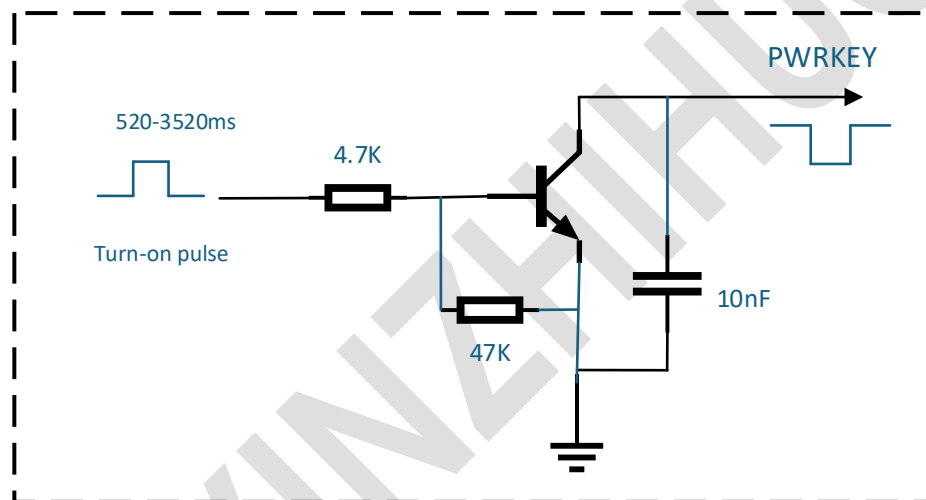


Figure 3 : Turn On the Module with a Driver Circuit

Another way to control the PWRKEY is using a push button. As electrostatic strike may be generated from the finger touching when the button is pressed, a TVS component is indispensable to be placed near the button for ESD protection. A reference circuit is illustrated in the following figure.

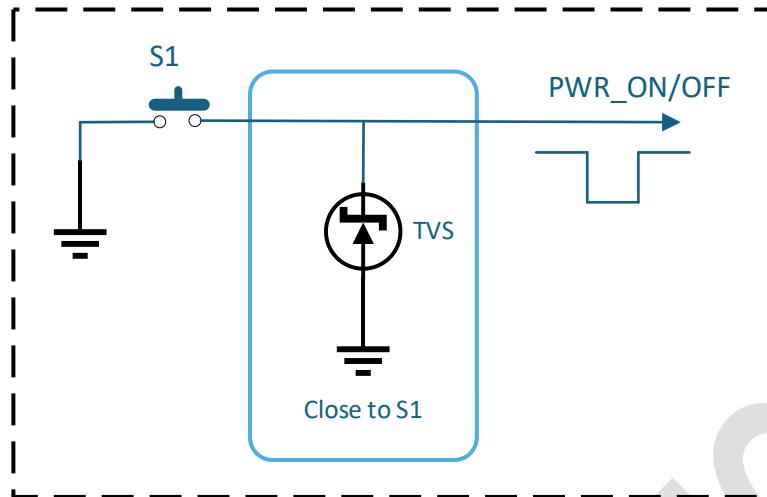


Figure 4 : Turn On the Module with a Push Button同上

3.6.2 Turn Off

Either of the following methods can be used to turn off the module:

- with PWRKEY
- with **AT+QPOWD**

Turn Off with PWRKEY

Driving PWRKEY low for 1s -7s (default value is 1s) and then releasing it, the module will execute power-down procedure.

Turn Off with AT Command

It is also a safe way to execute **AT+QPOWD** to turn off the module, which is similar to turning off the module with PWRKEY.

NOTE:

To avoid corrupting the data in the internal flash, do not switch off the power supply when the module is working. Only after the module is shut down with PWRKEY, fast shutdown function or AT command can the power supply be cut off.

While turning off the module with AT command, keep PWRKEY at high level after the execution of turn-off command, otherwise the module will be turned on again after it turns off.

It is recommended to judge whether the module has been shut down based on the state of STATUS.

3.7 Reset

RESET_N works to reset the module. Due to platform limitations.

Table 7 : Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description
RESET_N	17	DI	Reset the module

The module can be reset by driving RESET_N low for 32 ms–2048 ms, and default 512 ms.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or a button can be used to control RESET_N.

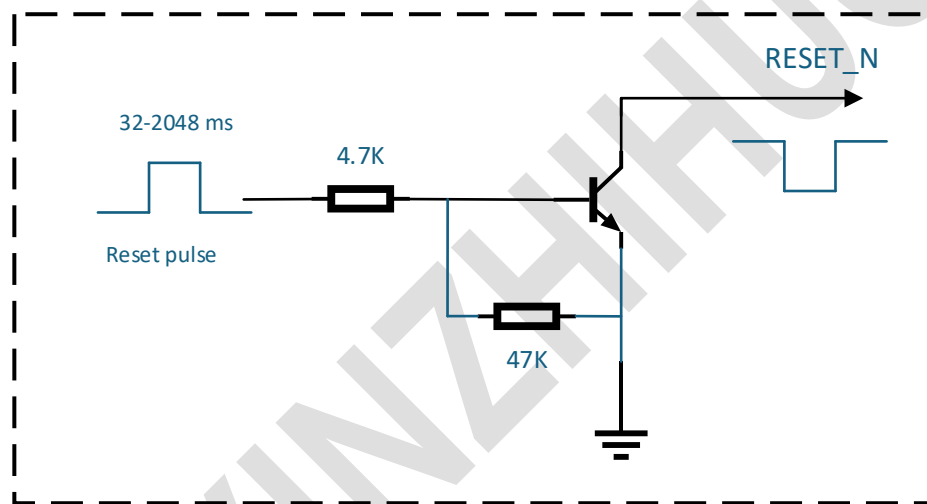


Figure 5 : Reference Design of RESET_N with a Driver Circuit

Another way to control the RESET_N is to use a push button.

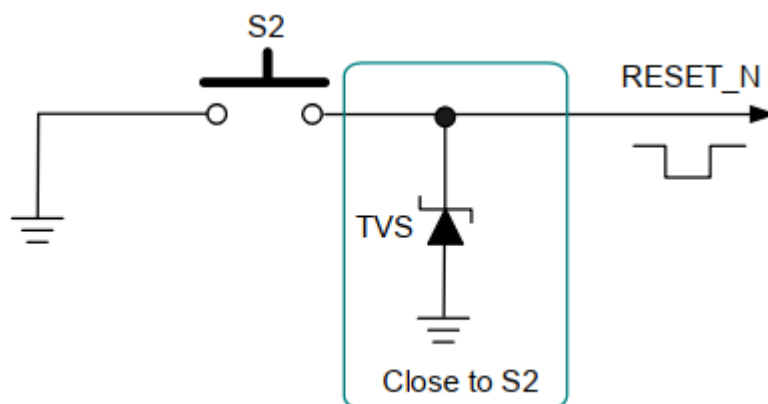


Figure 6 : Reference Design of RESET_N with a Push Button

NOTE: Ensure that there is no large capacitance on RESET_N.

3.8 PON_TRIG Interface

The module provides one PON_TRIG pin which is used to wake up the module from PSM. When the pin detects a rising edge and keeps at high level for at least 30 ms, the module wakes up from PSM.

Table 8 : Pin Definition of PON_TRIG Interface

Pin Name	Pin No.	I/O	Description	Comment
PON_TRIG	96	DI	Wake up the module from PSM	Rising-edge triggered. If unused, keep this pin open.

3.9 (U)SIM Interface

The module supports 1.8V/3V (U)SIM card. The (U)SIM interface circuit meets ETSI and IMT-2000 requirements.

Table 9 : Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_DET	42	DI	(U)SIM card hot-plug detect.	1.8 V power domain. If unused, keep this pin open.
USIM_VDD	43	PO	(U)SIM card power supply	1.8 V/3V (U)SIM card is supported.
USIM_RST	44	DO	(U)SIM card reset	1.8 V/3V power domain.
USIM_DATA	45	DIO	(U)SIM card data	
USIM_CLK	46	DO	(U)SIM card clock	

The module supports (U)SIM card hot-plug via the USIM_DET pin, and both high-level and low-level detections are supported. The function is disabled by default, and see **AT+QSIMDET** command.

If (U)SIM card detection function is not needed, keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

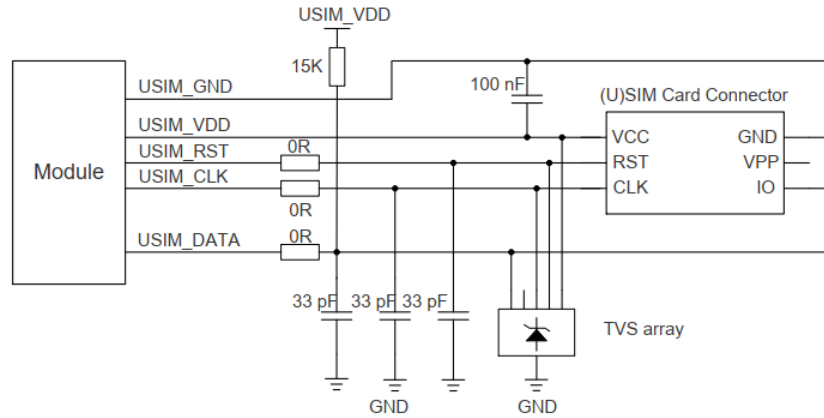


Figure 7 : Reference Design of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in (U)SIM circuit design:

- Keep the placement of (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and power supply traces.
- Assure the ground trace between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD not less than 0.5 mm to maintain the same electric potential. Make sure the bypass capacitor between USIM_VDD and USIM_GND is less than 1 μ F, and place it as close to (U)SIM card connector as possible. If the system ground plane is complete, USIM_GND can be connected to the system ground directly.
- To avoid crosstalk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground. USIM_RST should also be surrounded with ground.
- To offer good ESD protection, it is recommended to add a TVS array with parasitic capacitance not exceeding 15 pF. To facilitate debugging, it is recommended to reserve series resistors for the (U)SIM signals of the module. The 33 pF capacitors are used for RF filtering interference. Note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

NOTE:

eSIM function is optional. If eSIM is selected, then the external (U)SIM card cannot be used simultaneously.*

3.10 USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with

the USB 2.0 specification and supports operation at low-speed (1.5 Mbps), full-speed (12 Mbps) and high-speed (480 Mbps) modes.

The USB interface is used for AT command communication, data transmission, software debugging and firmware upgrade. The following table shows the pin definition of USB interface.

Table 10 : Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	Typical 5.0 V
USB_DP	9	AIO	USB differential data (+)	Require differential impedance of 90 Ω .
USB_DM	10	AIO	USB differential data (-)	
GND	3		Ground	

For more details about USB 2.0 specification, visit <https://www.usb.org/home>.

The USB interface is recommended to be reserved for firmware upgrade and software debugging in application designs. The following figure shows a reference design of USB interface.

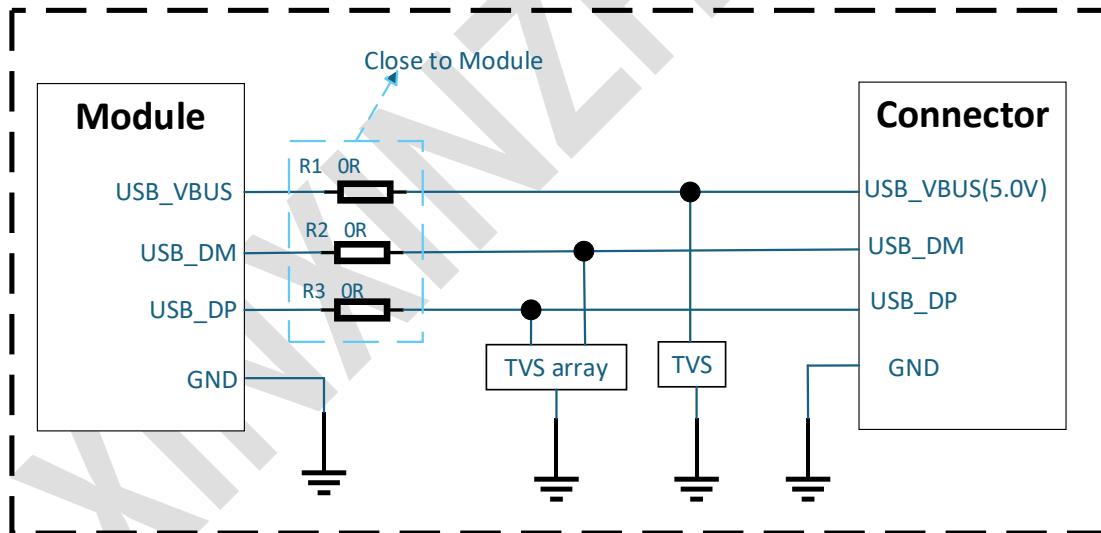


Figure 8 : Reference Design of USB Interface

To ensure the integrity of USB data trace signal, resistors should be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

To meet USB 2.0 specification, comply with the following principles while designing the USB interface.

- It is important to route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω .
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces.

It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.

- Junction capacitance of the ESD protection components might cause influences on USB data traces, so pay attention to the selection of the components. Typically, the stray capacitance should be less than 2 pF.
- Keep TVS components as close to the USB connector as possible.

NOTE: The USB interface supports slave mode only.

3.11 UART

The module provides three UART: the main UART, debug UART. Their features are outlined below:

- The main UART supports 4800, 9600, 14400, 19200, 28800, 38400, 57600, 115200, 230400, 460800 and 921600,1000000 bps baud rates, and the default baud rate is 115200 bps. It is used for data transmission and AT command communication, and supports RTS and CTS hardware flow control. The default frame format is 8N1 (8 data bits, no parity, 1 stop bit).
- The debug UART supports a fixed baud rate of 2880000 bps, and is used for software debugging and log output.

Table 11 : Pin Definition of Main UART

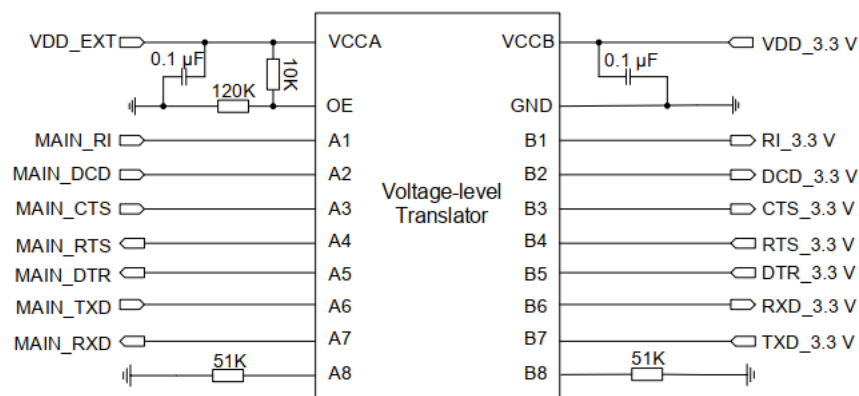
Pin Name	Pin No.	I/O	Description	DC	Comment
MAIN_DTR	30	DI	Main UART data terminal ready	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	1.8V power domain. If not used, keep open.
MAIN_RXD	34	DI	Main UART receive		
MAIN_TXD	35	DO	Main UART transmit	VOLmax=0.45V VOHmin=1.35V	1.8V power domain. If not used, keep open. Connect to the MCU's CTS. 1.8V power domain. If not used, keep open.
MAIN_CTS	36	DO	Clear to send signal from the module.		
MAIN_RTS	37	DI	Request to send signal to the module.	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	Connect to the MCU's RTS. 1.8V power domain. If not used, keep open.
MAIN_DCD	38	DO	Main UART data carrier detect.	VOLmax=0.45V VOHmin=1.35V	1.8V power domain. If not used, keep open.
MAIN_RI	39	DO	Main UART ring indication.		

Note: *AT+IPR* can be used to set the baud rate of the main UART, and *AT+IFC* can be used to enable/disable the hardware flow control (the function is disabled by default).

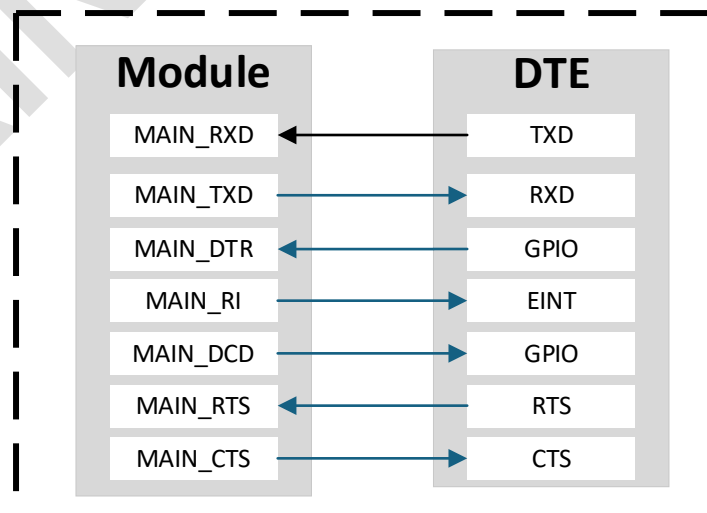
Table 12 : Pin Definition of Debug UART

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	22	DI	Debug UART receive	1.8 V power domain. If unused, keep these pins open.
DBG_TXD	23	DO	Debug UART transmit	

The module provides 1.8 V UART. A voltage-level translator should be used if your application is equipped with a 3.3 V UART. The voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended.



Another example with transistor translation circuit is shown as below. For the design of circuits shown in dotted lines, refer to the solid lines, but pay attention to the direction of connection.



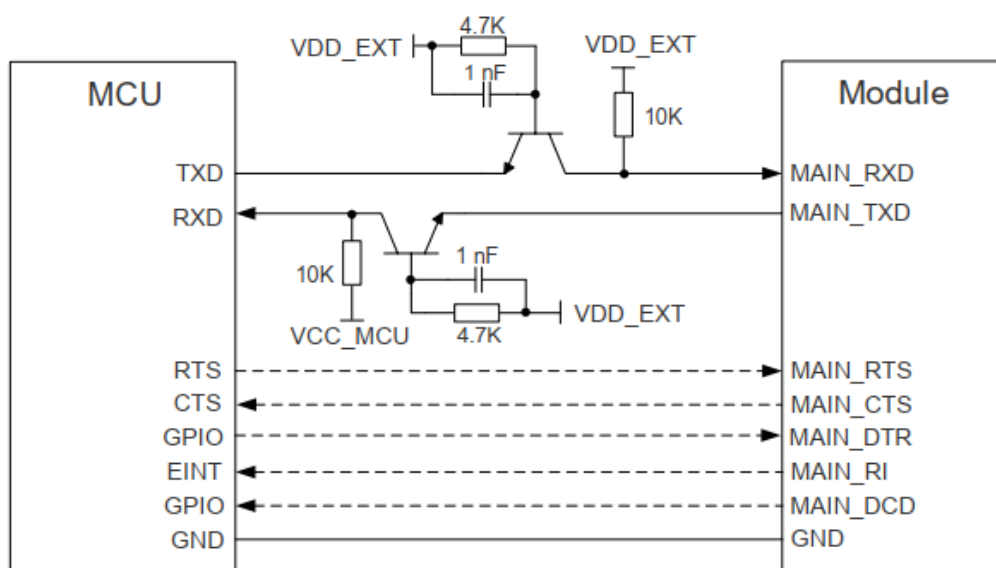


Figure 9 : Main UART Reference Design (Transistor Solution)

Note:

1. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.
2. The level shifting circuit of debug UART is similar to main UART.

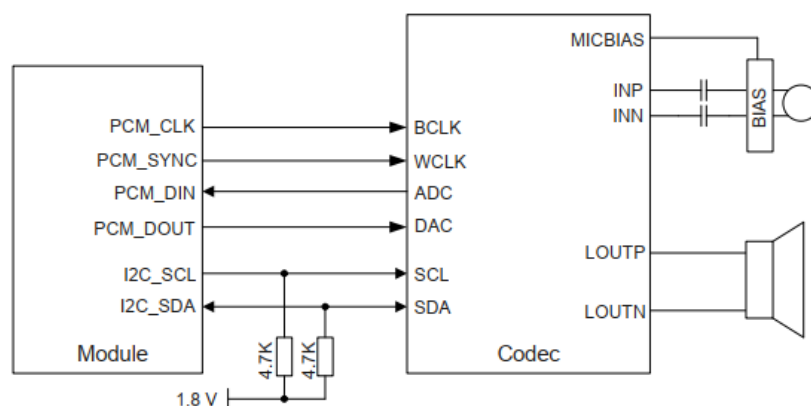
3.12 PCM and I2C Interfaces

The module provides one Pulse Code Modulation (PCM) digital interface and one inter-integrated circuit (I2C) interface which are used for audio recording and replaying application.

The following table shows the pin definition of the two interfaces which can be applied to audio codec design.

Table 13 : Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_CLK	4	DO	PCM clock	1.8 V power domain. If unused, keep these pins open.
PCM_SYNC	5	DO	PCM data frame sync	
PCM_DIN	6	DI	PCM data input	
PCM_DOUT	7	DO	PCM data output	
I2C_SCL	40	OD	I2C serial clock (for external codec).	External pull-up resistors are required. 1.8 V only. If unused, keep these pins open
I2C_SDA	41	OD	I2C serial data (for external codec).	



3.13 NET_STATUS*

This function is temporarily not supported during the development process.

3.14 STATUS*

This function is temporarily not supported during the development process.

3.15 USB_BOOT

FX095 series provides a USB_BOOT pin. During development or factory production, USB_BOOT can force the module to boot from USB interface for firmware upgrade.

Table 14 : Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module into emergency download mode.	1.8 V power domain. Active high. If not used, keep this pin open.

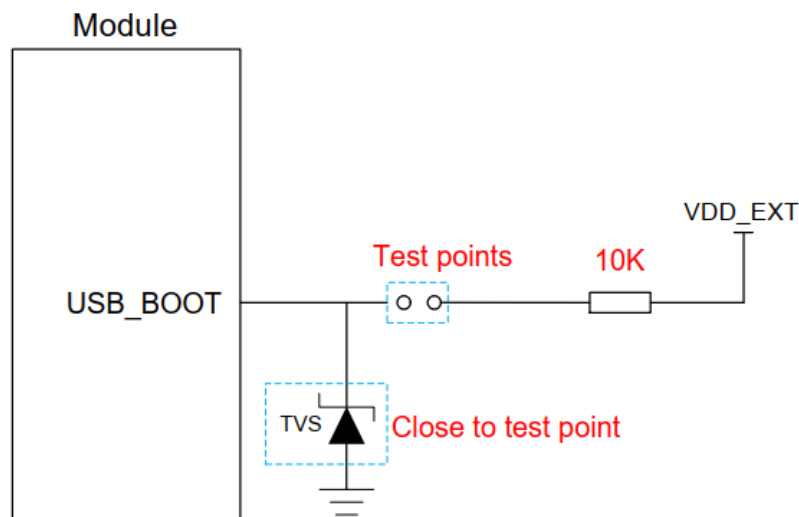


Figure 10 : Reference Design of USB_BOOT Interface

NOTE:

It is recommended to reserve the above circuit design during application design.

Ensure that VBAT is stable before pulling down PWRKEY. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY is not less than 30 ms.

*When using MCU to control the module entering emergency download mode, follow the above timing. Connecting the test points as shown in **Figure 10** can manually force the module to enter download mode.*

3.16 ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces.

AT+QADC=<port> (<port> values 0-1 correspond to channels ADC1 and ADC2 respectively) can be used to read the voltage value on the ADC being used.

To improve the accuracy of ADC voltage values, the traces of ADC should be surrounded with ground.

Table 15 : Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	General purpose	
ADC1	2	AI	ADC interface.	

NOTE:

It is prohibited to supply any voltage to ADC pin when VBAT is removed.

It is recommended to use resistor divider circuit for ADC application, and the divider resistor

accuracy should be not less than 1 %.

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4 Antenna Interfaces

The module includes a main antenna interface. The impedance of antenna ports is 50 Ω .

4.1 Main Antenna Interface

4.1.1 Pin Definition

Table 16 : Pin Definition of Main Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance

4.1.2 Operating Frequency

Table 17 : Operating Frequency of FX095 Series Module

3GPP Band	Transmit	Receive	Unit
LTE FDD B1	1920–1980	2110–2170	MHz
LTE FDD B2	1850–1910	1930–1990	MHz
LTE FDD B3	1710–1785	1805–1880	MHz
LTE FDD B4	1710–1755	2110–2155	MHz
LTE FDD B5	824–849	869–894	MHz
LTE FDD B7	2500–2570	2620–2690	MHz
LTE FDD B8	880–915	925–960	MHz
LTE FDD B12	699–716	729–746	MHz
LTE FDD B13	777–787	746–756	MHz
LTE FDD B18	815–830	860–875	MHz
LTE FDD B19	830–845	875–890	MHz
LTE FDD B20	832–862	791–821	MHz
LTE FDD B25	1850–1915	1930–1995	MHz
LTE FDD B26	814–849	859–894	MHz
LTE FDD B28	703–748	758–803	MHz
LTE FDD B66	1710–1780	2110–2180	MHz
LTE TDD B34	2010~2025	2010~2025	MHz
LTE TDD B38	2570~2620	2570~2620	MHz
LTE TDD B39	1880~1920	1880~1920	MHz
LTE TDD B40	2300~2400	2300~2400	MHz
LTE TDD B41	2535~2675	2535~2675	MHz

4.1.3 Reference Design

A reference design of main antenna interface is shown as below. It is recommended to reserve a π -type matching circuit for better RF performance, and the π -type matching components (R1/C1/C2) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

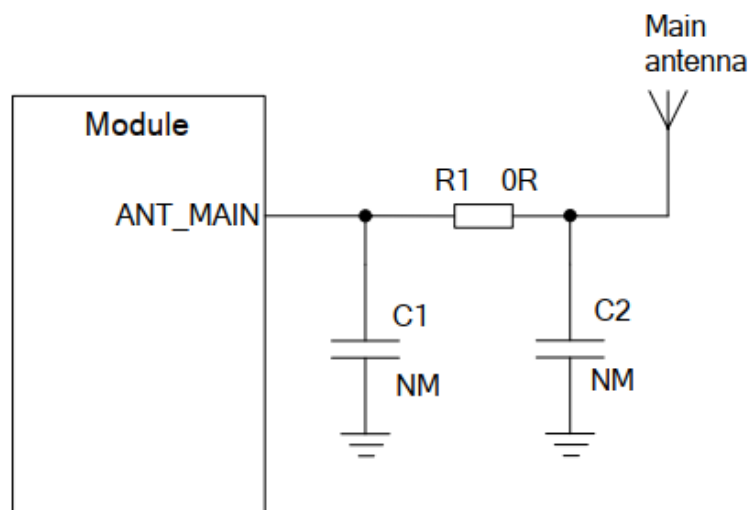


Figure 11 : Reference Design of Main Antenna Interface

4.2 RF Routing Guidelines

For your PCB, the characteristic impedance of all RF traces should be controlled to $50\ \Omega$. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

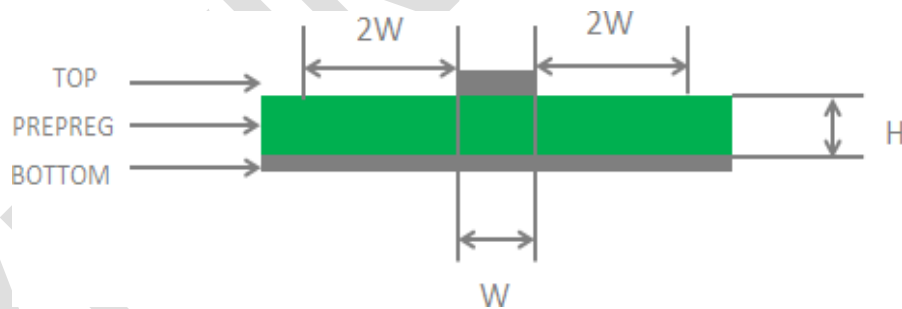


Figure 12 : Microstrip Design on a 2-layer PCB

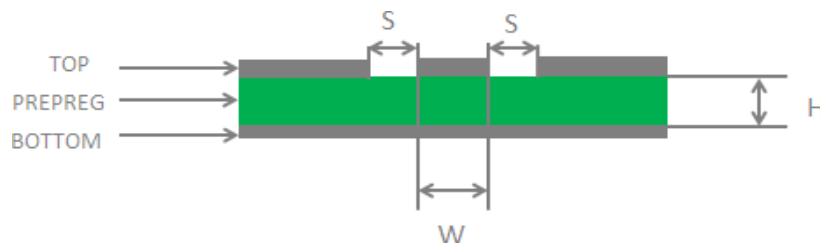


Figure 13 : Coplanar Waveguide Design on a 2-layer PCB

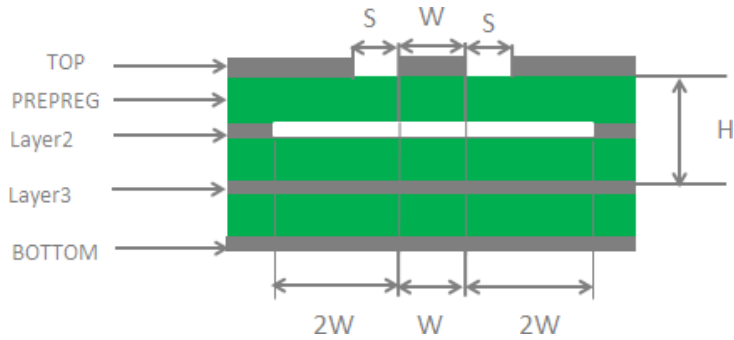


Figure 14 : Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

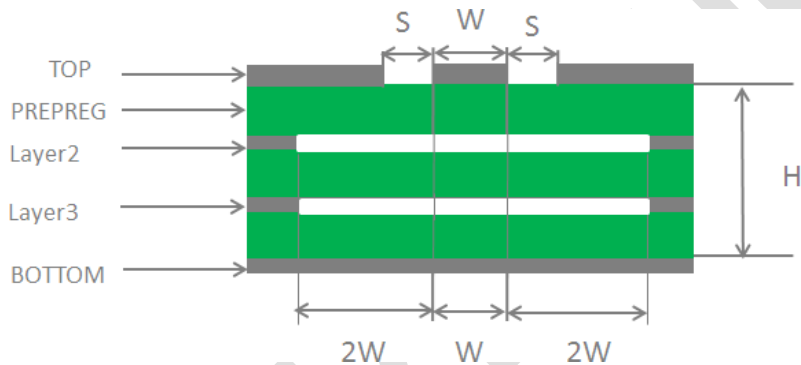


Figure 15 : Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω .
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces ($2 \times W$).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

4.2.1 Antenna Installation

Antenna type	Requirements
LTE antenna	$VSW \leq 2$
	EFFICITNCY >30%
	Max. input power 50W
	Input Impedance 50Ω
	Cable Insertion Loss: <1dB: LB (<1GHz) <1.5dB: MB (1-2.3GHz)

4.2.2 RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connectors provided by Hirose.

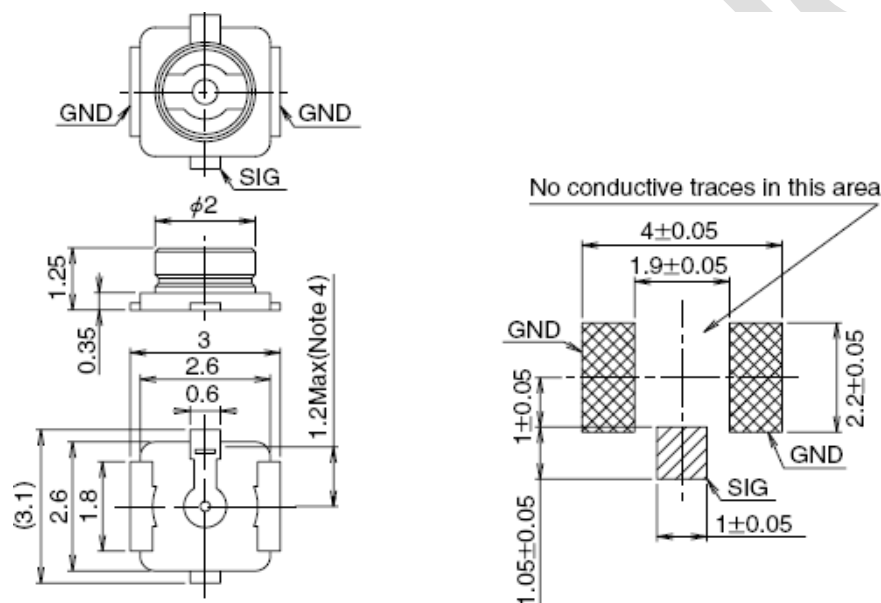


Figure 16 : Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Part No.					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 17 : Specifications of Mated Plugs

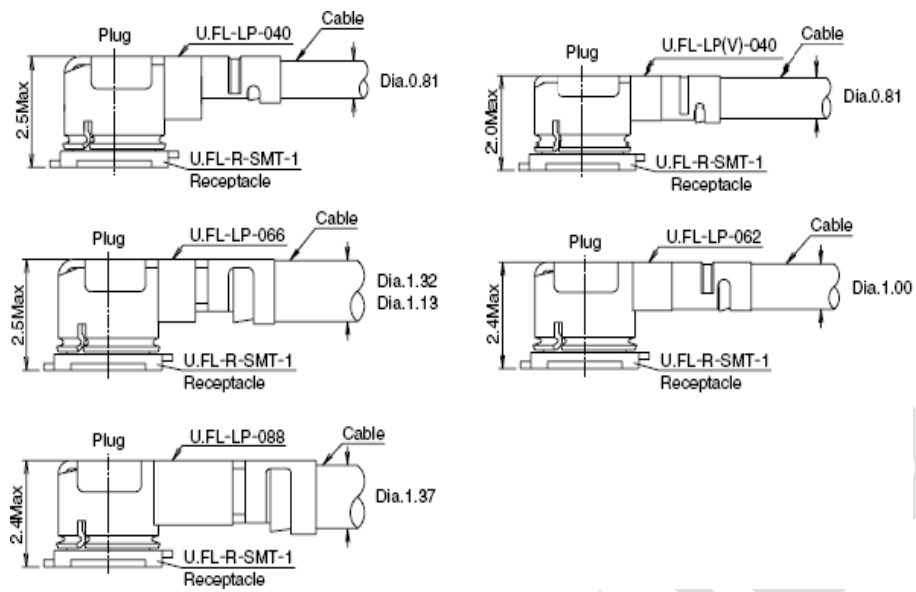


Figure 18 : Space Factor of Mated Connectors (Unit: mm)

5 Electrical Characteristics and Reliability

5.1 Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 18 : Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.5	6.0	V
USB_VBUS	-0.3	5.5	V
Voltage at Digital Pins	-0.3	2.09	V

5.2 Power Supply Ratings

Table 19 : Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT	The actual input voltage must be kept between the minimum and the maximum values.	3.4	3.8	4.5	V
IVBAT	Peak power consumption (during transmission slot)	At maximum power control level		1.8	2.7	A
	Peak power consumption	In LTE Cat 1 transmission modes.		0.8	1.0	A
USB_VBUS	USB connection detection		4.0	5.0	5.25	V

5.3 Operating and Storage Temperatures

Table 20 : Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range	-35	+25	+75	°C
Extended Temperature Range	-40	-	+85	°C
Storage Temperature Range	-40	-	+90	°C

NOTE:

- Within the operating temperature range, the module meets 3GPP specifications.
- Within the extended temperature range, the module remains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out} , may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again

5.4 Power Consumption

5.4.1 Power Consumption

Table 21 : FX095 Power Consumption (3.8 V Power Supply, Room Temperature)

Description	Conditions	Average	Unit
Leakage	Power-off @ USB and UART disconnected	3.3	μA
PSM	Power Saving Mode	4.1	μA
Rock Bottom	AT+CFUN=0 @ Sleep mode	0.215	mA
Sleep Mode	LTE Cat1 DRX = 1.28 s	0.554	mA
Idle Mode (USB disconnected)	LTE Cat.1 DRX = 1.28 s	2.1	mA
LTE Cat1 data transfer (@BW 10Mhz)	B1 @ 21.93 dBm	504.23	mA
	B2 @ 22.25 dBm	454.45	mA
	B3 @ 22.20 dBm	489.44	mA
	B4 @ 21.76 dBm	462.72	mA
	B5 @ 22.20dBm	480.54	mA
	B7 @ 21.73 dBm	460.20	mA
	B8 @ 21.98 dBm	464.89	mA
	B12 @ 21.78 dBm	541.14	mA
	B13 @ 22.11 dBm	493.82	mA
	B18 @ 22.13 dBm	473.83	mA
	B19 @ 22.11 dBm	478.61	mA
	B20 @ 22.18 dBm	499.95	mA
	B25 @ 22.35 dBm	452.63	mA
	B26 @ 22.12 dBm	489.18	mA
	B28 @ 22.13 dBm	463.86	mA
	B66 @ 21.63 dBm	509.43	mA
	B34 @ 21.93 dBm	230.88	mA
	B38 @ 21.77 dBm	228.93	mA
	B39 @ 21.89 dBm	227.65	mA
	B40 @ 21.79 dBm	212.32	mA
	B41 @ 21.84 dBm	232.72	mA

5.5 Tx Power

The device operates with the following frequency bands and transmitting power:

Table 22 : Conducted Tx Power of FX095

Frequency Bands	Max. Tx Power	Min. Tx Power
LTE -FDD B1/B2/B3/B4/B5/B7/B8/B12/B13/B18/ B19/B20/B25/B26/B28/B66	23 dBm $\pm$ 2 dB	< -39 dBm
LTE -TDD B34/B38/B39/B40/B41	23 dBm $\pm$ 2 dB	< -39 dBm

The device operates with the following frequency bands and transmitting power:

Frequency Bands	Maximum output power
LTE Band 1	22.67 dBm
LTE Band 3	23.61 dBm
LTE Band 5	22.91dBm
LTE Band 7	23.23 dBm
LTE Band 8	22.50dBm
LTE Band 20	23.05 dBm
LTE Band 28	23.06 dBm
LTE Band 34	22.44 dBm
LTE Band 38	24.53 dBm
LTE Band 40	22.60 dBm
LTE Band 41	23.97 dBm

Maximum Power Reduction (MPR) for Power Class 3

Modulation	Channel bandwidth / Transmission bandwidth configuration [RB]						3GPP 36.101 requirement MPR (dB)	MPR setting (dB)
	1.4 MHz	3.0 MHz	5 MHz	10 MHz	15 MHz	20 MHz		
QPSK	> 5	> 4	> 8	> 12	> 16	> 18	≤ 1	1
16 QAM	≤ 5	≤ 4	≤ 8	≤ 12	≤ 16	≤ 18	≤ 1	1
16 QAM	> 5	> 4	> 8	> 12	> 16	> 18	≤ 2	2

We expects LTE transmit power result to be within **0~1dB** of the expected MPR target values.

5.6 Rx Sensitivity

Table 23 : FX095 Conducted Rx Sensitivity

Mode	Band	Primary	Diversity	Receiving Sensitivity (dBm)
				Cat 1/3GPP BW 10M
LTE	LTE -FDD B1	Supported	-	-98.8
	LTE -FDD B2			-98.3
	LTE -FDD B3			-98.9
	LTE -FDD B4			-98.3
	LTE -FDD B5			-99.3
	LTE -FDD B7			-96.7
	LTE -FDD B8			-98.9
	LTE -FDD B12			-98.1
	LTE -FDD B13			-98.7
	LTE -FDD B18			-99.7
	LTE -FDD B19			-99.2
	LTE -FDD B20			-98.4
	LTE -FDD B25			-98.1
	LTE -FDD B26			-99.6
	LTE -FDD B28			-98.9
	LTE -FDD B66			-99.0
	LTE -TDD B34			-101.6
	LTE -TDD B38			-100.2

	LTE -TDD B39			-101.0
	LTE -TDD B40			-101.1
	LTE -TDD B41			-100.3

5.7 ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, it is imperative to adopt proper ESD countermeasures and handling methods. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 24 : Electrostatic Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Main Antenna Interfaces	±4	±6	kV

6 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ± 0.2 mm unless otherwise specified.

6.1 Mechanical Dimensions

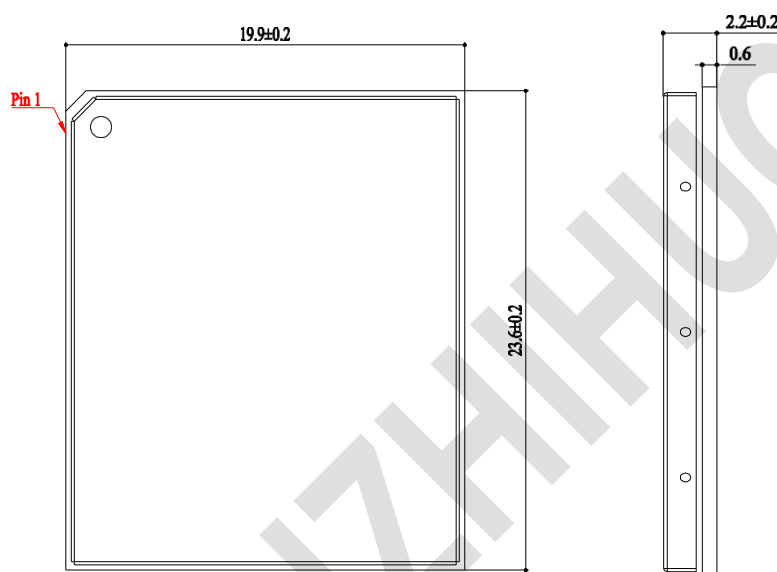


Figure 19 : Module Top and Side Dimensions

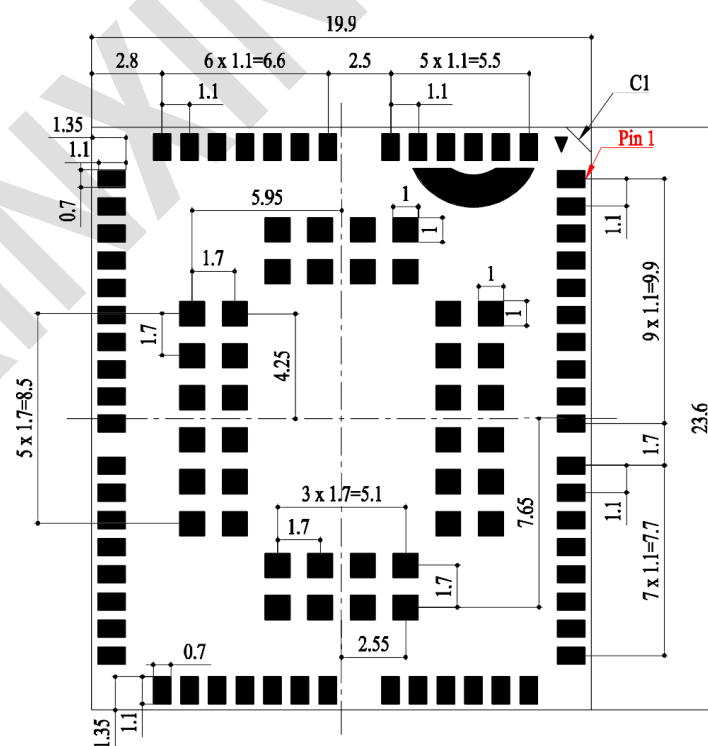


Figure 20 : Module Bottom Dimensions (Bottom View)

NOTE: The package warpage level of the module conforms to JEITA ED-7306 standard.

6.2 Recommended Footprint

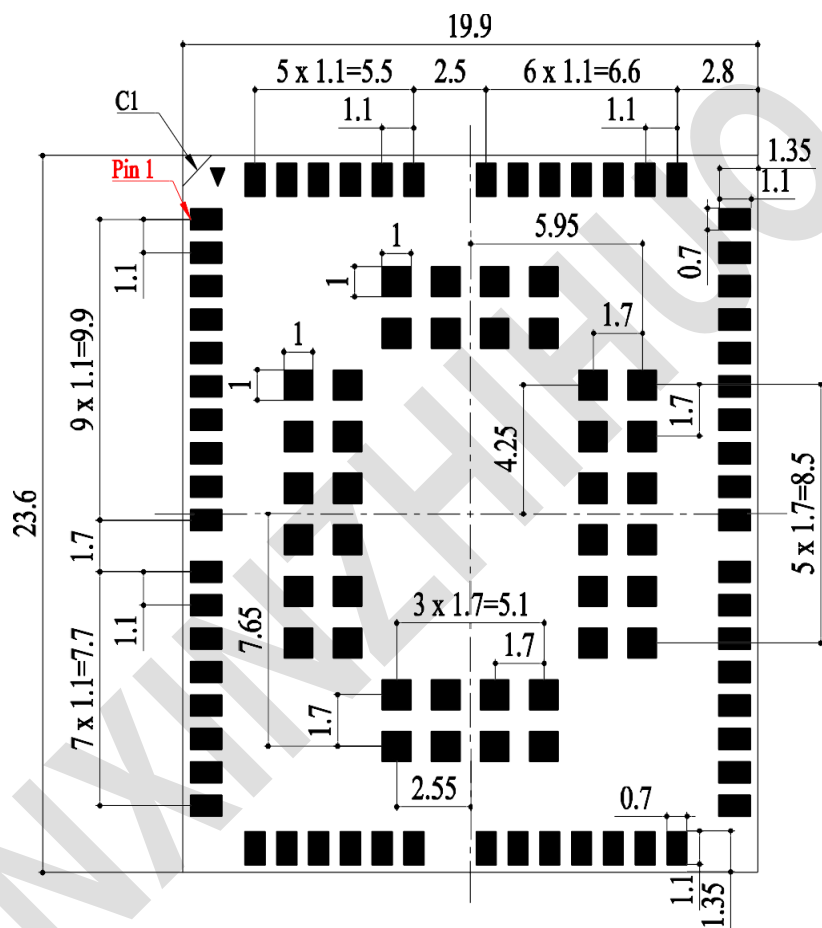


Figure 21 : Recommended Footprint (Top View)

NOTE: Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

6.3 Top and Bottom Views

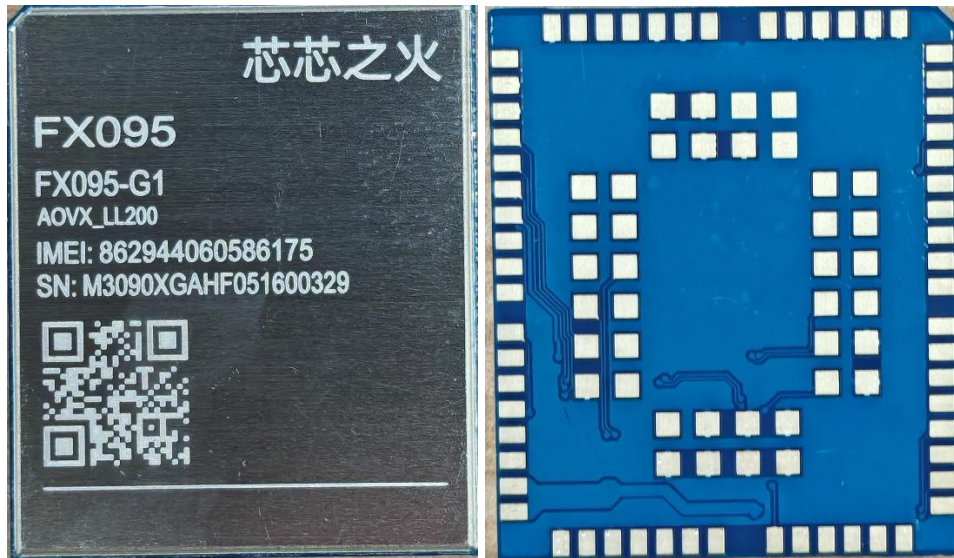


Figure 22 : Top and Bottom Views

NOTE: Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Xinxinzhifire.

7 Storage, Manufacturing and Packaging

7.1 Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

- 1) Recommended Storage Condition: the temperature should be 23 ± 5 °C and the relative humidity should be 35–60 %.
- 2) Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.
- 3) Floor life: 168 hours²⁸ in a factory where the temperature is 23 ± 5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).
- 4) The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:
 - The module is not stored in Recommended Storage Condition;
 - Violation of the third requirement mentioned above;
 - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
 - Before module repairing.
- 5) If needed, the pre-baking should follow the requirements below:
 - The module should be baked for 8 hours at 120 ± 5 °C;
 - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

Note:

To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.

Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see IPC/JEDEC J-STD-033 for the baking procedure.

Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

7.2 Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill

the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm.

The recommended peak reflow temperature should be 235–246 °C, with 246 °C as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

Temp. (°C)

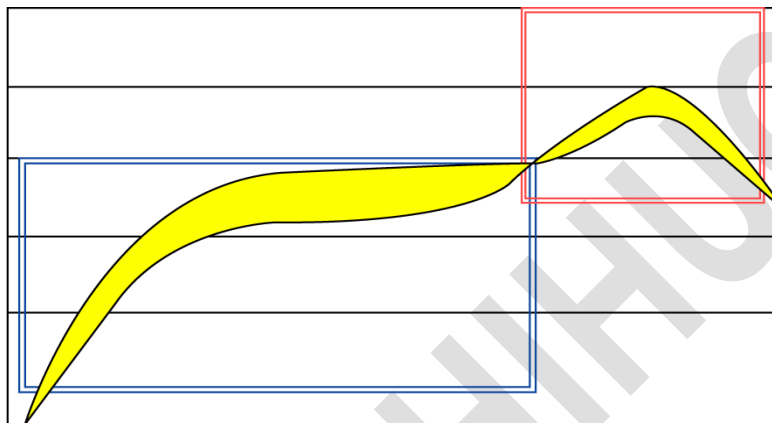


Figure 23 : Recommended Reflow Soldering Thermal Profile

Table 25 : Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217°C)	40–70 s
Max Temperature	235–246 °C
Cool-down Slope	-3–0 °C/s
Reflow Cycle	
Max Reflow Cycle	1

NOTE:

- 1) The above profile parameter requirements are for the measured temperature of the

solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.

- 2) If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.*
 - 3) Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.*
 - 4) Due to the complexity of the SMT process, please contact Technical Supports in advance for any situation that you are not sure about.*
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8 Appendix A References

ESD	Electrostatic Discharge
ASM	Antenna Switch Modules
bps	Bits per second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DTR	Data Terminal Ready
e-I-DRX	Extended Idle Mode Discontinuous Reception
EPC	Evolved Packet Core
FDD	Frequency Division Duplex
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
HSS	Home Subscriber Server
I2C	Inter-Integrated Circuit
I/O	Input/Output
LED	Light Emitting Diode
LDO	Low-dropout Regulator
LNA	Low Noise Amplifier
LPF	Low-Pass Filter
LTE	Long Term Evolution
MO	Mobile Originated
MOQ	Minimum Order Quantity
MT	Mobile Terminated
PA	Power Amplifier
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PMIC	Power Management IC
PPP	Point-to-Point Protocol
PSM	Power Saving Mode
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SAW	Surface Acoustic Wave
SMS	Short Message Service
TDD	Time Division Duplex
TX	Transmit
UL	Uplink
UE	User Equipment
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
VIHmax	Maximum High-Level Input Voltage
VIHmin	Minimum High-level Input Voltage

VILmax	Maximum Low-level Input Voltage
VILmin	Minimum Low-level Input Voltage
VImax	Absolute Maximum Input Voltage
VImin	Absolute Minimum Input Voltage
VOHmax	Maximum High-level Output Voltage
VOHmin	Minimum High-level Output Voltage
VOLmax	Maximum Low-level Output Voltage
VOLmin	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WWAN	Wireless Wide Area Network