

Product Manual_

SCS527E

LTE CAT.1 Module

V1.0

2025-10-21



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Service and Support



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Declaration

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Safety Instruction

By adhering to the following safety principles, personal security can be ensured while contributing to the protection of products and work environments from potential damage. Our company shall not be held liable for any losses incurred due to customers' failure to comply with these regulations.



Road Safety First! When driving, do not use handheld mobile terminal devices unless they are equipped with a hands-free function. Please pull over and then make a call!



Please turn off your mobile terminal device before boarding. The wireless functions of mobile terminals are prohibited from being activated on board to prevent interference with the aircraft's communication systems. Ignoring this notice may jeopardize flight safety and even violate the law.



When in a hospital or healthcare facility, pay attention to any restrictions on the use of mobile terminal devices. RF interference may cause medical equipment to malfunction; therefore, it may be necessary to turn off mobile terminal devices.



Your mobile terminal device will receive and transmit radio frequency signals when it is turned on. When it is close to a TV, radio, computer or other electronic devices, it will cause radio frequency interference.



Keep mobile terminal devices away from flammable gases. When you are near gas stations, oil depots, chemical plants, or explosive operation sites, please turn off your mobile terminal device. Operating electronic devices in any location with potential explosion hazards poses safety risks.

Version History

Ver.	Revision Date	Revision Log
V1.0	2025-10-21	Initial Release

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1 Product Overview

The SCS527E is an ultra-compact, highly integrated, low-power LTE CAT.1 chip-level wireless communication module that supports 4G long-range wireless transmission technology.

With a compact structure, it has a size of only 10*12*1.2mm, making it one of the smallest and thinnest modules in the industry. A variety of product series have been developed to adapt to different regions at home and abroad for customers to choose from.

It provides common interfaces such as USB2.0/UART/SPI/I2C/I2S/GPIO/ADC, which can meet the application requirements of most IoT industries, including smart water utilities, fire smoke detectors, smart cities, security, smart home appliances, wireless POS machines, etc.

1.1 Key Features

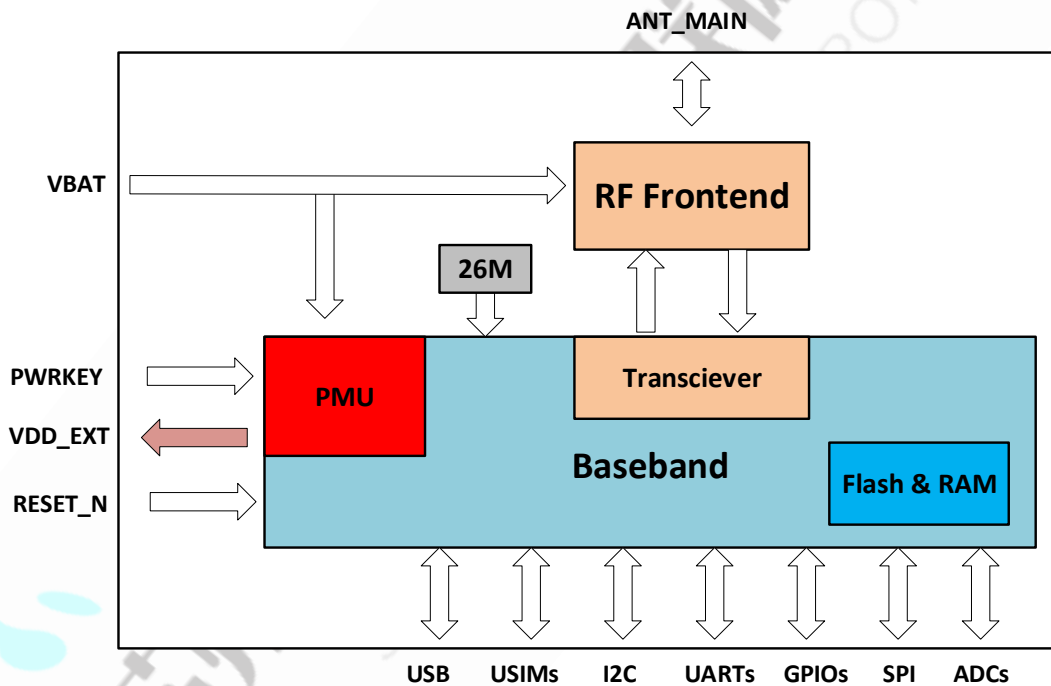


Figure 1-1 Functional Block Diagram

Table 1-1 Key Features

Item	Description
Footprint	LGA, 66Pin
Dimension	(10±0.1) mm x (12.0±0.1) mm x (1.2±0.10) mm
Weight	0.4g
CPU	Cortex M3 @ 306MHz, 16KB instruction cache
Memory	Nor Flash 4MB, SRAM 2MB, PSRAM 2MB (optional)
VIN	VBAT: 3.3V ~ 4.3V ; Tye: 3.8V
IO Level	1.8V/2.8V/3.3V (configurable)
Operating	LTE-FDD: B1/B3/B20/B8 LTE-TDD: B34/B38/B39/B40/B41

Item	Description
Band	
Transmit Power	LTE-FDD: Class 3 (23dBm±2.7dB) LTE-TDD: Class 3 (23dBm±2.7dB)
LTE Features	Supports Cat 1 FDD 和 TDD Supports 1.4/3/5/10/15/20MHz RF bandwidth LTE-FDD Max Rate: Upstream 5Mbps, Downstream 10Mbps, LTE-TDD Max Rate: Upstream 3.1Mbps, Downstream 8.96Mbps
Network Protocol	Supports TCP/UDP/PPP/HTTP/NITZ/NDIS/NTP/HTTPS/MQTT Complies with PAP and CHAP authentication of PPP protocol
USIM	1.8/3.0V USIM card, dual-card single-standby
USB	- Supports USB 2.0 High speed (slave mode only), data transmission rate up to 480Mbps - Used for AT commands, data transmission, software debugging and firmware upgrade - USB virtual serial port driver: Supports Windows 7/8.1/10 , Linux 2.6.x/3.x/4.1, Android 4.x/5.x/6.x/7.x and other OS USB drivers
UART	-Main UART: For AT command, data transmission and firmware upgrade, supports hardware flow control (RTS/CTS) - Debug UART (DBG_TXD/RXD): For software debugging, acquiring runtime logs -AUX UART
GPIO	x 39, excluding WAKEUP/CHRG_DET
Audio	X 1 I2S (digital audio interface) External codec chip can be connected
I2C	x 2, Compliant with I2C bus protocol specifications
SPI	x 2
ADC	x 2 , 12bits
WatchDog	Software watchdog
AT Command	Supports commands defined in 3GPP TS 27.005 and 3GPP TS 27.007 Supports our self-developed AT commands while being compatible with mainstream AT commands
Firmware Upgrade	Upgradable via USB interface or DFOTA
Antenna Interface	50Ω characteristic impedance
Temperature Range ⁽²⁾	Normal operating temperature: -35°C ~ +75°C Extended operating temperature: -40°C ~ +85°C Storage temperature: -40°C ~ +90°C
Certification	All components comply with RoHS/REACH standards

Notes:



(1) When the product operates within this temperature range, it can still maintain normal working conditions (e.g., supporting SMS, data transmission, and other functions), but some radio frequency (RF) indicators may deviate from the scope specified in the 3GPP standards.

1.2 Pin

1.2.1 Pin Assignment

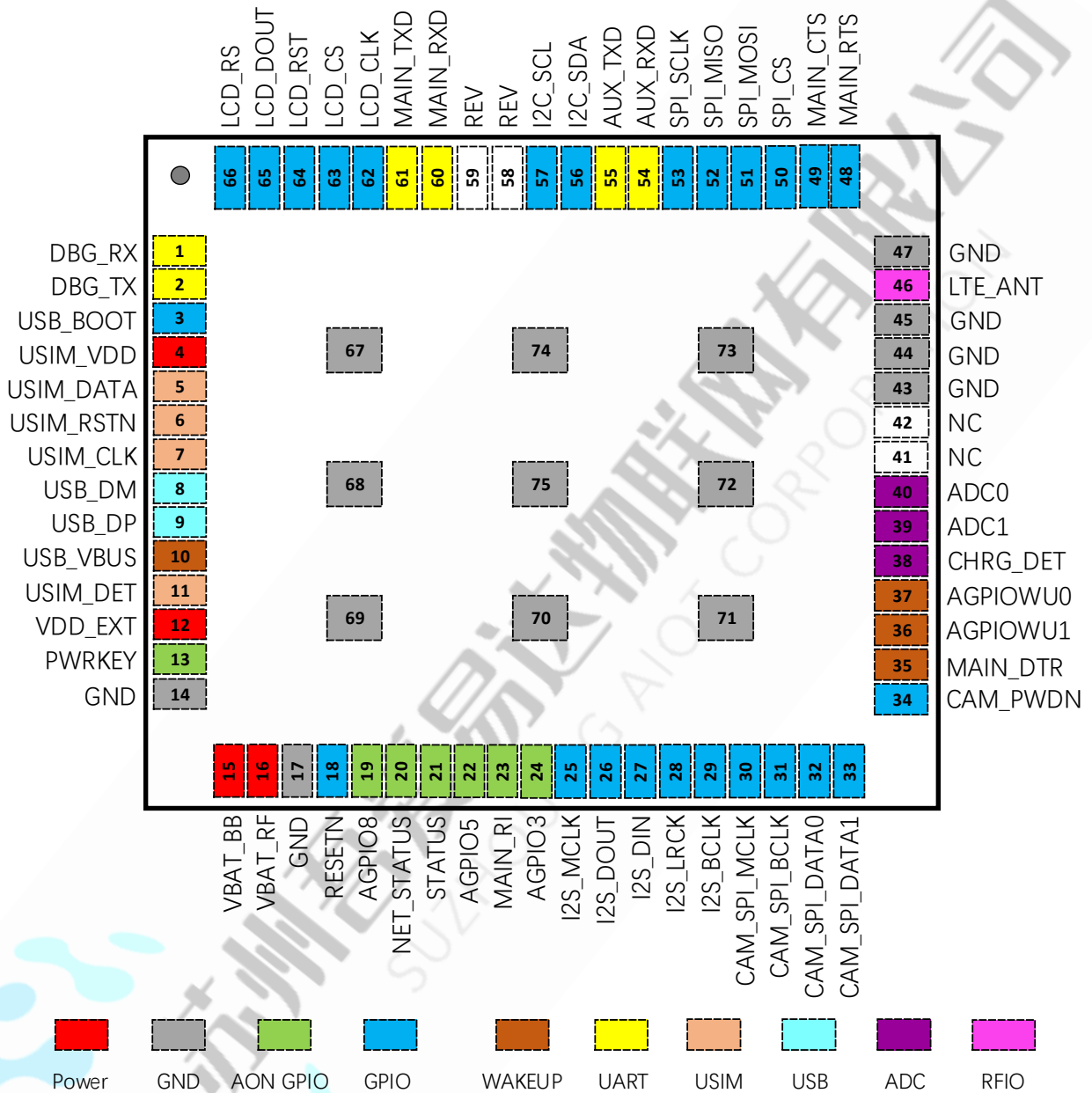


Figure 1-2 SCS527E Pinout (perspective view)

1.2.2 Pin Description

DIO: Digital Input/Output AIO: Analog Input/Output
DI: Digital Input AI: Analog Input PI: power input
DO: Digital Output AO: Analog Output PO: power output

Table 1-2 Pinout Description

Pin	Pin Num.	I/O	Description	Parameter	Notes
POWER					
VBAT_BB	15	PI	Power Input	Vmax=4.3V Vmin=3.3V Vnom=3.8V	
VBAT_RF	16	PI	RF Power	Vmax=4.3V Vmin=3.3V Vnom=3.8V	Supplies power to internal PA, requires a current - carrying capacity of 1.5A
VDD_EXT	12	PO	Power output	VDD_EXT=1.8V(Default); 1.8V/2.8V/3.3V (configurable)	1. leave floating if not used. 2. All IOs with VDD_EXT voltage will be powered off in sleep mode and periodically output high pulses, not to be used for pull - up of wake - up tubes or serial ports. 3. Max current 200mA, for each GPIO, max load current is about 6mA @1.8V, 14mA @3.3V.
GND	14,17,43,44,45,47, 67-75				
Power on/off					
PWRKEY	13	AI	Power on/off	V _{IL} max=0.5V	Internal pull - up, active low; 1. In grounded condition, the chip powers on when powered up. 2. In non - grounded condition: 1) In shutdown state, the pin is low for more than 500ms to power on the module. 2) In startup state, the pin is low for more than 650ms to power off the module. 3) When powering on, ensure the initial voltage of VBAT is less than 0.5V.
RESETN	18	DI	Reset	LDOAON	Internal pull - up, active low, leave floating if not used.
USIM card Interface(Note: When using USIM2, since the GPIO4/5/6 interfaces are occupied, the CAMERA interface cannot be used.)					
USIM_DATA	5	DIO	USIM1 data		The module automatically identifies 1.8V or 3.0V USIM cards.
USIM_RSTN	6	DO	USIM1 reset		
USIM_CLK	7	DO	USIM1 clock		It is recommended to use TVS diodes for ESD protection on the external USIM card interface. The wiring from the USIM card socket to the module shall not exceed 200mm.
USIM_VDD	4	PO	USIM1/2 power	Vnom=1.8/3.0V Iomax=34mA	
The GND of the USIM card shall be directly connected to the main ground.					

Pin	Pin Num.	I/O	Description	Parameter	Notes
USIM_DET [WAKEUP2]	11	DI	USIM card insertion/removal detection, only for USIM1	LDOAON	If not used, it can be left floating.
USIM2_DATA [GPIO6]	32	DIO	USIM2 data	VDD_EXT	When used, an external pull-up resistor to USIM_VDD is required.
USIM2_RST [GPIO4]	31	DO	USIM2 reset	VDD_EXT	USIM2 only supports 1.8V cards.
USIM2_CLK [GPIO5]	34	DO	USIM2 clock	VDD_EXT	When used, an external pull-up resistor to AGPIO3 is required.
CAMERA Interface					
CAM_SPI_MCLK [GPIO3]	30			VDD_EXT	No internal pull-up resistor
CAM_SPI_BCLK [GPIO4]	31			VDD_EXT	
CAM_PWDN [GPIO5]	34			VDD_EXT	
CAM_SPI_DATA0 [GPIO6]	32			VDD_EXT	
CAM_SPI_DATA1 [GPIO7]	33			VDD_EXT	
Main UART					
MAIN_RXD	60	DI	Main UART Receive	VDD_EXT	Supports LPUART, LPUART can wake up the module in sleep mode
MAIN_TXD	61	DO	Main UART Transmit	VDD_EXT	Supports LPUART, outputs power-on startup information during boot process
MAIN_DCD [GPIO36]	64	DO	Main UART Carrier Detect Signal	VDD_EXT	Important: Cannot be used simultaneously with LCD_RST function, choose one
MAIN_DTR [AGPIOWU2]	35	DI	Main UART Data Terminal Ready	LDOAON	Configurable as wake-up mode, pull low to wake up the module
MAIN_RI [AGPIO4]	23	DO	Main UART Ring Indicator	LDOAON	Ring signal, wakes up AP, can be maintained in sleep mode
MAIN_RTS [GPIO1]	48	DI	DTE Request To Send	VDD_EXT	Connect to DTE's RTS, leave floating if not used
MAIN_CTS [GPIO2]	49	DO	DTE Clear To Send	VDD_EXT	Connect to DTE's CTS, leave floating if not used
Aux UART					
AUX_RXD [GPIO12]	54	DI	Aux UART Receive Data	VDD_EXT	Not LPUART
AUX_TXD [GPIO13]	55	DO	Aux UART Transmit Data	VDD_EXT	Not LPUART
DBG_RXD [GPIO16]	1	DI	Debug UART Receive Data	VDD_EXT	Test points need to be reserved, default baud rate 3Mbps
DBG_TXD [GPIO17]	2	DO	Debug UART Transmit Data	VDD_EXT	
USB Interface					
USB_DM	8	AIO	USB DM(-)		Complies with USB2.0 specification, requires 90Ω differential impedance, test points need to be reserved for firmware upgrade and virtual serial port
USB_DP	9	AIO	USB DP(+)		

Pin	Pin Num.	I/O	Description	Parameter	Notes
USB_VBUS	10	AI	USB Insertion Wake-up	LDOAON	1) Internal resistor voltage division, supports USB insertion to trigger system sleep wake-up. 2) When connected, after the module is powered on, USB can be used as a serial port (AT and DBG_UART). 3) Leave floating if not used, only USB download is supported at this time, cannot be used as a serial port.
Status Indicator Interface					
NET_STATUS [GPIO7]	20	DO	Network Status Indication	LDOAON	
STATUS [GPIO6]	21	DO	Module Operation Status Indication	LDOAON	
Audio Interface_ I2S					
I2S_MCLK [GPIO33]	25	DIO	I2S Reference Clock	VDD_EXT	leave floating if not used.
I2S_DOUT [GPIO32]	26	DO	I2S Data Output	VDD_EXT	leave floating if not used.
I2S_DIN [GPIO31]	27	DI	I2S Data Input	VDD_EXT	leave floating if not used.
I2S_LRCK [GPIO30]	28	DO	Left/Right Channel Control Signal	VDD_EXT	leave floating if not used.
I2S_BCLK [GPIO29]	29	DO	I2S Clock Output	VDD_EXT	leave floating if not used.
I2C Interface					
I2C_SDA [GPIO14]	56	DIO	I2C Serial Data	VDD_EXT	When used as I2C, an external pull-up resistor is required.
I2C_SCL [GPIO15]	57	DO	I2C Serial Clock	VDD_EXT	leave floating if not used.
SPI Interface					
SPI_CS [GPIO8]	50	DO	SPI Chip Select Signal	VDD_EXT	leave floating if not used.
SPI_MOSI [GPIO9]	51	DO	SPI Data Output	VDD_EXT	leave floating if not used.
SPI_MISO [GPIO10]	52	DO	SPI Data Input	VDD_EXT	leave floating if not used.
SPI_SCLK [GPIO11]	53	DO	SPI Clock Signal	VDD_EXT	leave floating if not used.
LCM Interface					
LCD_CLK [GPIO34]	62	DO	SPI LCD Clock	VDD_EXT	leave floating if not used.
LCD_CS [GPIO35]	63	DO	SPI LCD Chip Select Signal	VDD_EXT	leave floating if not used.
LCD_RST [GPIO36]	64	DO	SPI LCD Reset	VDD_EXT	leave floating if not used. Multiplexed with the MAIN_DCD interface, choose one of the two.
LCD_DOUT [GPIO37]	65	DO	SPI LCD Data Output	VDD_EXT	leave floating if not used.
LCD_RS [GPIO38]	66	DO	SPI LCD Register Selection	VDD_EXT	Data Command Selection, leave floating if not used.

Pin	Pin Num.	I/O	Description	Parameter	Notes
ADC Interface					
ADC0 [AIO3]	40	AIO	ADC Interface	Voltage Range: 0-1.6V	12bits,
ADC1 [AIO4]	39	AIO	ADC Interface	VoltageRange: 0-1.6V	
Others					
USB_BOOT	3	DI	USB Download Mode Control	VDD_EXT	Test points need to be reserved. Pull high to VDD_EXT before power - on, the module will forcefully enter USB download mode.
CHRG_DET	38	AI	Charging Status Indication		1) Internal pull - up, leave floating if not used; 2) Supports charging wake - up in shutdown state, active low, initiates charging process.
AGPIO3	24	IO	GPIO AON	LDOAON	1) Can be maintained in sleep state. 2) When used as an external pull - up power supply for USIM2, it cannot be used for GPIO function.
AGPIOWU0	37	AI	External Input Interrupt, fixed level 1.1V	LDOAON	Supports interrupt wake - up in sleep mode.
AGPIOWU1	36	AI	External Input Interrupt, fixed level 1.1V	LDOAON	Supports interrupt wake - up in sleep mode, pull - up with VDD_EXT is prohibited in sleep state.
AGPIO5	22	IO	General - purpose GPIO, maintainable in sleep mode	LDOAON	Default off state.
AGPIO8	19	IO	General - purpose GPIO, maintainable in sleep mode	LDOAON	Default off state.
Antenna Interface					
LTE_ANT	46	AIO	Antenna Interface		50Ωcharacteristic impedance
Reserve					
REV	58,59				leave floating
Not Connect					
NC	41,42				Not connect

Notes:



- (1) For OpenCPU development requirements, the specific functional definitions of IO pins can be adapted based on the provided 'SCS527E Chip-Level Module GPIO Mapping Table' Please consult our Field Application Engineer (FAE) during the development process.

2 Product Performance

This chapter introduces the electrical characteristics and reliability of the SCS527E product, including power supply voltage, temperature characteristics, and ESD protection characteristics.

2.1 Electrical Characteristics

Table 2-1 Absolute Maximum Ratings

Symbol	Min.	Max.	Unit
VBAT_BB	-0.3	4.8	V
VBAT_RF	0.5	4.8	V
USB_VBUS	-0.3	5.5	V
Peak Current	0	1.5	A
Average Current (TDMA Frame Time)	0	0.7	A
VDD(digital signal)	-0.3	3.6	V
Vcc (Analog signal)	-0.3	3.6	V

Table 2-2 Electrical Characteristic

Parameter	Min.	Tye.	Max.	Unit
Power Supply VBAT_BB ⁽¹⁾	+3.3	+3.8	+4.3	V
VBAT_RF	+3.3	+3.8	+4.3	V
USB_VBUS	+3.3	+5.0	5.25	V

2.2 Temperature Features

Table 2-3 SCS527E Temperature Features

Parameter	Min.	Tye.	Max.	Unit
Normal operating temperature	-35	+25	+75	°C
Extended operating temperature ⁽¹⁾	-40~-35	-	+75~+85	°C
Storage temperature	-45	-	+90	°C

Notes:



(1) When the product operates within this temperature range, it can still maintain normal working conditions (e.g., supporting SMS, data transmission, and other functions), but some radio frequency (RF) indicators may deviate from the scope specified in the 3GPP standards.

2.3 DC Characteristics

Conditions: VBAT_BB=VBAT_RF=3.8V, Temp 25°C, CMW500

Table 2-4 DC characteristics (3.8Vbat)

Module Mode	Conditions	Min.	Typ.	Max.	Unit
Power-off Mode	Module is power-off		0.3		uA
PSM Mode	AT+WSCLK=3 (USB shutdown)		4		uA
Min-Function Mode (RF/SIM disable)	AT+CFUN=0 (USB shutdown)		0.05		mA
Flight Mode (RF disable)	AT+CFUN=4 , AT+WSCLK=2		0.13		mA
Sleep Mode (AT+WSCLK=3 USB shutdown)	LTE-FDD @PF=32		0.49		mA
	LTE-FDD @PF=64		0.26		mA
	LTE-FDD @PF=128		0.16		mA
	LTE-FDD @PF=256		0.12		mA
	LTE-TDD @PF=32		0.51		mA
	LTE-TDD @PF=64		0.28		mA
	LTE-TDD @PF=128		0.16		mA
	LTE-TDD @PF=256		0.12		mA
Idle	LTE-FDD @PF=64 (USB shutdown)		3.45		mA
	LTE-FDD @PF=64 (USB connecting)		26.1		mA
	LTE-TDD @PF=64 (USB shutdown)		3.57		mA
	LTE-TDD @PF=64 (USB connecting)		26.1		mA
LTE TX power = 23dbm	LTE-FDD B1: CH300 BW=10M		570		mA
	LTE-FDD B3: CH1575 BW=10M		525		mA
	LTE-FDD B20: CH6300 BW=10M		410		mA
	LTE-FDD B8: CH3625 BW=10M		460		mA
	LTE-TDD B34: CH40620 BW=10M		220		mA
	LTE-TDD B38: CH38000 BW=10M		205		mA
	LTE-TDD B39: CH38450 BW=10M		230		mA
	LTE-TDD B40: CH39150 BW=10M		190		mA
	LTE-TDD B41: CH40620 BW=10M		215		mA

2.4 ESD

In product applications, static electricity generated by human body static, electrostatic friction

between microelectronics, etc., may discharge to the product through various channels, which could cause certain damage to the product.

Customers shall consider adding corresponding ESD protection components based on the product's application environment during the design phase to ensure product quality. Special attention shall be paid especially during secondary design, production assembly, testing, transportation, and other processes.

Table 2-5 ESD Characteristics

Test Environment: Humidity 45%, Temperature 25°C		
Test Point	Contact Discharge	Air Discharge
VBAT, GND	± 5KV	± 10KV
ANT	± 4KV	± 8KV
Others	± 0.5KV	± 1KV

2.5 RF Characteristics

The SCS527E provides one antenna port, be used for LTE Cat.1 signal transmission.

Table 2-6 RF Characteristics-Operating Frequency

3GPP Band	UP Link	Down Link	Unit
LTE-FDD B1	1920~1980	2110~2170	MHz
LTE-FDD B3	1710~1785	1805~1880	MHz
LTE-FDD B20	832~862	791~821	MHz
LTE-FDD B8	880~915	925~960	MHz
LTE-TDD B34	2010~2025	2010~2025	MHz
LTE-TDD B38	2570~2620	2570~2620	MHz
LTE-TDD B39	1880~1920	1880~1920	MHz
LTE-TDD B40	2300~2400	2300~2400	MHz
LTE-TDD B41	2555~2655	2555~2655	MHz

Table 2-7 RF Characteristics- Conducted Output Power

Band	Max Output Power	Min Output Power
LTE FDD B1/B3/B20/B8	23dBm±2.7dB	<-44dBm
LTE TDD B34/38/B39/B40/B41	23dBm±2.7dB	<-42dBm

Table 2-8 RF Characteristics—Conducted Receiver Sensitivity

Band	Receiver Sensitivity Level - throughput≥95%
LTE FDD B1 (10M)	< -98dBm
LTE FDD B3 (10M)	< -99dBm
LTE FDD B20 (10M)	< -99dBm
LTE FDD B8 (10M)	< -99dBm
LTE TDD B34 (10M)	< -100dBm
LTE TDD B38 (10M)	< -100dBm
LTE TDD B39 (10M)	< -100dBm
LTE TDD B40 (10M)	< -100dBm
LTE TDD B41 (10M)	< -100dBm

3 Application

3.1 Operating Modes

The SCS527E module has three normal operating modes, briefly described as follows:

Table 3-1 Operating Modes

Mode	Description
Full-Function Mode	-Active(Connected State): Network connection is normal, with data, voice, or SMS interactions. In this mode, the module's power consumption depends on network settings and data transmission rate.
	-Idle State: Software runs normally, the module is registered on the network, but there is no data interaction with the network.
Min-Function Mode	The command AT+CFUN=0 can set the module to minimum-function mode. RF and USIM card functions are disabled.
Flight Mode	The command AT+CFUN=4 can set the module to flight mode. RF function is disabled.
Sleep Mode	In sleep mode, the module's power consumption drops to a very low level, but the module can still receive SMS and TCP/UDP data.
PSM Mode	The module's power consumption drops to an extremely low level. The network is in a disconnected state, and the module does not accept base station paging.
Shutdown Mode	VBAT power supply remains connected, but the PMU stops supplying power to the baseband and RF circuits, and the software stops running.

- After the SCS527E module enters sleep mode, the VDD_EXT power supply will be powered off. The GPIOs in the corresponding voltage domain and UARTs (excluding MAIN_UART) will all be in a powered-off state. The powered-off IOs cannot respond to interrupts and cannot wake the module to exit sleep mode.
- After entering sleep mode, the module can only be woken up to exit sleep mode via interrupts from the following pins:

Pin	Pin Num.	Function	Description
PWRKEY	13	Power on/off	Trigger an interrupt by pulling down the power-on pin to control module power.
MAIN_TXD/RXD	61/60	Main UART	Wake up the module by sending data through the main UART.
MAIN_DTR	35	For wake up the module	pull low to wake up the module
USIM_DET	11	USIM card insertion/removal detection, only for USIM1	pull low to wake up the module

Pin	Pin Num.	Function	Description
VBUS	10	USB insertion wake-up	Trigger wake-up when USB is inserted or the pin is pulled down.
AGPIOWU0	37	External interrupt wake-up	Trigger an interrupt wake-up by pulling down this pin.
AGPIOWU1	36	External interrupt wake-up	Trigger an interrupt wake-up by pulling down this pin.

3.2 Summary of Module Operating Mode Switching

Table 3-2 Summary of Mode Switching

Current Mode	Next Mode		
	Shutdown	Normal Mode	Sleep Mode
Shutdown	/	Use PWRKEY to power on, or trigger the power-on process via USB insertion wake-up	/
Normal Mode	Use PWRKEY, or when VBAT voltage drops below the shutdown voltage	/	Call the sleep interface via software to enter the corresponding state configured by the PMU
Sleep Mode	Use PWRKEY, or when VBAT voltage drops below the shutdown voltage	GPIO pin interrupt, timer, SMS reception, or network data	/

3.3 Sleep Mode

In sleep mode, the power consumption of the module will be significantly reduced.

3.3.1 UART Application Scenario

The module communicates with the host via UART. The module enters sleep mode only when both of the following conditions are met:

- Execute AT+WSCLK=1
- Ensure MAIN_DTR remains high or floating。

To exit sleep mode:

- The host can wake the module by pulling down the module's MAIN_DTR.
- When the module has URC (Unsolicited Result Code) to report, the MAIN_RI signal will wake the host.

3.3.2 USB Application Scenario

For the two cases below—"Supports USB suspend, wake-up, and USB remote wake-up functions" and "Supports USB suspend, wake-up, and MAIN_RI functions"—the module enters sleep mode only when all 3 of the following conditions are met:

- Execute AT+WSCLK=1.
- Ensure MAIN_DTR remains high or floating.
- The USB bus of the host connected to the module's USB interface enters suspend state.

(1) Supports USB suspend, wake-up, and USB remote wake-up functions

The host supports USB suspend, wake-up, and USB remote wake-up functions.

Refer to the figure below for the connection between the module and the host:

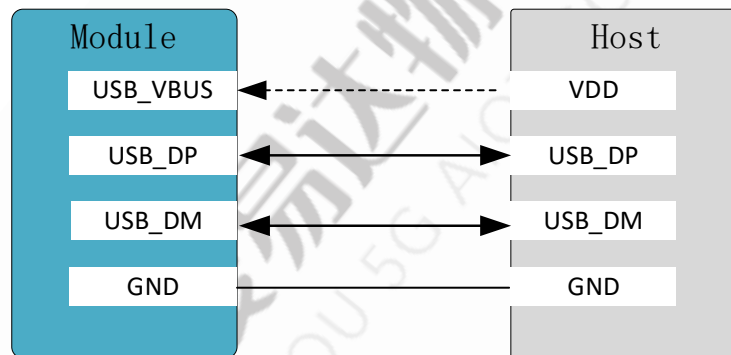


Figure 3-1 Sleep Application with USB Remote Wake-up Function

- Sending data to the module via USB will wake the module.
- When the module has URC to report, the module will send a remote wake-up signal through the USB bus to wake the host.

(2) Supports USB suspend, wake-up, and MAIN_RI functions

If the host supports USB suspend and wake-up but does not support USB remote wake-up, the host needs to be woken by the module's MAIN_RI signal.

Refer to the figure below for the connection between the module and the host:

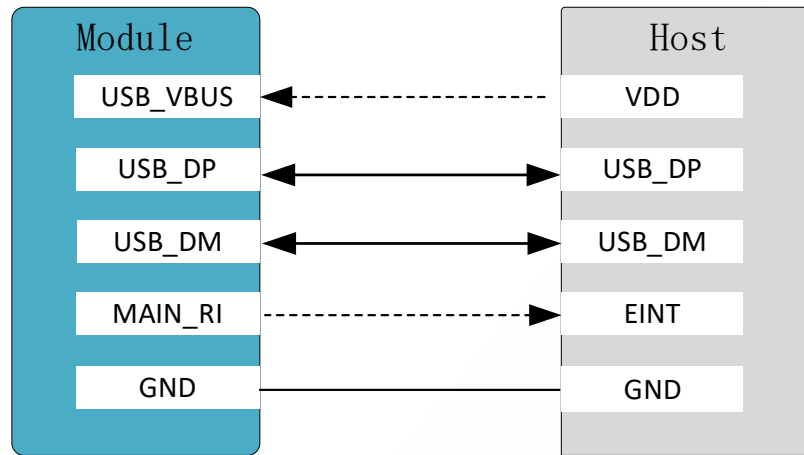


Figure 3-2 Sleep Application with MAIN_RI Function

- Sending data to the module via USB will wake the module.
- When the module has URC to report, the module will wake the host via MAIN_RI.

(3) Does not support USB suspend function

When the host does not support the USB suspend function, the module enters sleep mode only when all 3 of the following conditions are met:

- Execute AT+WSCLK=1.
- Ensure MAIN_DTR remains high or floating.
- Disconnect the USB_VBUS power supply.

If the host does not support the USB suspend function, the module can be put into sleep mode by disconnecting USB_VBUS through an external control circuit.

Refer to the figure below for the connection between the module and the host:

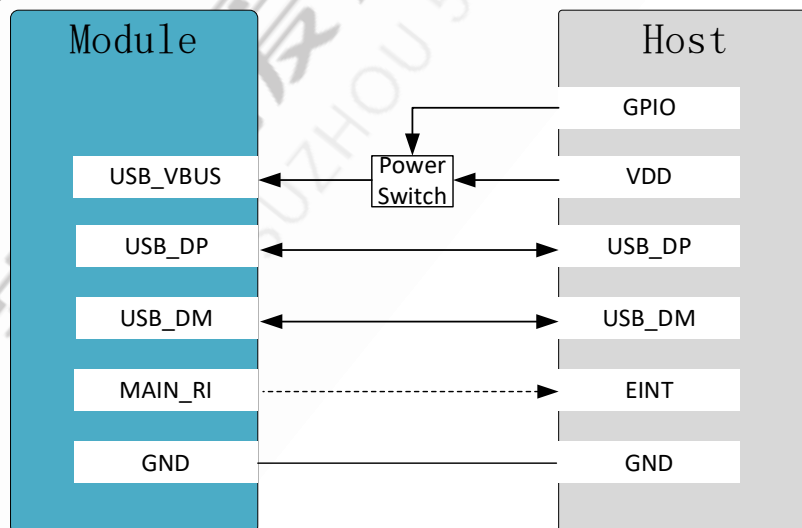


Figure 3-3 Sleep Application Without USB Suspend Function Support

Notes:



(1) Please note the level matching of the dashed connection signals between the module and the host as shown in the circuit diagram.

(2) For details about AT+WSCLK, refer to the AT Command Manual.

3.4 Flight Mode

When the module enters flight mode, the RF function becomes unavailable, and all RF-related AT commands cannot be accessed. The module can be put into flight mode in the following way:

Software method:

The mode can be set by sending the AT+CFUN=<fun> command. The <fun> parameter can be set to 0, 1, or 4.

- AT+CFUN=0: Min-Function Mode (RF function and USIM Card is disabled)。
- AT+CFUN=1: Full-Function Mode (Default)。
- AT+CFUN=4: Flight Mode (RF function is disabled)。

3.5 Power Supply Design

Table 3-3 Power Pins

Pin	Pin Num.	I/O	Description	Min.	Tye.	Max.	Unit
VBAT_BB ⁽¹⁾	15	PI	Power Input	+3.3	+3.8	+4.3	V
VBAT_RF ⁽¹⁾	16	PI	RF Power	+3.3	+3.8	+4.3	V
VDD_EXT	12	PO	VDD_EXT=1.8V(Default);	1.8V/2.8V/3.3V (configurable)			
GND	14,17,43,44,45,47,67-75						

3.5.1 VBAT Operating Characteristics

In the module application design, power supply design is a crucial part. Since the maximum peak current of the module operation can reach up to 1.5A, and there will be a continuous operating current of approximately 600mA at the maximum transmit power, the power supply must be capable of providing sufficient current. Otherwise, it may cause a drop in the supply voltage or even direct power-off and restart of the module.

The voltage input range of the module's power supply VBAT (unified power supply for VBAT_BB and VBAT_RF) is 3.3V~4.3V. However, the module usually generates a power supply voltage drop on the VBAT power supply during RF transmission. This is caused by the impedance of the power supply or the wiring path and is generally unavoidable. Therefore, special attention should be paid to the module's power supply design in the design process. At the VBAT input terminal, it is recommended to connect a 100uF tantalum capacitor with low ESR (ESR=0.7Ω), as well as 100nF, 33pF, and 10pF filter capacitors in parallel. The reference circuit of the VBAT input terminal is shown in the figure below. In addition, it is recommended that the PCB trace of VBAT be as short and wide as possible to reduce the equivalent impedance of the VBAT trace and ensure that no excessive voltage drop occurs under large

current at the maximum transmit power. The width of the VBAT trace is recommended to be no less than 1mm, and the longer the trace, the wider the line width should be.

It is advisable to add a TVS tube near the VBAT input terminal to improve the module's surge voltage withstand capability.

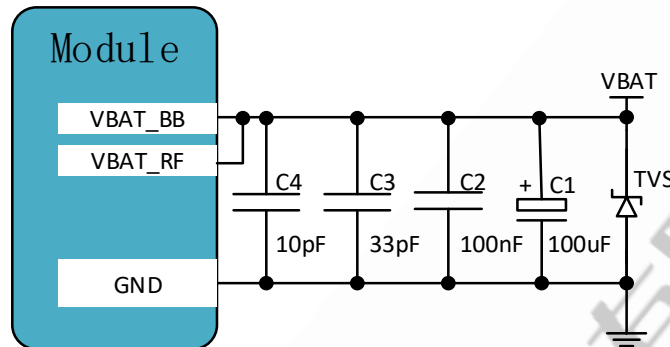


Figure 3-4 VBAT Input Reference Circuit for Non-Low-Voltage Requirements

3.5.2 Power Supply Reference Circuit

Power supply design is crucial for the module's power supply. A power supply capable of providing a current of at least 1.5A must be selected. If the voltage difference between the input voltage and the module's supply voltage is less than 2V, it is recommended to use an LDO (Low-Dropout Regulator) as the power supply. If the voltage difference between the input and output is greater than 2V, a switching power supply converter is recommended to improve power conversion efficiency.

LDO Power Supply (Component selection only needs to meet design requirements):

The figure below shows a reference design for 5V power supply, adopting an LDO from Micrel with the model number MIC29302WU. Its output voltage is 4.16V, and the peak load current reaches 3A. To ensure the stability of the output power supply, it is recommended to reserve a Zener diode at the output terminal and place it close to the VBAT pin of the module. It is advisable to select a Zener diode with a reverse breakdown voltage of 5.1V and a power dissipation of more than 1W.

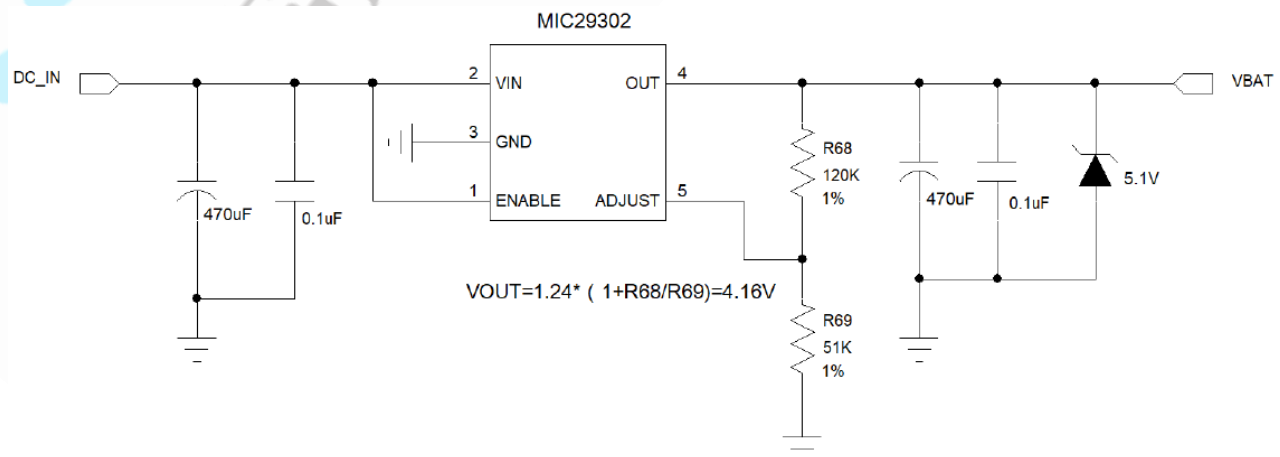


Figure 3-5 Power Supply Input Reference Design

3.5.3 VDD_EXT

Notes for Use:

- VDD_EXT serves as the internal power supply for most GPIOs. It will be powered off when the module enters sleep mode to reduce power consumption.
- During the module's sleep period, VDD_EXT will generate high pulses with irregular cycles as the module's underlying layer wakes up frequently for network interaction to maintain network registration status. If used for certain IOs (e.g., wake-up IO pins or pull-up of MAIN_UART), this may cause frequent IO interrupt triggers, preventing the module from entering sleep mode.
- In sleep mode, AGPIO3 can be used for pull-up.

3.6 Power on/off and Reset

Table 3-4 Power-on/off and Reset

Pin	Pin Num.	I/O	Description
PWRKEY	13	DI	Module Power On/Off Control Pin, Internally Pulled Up, No External Pull-Up Required
RESETN	18	DI	Reset Pin, Active Low, Internally Weakly Pulled Up

3.6.1 Power-on

The module can be powered on in the following two ways:

1. PWRKEY

After VBAT is powered on, the module can be started through the PWRKEY pin. Pull the PWRKEY pin low for more than 0.5 seconds to initiate the module's power-on process. It is required to ensure that the initial voltage of VBAT during power-on is less than 0.5V. The software will detect the voltage of the VBAT pin: if the VBAT pin voltage is higher than the software-configured power-on voltage (3.3V), the power-on operation will continue until the system is fully booted; otherwise, the power-on operation will stop and the system will shut down. The PWRKEY pin can be released after a successful power-on. It is recommended to use an open-collector driver circuit to control the PWRKEY pin.

Another method to control the PWRKEY pin is to use a pushbutton switch directly. A TVS tube should be placed near the pushbutton to prevent electrostatic discharge (ESD) caused by contact, and the TVS tube should be mounted close to the pushbutton.

The reference circuit is shown in the figure below:

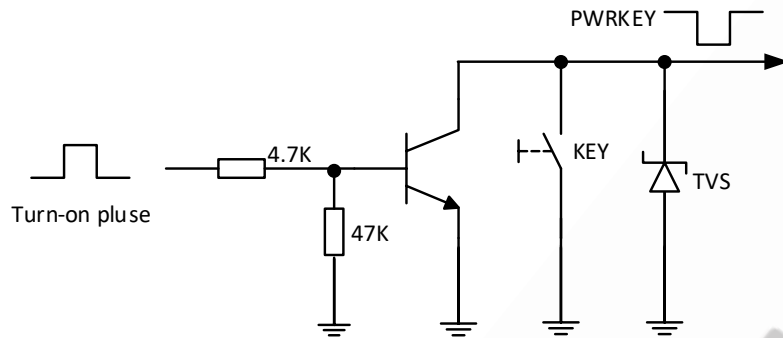


Figure 3-6 Open-Collector Driver and Pushbutton Power-On Reference Circuit

2. Automatic Power-On After Power-Up

- Connect the PWRKEY pin directly to GND with a pull-down resistor (recommended resistance $\leq 4.7K\Omega$).

Note: In the automatic power-on mode where the PWRKEY pin is directly pulled down to GND via a resistor, the system will not support shutdown functionality.

- Use the GPIO of an external MCU to set the PWRKEY pin to low level before the module is powered on (the low level must be maintained after power-on).

Notes:



- (1) In the automatic power-on mode where the PWRKEY pin is directly pulled down to GND via a resistor, the system will not support shutdown functionality.
- (2) For battery-powered application scenarios, the automatic power-on method of connecting the PWRKEY pin directly to GND is not recommended.

3.6.2 Power-off

The module can be shut down normally in the following ways:

- ✓ Normal shutdown: Controlled via the PWRKEY pin
- ✓ Normal shutdown: use the AT command (AT+ECPOWD)

1) shutdown via PWRKEY Pin

Pull the PWRKEY pin low for more than 650ms, and the module will execute the shutdown process.

During the shutdown, the module needs to deregister from the network and ensure critical data is saved by the software before complete power-off. Therefore, it is recommended to delay power-off or restart for 8 seconds after initiating the shutdown.

The timing diagram is shown below:

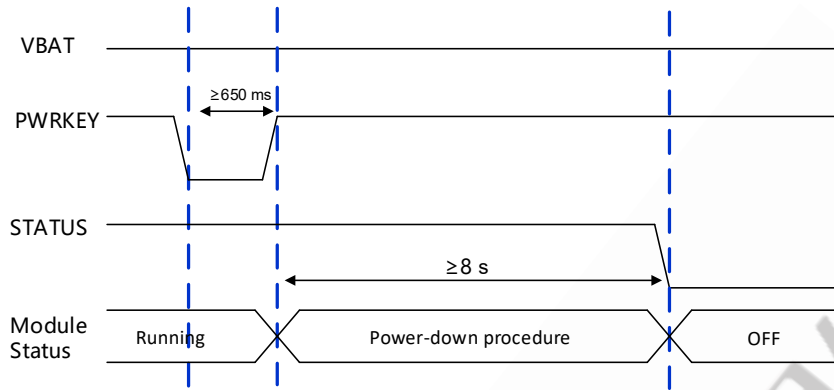


Figure 3-7 PWRKEY Shutdown Timing Diagram

2) AT Command Shutdown

Executing the AT+ECPOWD command will shut down the module. This operation has the same timing and effect as shutting down by pulling the PWRKEY pin low. At this time, it is necessary to ensure that the PWRKEY pin remains in a high-level state after executing the shutdown command; otherwise, the module cannot complete the shutdown process.

3.6.3 Reset

The RESETN pin is used for module reset. The reset signal is relatively sensitive to interference. Therefore, it is recommended that the wiring of the RESETN pin on the module interface board be as short as possible and adopt ground shielding.

The reference circuit for hardware reset is shown in the figure below:

When the module is powered on, pulling the RESETN pin low for reset will not power off the module (it remains in the powered-on state). It is recommended that the reset function be used only when AT command shutdown and PWRKEY pin shutdown fail.

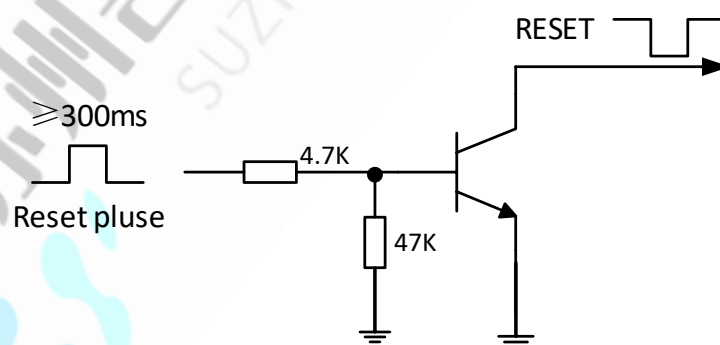


Figure 3-8 Reset Reference Circuit (RESET_N、PWRKEY)

3.7 UART

The module provides two Universal Asynchronous Receivers/Transmitters (UARTs): MAIN_UART and DBG_UART.

Table 3-5 UART

Interface	Pin	Pin Num.	IO	Power Domain	Description	Notes
MAIN UART	MAIN_RXD	60	DI	VDD_EXT	LPUART	used for AT command communication , Default 115200bps; For firmware upgrading, the default baud rate is 921600 bps
	MAIN_TXD	61	DO	VDD_EXT	LPUART	
	MAIN_RTS	48	DI	VDD_EXT	DTE Request To Send	
	MAIN_CTS	49	DO	VDD_EXT	DTE Clear To Send	
AUX UART	AUX_RXD	54	DI	VDD_EXT	Aux UART Receive Data	
	AUX_TXD	55	DO	VDD_EXT	Aux UART Transmit Data	
DBG UART	DBG_RXD	1	DI	VDD_EXT	Debug UART Receive Data	Test points need to be reserved, default baud rate 3Mbps
	DBG_TXD	2	DO	VDD_EXT	Debug UART Transmit Data	

For the AT command development method, MAIN_UART is used for AT command communication. MAIN_UART supports a fixed baud rate of 115200bps.

By default, the module's hardware flow control is disabled. When the customer requires hardware flow control, the RTS and CTS pins must be connected to the customer's end. The AT command "AT+IFC=2,2" can be used to enable hardware flow control.

The AT command "AT+IFC=0,0" can be used to disable flow control. For details, refer to the corresponding manual.

The low-power mode of MAIN_UART can wake up the module during sleep state.

➤ Main UART Characteristics:

- Includes data lines TXD and RXD, and hardware flow control lines RTS and CTS.
- 8 data bits, no parity check, 1 stop bit.
- Hardware flow control is disabled by default.
- Used for AT command transmission, data transfer, etc.
- Supported baud rates: 4900, 9600, 115200, 921600 bps, maximum 3 Mbps.

Note:

MAIN_UART outputs power-on startup information during the module's boot process.

➤ Auxiliary UART Characteristics:

- Does not support AT command interaction; used for communication with certain peripherals (e.g., connecting to GNSS).
- Shuts down after the module enters sleep mode; the module cannot be woken up by sending data to AUX_UART.

➤ Debug UART Characteristics:

- DBG_UART is used for output during software debugging; output is disabled by default. It is recommended to reserve test points for this interface.

3.7.1 UART Reference Design

The schematic diagram of the UART connection method is as follows:

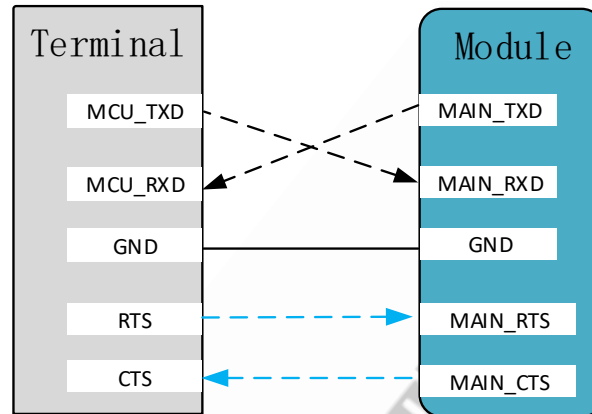


Figure 3-9 Schematic Diagram of the UART connection

Note:

Using UART connection with flow control (RTS/CTS) can improve the reliability of large-data-volume transmission and prevent data loss.

3.7.2 UART application

The UART level of the SCS527E module is 1.8V, which meets the direct UART requirements of most peripheral main controllers. However, if communication with MCUs or other UART peripherals operating at levels higher than 1.8V is needed, a level-shifting circuit must be added:

The reference circuit for level shifting is as follows:

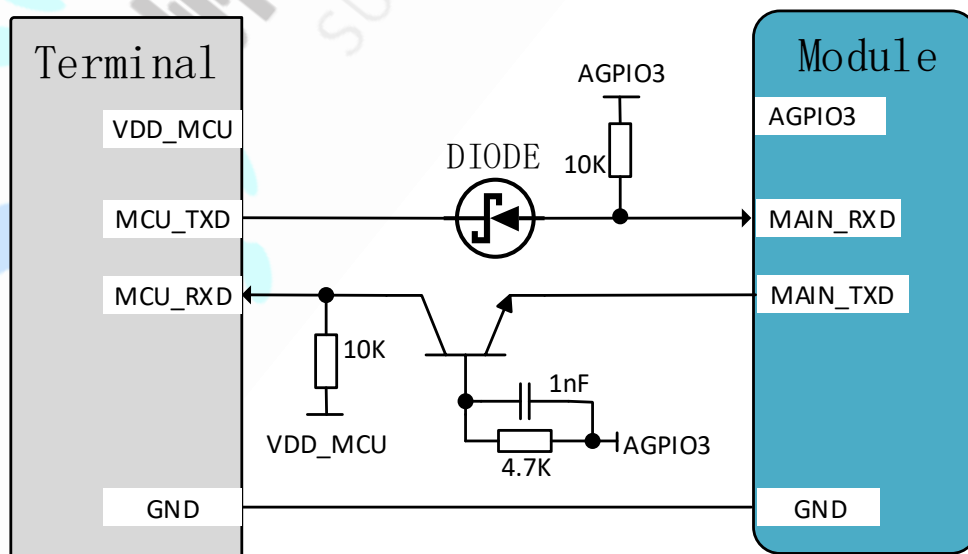


Figure 3-10 Level-Shifting Reference Circuit

Notes:

- 1) This level-shifting circuit is not suitable for applications with baud rates higher than 460800 bps. For firmware burning/upgrading, you can select a baud rate of 460800 bps or lower, but the process will take significantly longer than the default 921600 bps
- 2) VDD_EXT will power off in sleep mode. Therefore, if VDD_EXT is used as the pull-up source for UART level shifting in sleep-required scenarios, the module will fail to enter sleep mode. It is recommended to use AGPIO3 for pull-up in such scenarios.
- 3) The DIODE must be a Schottky diode with low forward voltage drop.

For applications with baud rates higher than 460800 bps, voltage conversion can be achieved by adding an external level-shifting chip. The reference circuit is as follows:

The level-shifting chip used in this circuit is TI's TXS0108E, an 8-bit bidirectional voltage level translator suitable for open-drain and push-pull applications. The maximum supported speeds are::

Push-pull: 110Mbps

Open-drain: 1.2Mbps

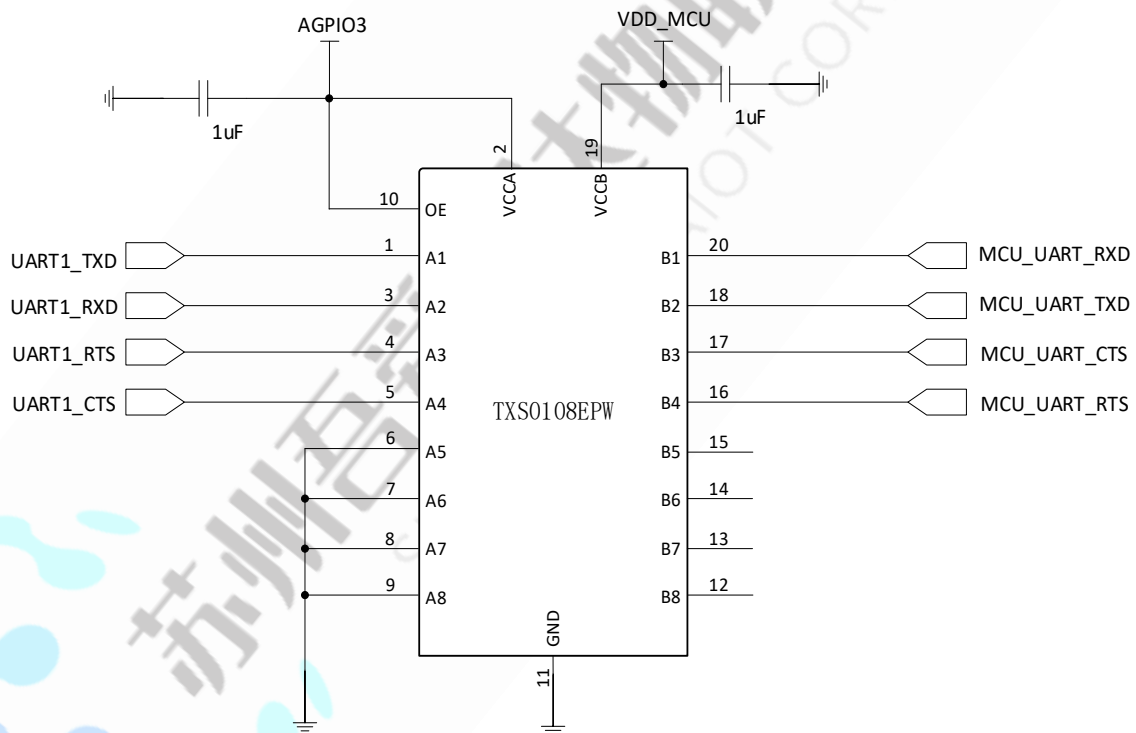


Figure 3-11 High-Baud-Rate Level-Shifting Reference Design

3.8 USB Interface

The USB interface of the SCS527E module complies with the USB 2.0 specification and supports High-Speed (480 Mbps) and Full-Speed (12 Mbps) modes. The USB interface can be used for AT command transmission, data transfer, software debugging, and software upgrading.

Table 3-6 USB Interface Definition

Pin	Pin Num.	I/O	Description	Notes
USB_DM	8	AIO	USB differential signal (-)	Complies with USB 2.0 specifications; traces must be controlled to 90-ohm differential impedance, and test points should be reserved.
USB_DP	9	AIO	USB differential signal (+)	
USB_VBUS	10	-	USB insertion wake-up	1) Internal resistor divider supports USB insertion to trigger system sleep wake-up. 2) When connected, after button power-on, the USB port can be used as a UART (for AT and DBG_UART). 3) May be left unconnected if not in use; in this case, only USB download is supported, and it cannot be used as a UART.

In design, it is recommended to use the USB interface for firmware upgrading and reserve test points for debugging. The test points are best placed on the main trace; if placed on a branch, the branch should be as short as possible.

The reference design circuit for the USB interface is as follows:

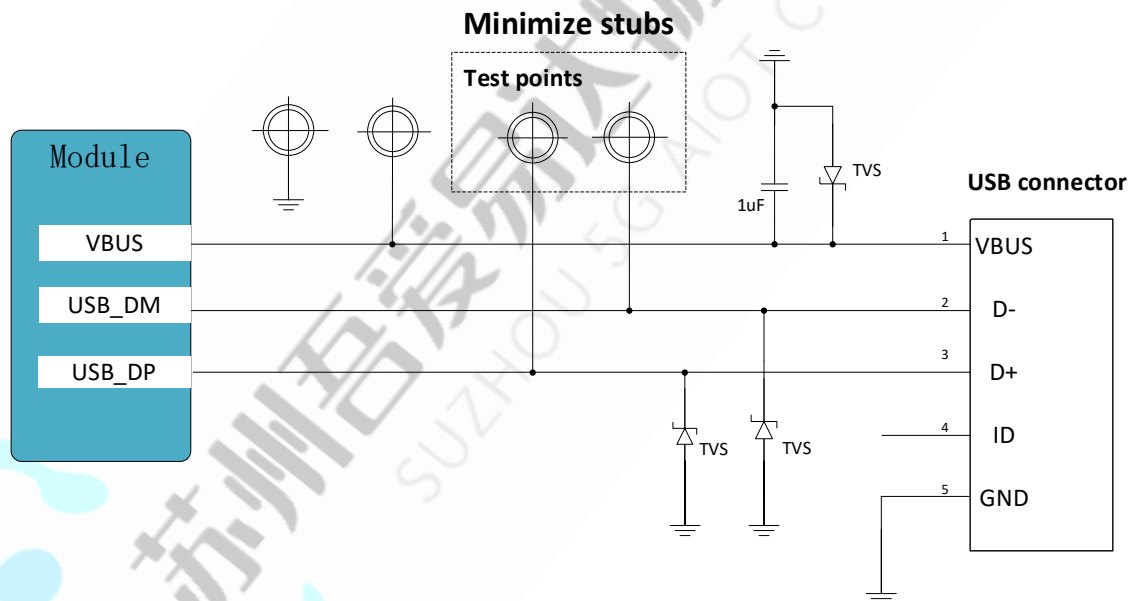


Figure 3-12 USB Reference Design

Notes:

- 1) The USB trace impedance should be designed as 90-ohm differential pairs. It is recommended to use 3D ground shielding, and ensure the traces are parallel and length-matched.
- 2) Minimize stubs on USB traces as much as possible to reduce signal reflection; test points for USB signals are best placed directly on the traces to minimize stubs.
- 3) Minimize the number of vias on USB traces as much as possible.
- 4) Add a TVS protection diode near the USB connector or test points. Due to the high speed of USB, pay attention to the selection of the TVS diode: ensure the parasitic capacitance of the selected

TVS diode is less than 1 pF.

5) USB_VBUS functions as a USB insertion wake-up source and does not directly participate in USB insertion detection. It is not mandatory and can be left unconnected in scenarios where USB insertion wake-up is not required.

3.9 USB Download

Table 3-7 USB Download Mode Interface Definition

Pin	Pin Num.	I/O	Description	Notes
USB_BOOT	3	DI	USB download mode control	Pull this pin up to VDD_EXT before power-on: the module will force-enter USB download mode. A test point for USB_BOOT is required to facilitate subsequent software upgrades.

Module Entry into USB Download Mode:

Before powering on the module, pull USB_BOOT up to VDD_EXT.

3.10 USIM Interface

The SCS527E module provides 2 sets of USIM card interfaces, supporting dual-SIM single-standby functionality—only one SIM channel can be used at a time. The USIM card interfaces comply with 3GPP specifications and support cards powered by 1.8V/3.0V. Below are the module's USIM card interfaces and reference design.

Table 3-8 USIM Pin

Pin	Pin Num.	I/O	Description	Notes
USIM_VDD	4	P0	USIM1/2 Power	Vnom=1.8/3.0V; Iomax=34mA
USIM_DATA	5	DIO	USIM1 data	Note the Application Requirements of Pull-Up Resistors
USIM_RST	6	DO	USIM1 reset	
USIM_CLK	7	DO	USIM1 clock	
GND	—	—	USIM1 GND	Common Ground with Module GND
USIM_DET	11		USIM1 insertion/removal detection,	only for USIM1, In Sleep Mode, Pull-Up to VDD_EXT is Prohibited; Pull-Up to AGPIO3 is Allowed
USIM2_DATA	32	DIO	USIM2 data	When used, an external pull-up resistor to USIM_VDD is required.
USIM2_RST	31	DO	USIM2 reset	
USIM2_CLK	34	DO	USIM2 clock	When used, an external pull-up resistor to AGPIO3 is required.

Note: When using USIM2, since the GPI04/5/6 interfaces are occupied, the CAMERA interface cannot be used.

Notes:



- (1) The VDD of USIM1 and USIM2 is supplied by PIN4 (USIM_VDD).
- (2) For USIM2, the IO level of its corresponding voltage domain (VDD_EXT) can only be configured to 1.8V, so it only supports 1.8V SIM cards.

3.10.1 Dual-SIM Switching Instructions

The module supports dual-SIM single-standby, with only one channel usable at any given time. SIM card channel switching can be performed via the corresponding AT commands; refer to the relevant command manual for specific instructions.

Notes :

- 1) The module will default to detecting the SIM1 channel upon power-on. It will only detect the SIM2 channel if no card is detected in SIM1.
- 2) USIM_DET is the SIM1 card insertion/removal detection pin, which triggers an interrupt on both rising and falling edges to initiate the system's SIM1 card presence detection. The SIM2 channel does not support SIM card insertion/removal detection.
- 3) For scenarios requiring one removable card and one soldered (embedded) card, it is recommended to place the removable card in the SIM1 channel first. This facilitates priority use of the removable card and flexibly meets various application requirements.

3.10.2 SIM Card Reference Circuit

The module supports hot-swapping of USIM Card 1 via the USIM_DET pin. This function is disabled by default and supports both high-level and low-level detection.

If the USIM card detection function is not required, the USIM_DET pin can be left floating or a 6-pin USIM card can be used.

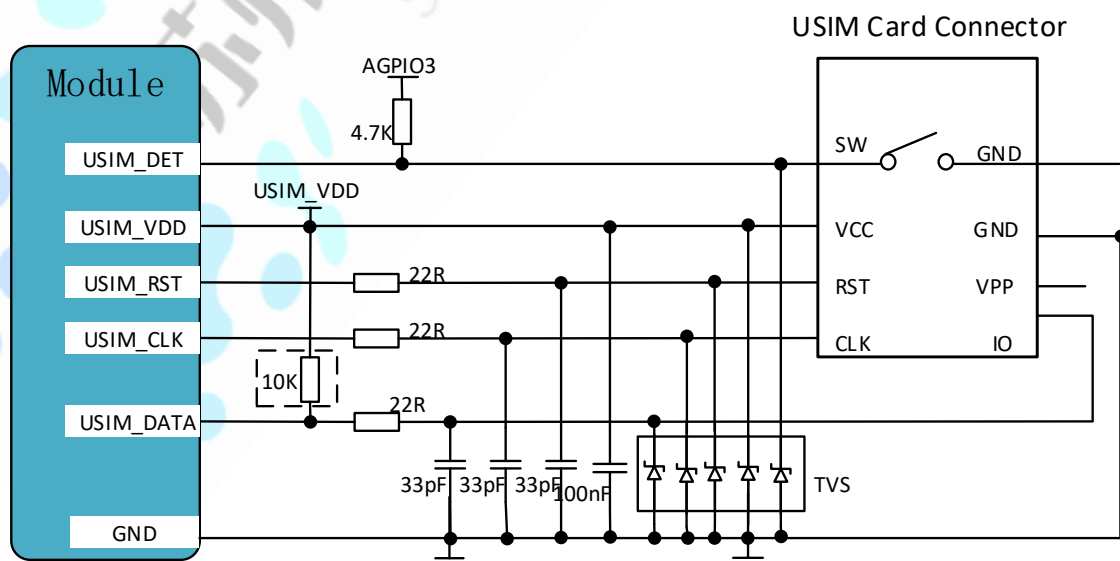


Figure 3-13 Reference Circuit- SIM1 Card(8PIN)

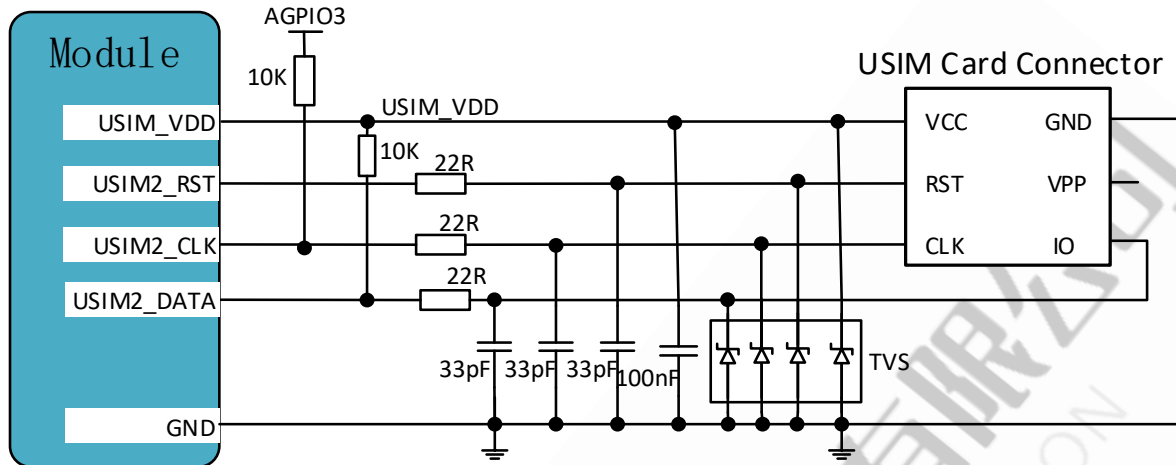


Figure 3-14 Reference Circuit- SIM2 Card(6PIN)

Notes:

To ensure the reliability and availability of the USIM card in applications, please carefully read and follow the following standards for USIM card circuit design:

- Place the USIM card and card holder as close to the chip as possible. Excessively long traces will affect signal quality, and the recommended trace length shall not exceed 20cm.
- Route USIM card signal lines away from RF traces and VBAT power supply lines.
- To avoid mutual crosstalk between USIM_DATA and USIM_CLK signals, the two traces must not be placed too close. Add ground shielding between the two traces. Meanwhile, USIM_DATA generally requires a pull-up resistor to USIM_VDD to improve driving capability. The 10K resistor marked with a dashed box in the reference design is already built-in inside the chip, so no external resistor is needed. In addition, the USIM_RST signal also requires ground protection.
- The GND trace of the USIM card should be short and thick, with a recommended trace width of no less than 0.5mm. The decoupling capacitor for USIM_VDD shall not exceed 1uF, and the capacitor should be placed close to the VCC pin of the external USIM card.
- To ensure good ESD protection performance, it is recommended to add a TVS tube near the USIM card with a parasitic capacitance of no more than 50pF. Ensure that the protected USIM card signal lines pass through the ESD protection device before connecting to the chip. A 22-ohm resistor must be connected in series between the chip and the USIM card signal lines to suppress spurious EMI and enhance ESD protection. Additionally, a 33pF capacitor connected in parallel is used to filter out RF interference.
- In scenarios where the module needs to enter sleep mode, the USIM_DET pin must not be pulled up to VDD_EXT; otherwise, the module will fail to enter sleep mode. It is recommended to use AGPIO3 for pull-up or the internal pull-up function of the USIM_DET IO pin.

3.11 I2C Interface

Table 3-9 I2C Interface

Pin	Pin Num.	I/O	Description	Notes
I2C_SDA	56	I/O	I2C Serial Data	VDD_EXT;
I2C_SCL	57	I/O	I2C Serial Clock	When used as I2C, an external pull-up resistor is required.

Up to two I2C interfaces are supported:

- ✓ Compliant with the Philips I2C standard protocol
- ✓ Supports Slow-mode (100KHz), Fast-mode (400KHz), and Fast-mode Plus (1MHz)
- ✓ Configurable for Master mode or Slave mode
- ✓ Internal pull-up resistors (1.8K or 20K) can be configured via software
- ✓ Theoretically supports up to 127 slave devices

The reference circuit for I2C is as follows:

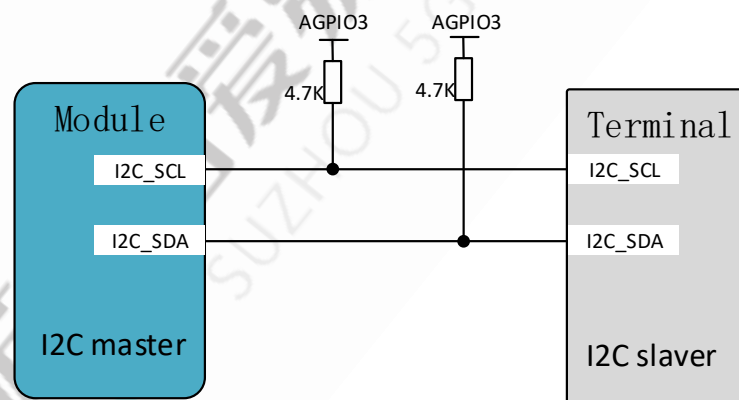


Figure 3-15 Reference circuit for I2C

The I2C interface voltage is configurable as 1.8V or 3.3V, which meets the direct requirements of most peripherals. However, if communication with peripherals operating at 5V or higher voltage levels is needed, a level-shifting circuit must be added.

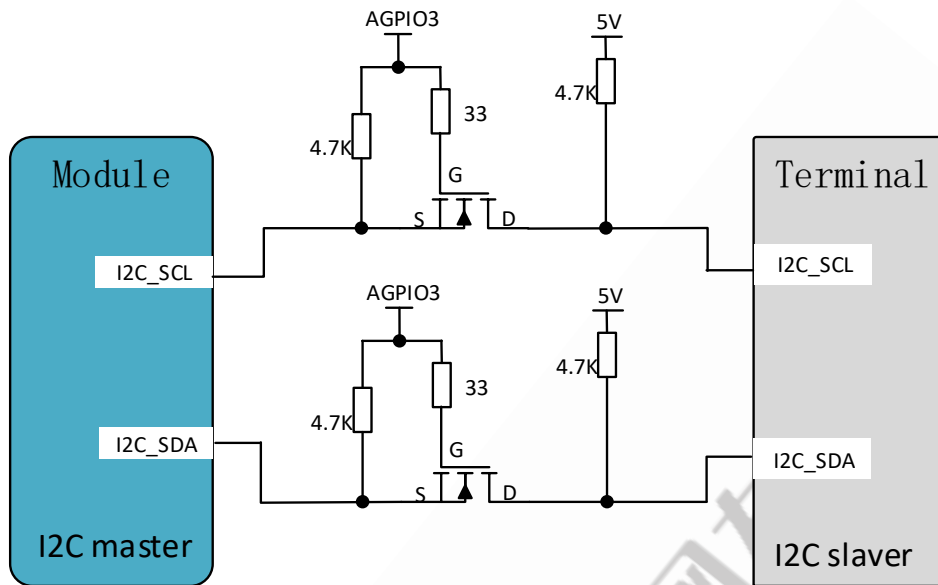


Figure 3-16 Level-shifting circuit

In the diagram above, using AGPIO3 for pull-up is recommended. In scenarios where the module does not need to enter sleep mode, or where sleep-mode power-off is acceptable, VDD_EXT can also be used for pull-up.

The NMOS transistor used for level shifting must be a model with a junction capacitance of less than 50pF.

3.12 General Purpose ADC

The module provides 2 general-purpose ADC interfaces. For wiring of the ADC interfaces, it is recommended to use ground shielding to improve the voltage measurement accuracy of the interfaces.

Table 3-10 ADC Interface Definition

Pin	Pin Num.	I/O	Description	Notes
ADC0	40	AIO	General-purpose ADC	12-bit resolution; external DC input range: 0-1.6V.
ADC1	39	AIO	General-purpose ADC	

AT+WADC=<port> can be used to read the voltage value of the ADC interface:

AT+WADC=0: Read the voltage value of ADC0

AT+WADC=1: Read the voltage value of ADC1

If the collected voltage is $\geq 1.6V$, it is recommended to use a resistor divider circuit for the ADC pin input. The resistance value of the divider resistors should not exceed 100K Ω , and the resistor tolerance should not exceed 1%. Otherwise, the measurement accuracy of the ADC will be reduced. During design, reserve a 100nF capacitor to be connected in parallel across the grounded divider resistor.

3.13 Indicator Signal Interface

3.13.1 Network Status Indication

As an indicator pin, NET_STATUS is used to indicate the module's network status and drive an LED indicator.

Table 3-11 Network Status Pin

Pin	Pin Num.	I/O	Description	Notes
NET_STATUS	20	DO	Indicates the module's network operating status; configurable to remain powered on during sleep.	

The table below describes the pin definition and logic level changes under different network states.

Table 3-12 NET_STATUS Indication Definition

Pin	Level State	Network Status
NET_STATUS	Slow flashing: on for 200 ms, off for 1800 ms	searching network status
	Slow flashing: on for 1800 ms, off for 1800 ms	Standby
	Fast flashing: on for 125 ms, off for 125 ms	Data transmission status

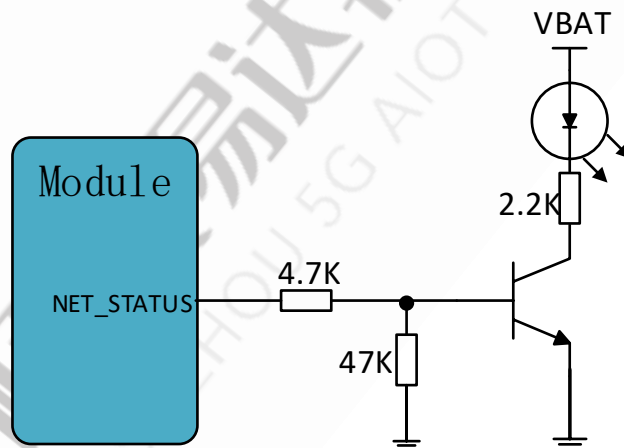


Figure 3-17 Network Status Indication Reference Design

3.13.2 Module Operating Status

As an indicator pin, STATUS is used to indicate the module's operating status. When the module boots up normally, STATUS outputs a high level to drive the LED indicator.

Table 3-13 STATUS Definition

Pin	Pin Num.	I/O	Description	Notes
STATUS	21	DO	Indicates the module's operating status	Outputs high level after boot, turning the LED on

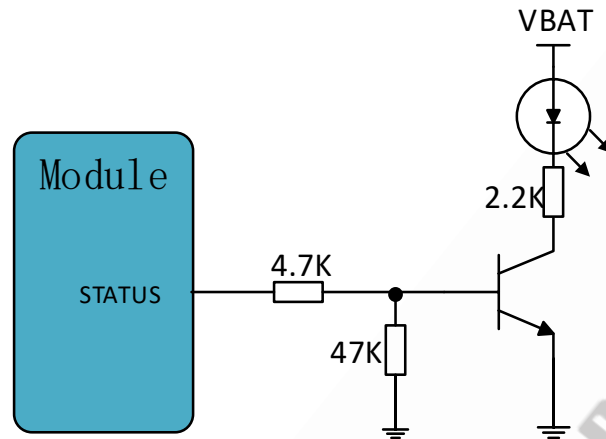


Figure 3-18 Module Operating Status Reference Design

3.13.3 MAIN_RI

MAIN_RI is a ring signal used to wake the AP (Application Processor). It can be maintained in sleep mode, with the default indication method as follows:

Table 3-14 MAIN_RI Indication Method

State	Level State
Idle	High Level
Call/SMS	When a call or SMS is received, MAIN_RI outputs low level (for at least 120ms), then returns to high level before starting data output

3.14 Other Interfaces

For other function interfaces (e.g., analog audio, LCD display, key functions) that require OPEN development, please contact us.

3.15 RF Interface

The SCS527E module provides an antenna transceiver interface for LTE Cat NB1 signal transmission. A matching antenna should be used to achieve optimal performance. The RF antenna port is a standard 50-ohm interface.

Table 3-15 RF Antenna Pin

Pin	Pin Num.	I/O	Description	Notes
LTE_ANT	46	AIO	LTE Antenna Interface	50-ohm characteristic impedance
GND	43, 44, 45, 47			

3.15.1 RF Antenna Reference Design

ANT serves as the RF antenna interface for wireless communication, with a characteristic impedance of 50Ω.

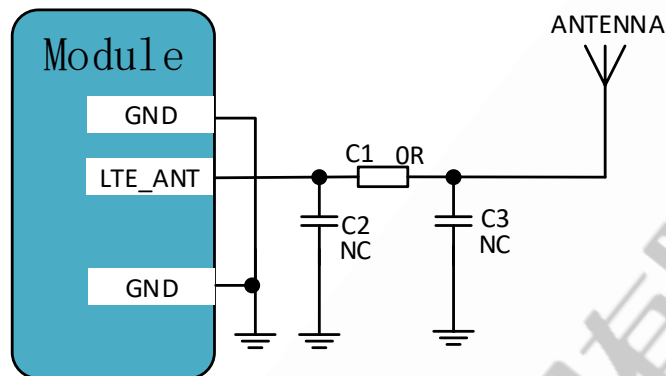


Figure 3-19 RF Antenna Reference Design

Design Notes:

1) Reserve the Π -type matching circuit (it can be used for antenna adaptation debugging; in PCB design, it is recommended to place it near the antenna end). In the default design, place a 0-ohm resistor at the position of capacitor C1, and leave C2 and C3 unpopulated. The recommended package for C1/C2/C3 components is 0201 or 0402.

3.15.2 Layout Guidelines for Common RF Signal Traces

During PCB design, the characteristic impedance of all RF signal traces should be controlled at 50Ω. There are multiple structural designs for PCB impedance trace control; the following introduces the common complete coplanar waveguide structure:

In the coplanar waveguide structure, the RF signal trace is routed on the top layer of the PCB (commonly referred to as TOP LAYER). Generally, the impedance of the RF trace is determined by the dielectric constant (ϵ_r) of the material, the width (W) of the RF trace, the gap (D) to the ground, and the thickness (H) of the reference ground dielectric plane.

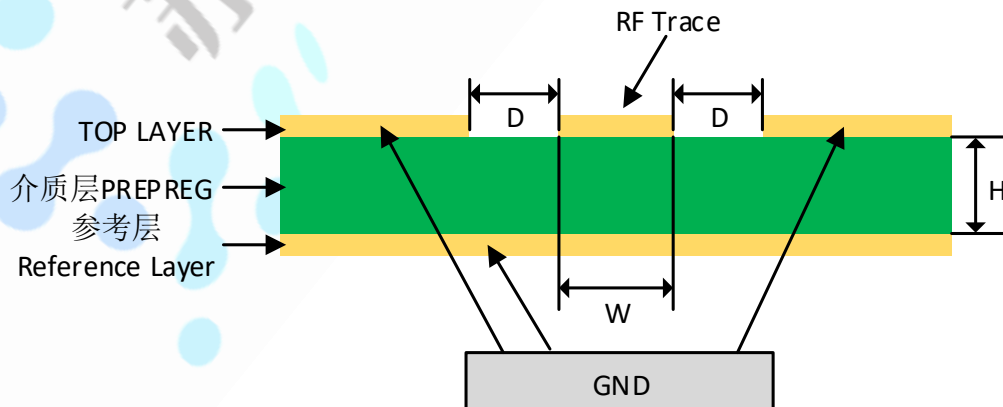


Figure 3-20 Coated Coplanar Waveguide of RF Signal Traces

In the circuit design of RF antenna interfaces, the following design principles shall be followed to ensure good performance and reliability of RF signals:

- 1) Use an impedance simulation and calculation tool; the Polar Si9000 design software is recommended. Based on the reference dielectric thickness (H) and dielectric constant of the PCB, derive the precise ground clearance (D) and RF trace width (W) to achieve higher characteristic impedance matching.
- 2) The total length of RF signal traces shall be as short as possible. Meanwhile, right-angle traces shall be avoided; a trace angle of 135° is recommended to minimize the insertion loss of RF signal traces. In addition, an appropriate number of ground vias shall be added around the reference ground adjacent to the signal traces on the same layer.
- 3) RF signal traces must be kept away from interference sources. Ensure that the layer adjacent to the RF signal traces is a complete GND plane, and no signal traces other than GND are allowed on the adjacent layer to avoid mutual signal interference.

The reference values for several common scenarios are provided below. To ensure higher impedance matching accuracy, adjust and calculate the relevant parameters according to the board manufacturer's material and process selection in practical applications. Meanwhile, it is not recommended to use excessively narrow RF trace widths (e.g., less than 0.254 mm / 10 mil), especially when the RF traces need to be relatively long.

- 1) Double-Sided PCB Design: For a double-sided PCB (finished thickness: 1.6mm, standard FR4 material), the RF trace width (W) is 0.65mm, and the trace gap (D) is 0.14mm.

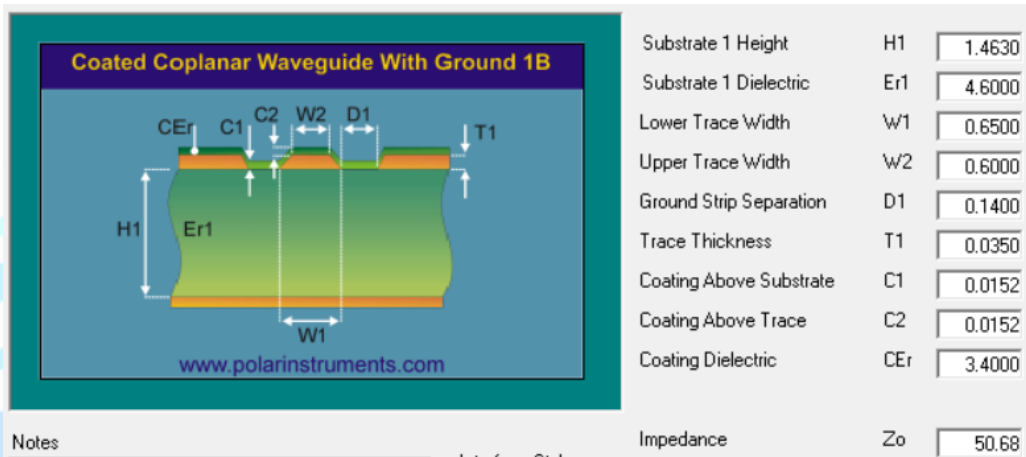


Figure 3-21 Double-Sided PCB Reference Design (H=1.6mm, FR4 material)

- 2) Double-Sided PCB Design: For a double-sided PCB (finished thickness: 1.0mm, standard FR4 material), the RF trace width (W) is 0.6mm, and the trace gap (D) is 0.14mm.

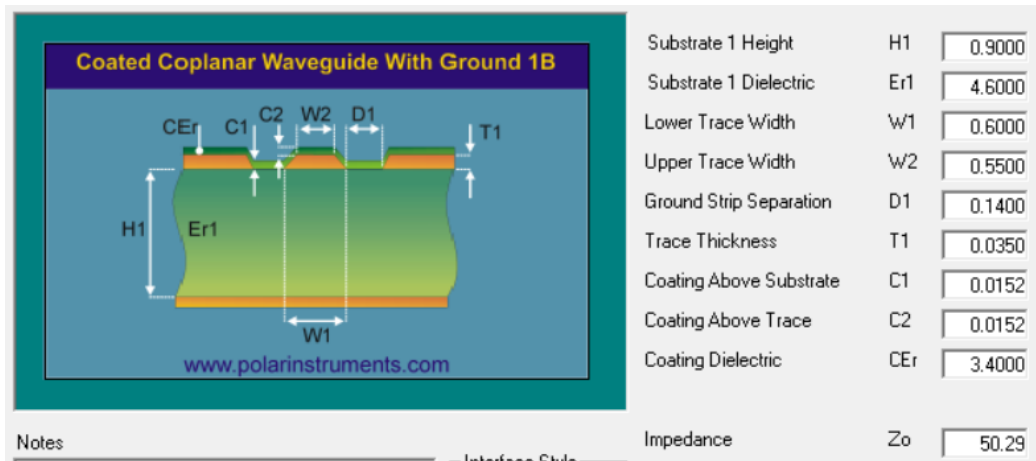


Figure 3-22 Double-Sided PCB Reference Design (H=1.0mm, FR4 material)

3) Four-Layer PCB Design: The PP (prepreg) thickness (H1) is a critical factor affecting impedance—actual W/D parameters must be adjusted based on the board manufacturer's PP model (as PP dielectric properties vary by vendor).

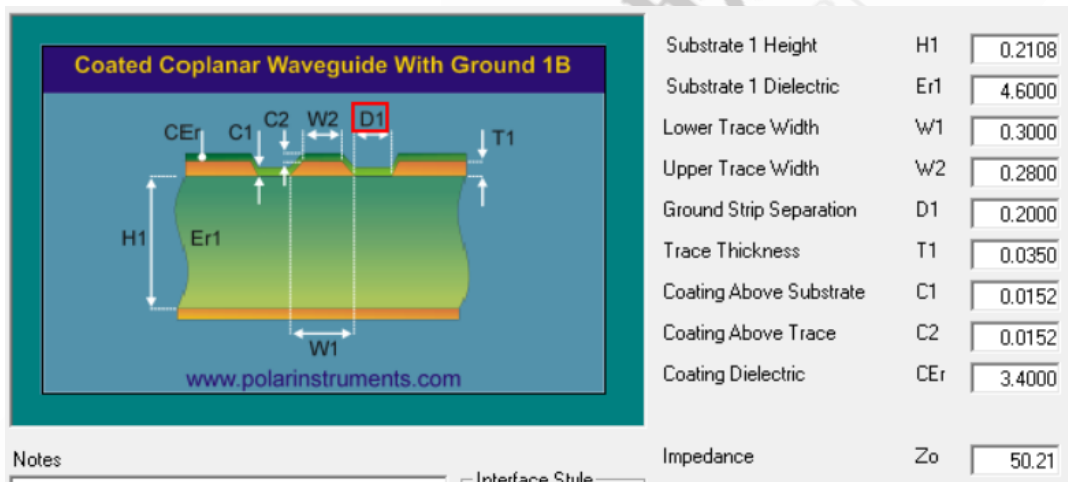


Figure 3-23 four-layer PCB (FR4, the reference layer is Layer 2)

4 Mechanical Information

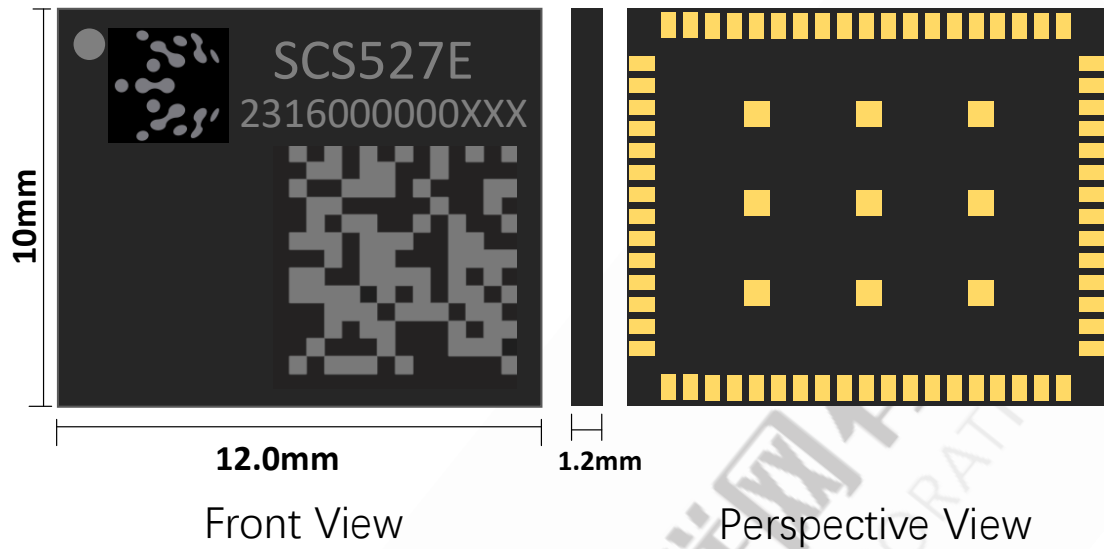
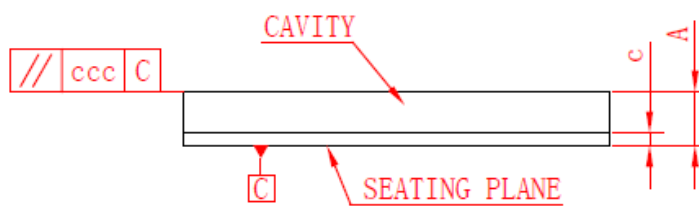
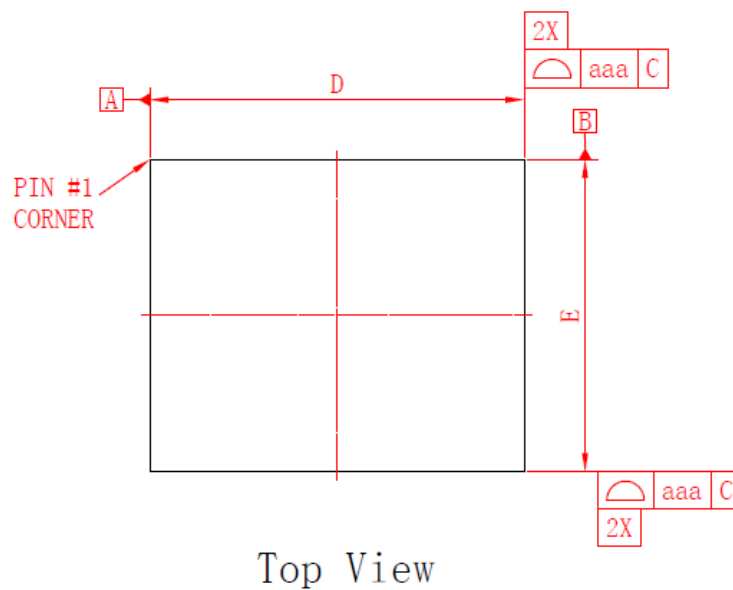
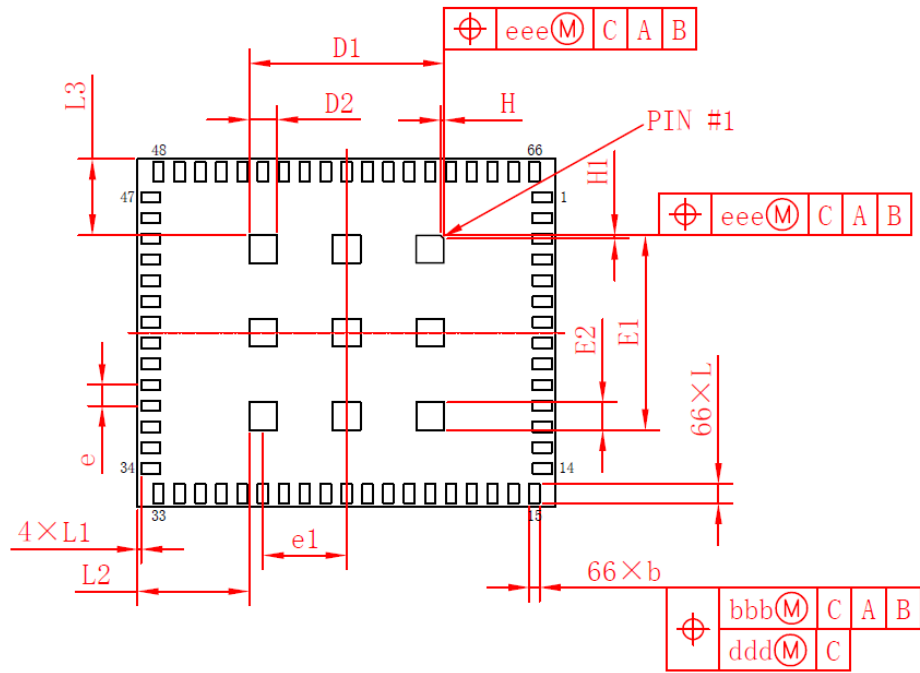


Figure 4-1 Product Illustration

4.1 Mechanical Dimensions



Side View



Bottom View

symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.100	1.200	1.300	0.043	0.047	0.051
c	0.310	0.350	0.390	0.012	0.014	0.015
D	11.900	12.000	12.100	0.469	0.472	0.476
E	9.900	10.000	10.100	0.390	0.394	0.398
D1	5.500	5.600	5.700	0.217	0.220	0.224
E1	5.500	5.600	5.700	0.217	0.220	0.224
D2	0.725	0.800	0.875	0.029	0.031	0.034
E2	0.725	0.800	0.875	0.029	0.031	0.034
H	---	0.100	---	---	0.004	---
H1	---	0.100	---	---	0.004	---
L	0.475	0.550	0.625	0.019	0.022	0.025
L1	0.025	0.100	0.175	0.001	0.004	0.007
L2	3.125	3.200	3.275	0.123	0.126	0.129
L3	2.125	2.200	2.275	0.084	0.087	0.090
e	---	0.600	---	---	0.024	---
e1	---	2.400	---	---	0.094	---
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.100			0.004		
bbb	0.150			0.006		
ccc	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		

Figure 4-2 Mechanical Dimensions

4.2 PCB Layout Footprint Suggestion

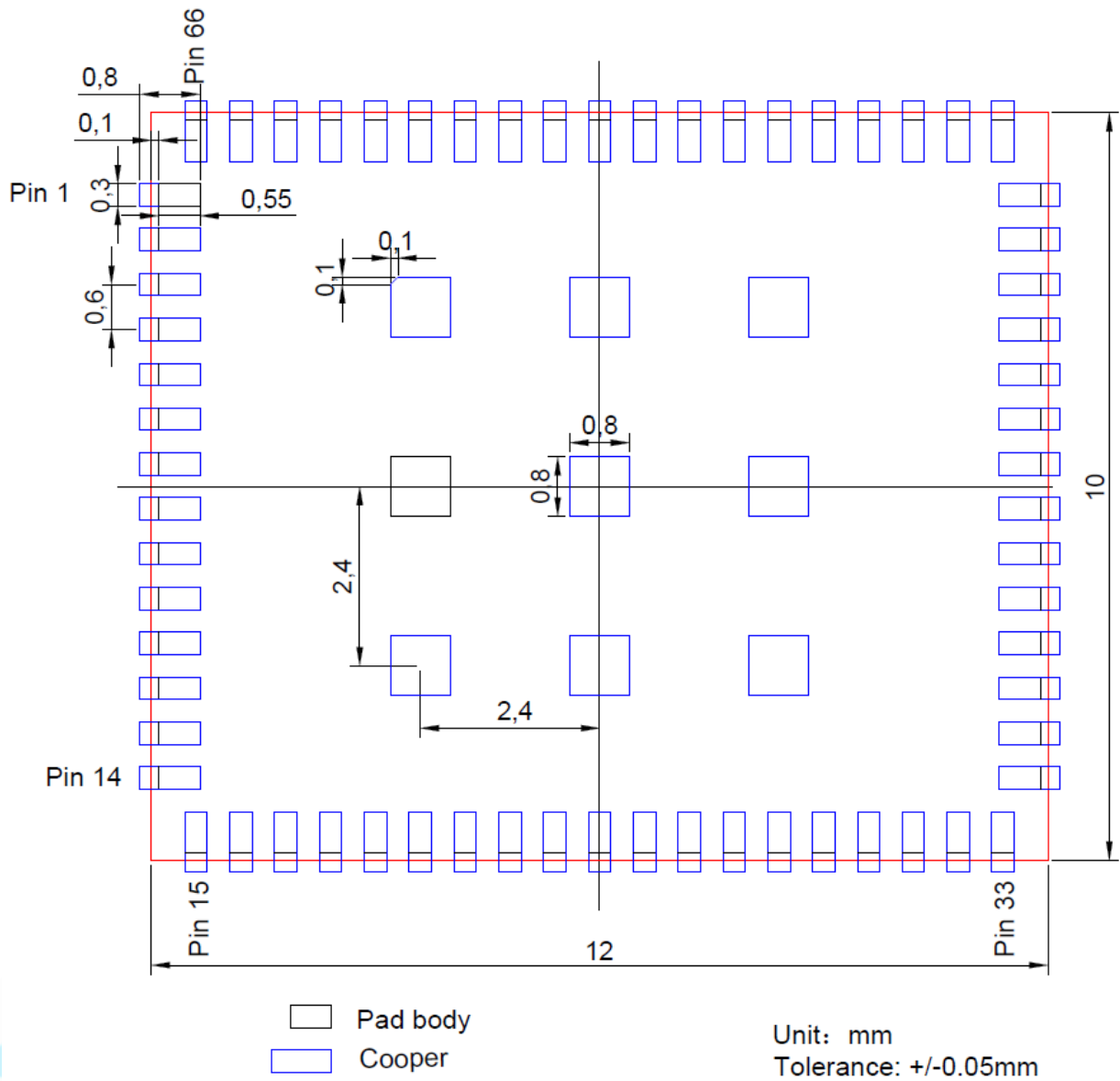


Figure 4-3 Recommendable Land Pattern

4.3 Stencil Opening Suggestion

Users can also optimize the design according to their own production process requirements:

- Stencil thickness: 0.1mm (**extremely important**). Increasing the thickness may easily cause device short circuits.
- Please note that any changes to this drawing will not be notified separately.

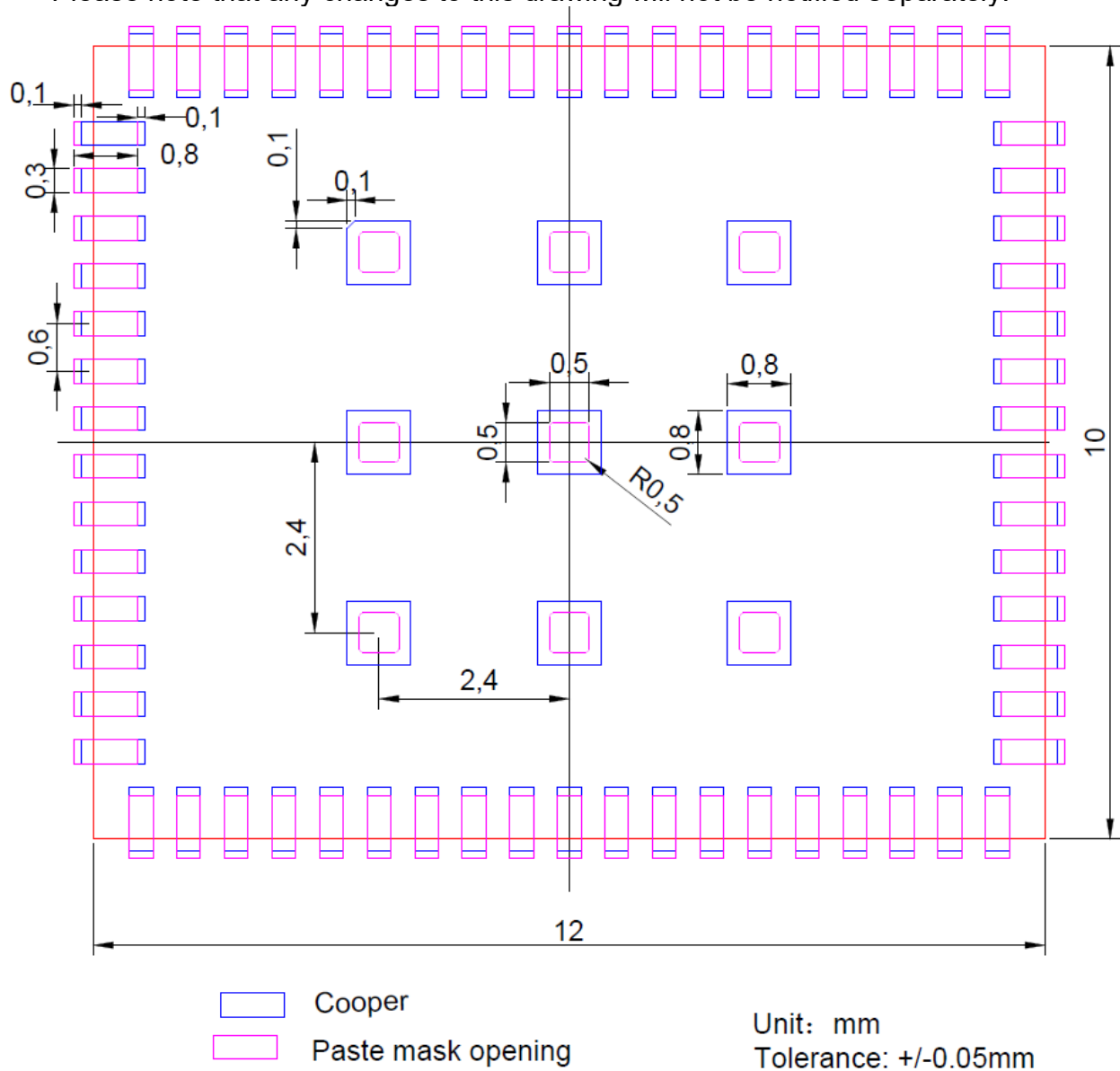


Figure 4-4 Stencil Opening Suggestion

5 Package and Storage Requirements

This chapter describes the product's factory packaging, Surface Mount Technology (SMT) process, storage, and other guidance information, which applies to product production instructions.

5.1 Product Packaging

The product is shipped in tape and reel packaging with vacuum sealing.

The dry vacuum packaging materials include: Humidity Indicator Card (HIC), Moisture Barrier Bag (MBB), and desiccant.

Users are required to inspect the product packaging before production and use (SMT), checking for packaging damage, air leakage, discoloration of the humidity indicator card, etc.

5.2 Storage Conditions

The SCS527E module is shipped in vacuum-sealed tape and reel bags with a Moisture Sensitivity Level (MSL) of 3.

Storage Conditions:

- 1) When the packaging is properly sealed, the module can maintain solderability for 12 months under conditions of temperature $< 40^{\circ}\text{C}$ and humidity $< 90\% \text{ RH}$.
- 2) After unpacking, the module must be assembled via SMT within 168 hours under environmental conditions of temperature $< 30^{\circ}\text{C}$ and relative humidity $< 60\% \text{ RH}$.

If the above conditions are not met, or if the humidity indicator card shows that baking is required at $23\pm 5^{\circ}\text{C}$, refer to the specifications of "IPC/JEDEC J-STD-033" for baking guidelines. Baking can be performed at $125^{\circ}\text{C}\pm 5^{\circ}\text{C}$ with humidity $\leq 60\% \text{ RH}$ for 8 hours, and the cumulative baking time shall not exceed 96 hours.

Notes:

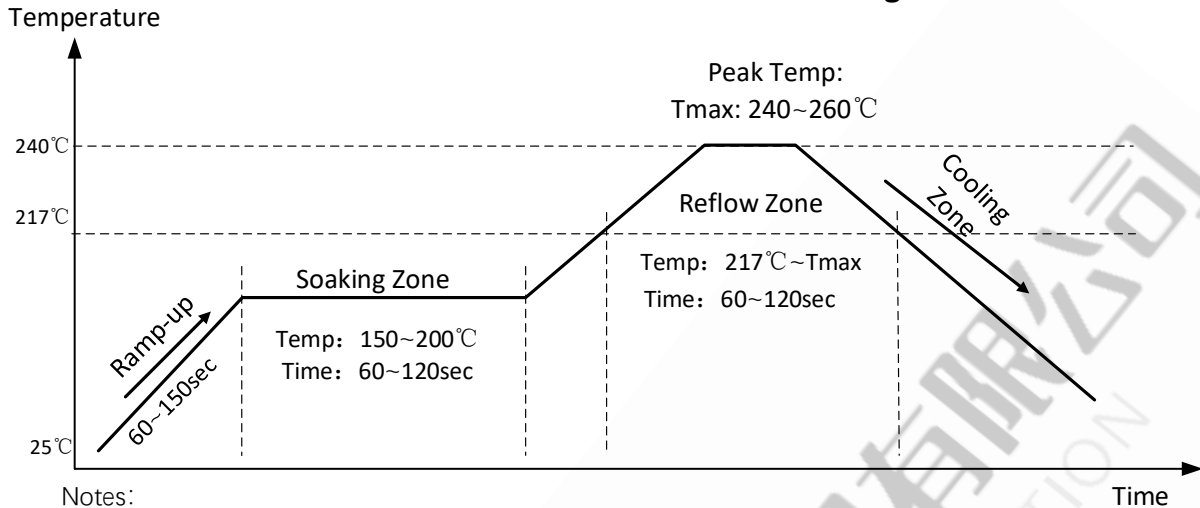
- 1) The module's packaging cannot withstand such high temperatures. Remove the module from its packaging before baking. For short-duration baking, refer to the IPC/JEDEC J-STD-033 specification.
- 2) Pay attention to Electrostatic Discharge (ESD) protection when unpacking and handling the module, e.g., wear anti-static gloves.

5.3 Soldering and Mounting Instructions

This product is packaged using a lead-free process. It is recommended that the reflow soldering process parameters be set in accordance with JEDEC standards. Please refer to the design specifications for lead-free reflow soldering temperature profiles in JEDEC J-STD-020 for configuration.

As a recommendation, the SMT lead-free reflow soldering profile is shown in the figure below.

Reference for Lead-Free Reflow Soldering Process



Notes:

1. Preheating Zone

The temperature rise rate shall be 1-2°C/s to prevent solder paste slumping caused by rapid temperature increase.

Insufficient preheating time tends to cause the formation of large solder balls; on the contrary, excessive preheating will lead to dense occurrence of both small and large solder balls.

2. Soaking Zone

The temperature in this zone must rise slowly and steadily. Otherwise, it is prone to poor soldering. The temperature shall increase stably from 150°C to 200°C at a rate of <1°C/s.

3. Reflow Zone

The temperature profile shall follow the range of 217°C ~ Tmax ~ 217°C, with a target dwell time of 60-90 seconds and a temperature rise rate of 1-3°C/s. Avoid excessive temperature rise rate to prevent solder paste slumping. For components with large heat capacity that cannot meet the above time requirement, the reflow dwell time can be extended to 120 seconds. The temperature resistance standard of the package shall comply with IPC/JEDEC J-STD-020D.

4. Cooling Zone

The temperature shall drop from Tmax to 180°C at a rate of ≤4°C/s to ensure rapid cooling of the solder joints.

***The above lead-free reflow soldering profile is for reference only. Customers shall make appropriate adjustments according to actual production conditions.**

Figure 5-1 Reference for Lead-Free Reflow Soldering Process

Table 5-1 Lead-Free Device Package Temperature Resistance Standard (IPC/JEDEC J-STD-020D)

Package Thickness	Volume(mm ³) < 350	Volume (mm ³) 350~2000	Volume (mm ³) > 2000
< 1.6mm	260°C	260°C	260°C
1.6mm~2.5mm	260°C	250°C	245°C
> 2.5mm	250°C	245°C	245°C

5.4 Disposal

The disposal of the company's products shall comply with applicable local/regional/national/international regulations.

Frequency Bands:

LTE Band 1: 1920 MHz to 1980 MHz
LTE Band 3: 1710 MHz to 1785 MHz
LTE Band 8: 880 MHz to 915 MHz
LTE Band 20: 832 MHz to 862 MHz
LTE Band 34: 2010MHz to 2025MHz
LTE Band 38: 2570 MHz to 2620 MHz
LTE Band 40: 2305 MHz to 2400MHz
LTE Band 41: 2496 MHz to 2690MHz

LTE Band 1: 24.13dBm
LTE Band 3: 24.43dBm
LTE Band 8: 24.51dBm
LTE Band 20: 24.29dBm
LTE Band 34: 24.50dBm
LTE Band 38: 24.28dBm
LTE Band 40: 24.86dBm
LTE Band 41: 24.77dBm

Modulation Mode: QPSK/16QAM

Antenna: Rod-shaped Antenna Antenna

Antenna Gain: LTE: B1: 3dBi; B3: 3dBi; B8: 2dBi; B20: 2dBi; B34: 3dBi; B38: 4dBi;
B40: 3dBi; B41: 4dBi

CE Maintenance

The device complies with RF specifications when the device used at 20cm you're your body.

Declaration of Conformity

Suzhou Wuai Yida Internet of Things Co., Ltd hereby declares that this LTE Cat.1
Communication Module is in compliance with the essential requirements and other
relevant provisions of Directive 2014/53/EU. In accordance with Article 10(2) and Article
10(10), This product is allowed to be used in all EU member states.



KDB 996369 D03 statements

2.2 List of applicable FCC rules:

The module complies with FCC Part 22H and 24E, 27, 90.

FCC ID: 2BTZW-SCS527E on User manual and on the external of the packaging.

2.3 Summarize the specific operational use conditions

The module is only designed to be implemented in Grantee's host devices. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

2.4 Limited module procedures

The module did not contain RF shield, so consider as limited single module.

2.5 Trace antenna designs

Not applicable

2.6 RF exposure considerations

This equipment complies with FCC's RF radiation exposure limits set forth for an uncontrolled environment.

The antenna(s) used for this transmitter must not be collocated or operating in conjunction with any other antenna or transmitter.

2.7 Antennas

Dipole antenna, antenna gain: Band 2: -2dBi, Band 4: -2dBi, Band 5: -3dBi, Band 12: -3dBi, Band 17: -3dBi, Band 25: -2dBi, Band 26: -3dBi, Band 38: -1dBi, Band 40: -1dBi, Band 41: -1dBi, Band 66: -2dBi

Label and compliance information

The host system using this module, should have label in a visible area indicated the following texts: "Contains FCC ID: 2BTZW-SCS527E"

2.9 Information on test modes and additional testing requirements

When testing host product, the host manufacture should follow FCC KDB Publication 996369 D04 Module Integration Guide for testing the host products. The host manufacturer may operate their product during the measurements. In setting up the configurations, if the pairing and call box options for testing does not work, then the host product manufacturer should coordinate with the module manufacturer for access to test mode software.

The module has been certified for Potable applications. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

2.10 Additional testing, Part 15 Subpart B disclaimer

The module without unintentional-radiator digital circuitry, so the module does not require an evaluation by FCC Part 15 Subpart B. The host should be evaluated by the FCC Subpart B.

2.11 Note EMI Considerations

host manufacture is recommended to use D04 Module Integration Guide recommending as "best practice" RF design engineering testing and evaluation in case non-linear interactions generate additional non-compliant limits due to module placement to host components or properties.

2.12 How to make changes

This module is stand-alone modular. If the end product will involve the Multiple simultaneously transmitting condition or different operational conditions for a stand-alone modular transmitter in evaluation (i.e., no C2PC required when no emission exceeds the limit of any individual device (including unintentional radiators) as a composite. The host manufacturer must fix any failure a host, host manufacturer have to consult with module manufacturer for the installation method in end system. According to the KDB 996369 D02 Q&A Q12, that a host manufacture only needs to do an evaluation (i.e., no C2PC required when no emission exceeds the limit of any individual device (including unintentional radiators) as a composite. The host manufacturer must fix any failure.

FCC Caution.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference, and
- (2) this device must accept any interference received, including interference that may cause undesired operation.

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

C2PC test plan

The modular has no RF shielding as required in §15.212(a) (1)i) and it cannot be tested in a stand-alone configuration as required in §15.212(a)(1), as required in KDB 996369 D01 V03, C2PC is required for every different specific host using the module.

The following tests will be performed according to FCC Part 22H and 24E, 27 on the host which installed this modular:

Conducted Power & ERP & EIRP

The following list shows the maximum conducted power of the module. When testing the conducted power within the host, it should not exceed the maximum conducted power of the modular.

ERP and EIRP must comply with FCC standard limits.

Note: EIRP = Conducted Power + Ant Gain

ERP = EIRP - 2.15

Maximum conducted power of modular		
LTE Band	Power(dBm)	Power(W)
Band2	24.61	0.2891
Band4	24.34	0.2716
Band5	24.48	0.2805
Band12	24.40	0.2754
Band17	24.45	0.2786
Band25	24.64	0.2911
Band26(814-824)	21.30	0.1349
Band26(824-849)	21.23	0.1327
Band38	24.95	0.3126
Band40(2305-2315)	21.14	0.1300
Band40(2350-2360)	21.37	0.1371
Band41	25.11	0.3243
Band66	24.35	0.2723

99% Bandwidth

Test all low and high channels of LTE Band bandwidth to ensure that the operating frequency is within the LTE band.

Conducted Band Edge

Test all low and high channels of LTE Band bandwidth to ensure that the host also meets Band edge requirements.

Radiated Spurious Emission

Test the low, middle, and high channels of the LTE Band's maximum bandwidth to ensure that the host also meets radiated spurious emissions requirements.

The following list is the LTE Band test setup parameters:

ITEMS	Band	Bandwidth (MHz)						Modulation		RB #			Test Channel		
		1.4	3	5	10	15	20	QPSK	16QAM	1	Half	Full	L	M	H
Conducted Power & ERP & EIRP	2	v	v	v	v	v	v	v	v	v	v	v	v	v	v
	4	v	v	v	v	v	v	v	v	v	v	v	v	v	v
	5	v	v	v	v			v	v	v	v	v	v	v	v
	12	v	v	v	v			v	v	v	v	v	v	v	v
	17			v	v			v	v	v	v	v	v	v	v
	25	v	v	v	v	v	v	v	v	v	v	v	v	v	v
	26	v	v	v	v	v		v	v	v	v	v	v	v	v
	38	v	v	v	v	v	v	v	v	v	v	v	v	v	v
	40			v	v			v	v	v	v	v	v	v	v
	41	v	v	v	v	v	v	v	v	v	v	v	v	v	v
	66	v	v	v	v	v	v	v	v	v	v	v	v	v	v
99% Bandwidth	2	v	v	v	v	v	v	v	v			v	v		v
	4	v	v	v	v	v	v	v	v			v	v		v
	5	v	v	v	v			v	v			v	v		v
	12	v	v	v	v			v	v			v	v		v
	17			v	v			v	v			v	v		v
	25	v	v	v	v	v	v	v	v			v	v		v
	26	v	v	v	v	v		v	v			v	v		v
	38	v	v	v	v	v	v	v	v			v	v		v
	40			v	v			v	v			v	v		v
	41	v	v	v	v	v	v	v	v			v	v		v
	66	v	v	v	v	v	v	v	v			v	v		v
Conducted Band Edge	2	v	v	v	v	v	v	v	v	v		v	v		v
	4	v	v	v	v	v	v	v	v	v		v	v		v
	5	v	v	v	v			v	v	v		v	v		v
	12	v	v	v	v			v	v	v		v	v		v
	17			v	v			v	v	v		v	v		v

	25	v	v	v	v	v	v	v	v	v		v	v		v
	26	v	v	v	v	v		v	v	v		v	v		v
	38	v	v	v	v	v	v	v	v	v		v	v		v
	40			v	v			v	v	v		v	v		v
	41	v	v	v	v	v	v	v	v	v		v	v		v
	66	v	v	v	v	v	v	v	v	v		v	v		v
Radiated Spurious Emission	2						v	v		v			v	v	v
	4						v	v		v			v	v	v
	5				v			v		v			v	v	v
	12				v			v		v			v	v	v
	17				v			v		v			v	v	v
	25						v	v		v			v	v	v
	26				v	v		v		v			v	v	v
	38						v	v		v			v	v	v
	40				v			v		v			v	v	v
	41						v	v		v			v	v	v
	66						v	v		v			v	v	v