CD6697BL TECHNICAL DESCRIPTION

This unit is powered by an AC-DC converter with 14.5V DC supply, after some necessary regulator circuits, then distribute the power supply to MCU (IC602 GS3012), CD (IC601 CD5888CB), Bluetooth Module (BT101 WB9805 with FM radio function), Volume control IC (IC401 CFC2314F), Power amplifier (IC2 WE8810), and USB changer (IC502 FP6115) respectively. 16.9344MHz crystal (X601) is clock for digital audio. 32.768kHz crystal (X602) is clock for MCU (IC602 GS3012) Another 32.768kHz crystal (X101) is for the FM tuner in the Bluetooth module (BT101 WB9805). 3196A (IC101) is LED driver. The unit accepts 120VAC.

CD mode:

When starting up the unit, the software defaults to CD function. MCU issues a Command to start up CD and go into CD mode, also enables the Volume Control IC to work in CD Channel, through CD Mechanism to read and get the data of CD R/RW Disc, and after data processing by MCU, output L&R channel audio signals, and performing volume and EQ control by Volume Control IC, then output to Power Amplifier for amplifying the audio signal and drive the external Speakers.

FM Radio mode:

Input MCU command by Keyboard and turn to Radio Receiver, and turn on the power supply of Radio Receiver in Bluetooth module, also enables the Volume Control IC to work in Radio Channel. It will convert the radio RF signals received into audio signals, and output through the Radio channel of Volume Control IC, then via Power Amplifier to the external Speakers.

Bluetooth mode: (BT101 WB9805)

26MHz crystral (YB1) provide clock signal for Bluetooth 2.1 + EDR compliant radio RF IC (UB1 RDA5876). UZ1 (ATS2805A) is MCU and audio DSP. UN1 (QH16-104HIP) is serial 16Mb EEPROM for parameter backup. 32.768kHz crystal (YZ1) provides clock for UZ1.

Input MCU command by Keyboard, switch to Bluetooth mode, and enables MCU to issue a Command to start up the Bluetooth Module, Volume control IC, power supply of the Power amplifier, and make Volume control IC turn to work in Bluetooth Channel. The Bluetooth Module use a PCB antenna, and works in the frequency range of 2.402GHz ～ 2.480GHz. Modulation type is GFSK. The Bluetooth Module will convert the Bluetooth signals into to Audio signals, and output to the Power Amplifier for amplifying through the Bluetooth Channel of Volume Control IC, and then drives the Speakers by the Amplifier.

Aux mode:

Input the command into the MCU by keyboard, and switch to AUX mode.
External Audio signal input to Volume Control IC via 3.5MM Jack for volume and EQ control, and output Audio Signal to Power Amplifier for amplifying, and then drives the Speakers by the Amplifier.

USB Changer:

Supply 5V (Maximum 500mA) from DC/DC converter (IC502 FP6115), and charge to the external device through USB 2.0 Jack.

2.4GHz Bluetooth Module:
Modulation Type: GFSK
Antenna Type: Integral, Internal (PCB Trace)
Frequency Range: 2402MHz - 2480MHz, 1MHz channel spacing, 79 channels

Nominal field strength is 108.8dBuV/m @ 3m
Production Tolerance of field strength is +/- 3dB
Antenna gain is 0dBi

Channel Frequency Table of Bluetooth Module

CH. NO.	FRE.	Hex Value		CH. NO.	FRE.	Hex Value		CH. NO	FRE.	Hex Value		CH. NO	FRE.	Hex Value
CH0	2402MHz	0		CH26	2428MHz	1A		CH52	2454MHz	34		CH78	2480MHz	4E
CH1	2403MHz	1		CH27	2429MHz	1B		CH53	2455MHz	35				
CH2	2404MHz	2		CH28	2430MHz	1C		CH54	2456MHz	36				
CH3	2405MHz	3		CH29	2431MHz	1D		CH55	2457MHz	37				
CH4	2406MHz	4		CH30	2432MHz	1E		CH56	2458MHz	38				
CH5	2407MHz	5		CH31	2433MHz	1F		CH57	2459MHz	39				
CH6	2408MHz	6		CH32	2434MHz	20		CH58	2460MHz	3A				
CH7	2409MHz	7		CH33	2435MHz	21		CH59	2461MHz	3B				
CH8	2410MHz	8		CH34	2436MHz	22		CH60	2462MHz	3C				
CH9	2411MHz	9		CH35	2437MHz	23		CH61	2463MHz	3D				
CH10	2412MHz	A		CH36	2438MHz	24		CH62	2464MHz	3E				
CH11	2413MHz	B		CH37	2439MHz	25		CH63	2465MHz	3F				
CH12	2414MHz	C		CH38	2440MHz	26		CH64	2466MHz	40				
CH13	2415MHz	D		CH39	2441MHz	27		CH65	2467MHz	41				
CH14	2416MHz	E		CH40	2442MHz	28		CH66	2468MHz	42				
CH15	2417MHz	F		CH41	2443MHz	29		CH67	2469MHz	43				
CH16	2418MHz	10		CH42	2444MHz	2A		CH68	2470MHz	44				
CH17	2419MHz	11		CH43	2445MHz	2B		CH69	2471MHz	45				
CH18	2420MHz	12		CH44	2446MHz	2C		CH70	2472MHz	46				
CH19	2421MHz	13		CH45	2447MHz	2D		CH71	2473MHz	47				
CH20	2422MHz	14		CH46	2448MHz	2E		CH72	2474MHz	48				
CH21	2423MHz	15		CH47	2449MHz	2F		CH73	2475MHz	49				
CH22	2424MHz	16		CH48	2450MHz	30		CH74	2476MHz	4A				
CH23	2425MHz	17		CH49	2451MHz	31		CH75	2477MHz	4B				
CH24	2426MHz	18		CH50	2452MHz	32		CH76	2478MHz	4C				
CH25	2427MHz	19		CH51	2453MHz	33		CH77	2479MHz	4D				

WB-9805 Bluetooth Module Operation Manual

1. Product Description

WB-9805 is a high performance Bluetooth audio module. It contains a Bluetooth radio communication core IC supporting Bluetooth devices such as mobile phone. The module incorporates an audio DSP with 16-bit DAC. The DAC output can directly drive earphone. The Bluetooth module is using Bluetooth 2.1 + EDR with data rate up to 3M bit/sec.

2. Application

The Bluetooth module is suitable for communication with notebook computer, mobile phone, PDA, and other digital Bluetooth devices:
* Bluetooth audio
* Stereo Bluetooth headphone
* Bluetooth handfree device
* Buuilt-in FM radio
* Support keypad control and LED dispaly

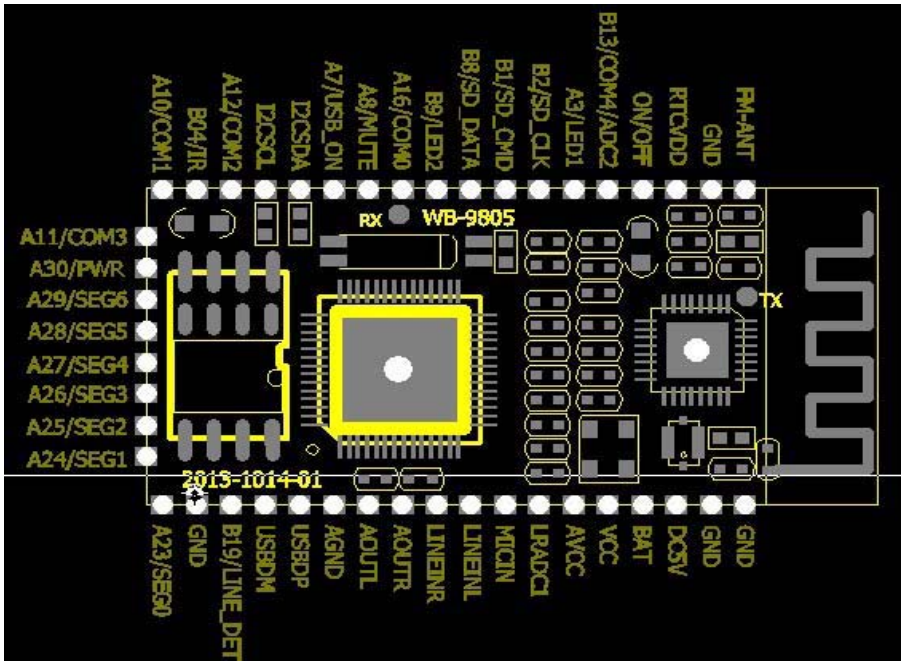
3. Product Specification

Model	WB 9805
Bluetooth Standard	Bluetooth V2.1+EDR
Support Protocol	AVCTP 1.0，AVRCP 1.0，GAVDP 1.2，AVDTP 1.0，A2DP 1.2，Hands-Free Profile 1.5，Headset Profile v1.1
Operating current	60mA
Standby current	<0.03 mA
Working Voltage	DC5V or VBAT (3.4V to 4.2V)
Temperature range	-20 C to +55 C
Wireless distance	15 metre
Transmit power	CLASS2 4dBm (max)
Sensitivity	-80dBm@0.1%BER
Frequency range	2.4GHz-2.480GHz
External connection	PIO, SPI，Speake，Microphone
Audio Performance	High acoustic fidelity sound
Audio S/N ratio	≥75dB
Disrortion	≤0.01%
Dimension	15X32X 2.5 MM

4. Product Photo

WB-9805

5. Pin Connection



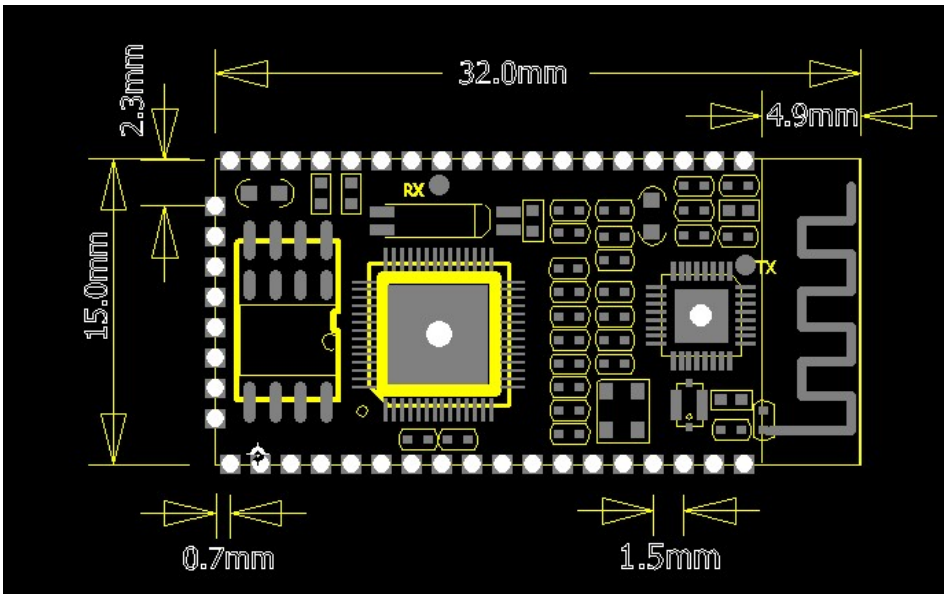
WB-9805

6. Pin Configuration

No	Name	Function
1	FM_ANT	FM antenna
2	GND	Ground
3	RTCVDD	Internal supply
4	ON/OFF	Power and reset
5	GPIO_B13	GPIO port
6	GPIO_A3	GPIO port
7	GPIO_B2	SD and CLK
8	GPIO_B1	SD and CMD
9	GPIO_B8	SD and DAT0
10	GPIO_B9	GPIO port
11	GPIO_A16	GPIO port
12	GPIO_A8	GPIO port
13	GPIO_A7	GPIO port
14	I2CSDA	GPIO_A6 and I2C
15	I2CSCL	GPIO_A5 and I2C
16	GPIO_A12	GPIO port
17	IR	GPIO_B04 IR
18	GPIO_A10	GPIO port
19	GPIO_A11	GPIO port
20	GPIO_A30	GPIO port
21	GPIO_A29	GPIO port
22	GPIO_A28	GPIO port
23	GPIO_A27	GPIO port
24	GPIO_A26	GPIO port
25	GPIO_A25	GPIO port
26	GPIO_A24	GPIO port
27	GPIO_A23	GPIO port
28	GND	Ground
29	GPIO_B19	GPIO port
30	USBDM	USB --DM
31	USBDP	USB --DP
32	AGND	Analog Ground
33	AOUTL	Analog out L
34	AOUTR	Analog out R

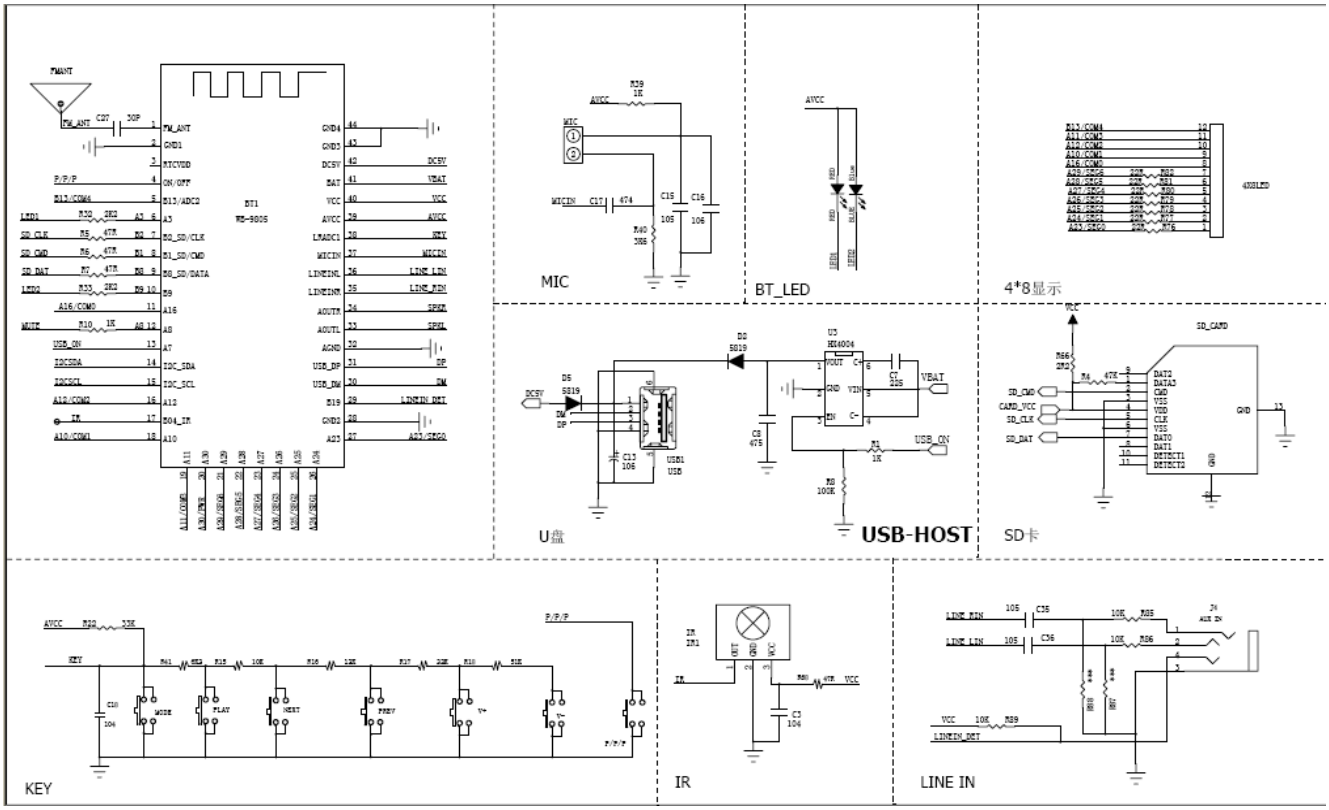
35	LINEINR	Line in R
36	LINEINL	Line in L
37	MICIN	mic input
38	LRADC1	ADC control
39	AVCC	ATS2805A analog supply
40	VCC	ATS2805A digital supply
41	VBAT	Battery supply 3.4V to 4.2V
42	DC5V	5V supply 4.75V～5.25V
43	GND	Ground
44	GND	Ground

7. PCB Deminsion



WB-9805 PCB

8. Circuit Diagram



RDA5876

SINGLE CHIP FOR BLUETOOTH & FM RADIO TUNER

Rev.1.2–07.2011

1 General Description

RDA5876 integrates industry-lead Bluetooth and FM radio tuner into one chip and is optimized for mobile applications. Bluetooth and FM can work simultaneously and independently, with low power consumption levels target to battery powered devices. For the highest integration level, the required board space has been minimized and customer cost has been reduced. Manufacturers can easily and fast integrate RDA5876 on their product to enable a rapid time to market.
RDA5876 uses CMOS process with a compact

4*4mm 32-pin QFN package.

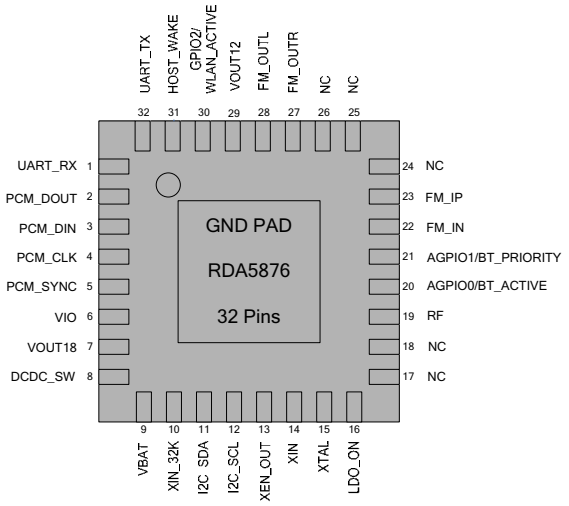


Figure1-1. RDA5876 Top View

1.1 Bluetooth Features

- CMOS single-chip fully-integrated radio and baseband
- Compliant with Bluetooth 2.1 + EDR specification
- Bluetooth Piconet and Scatternet support
- ARM7-based microprocessor with on-chip ROM and RAM
- Meet class 2 and class 3 transmitting power requirement, support class1 operation with external power amplifier
- Provides +10dbm transmitting power
- NZIF receiver with -90dBm sensitivity
- Battery power supply directly with internal LDO
- Support DCXO with internal oscillator circuit
- Up-to 4Mbps high speed UART HCI support
- Support AFH
- Support 3-wire WIFI Co-existence handshake signals
- Low power consumption
- Minimum external component
- Internal 32k LPO.

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1.2 FM Features

- CMOS single-chip fully-integrated FM tuner
- Low power consumption
  - Total current consumption lower than 20mA at 3.0V power supply
- Support worldwide frequency band
  - 50 -115 MHz
- Support flexible channel spacing mode
  - 100KHz, 200KHz, 50KHz and 25KHz
- Support RDS/RBDS
- Digital low-IF tuner
  - Image-reject down-converter
  - High performance A/D converter
  - IF selectivity performed internally
- Fully integrated digital frequency synthesizer
  - Fully integrated on-chip RF and IF VCO
  - Fully integrated on-chip loop filter
- Autonomous search tuning
- Support 32.768KHz crystal oscillator
- Digital auto gain control (AGC) Digital adaptive noise cancellation
  - Mono/stereo switch
  - Soft mute
  - High cut
- Programmable de-emphasis (50/75 μs)
- Receive signal strength indicator (RSSI)
- Bass boost
- Volume control
- Line-level analog output voltage
- I2C control bus interface
- Directly support 32Ω resistance loading
- Integrated LDO regulator
  - 1.8 to 5.5 V operation voltage

1.3 Applications

- Mobile handset
- MP3,MP4 and PMP
- PDA
- Cordless phone

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3 Bluetooth Section Functional Description

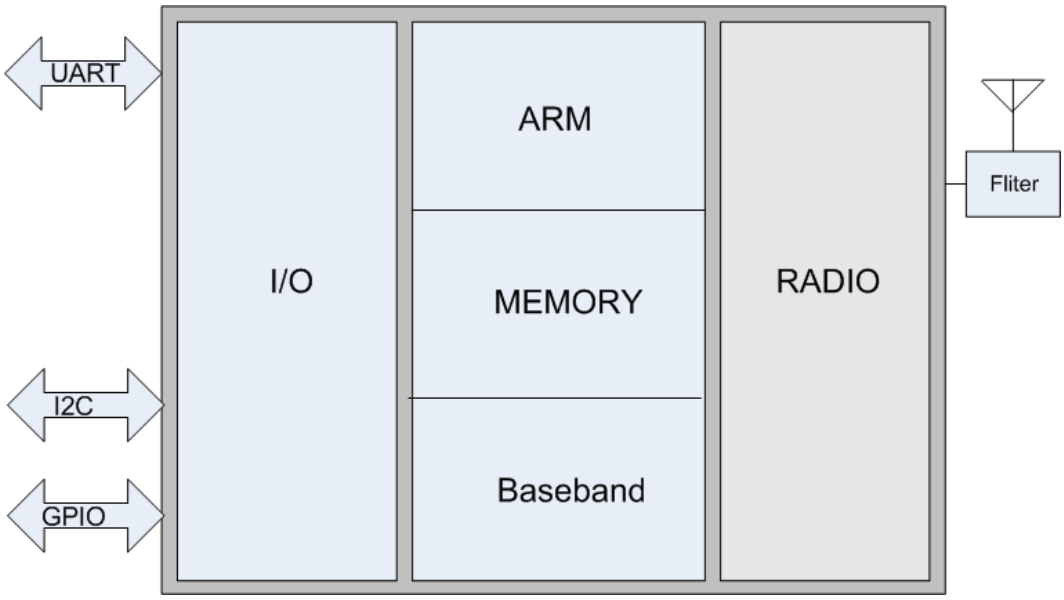

Figure3-1. RDA5876 Bluetooth Block Diagram

RDA5876 is designed for use in UART HCI with handset chipsets. As shown in Figure3-1, RDA5876 integrates radio unit, baseband core, ARM7 core and memory which provides a complete lower Bluetooth protocol stack including the LC, LM and HCI interface.

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4 Bluetooth Section Features

■ Radio

- Build-in TX/RX switch
- Fully integrated synthesizer without any external component
- Support DCXO or external reference clock direct input
- Class2 and class3 transmit output power supported and over 30dB dynamic control range
- Supports π/4 DQPSK and 8DPSK modulation
- High performance in receiver sensitivity and over 80dB dynamic range
- Integrated channel filter

■ Auxiliary features

- On-chip regulator to support battery power supply directly
- Power management support low power mode
- Support share handset system reference clock
- Support 3-wire wifi cooperation handshake protocol
- Support external class1 PA and antenna switch

■ Baseband

- Internal RAM allows fully speed data transfer, mixed voice and data, and fully piconet operation
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation , encryption bit stream generation, whitening and transmit pulse shaping
- Support eSCO and AFH
- Support up to Bluetooth v2.1 + EDR
- Support A-law, μ-law and CVSD digitize audio CODEC in PCM interface

■ Interface

- Provides UART HCI interface, up-to 4Mbps
- Provides I2C interface for host to do configuration
- Provides PCM audio interface
- Provides 3-wire and 2-wire WIFI Co-existence handshake interface

■ Bluetooth Stack

- Compliant with Bluetooth 2.1 + EDR specification

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5 Bluetooth Section Electrical Characteristics

Table 5-1 DC Electrical Specification (Recommended Operation Conditions):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VBAT	Supply Voltage from battery or LDO	3.3	4.0	4.2	V
T_{amb}	Ambient Temperature	-20	27	+50	℃
V_{IL}	CMOS Low Level Input Voltage	0		0.3*VIO	V
V_{IH}	CMOS High Level Input Voltage	0.7*VIO		VIO	V
V_{TH}	CMOS Threshold Voltage		0.5*VIO		V

Notes:

1. VIO=1.8~3.3V

Table 5-2 DC Electrical Specification (Absolute Maximum Ratings):

SYMBOL	DESCRIPTION	MIN		MAX	UNIT
T_{amb}	Ambient Temperature	-20		+80	°C
I_{IN}	Input Current	-10		+10	mA
V_{IN}	Input Voltage	-0.3		VIO+0.3	V
V_{lna}	LNA Input Level			+10	dBm

Table 5-3 LDO Power consumption specification

(VBAT = 4.0 V, VIO = 2.8V, T_A = +27℃, RF 9dBm, LDO mode unless otherwise specified)

STATE	DESCRIPTION	Condition	TYP	UNIT
Headset voice	HV3 type		18	mA
Headset SNIFF	500ms cycle	NO INQUIRE and PAGE SCAN	0.5	mA
HCI only active			5.7	mA
Both SCAN	1.28S cycle	INQUIRE and PAGE SCAN	1.0	mA
DeepSleep	26Mhz crystal off	Ivbat=105uA,Ivio=13uA,External 32K input	118	μA
internal LDO off	LDO_ON off	Ivbat=6uA,Ivio=1uA	7	μA

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Table5-4 DCDC Power consumption specification

(VBAT = 4.0 V, VIO = 2.8V, T_A = +27℃, RF 9dBm, DCDC mode unless otherwise specified)

STATE	DESCRIPTION	Condition	TYP	UNIT
Headset voice	HV3		12	mA
Headset SNIFF	500ms cycle	NO INQUIRE and PAGE SCAN	0.5	mA
HCI only active			3.8	mA
Both SCAN	1.28S cycle	INQUIRE and PAGE SCAN	0.8	mA
DeepSleep	26Mhz crystal off	Ivbat=105uA,Ivio=13uA, External 32K input	118	μA
internal LDO off	LDO_ON off	Ivbat=6uA,Ivio=1uA	7	μA

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6 Bluetooth Section Radio Characteristics

Table 6-1 Receiver Characteristics ------ Basic Data Rate

(VBAT = 4.0 V, TA = 27°C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications						
Sensitivity @0.1% BER			/	-90	/	dBm
Maximum received signal@0.1% BER			0	/	/	dBm
C/I c-channel			/	+10	/	dB
Adjacent channel selectivity C/I		F=F0 + 1MHz	/	/	-5	dB
		F=F0 - 1MHz	/	/	0	dB
		F=F0 + 2MHz	/	/	-33	dB
		F=F0 - 2MHz	/	/	-30	dB
		F=F0 + 3 MHz	/	/	-45	dB
		F=F0 - 3MHz	/	/	-40	dB
Adjacent channel selectivity C/I		$F=F_{image}$	/	/	0	dB
Out-of-band blocking performance		30MHz–2000MHz	-10	/	/	dBm
		2000MHz–2400MHz	-27	/	/	dBm
		2500MHz–3000MHz	-27	/	/	dBm
		3000MHz–12.5GHz	-10	/	/	dBm
Intermodulation			-35	/	/	dBm
Spurious output level			-150	/	/	dBm/Hz

Notes:

Table 6-2 Transmit Characteristics ------ Basic Data Rate

(VBAT = 4.0V, TA = 27 °C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications						
Maximum RF transmit power			/	+10	/	dBm
RF power control range			30	/	/	dB
20dB band width			/	0.9	/	MHz
Adjacent channel transmit power		F=F0 + 1MHz	/	-35	/	dBm
		F=F0 - 1MHz	/	-34	/	dBm
		F=F0 + 2MHz	/	-55	/	dBm
		F=F0 - 2MHz	/	-55	/	dBm
		F=F0 + 3MHz	/	-58	/	dBm
		F=F0 - 3MHz	/	-58	/	dBm
		F=F0 + >3MHz	-58	/	/	dBm

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	F=F0 - >3MHz	-58	/	/	dBm
$\triangle f1_{avg}$ Maximum modulation		/	164	/	kHz
$\triangle f2_{max}$ Minimum modulation		/	145	/	kHz
$\triangle f2_{avg}/\triangle f1_{avg}$		0.80	/	/	/
ICFT		/	+4	/	kHz
Drift rate		/	0.1	/	kHz/50us
Drift (1 slot packet)		/	-2	/	kHz
Drift (5 slot packet)		/	-2	/	kHz

Notes:

Table 6-3 Receiver Characteristics ------ Enhanced Data Rate

(VBAT = 4.0 V, TA = 27°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
π /4 DQPSK					
Sensitivity @0.01% BER		/	-87	/	dBm
Maximum received signal@0.1% BER		0	/	/	dBm
C/I c-channel		/	/	+13	dB
Adjacent channel selectivity C/I	F=F0 + 1MHz	/	/	+5	dB
	F=F0 - 1MHz	/	/	0	dB
	F=F0 + 2MHz	/	/	-30	dB
	F=F0 - 2MHz	/	/	-20	dB
	F=F0 + 3MHz	/	/	-40	dB
	F=F0 - 3MHz	/	/	-40	dB
Adjacent channel selectivity C/I	$F=F_{image}$	/	/	-7	dB
8DPSK					
Sensitivity @0.01% BER		/	-81	/	dBm
Maximum received signal@0.1% BER		0	/	/	dBm
C/I c-channel		/	/	+18	dB
Adjacent channel selectivity C/I	F=F0 + 1MHz	/	/	+5	dB
	F=F0 - 1MHz	/	/	+5	dB
	F=F0 + 2MHz	/	/	-25	dB
	F=F0 - 2MHz	/	/	-13	dB
	F=F0 + 3MHz	/	/	-33	dB
	F=F0 - 3MHz	/	/	-33	dB
Adjacent channel selectivity C/I	$F=F_{image}$	/	/	0	dB

Notes:

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Table 6-4 Transmit Characteristics ------ Enhanced Data Rate

(VBAT = 4.0 V, TA = 27°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications					
Maximum RF transmit power		/	+7	/	dBm
Relative transmit control		/	-1.6	/	dB
					kHz
π /4 DQPSK max w_0		/	+7.4	/	kHz
π /4 DQPSK max w_i		/	+6.7	/	kHz
π /4 DQPSK max $\|w_i + w_0\|$		/	+2.4	/	kHz
8DPSK max w_0		/	+7.1	/	kHz
8DPSK max w_i		/	+4.4	/	kHz
8DPSK max $\|w_i + w_0\|$		/	+2.7	/	kHz
π /4 DQPSK Modulation Accuracy	RMS DEVM	/	8	/	%
	99% DEVM	/	/	30	%
	Peak DEVM	/	16	/	%
8DPSK Modulation Accuracy	RMS DEVM	/	8	/	%
	99% DEVM	/	/	20	%
	Peak DEVM	/	16	/	%
In-band spurious emissions	F=F0 + 1MHz	/	-14.7	/	dBm
	F=F0 - 1MHz	/	-15.2	/	dBm
	F=F0 + 2MHz	/	-51.0	/	dBm
	F=F0 - 2MHz	/	-52.2	/	dBm
	F=F0 + 3MHz	/	-55.5	/	dBm
	F=F0 - 3MHz	/	-55.8	/	dBm
	F=F0 +/- > 3MHz	/	/	-55	dBm
EDR Differential Phase Coding		/	100	/	%

Notes:

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7 FM Section Functional Description

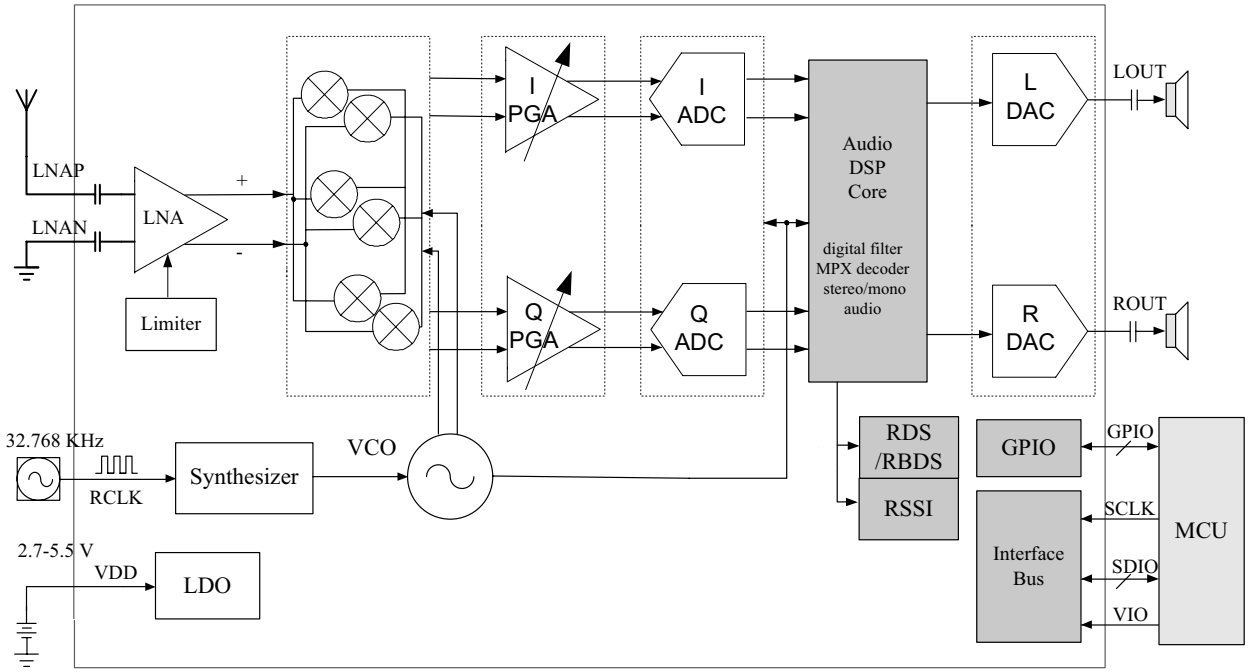

Figure 7-1. RDA5876 FM Tuner Block Diagram

FM Receiver

The receiver uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering lower solution cost and reduces complexity, and integrates a low noise amplifier (LNA) supporting the FM broadcast band (50 to 115MHz), a quadrature image-reject mixer, a programmable gain control (PGA), a high resolution analog-to-digital converters (ADCs), an audio DSP and a high-fidelity digital-to-analog converters (DACs).

The LNA has differential input ports (LNAP and LNAN) and supports any input port by set according registers bits (LNA_port_sel[1:0]). It default input common mode voltage is GND.

The limiter prevents overloading and limits the amount of intermodulation products created by strong adjacent channels.

The quadrature mixer down converts the LNA output differential RF signal to low-IF, it also has image-reject function.

The PGA amplifies the mixer output IF signal and then digitized with ADCs.

The DSP core finishes the channel selection, FM demodulation, stereo MPX decoder and output audio signal. The MPX decoder can autonomous switch from stereo to mono to limit the output noise.

The DACs convert digital audio signal to analog and change the volume at same time. The DACs has low-pass feature and -3dB frequency is about 30 KHz.

Synthesizer

The frequency synthesizer generates the local oscillator signal which divide to quadrature, then be used to downconvert the RF input to a constant low intermediate frequency (IF). The synthesizer reference clock is 32.768 KHz.

The synthesizer frequency is defined by bits CHAN[9:0] with the range from 50MHz to 115MHz.

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Power Supply

The RDA5876 FM section integrated LDO which supplies power to the chip. The external supply voltage range is 1.8-5.5 V.

RESET and Control Interface select

The RDA5876 FM section is RESET itself When VIO is Power up. And also support soft reset by trigger 02H BIT1 from 0 to 1. The control interface is I2C.

Control Interface

The I2C interface is compliant to I2C Bus Specification 2.1. It includes two pins: SCL and SDA. A I2C interface transfer begins with START condition, a command byte and data bytes, each byte has a followed ACK (or NACK) bit, and ends with STOP condition. The command byte includes a 7-bit chip address (0010000b) and a R/W bit. The ACK (or NACK) is always sent out by receiver. When in write transfer, data bytes is written out from MCU, and when in read transfer, data bytes is read out from RDA5876. There is no visible register address in I2C interface transfers. The I2C interface has a fixed start register address (0x02h for write transfer and 0x0Ah for read transfer), and an internal incremental address counter. If register address meets the end of register file, 0x3Ah, register address will wrap back to 0x00h. For write transfer, MCU programs registers from register 0x02h high byte, then register 0x02h low byte, then register 0x03h high byte, till the last register. RDA5876 always gives out ACK after every byte, and MCU gives out STOP condition when register programming is finished. For read transfer, after command byte from MCU, RDA5876 sends out register 0x0Ah high byte, then register 0x0Ah low byte, then register 0x0Bh high byte, till receives NACK from MCU. MCU gives out ACK for data bytes besides last data byte. MCU gives out NACK for last data byte, and then RDA5876 will return the bus to MCU, and MCU will give out STOP condition.

Details please refer to RDA5876 Programming Guide and RDA5802N Programming Guide and Datasheet.

I^2S Audio Data Interface

The RDA5876 supports I^2S (Inter_IC Sound Bus) audio interface. The interface is fully compliant with I^2S bus specification. When setting I2SEN bit high, RDA5876 will output SCK, WS, SD signals from GPIO_FM3, GPIO_FM1, GPIO_FM2 as I^2S master and transmitter, the sample rate is 48Kbps， 44.1kbps,32kbps….. RDA5876 also support as I^2S slaver mode and transmitter, the sample rate is less than 100kbps.

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8 FM Section Electrical Characteristics

Table 8-1 DC Electrical Specification (Recommended Operation Conditions):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VBAT	Supply Voltage	3.3	4.0	4.2	V
VIO	Interface Supply Voltage	1.5	3.0	3.6	V
Tamb	Ambient Temperature	-20	27	+75	℃
VIL	CMOS Low Level Input Voltage	0		0.3*VIO	V
VIH	CMOS High Level Input Voltage	0.7*VIO		VIO	V
VTH	CMOS Threshold Voltage		0.5*VIO		V

Notes:

1. VIO=1.8~3.3V

Table 8-2 DC Electrical Specification (Absolute Maximum Ratings):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VIO	Interface Supply Voltage	-0.5		+3.6	V
Tamb	Ambient Temperature	-40		+90	°C
IIN	Input Current (1)	-10		+10	mA
VIN	Input Voltage(1)	-0.3		VIO+0.3	V
VIna	LNA FM Input Level			+10	dBm

Notes:

1. For Pin: SCL, SDA

Table 8-3 Power Consumption Specification

(VBAT = 4.0 V, VIO=1.5 to 3.6V, TA = -25 to 85 ℃, unless otherwise specified)

SYMBOL	DESCRIPTION	Condition	TYP	UNIT
IA	Analog Supply Current	ENABLE=1	20	mA
IVIO	Interface Supply Current	SCL and SDA inactive	90	μA
IAPD	Analog Powerdown Current	ENABLE=0	5	μA
IVIO	Interface Powerdown Current	ENABLE=0	10	μA

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9 FM Section Receiver Characteristics

Table 9-1 Receiver Characteristics (VBAT = 4.0 V, VIO= 3.0V, TA = 25 °C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
General specifications							
F_{in}	FM Input Frequency Range	Adjust BAND Register		50		115	MHz
V_{rf}	Sensitivity[1,2,3]	S/N=26dB	50MHz	-	1.4	1.8	μV EMF
			65MHz	-	1.2	1.5	
			88MHz	-	1.2	1.5	
			98MHz	-	1.3	1.5	
			108MHz	-	1.3	1.5	
			115MHz	-	1.3	1.8	
$IP3_{in}$	Input IP3[4]	AGCD=1		80	-	-	dBμV
α_{am}	AM Suppression[1,2]	m=0.3		60	-	-	dB
S_{200}	Adjacent Channel Selectivity	±200KHz		50	70	-	dB
S_{400}	400KHz Selectivity	±400KHz		60	85	-	dB
V_{AFL}; V_{AFR}	Audio L/R Output Voltage[1,2] (Pins LOUT and ROUT)	Volume [3:0] =1111		-	360	-	mV
S/N	Maximum Signal to Noise Ratio[1,2,3,5]			55	57	-	dB
			Stereo[6]	53	55	-	
α_{SCS}	Stereo Channel Separation			35	-	-	dB
R_L	Audio Output Loading Resistance	Single-ended		32	-	-	Ω
THD	Audio Total Harmonic Distortion	Volume[3:0] =1111	R_{load}=1KΩ	-	0.15	0.2	%
			R_{load}=32Ω	-	0.2	-	
α_{AOI}	Audio Output L/R Imbalance			-	-	0.05	dB
R_{mute}	Mute Attenuation Ratio[1]	Volume[3:0]=0000		60	-	-	dB
BW_{audio}	Audio Response[1]	1KHz=0dB ±3dB point	Low Freq[9]	-	100	-	Hz
			High Freq	-	14	-	
Pins LNAN, LNAP, LOUT, ROUT and NC(22,23)							
V_{com_rfin}	Pins LNAN/LNAP Input Common Mode Voltage				**0**		V
V_{com}	Audio Output Common Mode Voltage[8]			1.0	1.05	1.1	V
V_{com_nc}	Pins NC (22,23) Common Mode Voltage				**Floating**		V

Notes: 1. F_{in}=65 to 115MHz; F_{mod}=1KHz; de-emphasis=75μs; MONO=1; L=R unless noted otherwise;
2. Δf=22.5KHz; 3. B_{AF} = 300Hz to 15KHz, RBW <=10Hz; 4. $|f_2-f_1|$>1MHz, $f_0=2xf_1-f_2$, AGC disable, F_{in}=76 to 108MHz;
5. P_{RF}=60dB$_U$V; 6. Δf=75KHz,fpilot=10% 7. Measured at V_{EMF} = 1 m V, f_{RF} = 65 to 108MHz
8. At LOUT and ROUT pins 9. Adjustable

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10 Pins Description

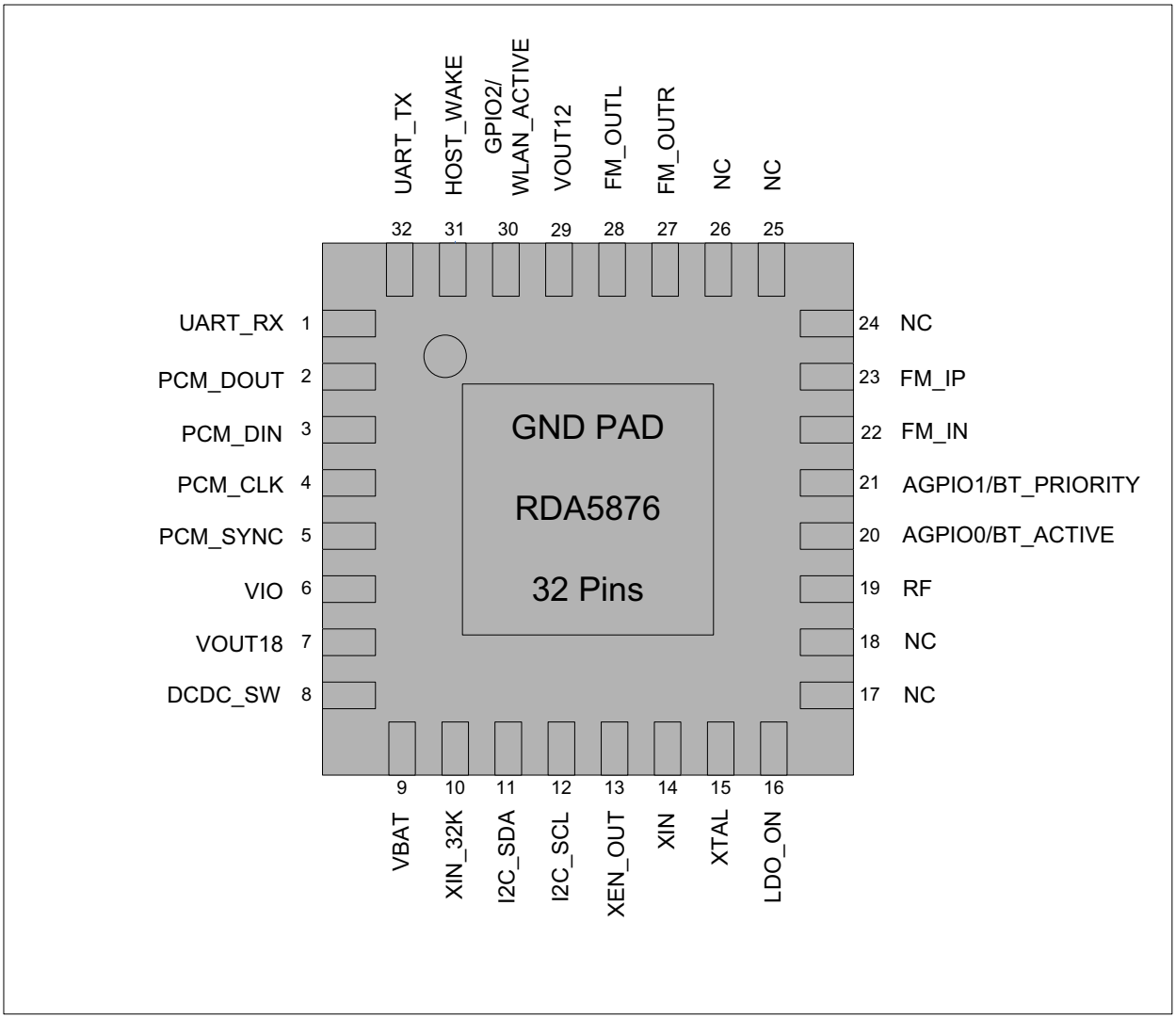

Figure10-1. RDA5876 Top View

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Table 10-1 RDA5876 Pins Description

PIN	NO.	DESCRIPTION
UART_RX	1	UART data input
PCM_DOUT	2	Synchronous data output
PCM_DIN	3	Synchronous data input
PCM_CLK	4	Synchronous data clock
PCM_SYNC	5	Synchronous data sync
VIO	6	IO power supply
VOUT18	7	Analog voltage output, connected with decouple capacitor
DCDC_SW	8	Internal DC/DC switch voltage output
VBAT	9	Bluetooth and FM power supply
XIN_32K	10	32.768K clock input or external 32.768K crystal
I2C_SDA	11	I2C interface Data signal
I2C_SCL	12	I2C interface Clock signal
XEN_OUT	13	Clock request output
XIN	14	For 26Mhz crystal input or external clock input
XTAL	15	For 26Mhz crystal input
LDO_ON	16	Internal LDO power on
NC	17	Should be not connected
NC	18	Should be not connected
RF	19	Bluetooth Radio signal
AGPIO0	20	Programmable I/O Also used ad bt_active when using WIFI co-existence handshake interface.
AGPIO1	21	Programmable I/O. Also used as bt_priority when using WIFI co-existence handshake interface.
FM_IN	22	LNA input port. For single-ended input, LNAN should be connected to RFGND
FM_IP	23	LNA input port. For single-ended input, LNAN should be connected to RFGND
NC	24	Connect to ground
NC	25	Should be not connected
NC	26	Connect to ground
FM_OUTR	27	Right audio output
FM_OUTL	28	Left audio output
VOUT12	29	Digital voltage output, connected with decouple capacitor
GPIO2	30	Programmable I/O. Also used as wl_active when using WIFI co-existence handshake interface.
HOST_WAKE	31	Output to wakeup host
UART_TX	32	UART data output

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11 Application Circuit

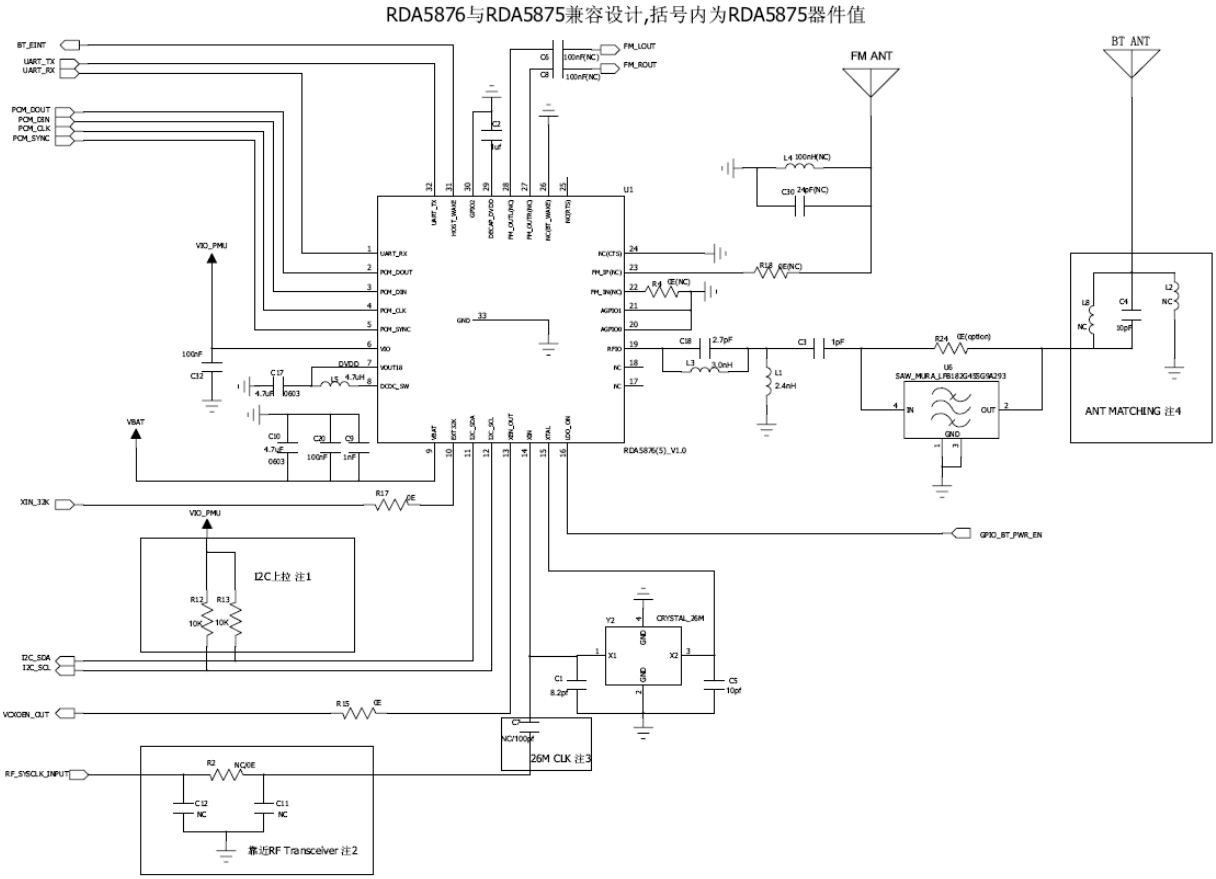

Figure 11.1 Application schematic

1) AGPIO0, AGPIO1, GPIO2 connect to GND.
2) L5 4.7uH only for DCDC mode, LDO mode NC .

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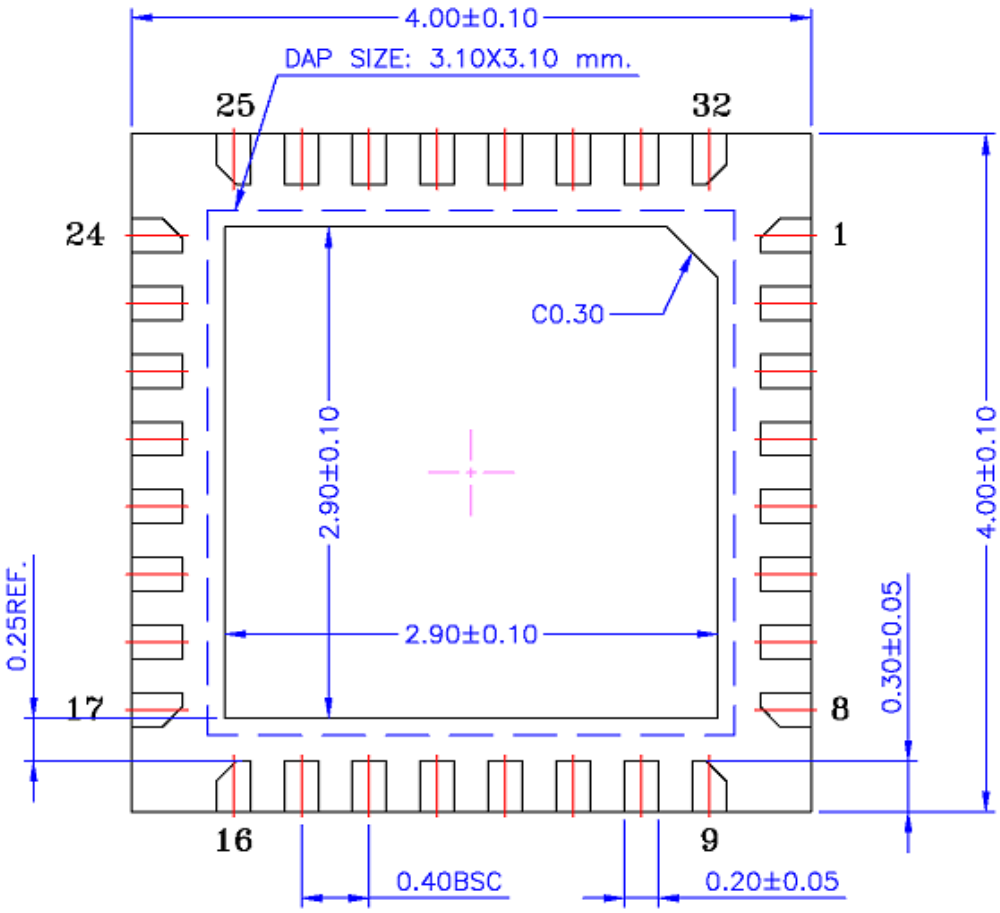
12 Package Physical Dimension

Figure12-1illustratesthepackage details for the RDA5876. The package is lead-free and RoHS-compliant.

POD IN BOTTOM VIEW



POD IN SIDE VIEW

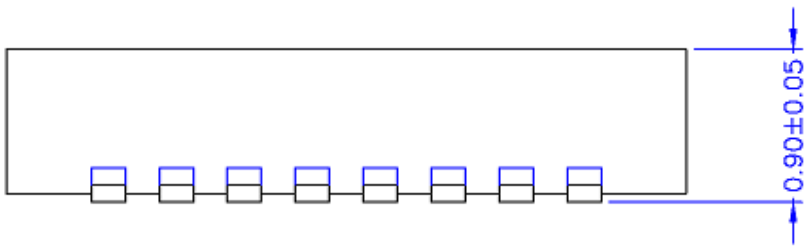


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Figure12-1. 32-Pin 4x4 Quad Flat No-Lead (QFN)

13 PCB Land Pattern

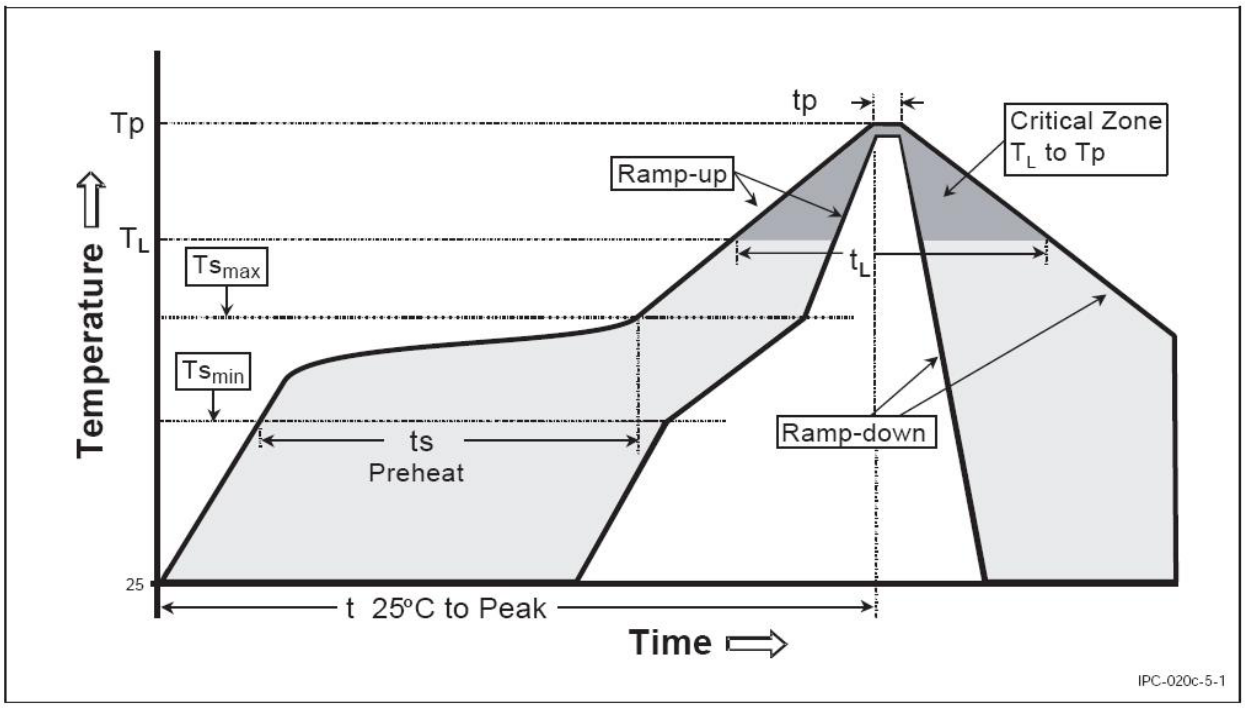

Figure13-3.Classification Reflow Profile

Table 13-1 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (TSmax to Tp)	℃/second max.	3 ℃/second max.
Preheat -Temperature Min (Tsmin) -Temperature Max (Tsmax) -Time (tsmin to tsmax)	 100 ℃ 100 ℃ 60-120 seconds	 150 ℃ 200 ℃ 60-180 seconds
Time maintained above: -Temperature (TL) -Time (tL)	 183 ℃ 60-150seconds	 217℃ 60-150 seconds
Peak /Classification Temperature(Tp)	See Table 9-2	See Table 9-3
Time within 5 oC of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 ℃/second max.	6 ℃/seconds max.
Time 25 oC to Peak	6 minutes max.	8 minutes max.

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Temperature		

Table 13-2 Pb-free Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm3 <350	Volume mm3 ⩾350
＜2.5mm	240 + 0/-5 ℃	225 + 0/-5 ℃
⩾2.5mm	225 + 0/-5 ℃	225 + 0/-5 ℃

Table 13-3 Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm3 ＜350	Volume mm3 350-2000	Volume mm3 ＞2000
＜1.6mm	260 + 0 ℃ *	260 + 0 ℃ *	260 + 0 ℃ *
1.6mm – 2.5mm	260 + 0 ℃ *	250 + 0 ℃ *	245 + 0 ℃ *
⩾2.5mm	250 + 0 ℃ *	245 + 0 ℃ *	245 + 0 ℃ *
*Tolerance : The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 . For example 260+ 0 ℃) at the rated MSL Level.			

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 ℃, - X ℃ (based on machine variation capability)whatever is required to control the profile process but at no time will it exceed – 5 ℃. The producer assures process compatibility at the peak reflow profile temperatures defined in Table 13-3.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

Note 5: Components intended for use in a “lead-free” assembly process shall be evaluated using the “lead free” classification temperatures and profiles defined in Table13-1, 13-2, 13-3 whether or not lead free.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated biphenyl ethers (PBDE), and are therefore considered RoHS compliant.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

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14 Change List

REV	DATE	AUTHER	CHANGE DESCRIPTION
V1.0	03/25/2011	Gibson	Initial version.
V1.1	07/01/2011	Daihongjun	Modify 24pin,25pin, 26pin PIN name Modify the Application Circuit
V1.2	09/20/2011	Daihongjun	Modify 27pin,28pin, PIN name

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