



Operational Description / Schematics Note (Confidential)

FCC ID: [A3LGTS7275](#)

Model: [GT-S7275](#)

Date: [2013-06-06](#)

Please note that this Operational Description provides a complete description of the subject model. However, the chip(s) within the device may include additional capabilities that are not implemented for this device. Technical information pertaining to these additional capabilities may be shown within this document. The actual supported capabilities as implemented for this model are listed below.

Please find below the capabilities that are operational for this device:

Within USA:

- GSM/GPRS 850
- GSM/GPRS 1900
- UMTS 850
- GPRS Multi-slot Class 33
- 2.4 GHz 802.11b/g/n(HT20)
- Bluetooth v4.0
- Mobile Hotspot
- FM Receiver
- EDGE
- Wifi Direct
- RFID(NFC)

Non-USA:

- GSM/GPRS/EDGE 900
- GSM/GPRS/EDGE 1800
- UMTS 2100
- UMTS 900
- HSDPA (Cat 24)
- HSUPA (cat 6)
- LTE B3, B7, B8, B20

Although the chipset documentation may indicate possible functions, the following have been permanently hardware disabled in this device and cannot be enabled by the end user or service provider

GT-S7275 Operational Description

1. RF Circuit Description

1. ANTENNA SWITCH

Switching over Tx, Rx, path from antenna to RF connector when RF connector is connected.

2. Front-End Module (LMSW65GJ-E94)

Antenna Switch control Logic → True Table

Function	Sequence Start Condition		USID (Slave ID Address)				Command			Register Address					Parity		Data								Parity		Bus Park
Isolated	1	0	1	0	1	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0	
1900Rx	1	0	1	0	1	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	
GSMLTx	1	0	1	0	1	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	1	0	0	0	
GSMHTx	1	0	1	0	1	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	0	
1800Rx	1	0	1	0	1	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	1	1	0	
Band8	1	0	1	0	1	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	0	1	0	
Band5	1	0	1	0	1	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	
Band3	1	0	1	0	1	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	1	0	
TRx1(High)	1	0	1	0	1	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	1	0	1	0	1	0	
TRx2(Low)	1	0	1	0	1	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	0	1	0	
Band1	1	0	1	0	1	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	1	0	0	
Isolated	1	0	1	0	1	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	1	1	1	1	1	0	

3. TCXO

To generate The 26MHz reference clock to drive the logic and RF

4. PAM(SKY77611)

SKY7761-51 is a hybrid, multimode, multiband Power Amplifier Module (PAM) that supports 2.5G and 3G/4G handsets and operates efficiently in GSM, EGPRS, EDGE, WCDMA, CDMA, and LTE modes. The PAM consists of: a GSM 800 / EGSM 900 PA block, a DCS1800 / PCS1900 PA block, separate WCDMA blocks operating in low and high bands, a logic control block for multiple power control levels, and band enable functions in both cellular and UMTS. RF I/O ports are internally matched to 50 Ω to minimize the number of external components. Extremely low leakage current maximizes handset standby time. The InGaP/GaAs die and passive components are mounted on a multi-layer laminate substrate and the assembly encapsulated in plastic overmold.

GSM/EDGE: The SKY77611-51 uses a new compact architecture supporting the GSM850, EGSM900, DCS1800 and PCS1900 bands. The PAM also supports 2.5G Class 12 Enhanced General Packet Radio Service (EGPRS) multislot operation and EDGE linear modulation.

WCDMA: The SKY77611-51 uses an enhanced architecture to support WCDMA / CDMA High-Speed Downlink Packet Access (HSDPA), and High-Speed Uplink Packet Access (HSUPA) and LTE modulations; cover multiple bands for 3GPP, including bands I, II, III/IV, III/V, and VIII; and operate at different power modes. The module is fully controllable via four logic lines and band-enable interfaces.

LTE: The SKY77611-51 meets spectral linearity requirements of LTE modulation with QPSK/16QAM up to 20 MHz bandwidth, including various resource block allocations, with good power-added efficiency.

5. Duplexer

This product specification is applied to the 2500/2600MHz range SAW Duplexer for communication equipment.

6. Transceiver (B10L2)

The purpose of this B10L2 Data Sheet document is to detail the RF/Analog target specifications for the B10L2 RFIC product.

The B10L2 product is a triple mode 2.5G/3G/LTE transceiver that supports: GSM850/EGSM900/DCS/PCS operations in 2.5G mode.

UTRA bands 1, 2, 4, 5, 8, 9, 11 in 3G.

E-UTRA bands 1, 2, 3, 4, 5, 7, 8, 9, 11, 17, 19, 20 and 21 in FDD LTE mode.

E-UTRA band 38 in TDD LTE mode.

AXGP (Advanced eXtended Global Platform: 2545MHz ~ 2575MHz)

2. BB Circuit Description

1. D2153((CP PMIC)_

The power management section of D2153 contains an integrated Power Management Controller (PMC) for

multiple power supplies (programmable LDO regulators and Buck converters).

All linear regulators use Dialog's Smart Mirror™ dynamic biasing technique which maintains high

performance over a wide range of operating conditions and a power saving mode (Sleep Mode) to minimize the quiescent current.

The regulators have output voltages independently programmable via the device control interface.

The buck converters do not require external Schottky diodes and offer a sleep mode (PFM mode) for optimal efficiency at low load currents. All DC-DC converters (except the Core and RF Bucks) use a 2MHz

switching frequency giving high efficiency and allowing the use of small external inductors (down to 2.2uH). Beside the power modules there are different core modules like real-time-clock (RTC), general purpose analog-to-digital converter (GPADC) and general-purpose IO pins (GPIO) implemented on the IC. These modules are implemented to support different functions like battery voltage supervision and device overtemperature protection.

D2153 is completely SW-controlled from the host by registers allowing high flexibility of the customer's applications.

Key features of the Power Management section:

- 20 x programmable LDO regulators

- 3 x internal LDO for Audio and PMIC circuits

- 1 x dual phase high efficiency programmable buck converter
- 4 x single phase high efficiency programmable buck converters
- 1 x high efficiency RF buck converter
- Low power back up battery charger
- Ultra-low power 32kHz Real Time Clock (RTC) with alarm wakeup capability
- 12 bit general purpose ADC with built-in auto-mode controller
- Accurate band gap reference
- Temperature / voltage supervision
- High Speed I2C Interface
- OTP memory

2. MP5232 (CP : Call Processor)

Table1.1 Features of this LSI (Baseband part)

Item	Features	
WGE Modem (WGEM)	WGEM can be used as WCDMA or GSM or LTE modem	
	WGEM Uses two Cortex R4 for L1/L2/L3 processing	
	L1 Cortex R4 features:	L2/L3 Cortex R4 features:
	- 32 KB L1 instruction cache	- 32 KB L1 instruction cache
	- 16 KB L1 data cache	- 16 KB L1 data cache
	- 256 KB L2 cache	- 256 KB L2 cache
	- 3x32KB Tightly coupled memory (TCM)	- 16KB Tightly coupled memory (TCM)
	- Memory protection unit (MPU) with 12 regions	- Memory protection unit (MPU) with 12 regions
	- ETM	- ETM
	- Version : R1P3	- Version : R1P3
	GERAN Features: - All mandatory and selected optional 3GPP R99, Rel4 and Rel5 features - Selected Rel6, Rel7 and Rel8 features (where network implementation allows) - CS support for HR, FR, EFR, NB-AMR and WB-AMR speech over GMSK - GPRS/EGPRS/DTM MSC33 (5DL + 4UL, sum 6): max 296 kbps DL / 236.8 kbps UL - Downlink Advanced Receiver Performance (DARF), aka "3GPP SAIC" - EDTM – enables PS data continuation while CS connection is established/released - Cell selection after CS connection release – reduces signalling in network - RRLP LCS Protocol	
	WCDMA Features - All mandatory and selected optional 3GPP Rel99, Rel4 and Rel5 features (where network implementation allows) - Selected Rel6, Rel7 and Rel8 features supported according to network implementation - DRx, DTx and F-DPCH for PS power saving - DCH CS for NB & WB-AMR voice data transfer and transparent data up to 384/384kbps (64/64kbps with simultaneous HSPA) - DCH PS bearers up to 384/384kbps (64/64kbps with simultaneous HSPA)	

- HSDPA Cat 24 (MIMO with 64QAM, peak rate 42Mbps @L1)
- HSDPA Rx diversity

EUTRAN features

- Category 4:
- Downlink: 150 Mbps (64QAM)
- Uplink: 50 Mbps (16QAM)
- 1.4,3,5,10,15, 20MHz bandwidth
- 4x2 MIMO, RX Diversity
- Single transmitter supported
- UE specific reference signal for TDD
- Inter-operability to/from GERAN
- Inter-operability to/from UTRAN

Figure 2.1 Shows the block diagram of R-Mobile-U2(ES2.0).

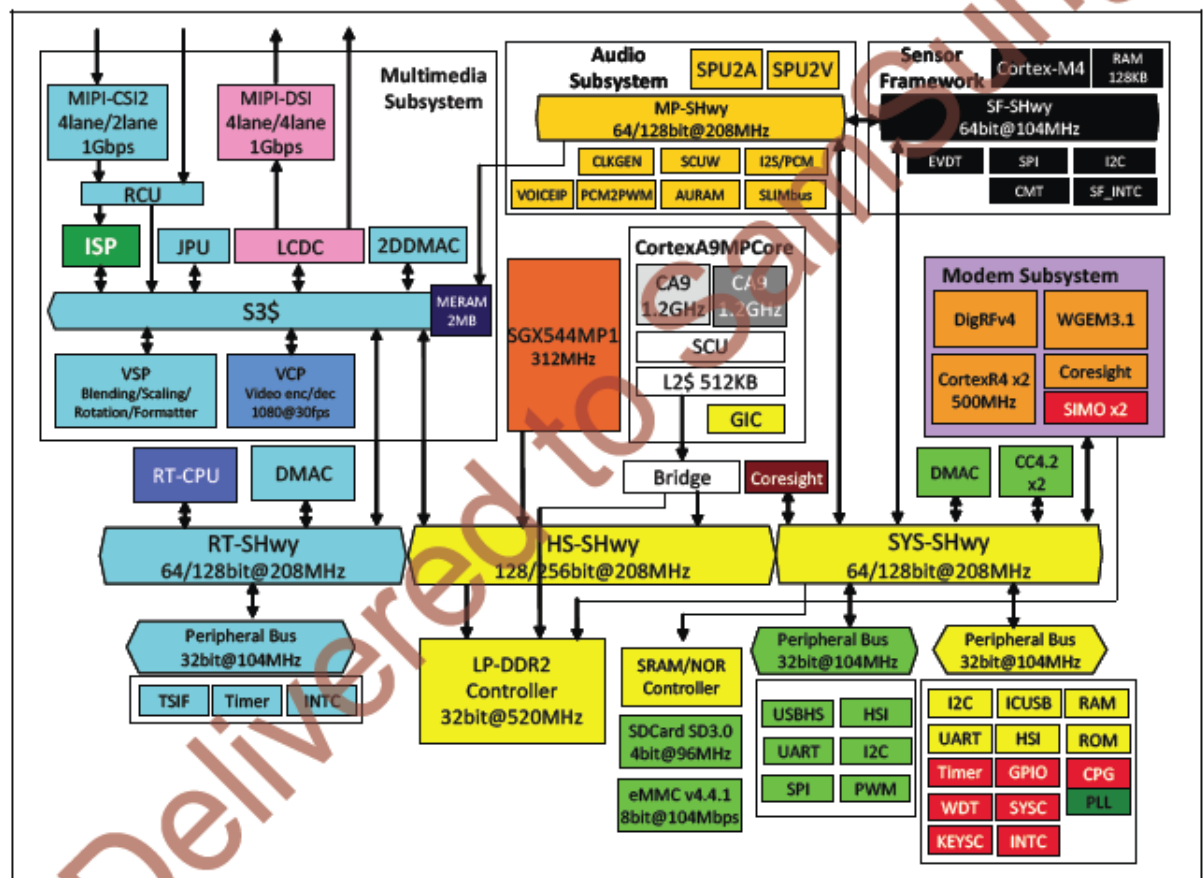


Figure 2.1 Block diagram of R-Mobile-U2(ES2.0)

3. Memory(K4P8G304EB-AGC2)

All LPDDR2 devices use a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

LPDDR2-S4 uses a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM core and four corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the LPDDR2 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. For LPDDR2-S4 devices, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR2 must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.