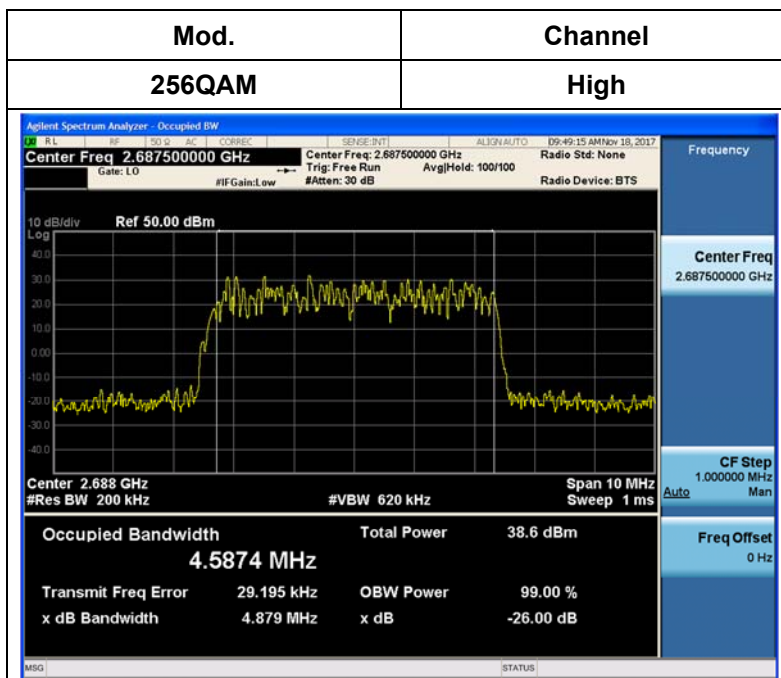
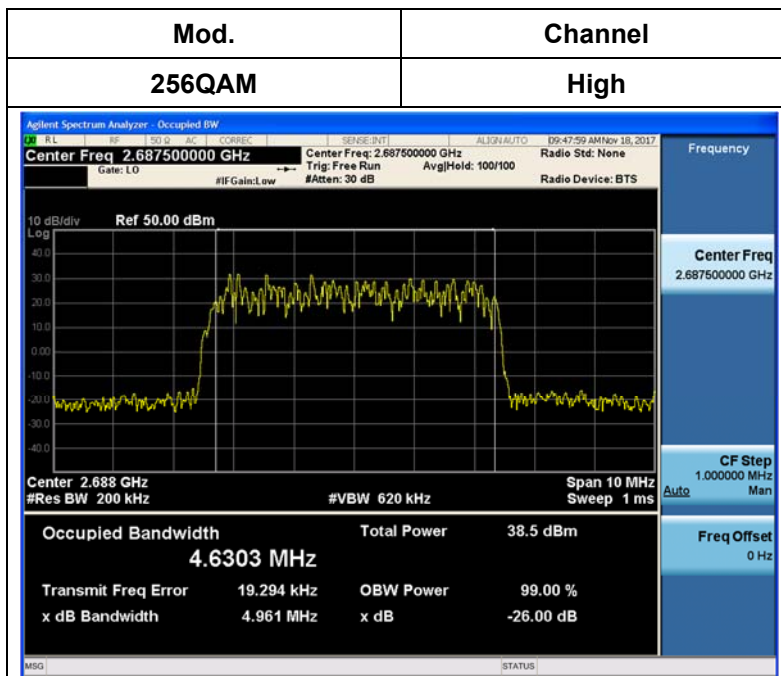


5 MHz / 1 Carrier (5 W)

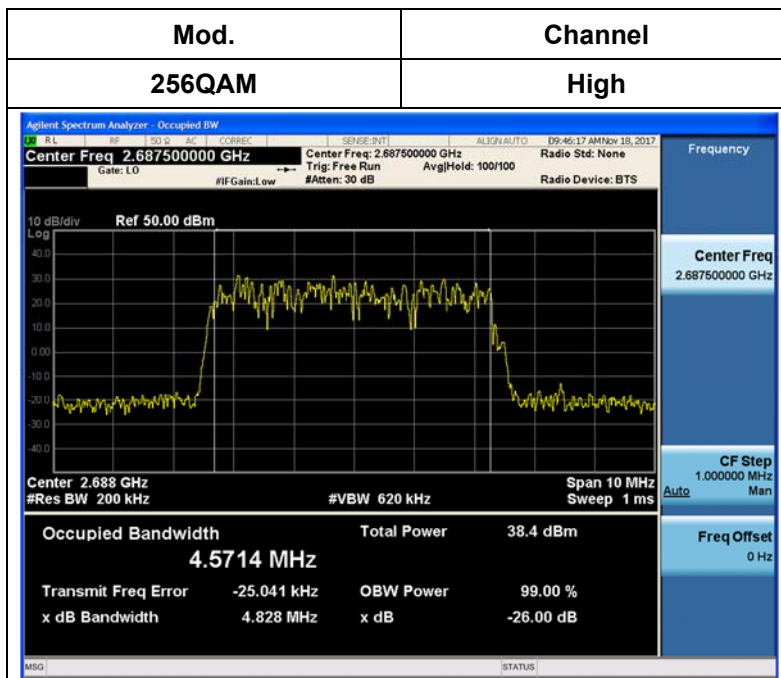
Plot Data for Output Port 0



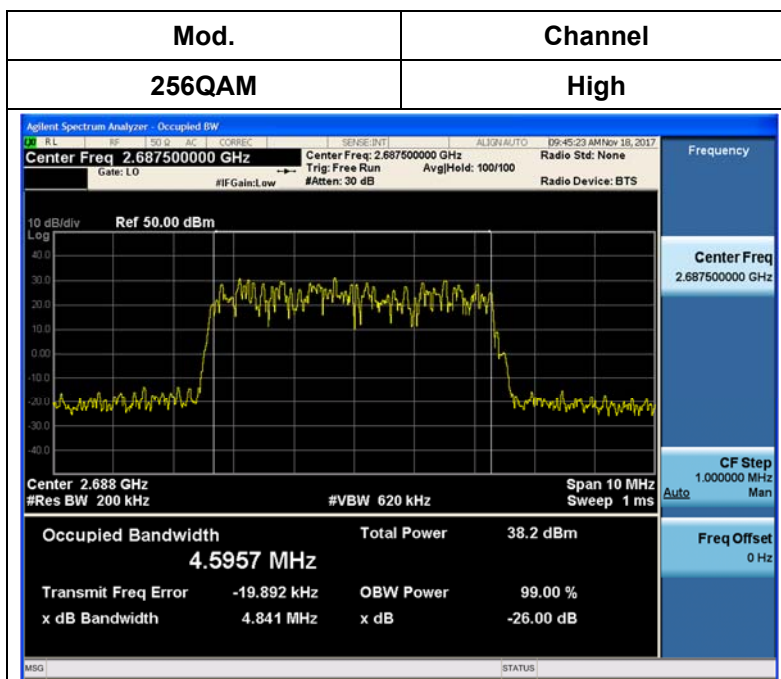
Plot Data for Output Port 1



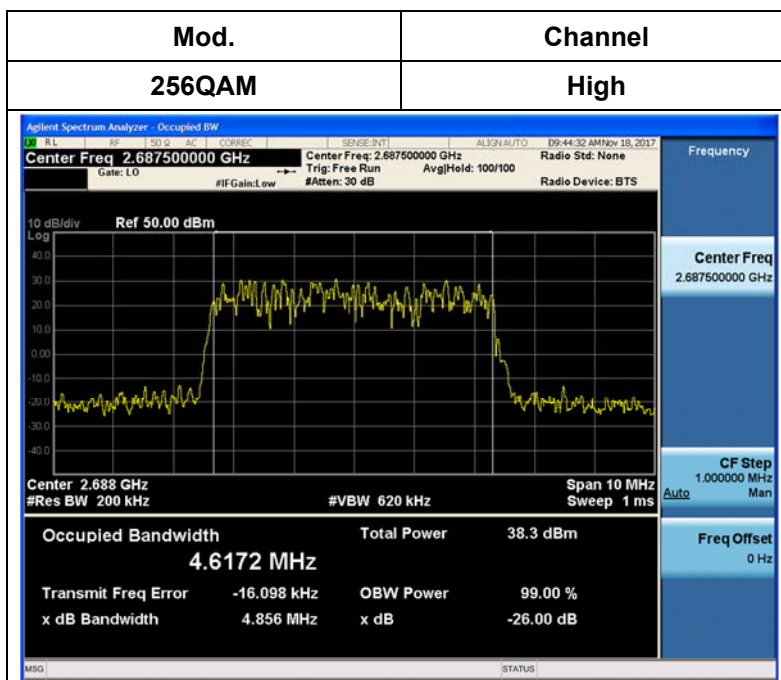
Plot Data for Output Port 2



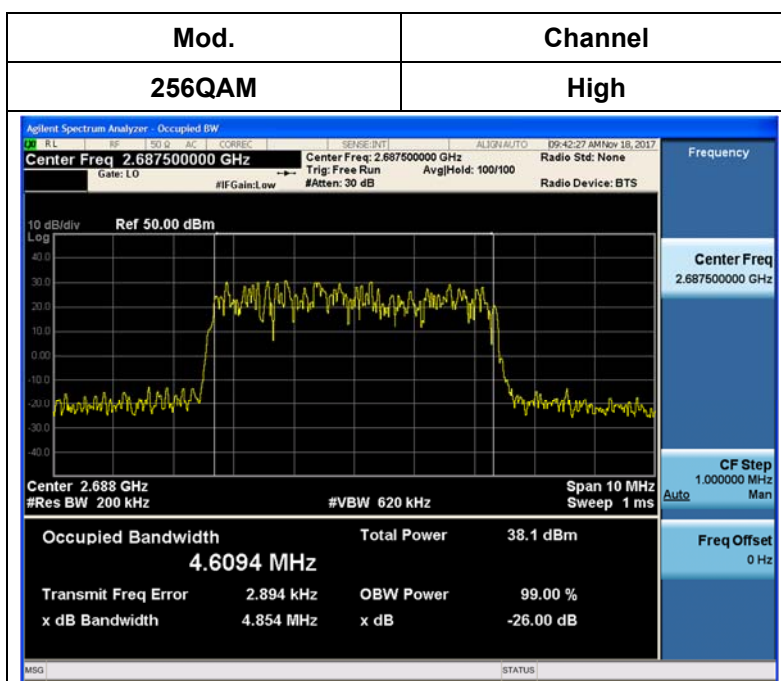
Plot Data for Output Port 3



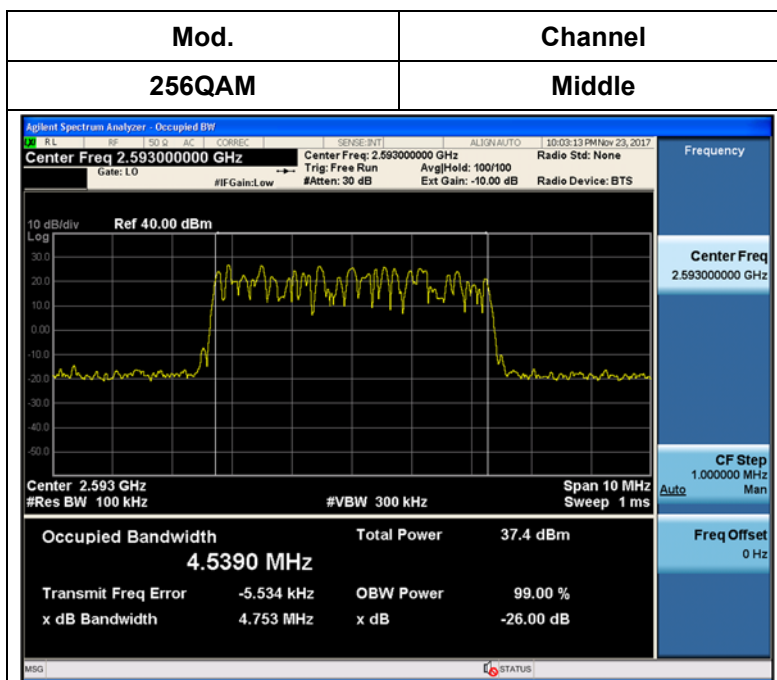
Plot Data for Output Port 4



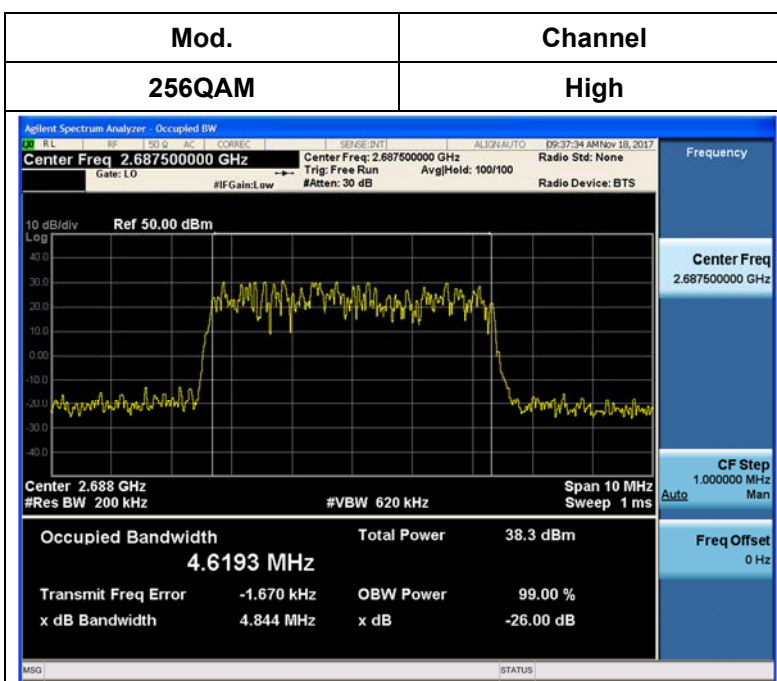
Plot Data for Output Port 5



Plot Data for Output Port 6

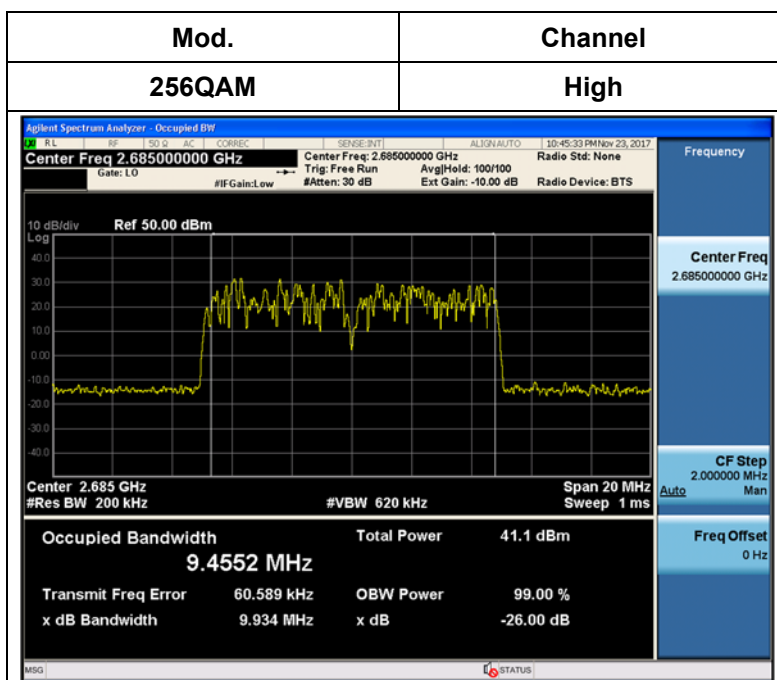


Plot Data for Output Port 7

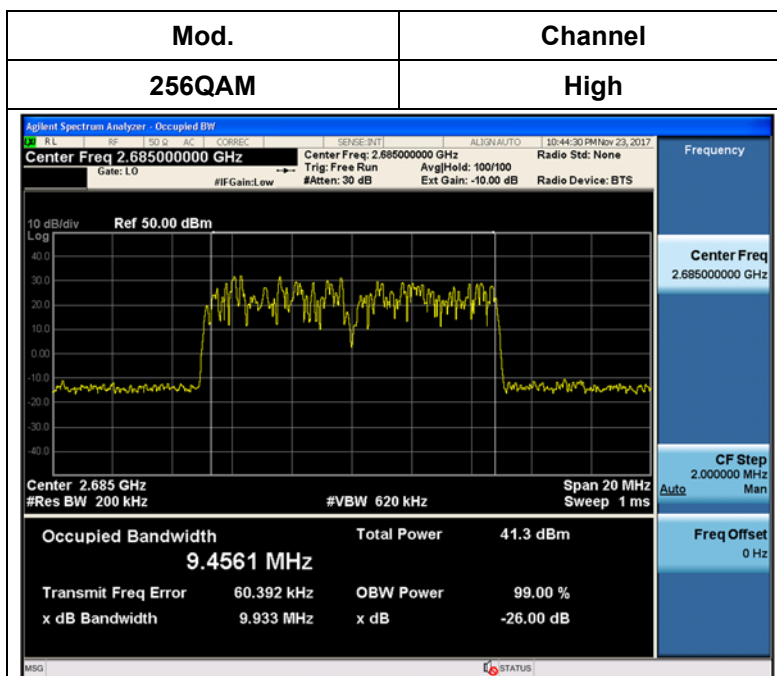


5 MHz + 5 MHz / 2 Carriers (5 W + 5 W)

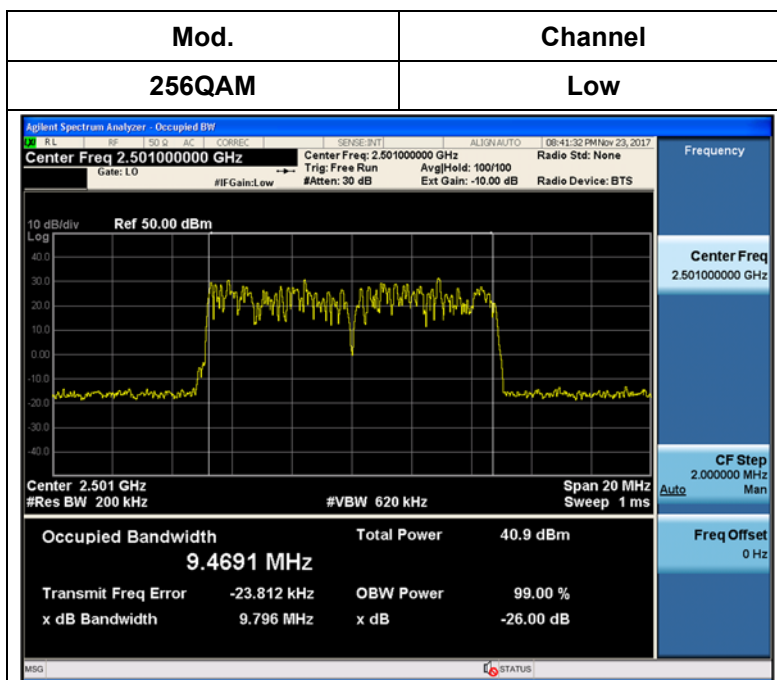
Plot Data for Output Port 0



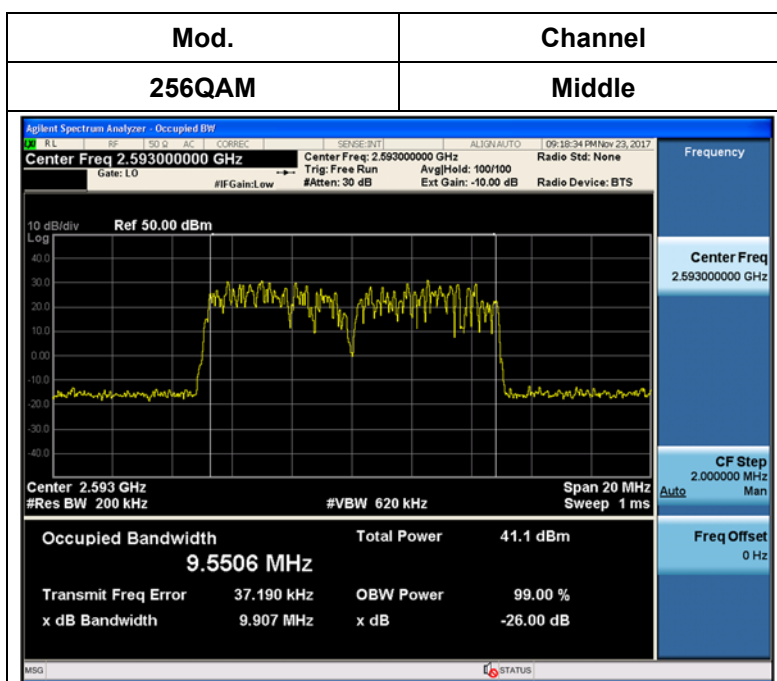
Plot Data for Output Port 1



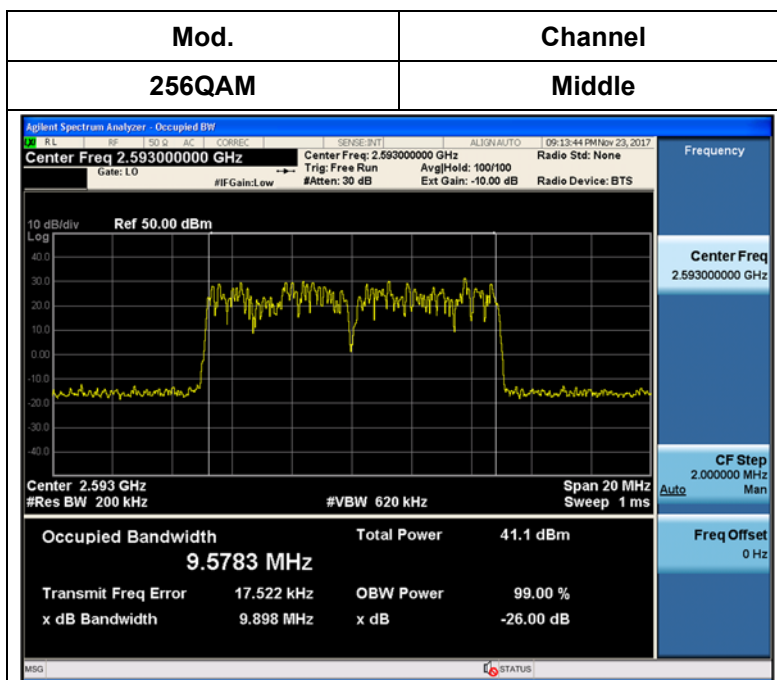
Plot Data for Output Port 2



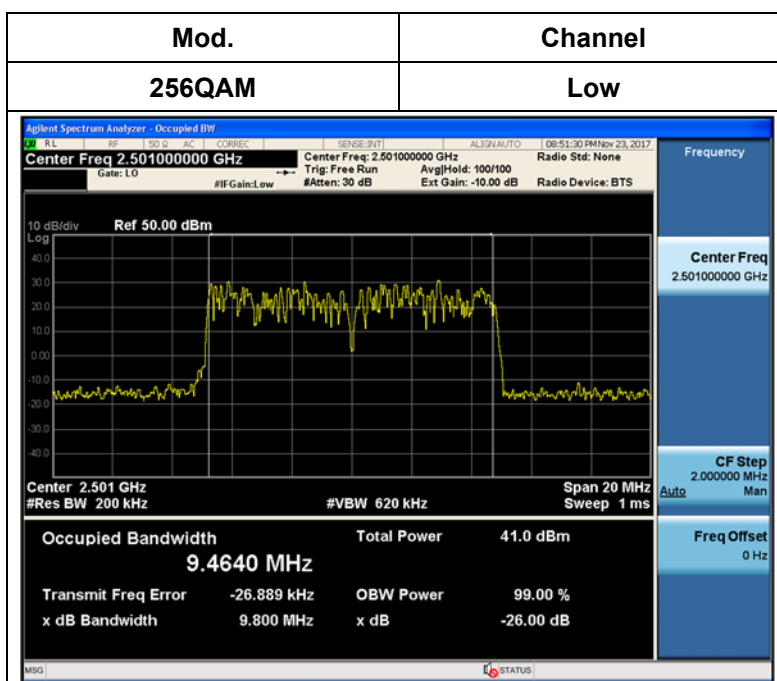
Plot Data for Output Port 3



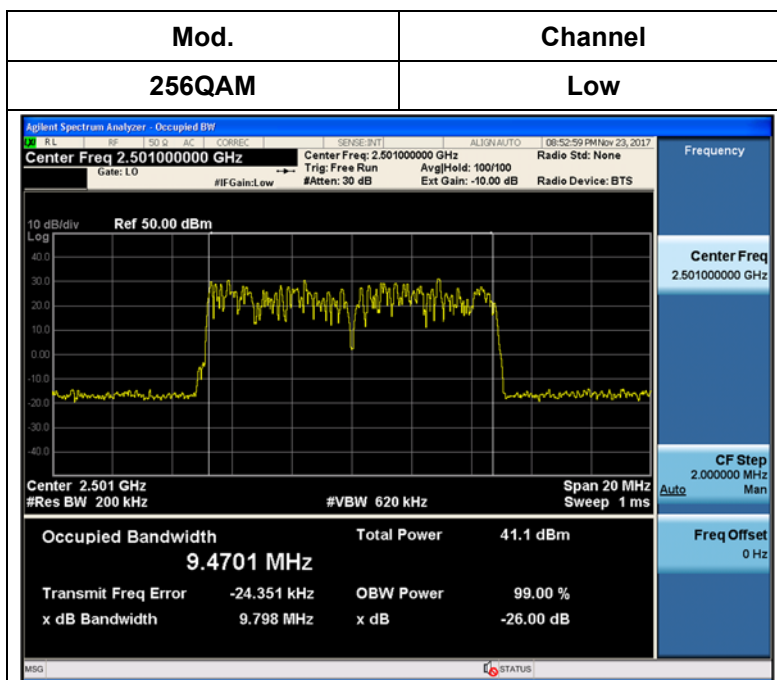
Plot Data for Output Port 4



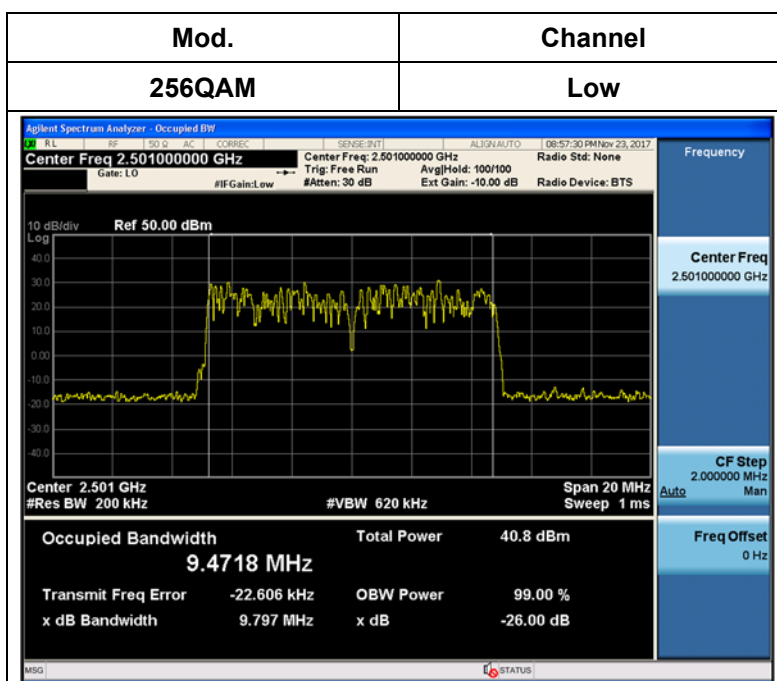
Plot Data for Output Port 5



Plot Data for Output Port 6

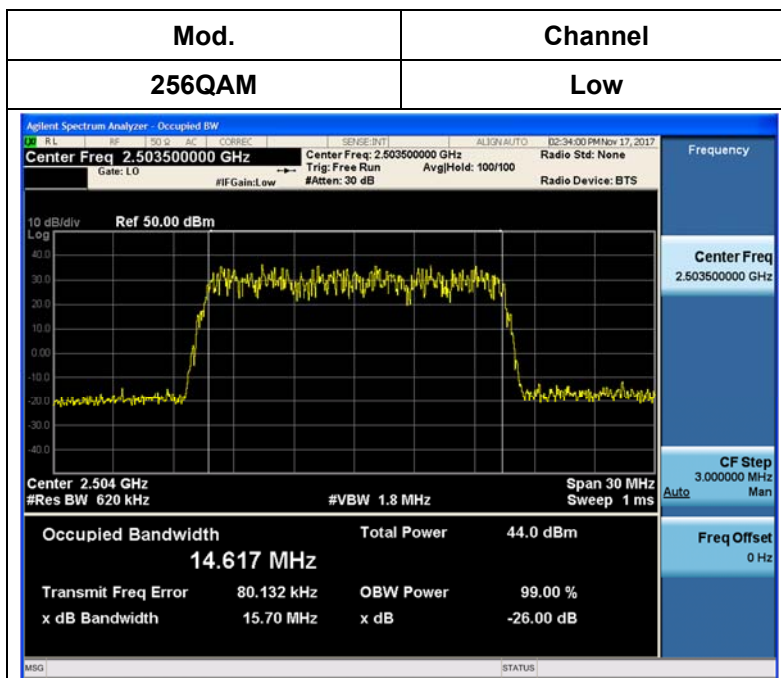


Plot Data for Output Port 7

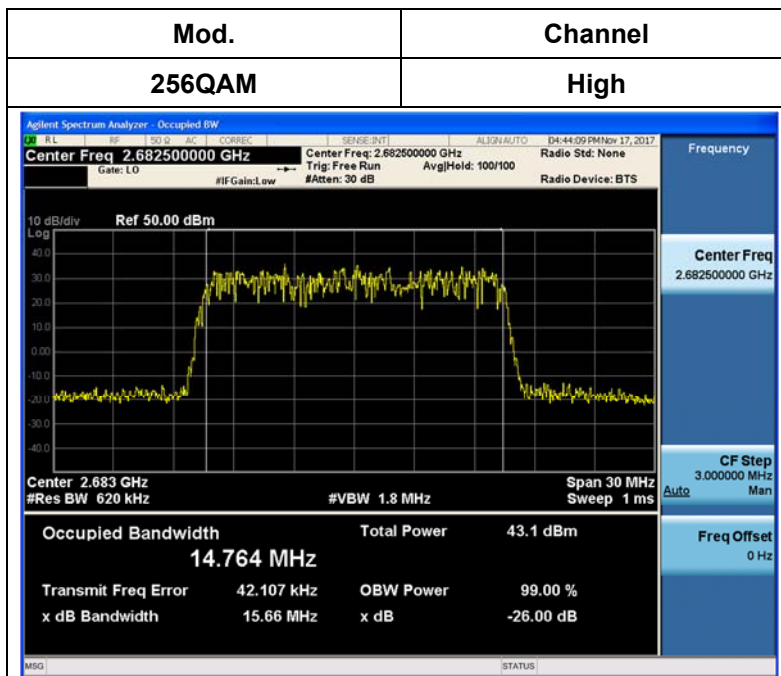


5 MHz + 5 MHz + 5 MHz / 3 Carriers (5 W + 5 W + 5 W)

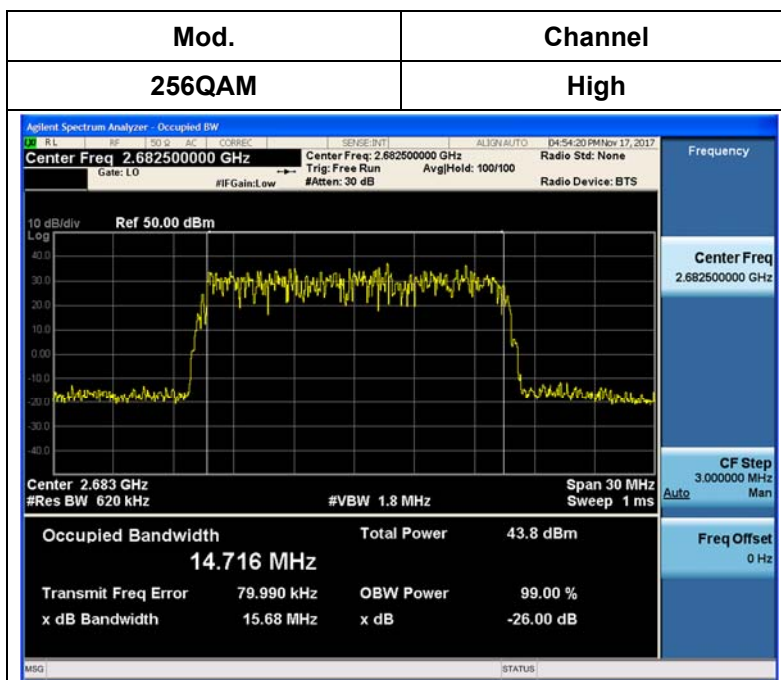
Plot Data for Output Port 0



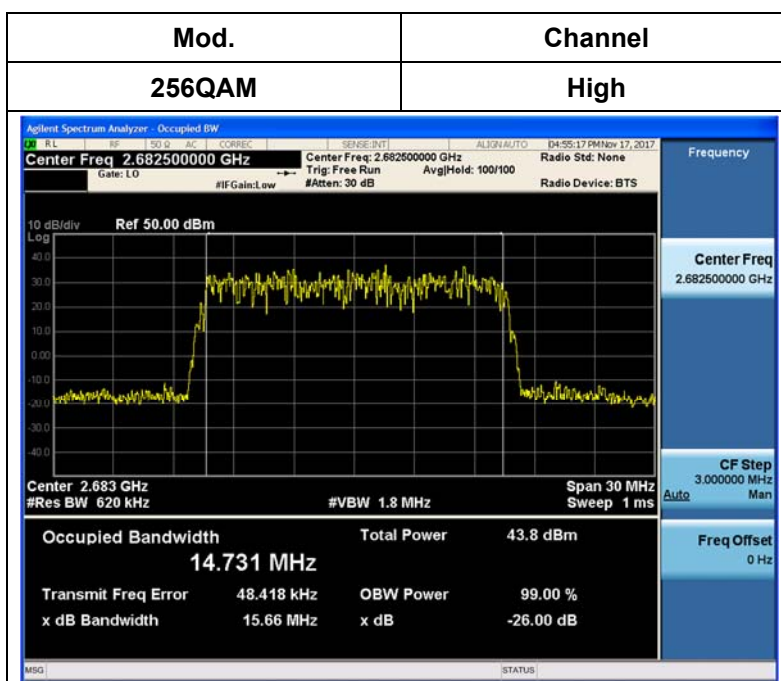
Plot Data for Output Port 1



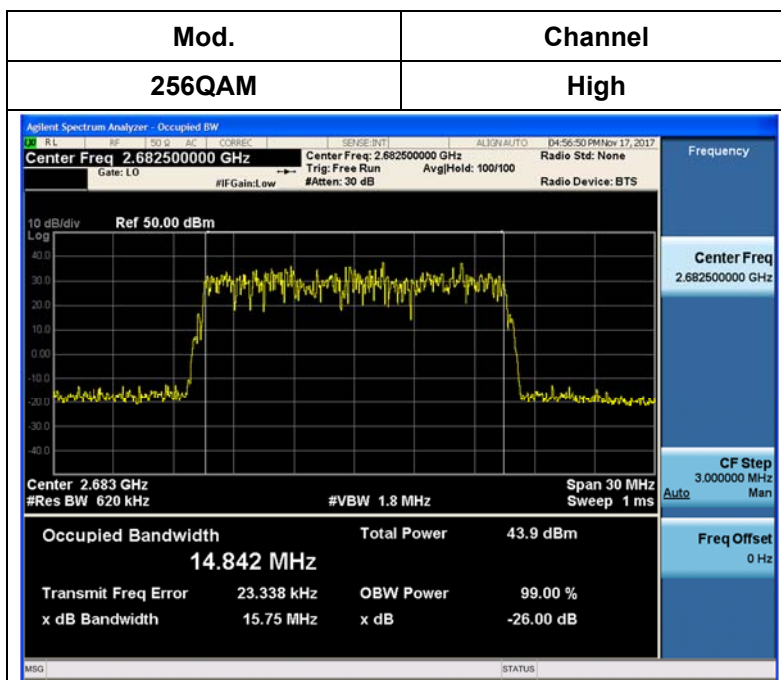
Plot Data for Output Port 2



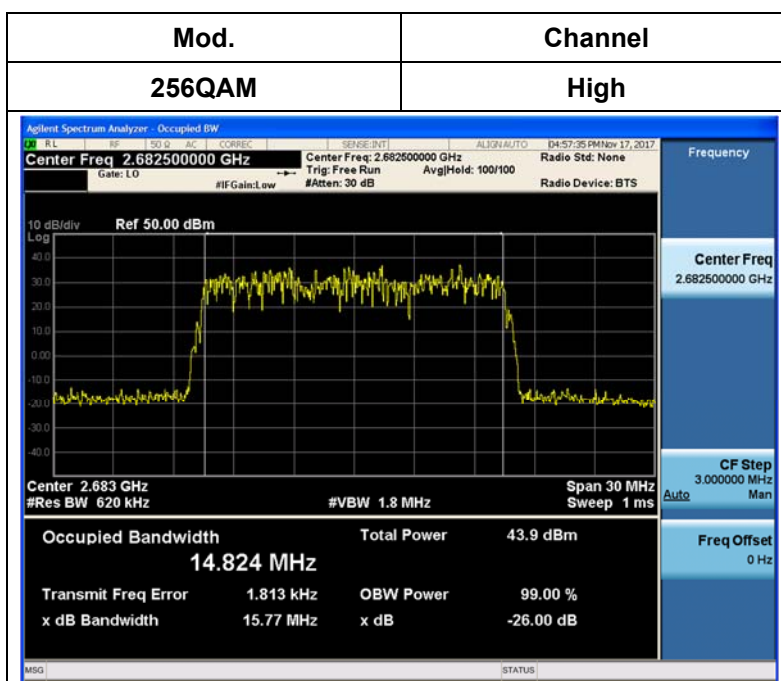
Plot Data for Output Port 3



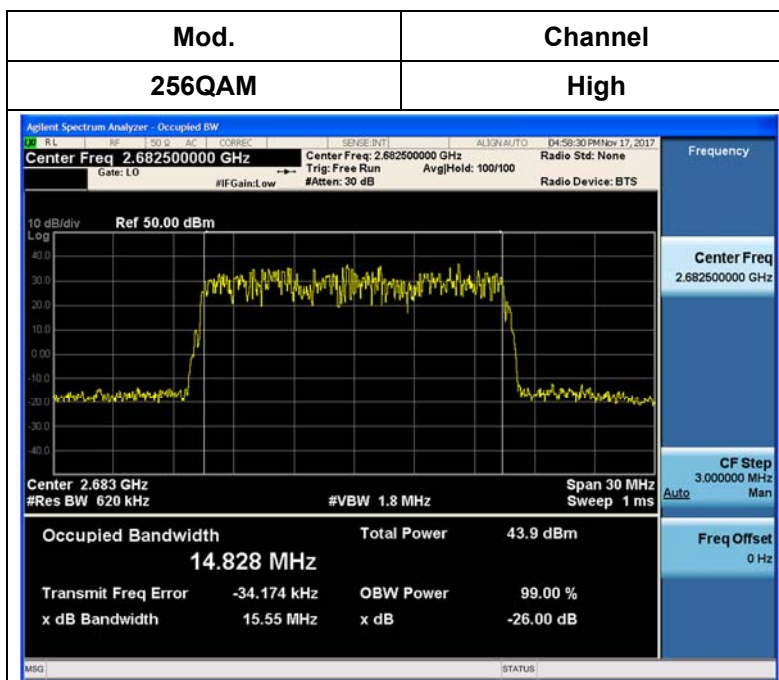
Plot Data for Output Port 4



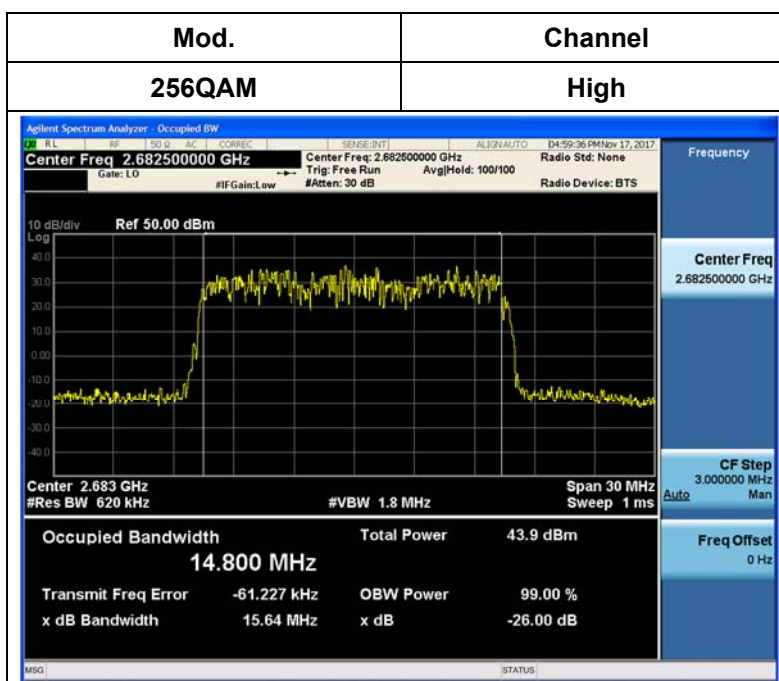
Plot Data for Output Port 5



Plot Data for Output Port 6

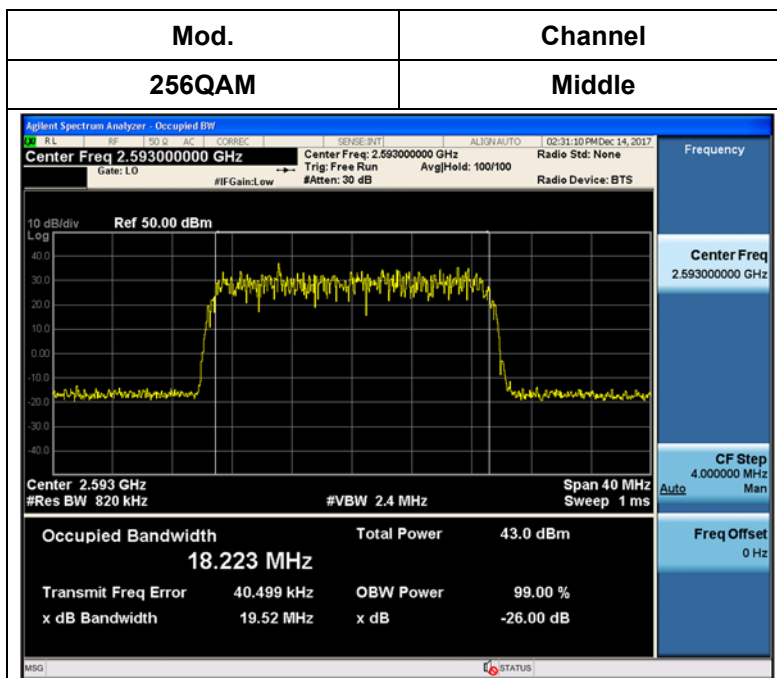


Plot Data for Output Port 7

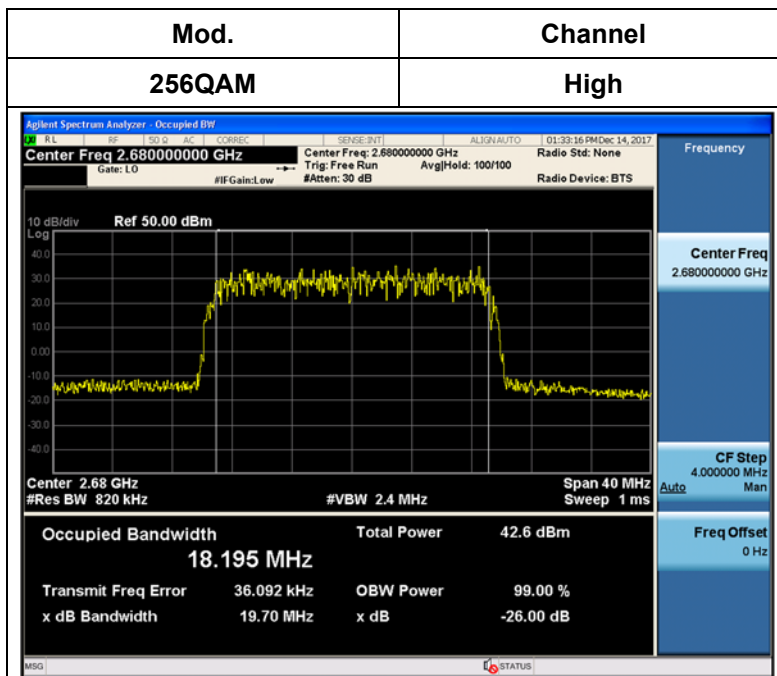


20 MHz / 1 Carrier (10 W)

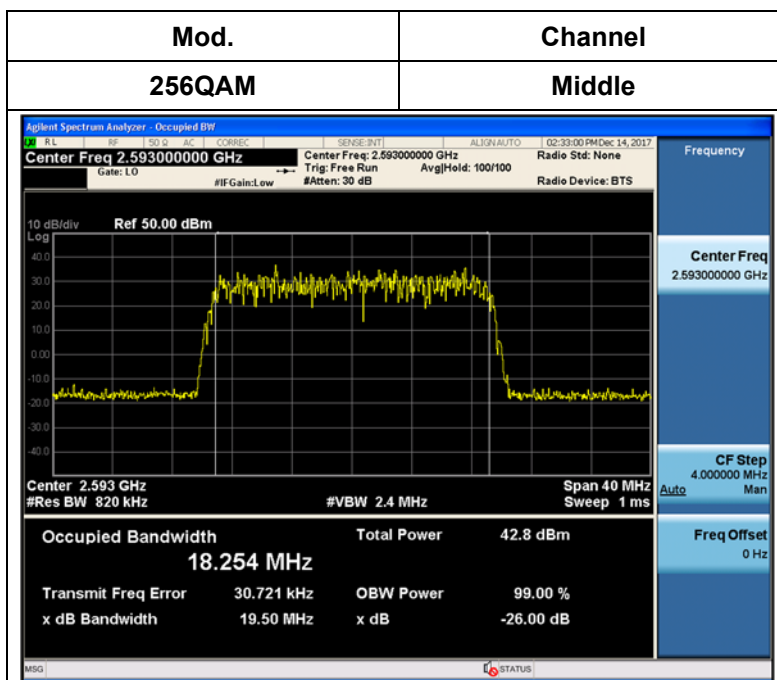
Plot Data for Output Port 0



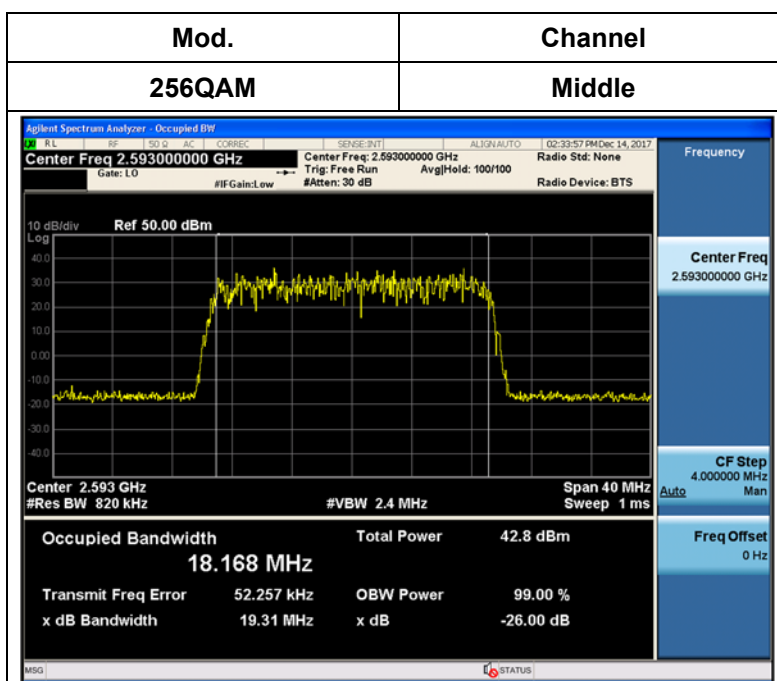
Plot Data for Output Port 1



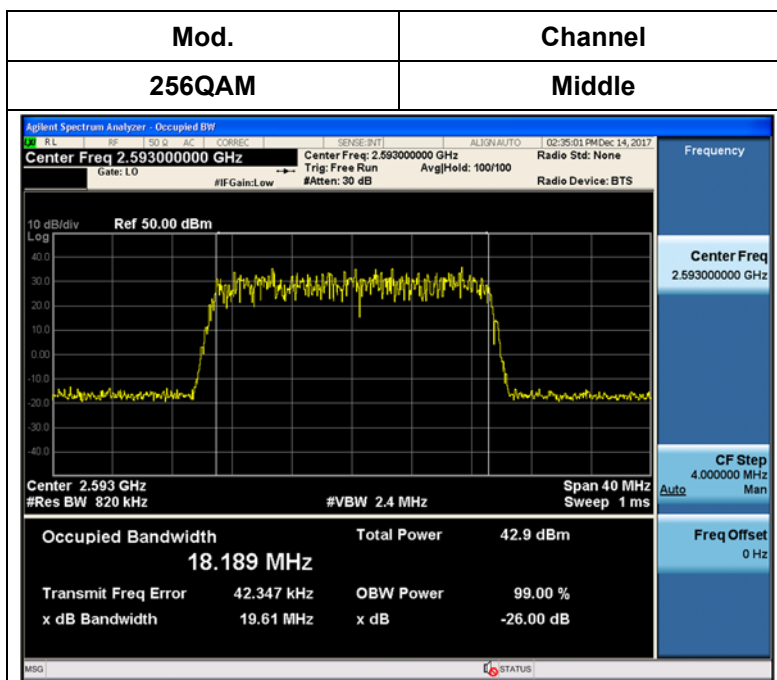
Plot Data for Output Port 2



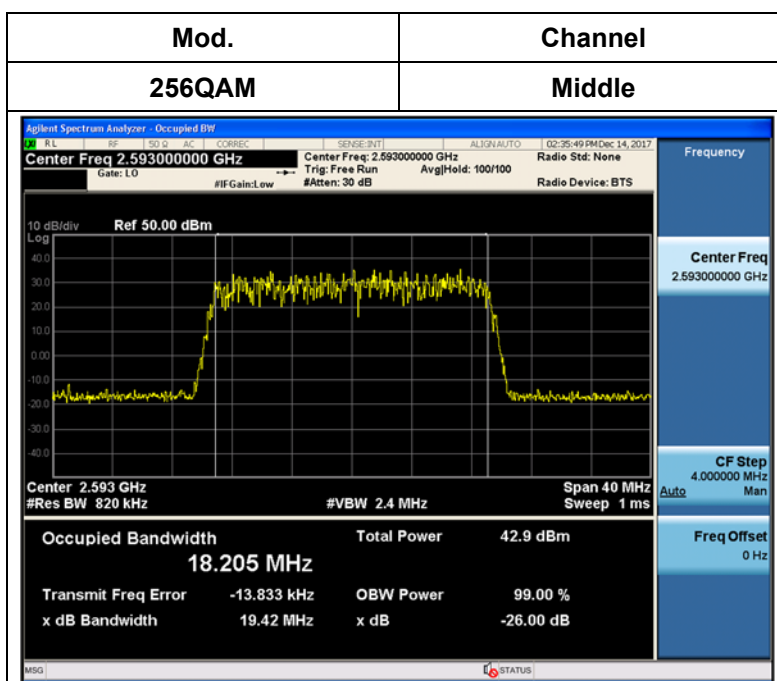
Plot Data for Output Port 3



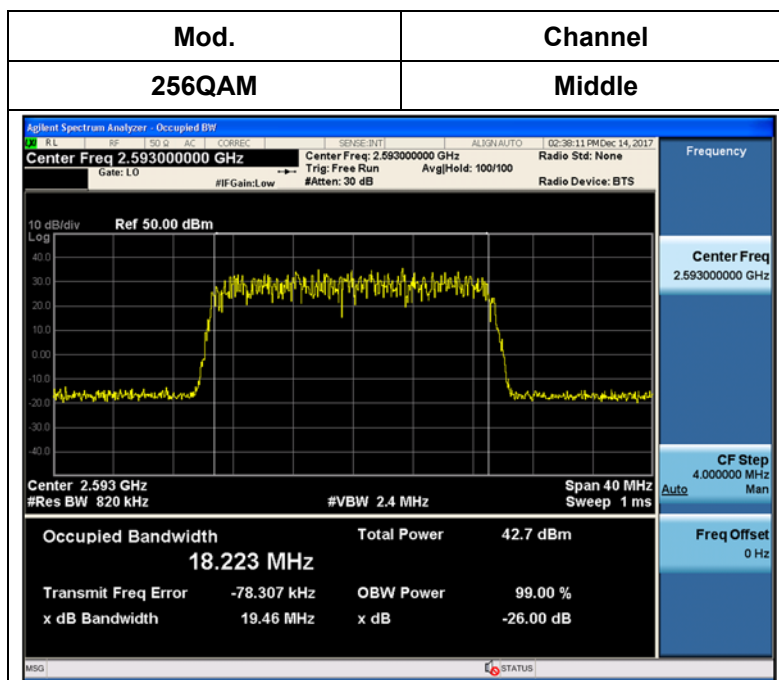
Plot Data for Output Port 4



Plot Data for Output Port 5



Plot Data for Output Port 6



Plot Data for Output Port 7

