

SiW1502 Radio Modem IC

1. INTRODUCTION

The SiW1502 Radio Modem IC is part of Silicon Wave's Odyssey™ solutions for Bluetooth™ wireless communications. The SiW1502 IC combines a 2.4-GHz radio transceiver and GFSK modem with digital control functions meeting Bluetooth specifications. The SiW1502 IC is designed to work with the Silicon Wave SiW1602 Link Controller IC or other compatible ICs to enable production of Bluetooth wireless communication products.

2. FEATURES

- Radio and modem with combined RF analog and digital CMOS circuits on a single integrated silicon chip.
- Fully qualified under Bluetooth Specification 1.1.
 - Suitable for Class 2 and 3 transmit power classifications, or Class 1 with external circuits.
- Direct-conversion radio architecture with integrated VCO and frequency synthesizer requiring minimal external components.
- Integrated analog-digital conversion circuits transform I/O signals between the radio and GFSK modem.
- Integrated GFSK modem with digital modulation, channel filtering, AFC, symbol timing recovery, and bit-slicer.
- Integrated 0-dBm transmit driver with eight output power levels.
- Direct interface to Bluetooth controller ICs through a low pin-count, digital interface.
- Optimized design for low power consumption, low cost, and small size.

3. APPLICATIONS

The SiW1502 Radio Modem is suitable for all applications requiring a radio link with Bluetooth wireless technology in a low-power and cost-effective implementation.

- **Cellular Use:** integration of mobile phone handsets and accessories.
- **Office:** office PCs, notebook PCs, and printers.
- **Personal Data:** PDAs, palmtops, personal organizer, and multimedia devices.
- **Consumer:** digital cameras and handheld game units.
- **Automotive:** hands-free car kits.

4. DESCRIPTION

Figure 1 shows the functional block diagram. During the receive process, the radio signal is taken from a pair of balanced RF I/O pins that feed into the low noise amplifier (LNA). Direct I/Q down conversion and on-chip filtering send the processed I/Q data to the analog-to-digital converter before processing by the GFSK demodulator. Within the demodulator, data detection and timing recovery circuits convert the data for transfer to an external device. The transmit process operates in a similar fashion in reverse order. Digital control functions and a programming interface provide radio modem control and a flexible interface to external Bluetooth link controller ICs.

For efficient power management, each section of the radio may be powered down when not in use. The active circuitry required for the master clock reference and low-power clock used to supply clock signals to external devices is located on the SiW1502.

The transmitted signal is GFSK modulated data that is amplified on the chip to yield a radiated output of 0 dBm. A power control signal for an external amplifier is provided.

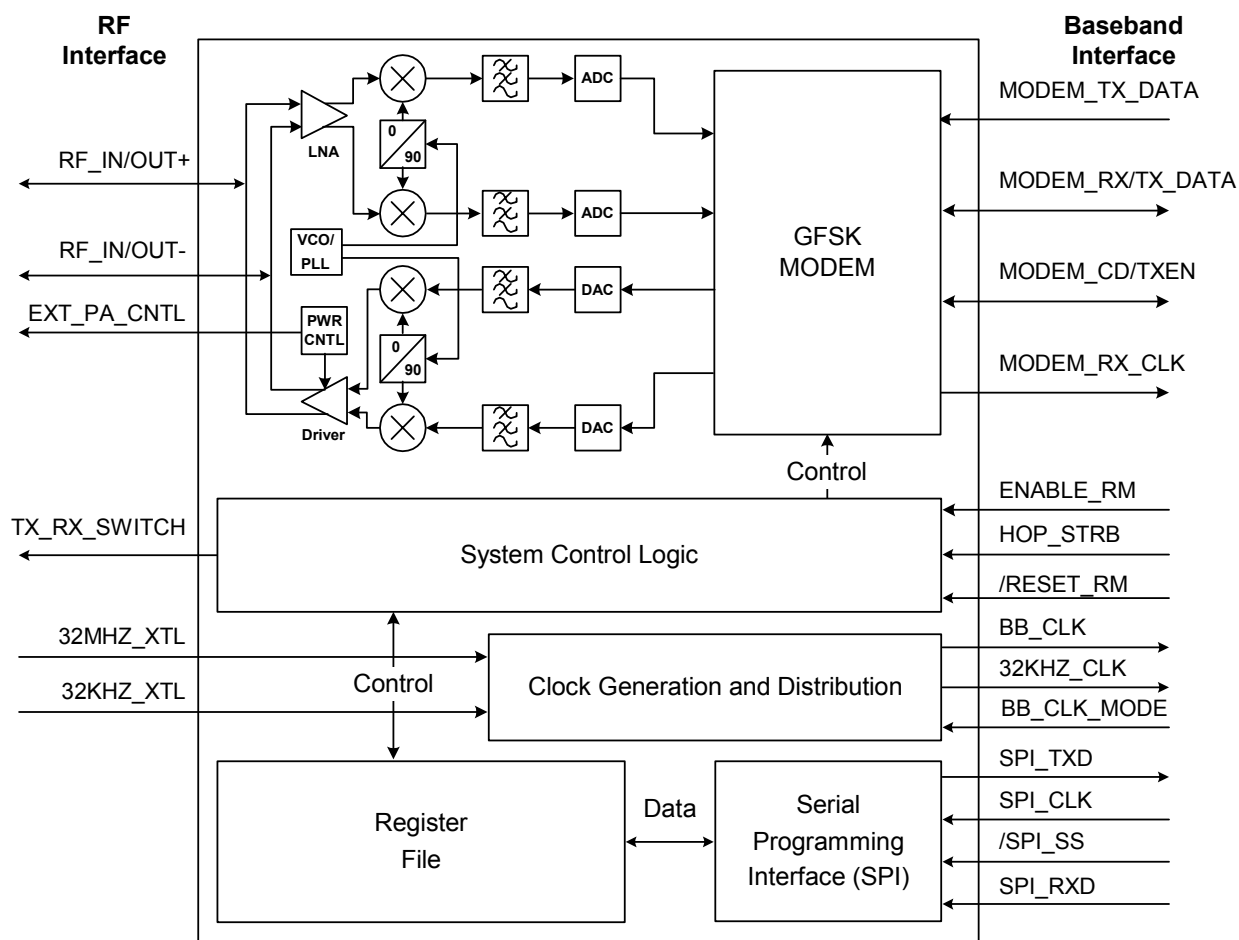


Figure 1: SiW1502 IC Block Diagram

5. PIN DESCRIPTION

The SiW1502 IC's radio and modem interface, the Serial Programming Interface (SPI), and the two clock inputs are required for proper operation.

5.1. Radio Interface

The radio interface provides an antenna connection through external circuitry to transmit and receive the Bluetooth radio signals. Control signals for the external transmit/receive switch and optional power amplifier are available.

External impedance matching and balun circuits are required to complete the interface to the antenna. Please refer to Figure 4 in Section 8 for the recommended external circuit details.

Name	Direction	Description
RF_IN/OUT+	I/O	Positive RF input and output pin.
RF_IN/OUT-	I/O	Negative RF input and output pin.
EXT_PA_CNTL	O	Power control to external power amplifier. This output provides a variable current source that can be used to control the external power amp.
TX_RX_SWITCH	O	Output to select external transmit/receive switch circuit for external PA (20 dBm) configurations. High = Receive Low = Transmit

Table 1: Signal Description

5.2. Modem Interface

The modem interface transfers the Bluetooth data between the SiW1502 and an external controller such as the SiW1602 IC. The programmable interface on the SiW1502 can be set to various operating modes, depending on the desired interface usage. Programming of the interface is done through internal registers. For reference purposes, Table 2 provides a brief description of typical interface modes.

Name	Direction	Description
MODEM_TX_DATA	I	Transmit data.
MODEM_RX_DATA	I/O	This pin has two possible programmable mode settings (through internal registers): 1. Symbol synchronized received data at 1 MHz. 2. Sliced receive data at 8 MHz (sliced output).
MODEM_CD/TXEN	I/O	Dual function carrier detect and transmit enable. This bi-directional signal can be enabled through internal registers. During transmit, this pin can be used as an INPUT to indicate valid transmit data (TXEN). During receive, this pin can be used as OUTPUT to indicate carrier detect (CD).
MODEM_RX_CLK	O	Receive clock output that is based on the Bluetooth packet data recovered timing of 1 MHz. The output can be optionally disabled.
ENABLE_RM	I	Enables 32-MHz oscillator.
HOP_STRB	I	Signal generated by the link controller to indicate the start of TX or RX ramp-up.

Table 2: Modem Interface Signal Description

Name	Direction	Description
BB_CLK	O	Clock output to baseband circuits. Clock is programmable to 1/1, 1/2, 1/3, or 1/4 of the 32-MHz input clock.
/RESET_RM	I	Reset for digital circuits only. State machines and internal registers reset to their default state. This signal is asynchronous input with a minimum pulse width requirement of 10 μ s. NOTE: When /RESET_RM is active, BB_CLK will be disabled.

Table 2: Modem Interface Signal Description (continued)

5.3. Clock Signals

The 32-MHz clock is used as a reference for the RF circuits, to synthesize clocks for most of the internal digital circuits, and to supply external processors with timing signals. The 32-kHz clock is used by external circuits during low power modes to conserve system power.

Name	Direction	Description
32KHZ_XTL+	I	32- or 32.768-kHz crystal oscillator out.
32KHZ_XTL-	I	32- or 32.768-kHz crystal oscillator in.
32MHZ_XTL+	I	32-MHz crystal oscillator out.
32MHZ_XTL-	I	32-MHz crystal oscillator in.
32KHZ_CLK	O	32-kHz output.
BB_CLK	O	Clock output to baseband circuit. The clock is programmable to 1/1, 1/2, 1/3, or 1/4 of the 32-MHz clock.
BB_CLK_MODE	I	Selects either 8 MHz or 16 MHz for baseband clock (BB_CLK) during system power up and before the internal clock control registers are set by software. "HIGH", the BB_CLK will be set to 16 MHz. "LOW", the BB_CLK will be set to 8 MHz.

Table 3: Clock Signals

5.4. Serial Programming Interface (SPI)

The Serial Programming Interface is used to access the internal registers of the SiW1502 IC. The SPI is a synchronous serial interface that can be clocked to speeds up to 4 MHz. SPI communication uses four signals. /SPI_SS, which selects the SiW1502 for transfer, is active low. Note that /SPI_SS does not have to de-assert and the serial clock does not have to pause after each byte transmission. Figure 2 shows a high-level block diagram of the interface.

Name	Direction	Description
SPI_RXD	I	SPI receive port for write/input.
SPI_TXD	O	SPI transmit port for read/output.
SPI_CLK	I	Clock input used for synchronous data transfers on the SPI bus.
/SPI_SS	I	Slave select input. Selects the SiW1502 IC as the target of a transfer.

Table 4: Programming Interface

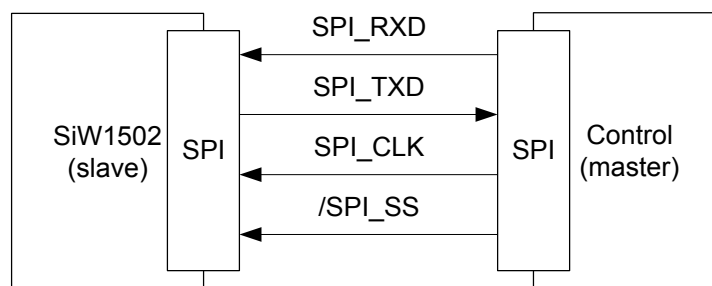


Figure 2: SPI Interface

5.5. Other I/O

The following pins are used by the system for various analog and digital circuits of the radio modem.

Name	Direction	Description
VREFP_CAP	I	Decoupling capacitor for voltage reference for internal A/D converter. Recommended value = 100 nF.
VREFM_CAP	I	Decoupling capacitor for voltage reference for internal A/D converter. Recommended value = 100 nF.
VC_CAP	I	Decoupling capacitor for voltage reference for internal A/D converter. Recommended value = 100 nF.
TUNE_IN	I	Control input for VCO tuning.
CHRG_PUMP	I	PLL charge pump output for external loop filter circuit.
DIGITAL_REG_CAP	I	An external capacitor for the internal digital regulator. Recommended value = 100 nF.
NC	NA	Used for manufacturing test only.

Table 5: Miscellaneous Signals

5.6. Power and Ground Pins

Separate 3-V supplies are recommended for the digital and analog circuits of the SiW1502.

Name	Direction	Description
VCC	I	Analog 3-V supply inputs.
VDD	I	Digital 3-V supply inputs.
VCC_BATT	I	This input is used to supply the on-chip low-power regulator.
V2.3_OUT	O	Low-power 2.3-V output from internal low power regulator.
GND	I	Ground pins (3 total). In addition, the package has a ground paddle on the package center to provide better grounding.

Table 6: Power and Ground Pins

6. PIN CONFIGURATION

6.1. 48-Pin MLF Package (SiW1502-NC)

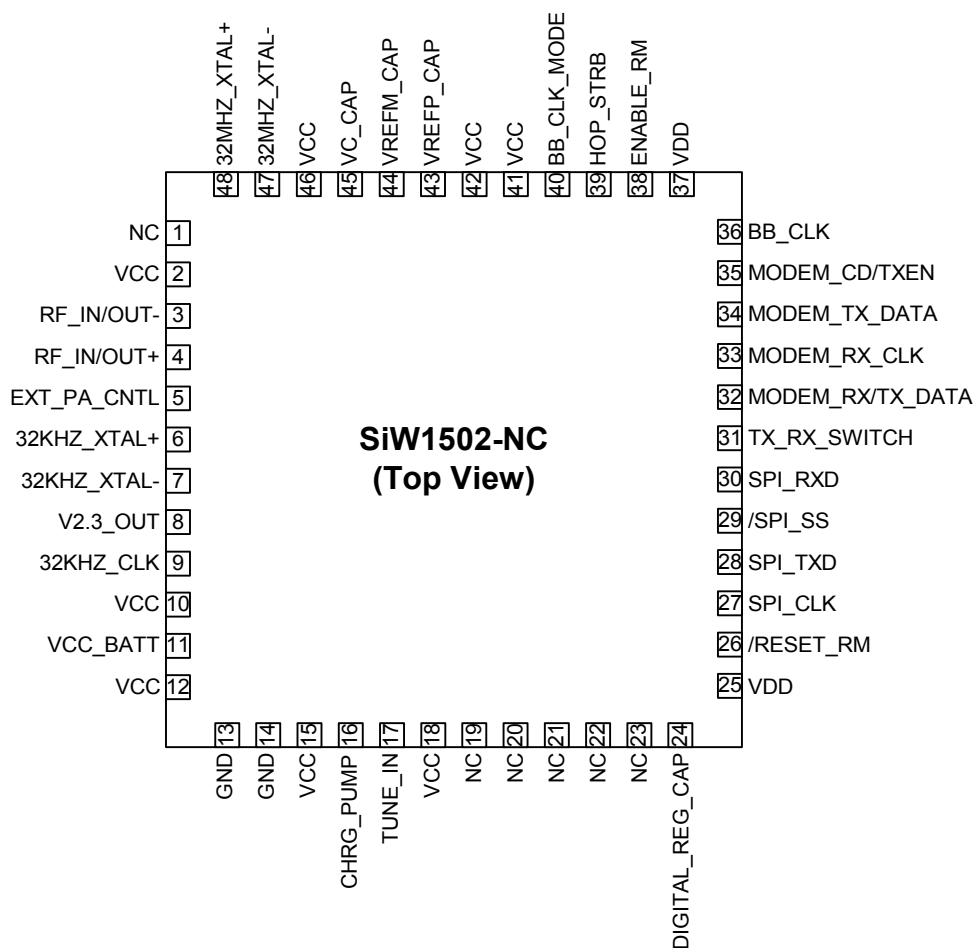


Figure 3: SiW1502-NC Pin Configuration

Pin	Pin Function	Pin	Pin Function	Pin	Pin Function
1	NC	17	TUNE_IN	33	MODEM_RX_CLK
2	VCC	18	VCC	34	MODEM_TX_DATA
3	RF_IN/OUT-	19	NC	35	MODEM_CD/TXEN
4	RF_IN/OUT+	20	NC	36	BB_CLK
5	EXT_PA_CNTL	21	NC	37	VDD
6	32KHZ_XTAL+	22	NC	38	ENABLE_RM
7	32KHZ_XTAL-	23	NC	39	HOP_STRB
8	V2.3_OUT	24	DIGITAL_REG_CAP	40	BB_CLK_MODE
9	32KHZ_CLK	25	VDD	41	VCC
10	VCC	26	/RESET_RM	42	VCC
11	VCC_BATT	27	SPI_CLK	43	VREFP_CAP
12	VCC	28	SPI_TXD	44	VREFM_CAP
13	GND	29	/SPI_SS	45	VC_CAP
14	GND	30	SPI_RXD	46	VCC
15	VCC	31	TX_RX_SWITCH	47	32MHZ_XTAL-
16	CHRG_PUMP	32	MODEM_RX/TX_DATA	48	32MHZ_XTAL+

Table 7: SiW1502-NC Pin Assignment

7. SPECIFICATIONS

7.1. ESD Precautions

These devices are electrostatic sensitive. Devices should be transported and stored in anti-static containers and handled in accordance with MIL-STD-1686. Equipment and personnel contacting the devices need to be properly grounded. Cover workbenches with grounded conductive mats.

7.2. Absolute Maximum Ratings

Parameter	Description	Min	Max	Units
VCC, VDD	Supply voltage NOTE: other than VCC_BATT	-0.3	3.6	V
ESD	ESD protection – analog/RF pins	500		V
	ESD protection – digital pins		2000	V
RF input level			-5	dBm
T _{ST}	Storage temperature	-55	+125	°C
T _j	Junction temperature		125	°C

7.3. Recommended Operating Conditions

Parameter	Description	Min	Max	Units
T _{OP}	Operating temperature	-20	+85	°C
VCC	VCC analog supply voltage	2.7	3.3	V
VDD	VDD digital supply voltage	2.7	3.3	V
VCC_BATT	Internal voltage regulator supply	2.7	4.8	V

7.4. Electrical Characteristics

7.4.1. DC Specification (T_{op} = 25°C; VDD = 3.0 V)

Parameter	Description	Min	Typ	Max	Units
VIL	Input low voltage	GND - 0.1		0.2 · VDD	V
VIH	Input high voltage	0.7 · VDD		VDD	V
VOL	Output low voltage	GND		0.1 · VDD	V
VOH	Output high voltage	0.8 · VDD		VDD	V
IOH	Output high current			1	mA
IOL	Output low current			1	mA
ICC (transmit)	Current consumption during transmit – analog VCC pins, power level 7		36		mA
IDD (transmit)	Current consumption during transmit – digital VDD pins		11		mA
ICC (receive)	Current consumption during receive – analog VCC pins, high gain		32		mA
IDD (receive)	Current consumption during receive – digital VDD pins		20		mA
Sleep Current	Current from VCC_BATT with VCC & VDD disconnected		7		μA

7.4.2. 2.3-V Regulator Specification ($T_{op} = 25^{\circ}\text{C}$; $V_{CC_BATT} = 2.7$ to 4.8 V)

Parameter	Min	Typ	Max	Unit
Output voltage (IOUT = 10 μA)	2.0	2.3	2.6	V
Line regulation (IOUT = 0 mA; VIN = 2.7 V to 4.8 V)			15	mV
Load regulation (IOUT = 0 μA to 10 μA ; VIN = 4.8 V)			8	mV
Minimum Dropout voltage (IOUT = 10 μA)			250	mV
Output absolute maximum current			1.0	mA
Quiescent current		2.5		μA
Ripple rejection at ($f_{RIPPLE} = 400$ Hz)		-30		dB

**7.4.3. EXT_PA_CNTL Output Current for External Power Amplifier Control
($T_{op} = 25^{\circ}\text{C}$; $V_{CC} = 3.0$ V)**

Internal control register bit setting (register 0x10)	Min	Typ	Max	Unit
111	900	1000	1100	μA
110	577	642	706	μA
101	342	380	418	μA
100	218	242	266	μA
011	131	146	155	μA
010	88	98	108	μA
001	45	50	55	μA
000	23	25	28	μA

7.4.4. Radio specification

Parameter	Description	Min	Max	Unit
Frequency operating range	VCO operating range	2400	2480	MHz

7.4.5. Receiver specification (At Chip RF input; $T_{op} = 25^{\circ}\text{C}$; $V_{CC} = 3.0$ V)

Parameter	Description	Min	Typ	Max	Unit
Receiver sensitivity	BER < 0.1%		-85	-80	dBm
Maximum useable signal		-15	-12		dBm
C/I co-channel (0.1% BER)	Co-channel selectivity		9	11	dB
C/I 1 MHz (0.1% BER)	Adjacent channel selectivity		-6	-3	dB
C/I 2 MHz (0.1% BER)	2nd adjacent channel selectivity		-41	-30	dB
C/I ≥ 3 MHz (0.1% BER)	3rd adjacent channel selectivity		-46	-40	dB
Intermodulation	3MHz, 6MHz offset	-30	-26		dBm
Receiver spurious emission	30 MHz to 1 GHz			-57	dBm
	1 GHz to 12.75 GHz			-47	dBm

7.4.6. Transmitter Specification (At Chip RF output; T_{op} = 25°C; VCC = 3.0 V)

Parameter	Description	Min	Typ	Max	Unit
Output RF transmit power	At maximum power output setting	-3	0		dBm
In-band spurious emission (±500 kHz)	Measured in accordance with FCC DA00-705			-20	dBc
In-band spurious emission	2 MHz offset		-55	-40	dBm
In-band spurious emission	>3 MHz offset			-60	dBm
Out-of-band spurious	30 MHz to 1 GHz, operating mode			-55	dBm
Out-of-band spurious	30 MHz to 1 GHz, idle mode			-57	dBm
Out-of-band spurious	1-to-12.75 GHz, operating mode ⁽¹⁾			-50	dBm
Out-of-band spurious	1-to-12.75 GHz, idle mode			-47	dBm
Out-of-band spurious	1.8-to-1.9 GHz			-62	dBm
Out-of-band spurious	5.15-to-5.3 GHz			-47	dBm

NOTE: (1) Except transmit harmonics.**7.4.7. VCO and PLL Specification**

Parameter	Description	Typ	Max	Unit
PLL lock up time		85	140	μs
Charge pump output	Charge pump output current	0.25		mA
VCO gain	VCO voltage gain	60		MHz/V

7.4.8. Crystal Requirements–32 MHz

The 32-MHz crystal should be in fundamental mode and of parallel resonant type.

Parameter	Description	Typ	Unit
F _o	Center frequency	32	MHz
Frequency tolerance	Worst case over all operating conditions ⁽²⁾	±20	PPM
ESR	Effective serial resistance	<60.	Ω

NOTE: (2) ±20 ppm frequency tolerance has to be guaranteed over all operating conditions including temperature, voltage, and component tolerances.

7.4.9. Crystal Requirements–32 kHz

The 32-kHz crystal should be in fundamental mode and of parallel resonant type. Either 32 kHz or 32.768 kHz can be used.

Parameter	Description	Typ	Unit
F _o	Center Frequency.	32 or 32.768	kHz
Frequency tolerance	Worst case over all operating conditions.	±250	ppm
ESR	Effective serial resistance	<50	kΩ

8. APPLICATION CIRCUIT

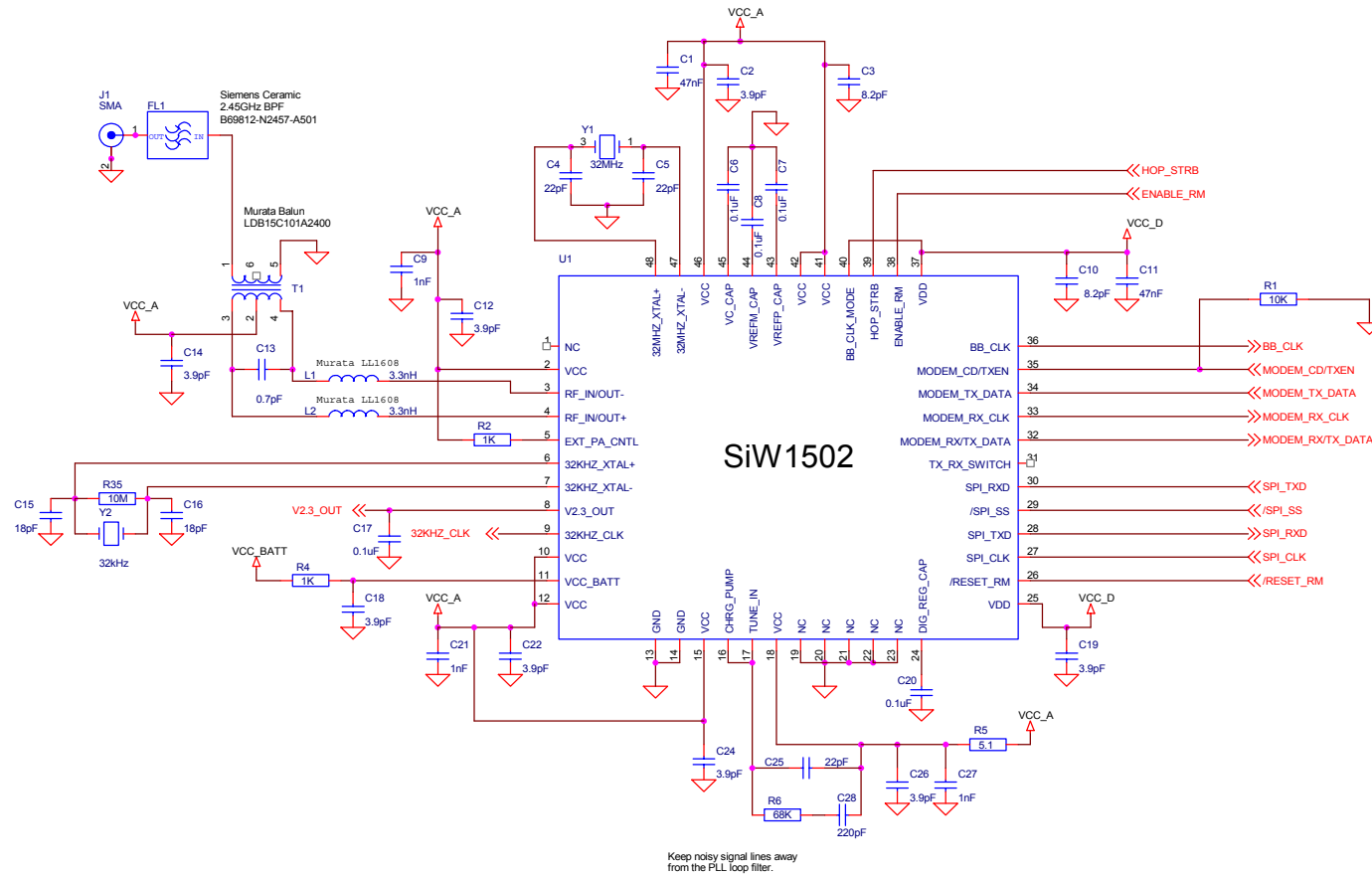
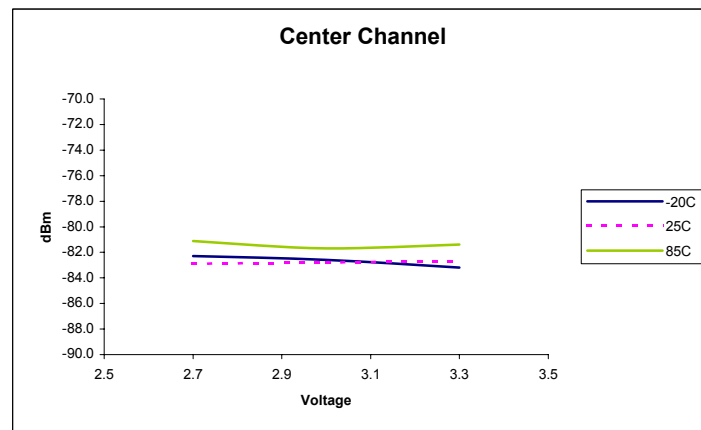


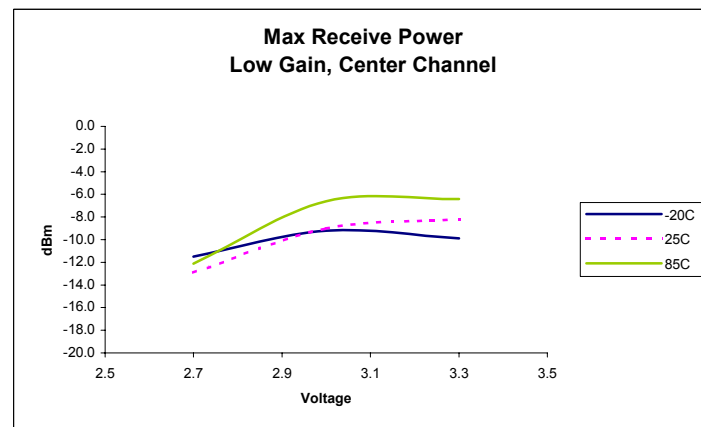
Figure 4: SiW1502-MC IC Application Circuit

9. CHARACTERIZATION DATA – OVER TEMPERATURE AND SUPPLY VOLTAGE

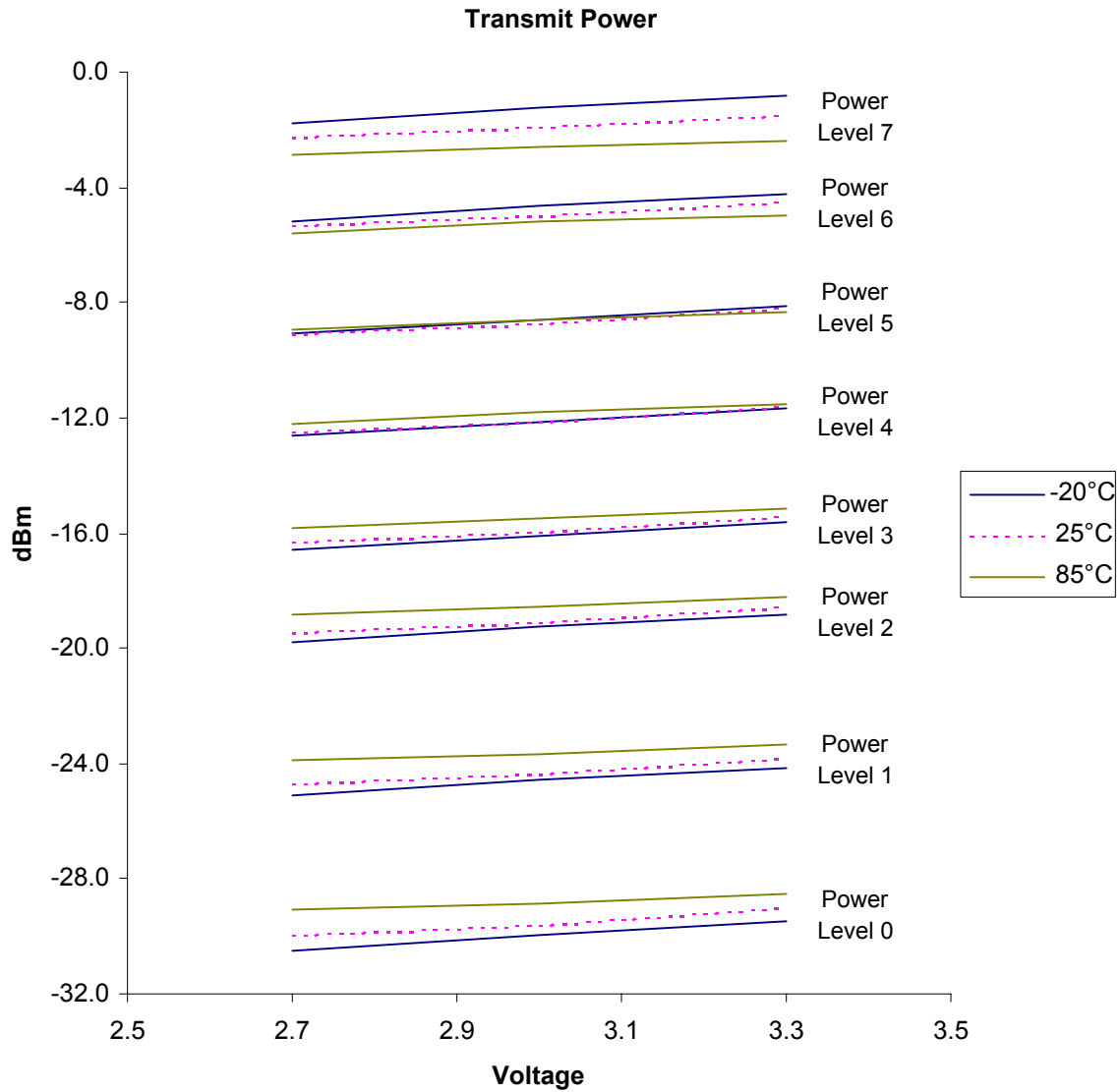
9.1. Receiver Sensitivity



9.2. Maximum Receive Power

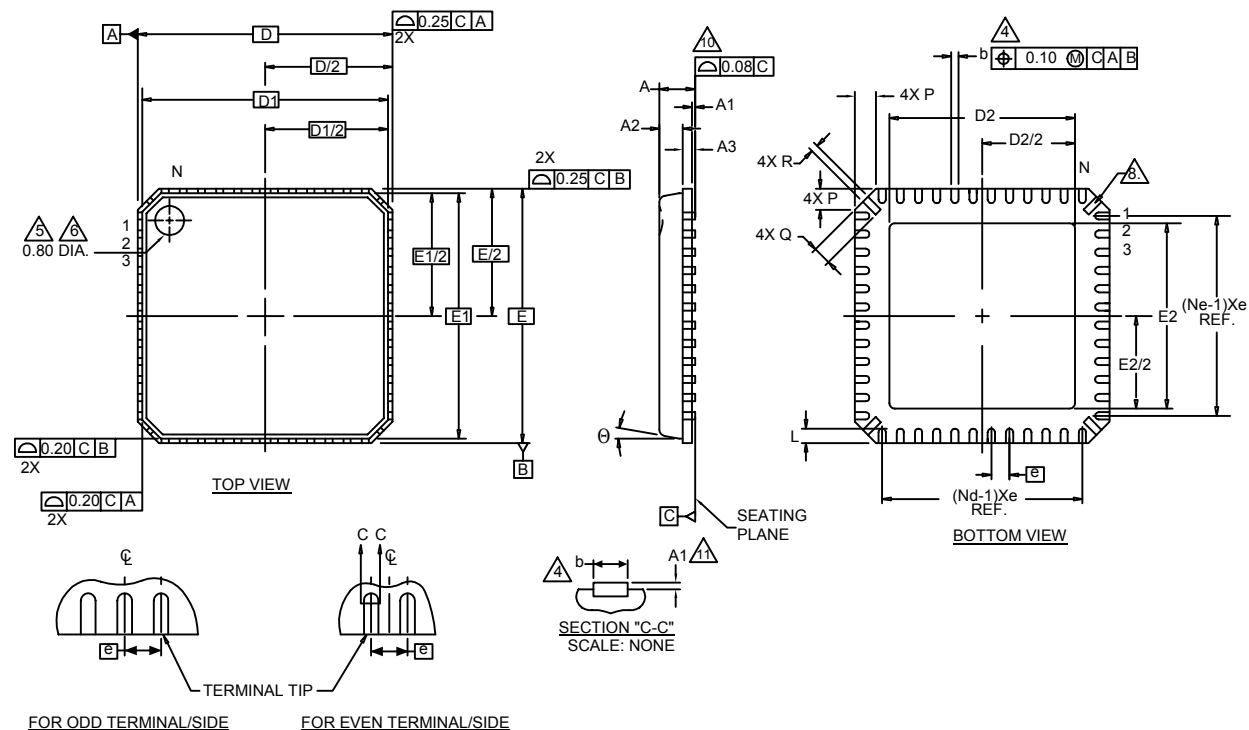


9.3. Transmit Output Power



10. PACKAGING AND PRODUCT MARKINGS

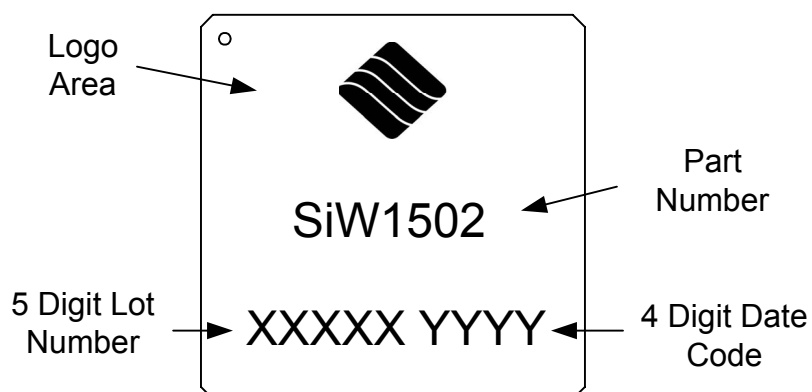
Please contact Silicon Wave for the most current packaging and product markings.

10.1. SiW1502 Package: 48 MLF Drawing and Dimensions

Symbol	Min	Nom	Max	NOTE
A	-	0.85	1.00	
A1	0.00	0.01	0.05	11
A2	-	0.65	0.80	
A3	0.20 REF.			
b	0.18	0.23	0.30	4
D	7.00 BSC			
D1	6.75 BSC			
D2	4.95	5.10	5.25	
E	7.00 BSC			
E1	6.75 BSC			
E2	4.95	5.10	5.25	
e	0.50 BSC			
L	0.30	0.40	0.45	
N	48			3
Nd	12			3
Ne	12			3
P	0.24	0.42	0.60	
Q	0.00	0.20	0.45	
R	0.13	0.17	0.23	
θ			12°	

NOTES:

- Die thickness allowable is 0.305 mm (.012 inches) maximum.
- Dimensioning & tolerances conform to ASME Y14.5M - 1994.
- N is the number of terminals.
Nd is the number of terminals in x-direction and Ne is the number of terminals in y-direction.
- Dimension b applies to plated terminal and is measured between 0.20 and 0.25 mm from terminal tip.
- The PIN #1 identifier must exist on the top surface of the package by using indentation mark or other feature of package body.
- Exact shape and size of this feature is optional.
- All dimensions are in millimeters.
- The shapes shown on four corners are not actual I/O.
- Package warpage max 0.08 mm.
- Applied for exposed pad and terminals. Exclude embedding part of exposed pad from measuring.
- Applied for terminals only.

10.2. SiW1502 Manufacturing Related Information**11. ORDERING INFORMATION**

Part Number	Ordering Quantity
SiW1502-NC	476 pcs. per tray
SiW1502-NC-TR	1000 on a 7" reel, 2500 on a 13" reel

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