NORTEL NETWORKS

EXHIBIT 3

Technical Description

Applicant: Northern Telecom Ltd.

For Type Acceptance/Certification on:

AB6NT800FRM

1 MCBTS 800 MHz Flexible Radio Module Hardware Description

The 800 MHz FRM is the RF equipment portion of Nortel's Multi-Carrier BTS product. All the IF and RF circuitry is contained in the FRM. The digital portion of the MCBTS product is contained in a Digital Enclosure (DE). The DE is responsible for the baseband signal processing and control circuitry.

1.1 Brief Description of Digital Equipment Module

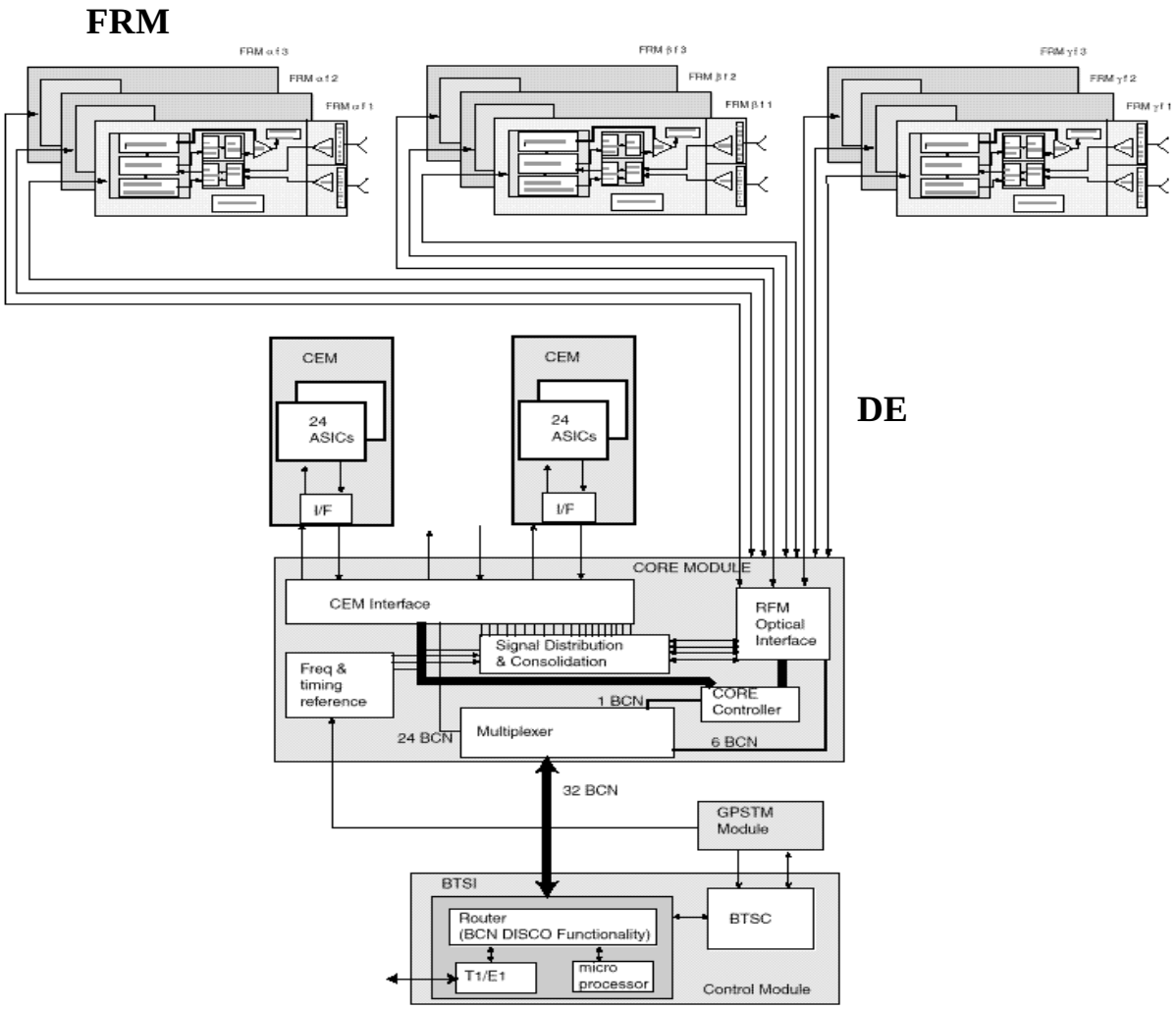


Figure 1: MCBTS Product Architecture

Figure 1 shows the product architecture of the MCBTS and the interfaces between the FRMs and the Digital Enclosure. The DE modules comprise: the Channel Element Module (CEM), COnfiguration REsource module (CORE), Control Module (CM), and Global Positioning System module (GPS).

The CEM contains 24 or 48 Channel Elements (CE) on one or two channel cards, CEM Interface circuitry, serial/parallel converters and a power supply. The CCs themselves are identical to the current design with the exception that the analogue output block is removed and Tx and Rx baseband data is transported through serial/parallel conversion circuitry to reduce the interconnect. Baseband digital Rx signals, BCN, and frequency/timing reference from each CORE are via high speed serial copper connections. Baseband

digital Tx signals to each CORE are via high speed serial copper connections. Power and the Tx/Rx baseband are distributed on a simple shielded backplane.

The CORE Module provides the interface between the FRMs and the CEMs. The CORE comprises optical interfaces to the FRMs, baseband signal routing, and timing reference circuitry. Essentially the CORE provides switching, routing, addition and multiplexing of signals between the CEMs and the FRMs. The CORE module can be flexibly programmed to support many different system configurations.

The Control Module consists of a BTSC and a BTS Interface (BTSI). The BTSI provides termination of up to 6 T1/E1 ports. The BTSI provides support for the following:

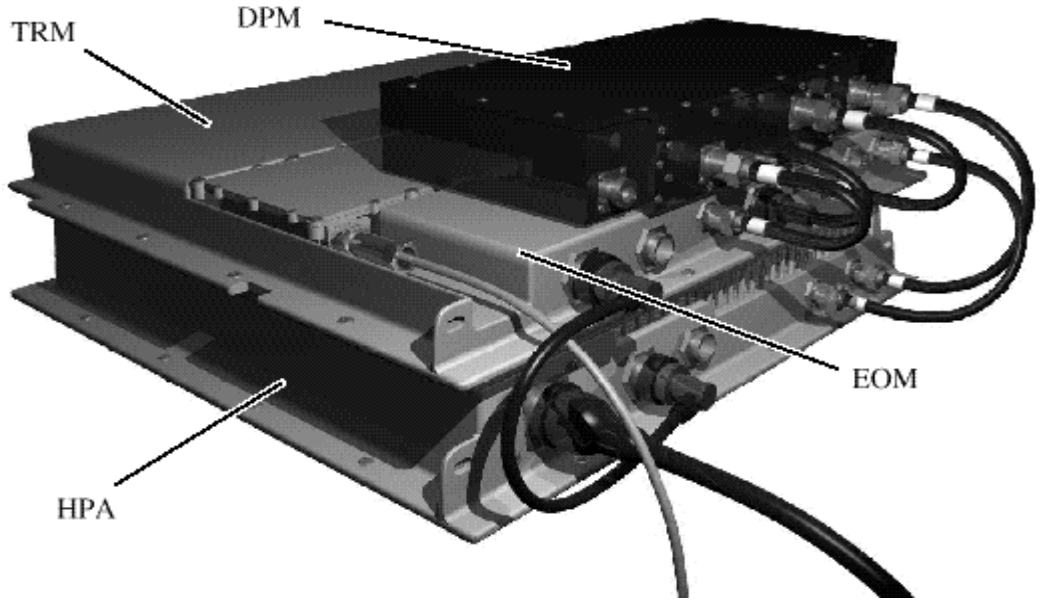
- BCN
- fractional, daisy-chained (drop and insert), and redundancy (1+1) for the T1/E1 ports

The BTSI utilizes an embedded processor to control/monitor the T1/E1 ports, to emulate the CSU interface, and to perform card level maintenance and diagnostics. In addition the BTSI provides the BCN interface to both the BTSC and the CORE modules.

The GPS module is the source of frequency reference and timing information for the BTS. The GPS module directly provides reference signals to the CORE module and Control module. Other modules (i.e., CEMs, RFM etc.) receive reference signals indirectly through the CORE module. The GPS module is controlled via an RS-422 port by the BTSC.

1.2 FRM Description

A picture of the FRM is shown below and the FRM architecture is shown in Figure 2:



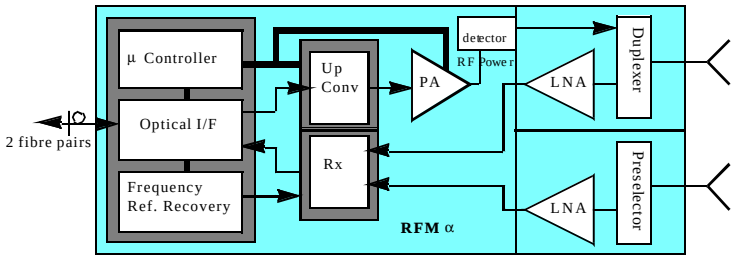


Figure 2: 800 MHz FRM Architecture

Each FRM can support one CDMA carrier on one sector. However, for compatibility with future multi carrier HPAs, the optical interface is designed for three carrier operation. With single carrier HPAs, multi-frequency operation is achieved using multiple FRMs.

Multi-frequency operation necessitates multiple antennas per sector. Multi-faceted antennas or multiple single facet antennas are to provide this functionality. A duplexer/LNA module is required for each antenna. Two carriers in each sector can be supported on a diversity pair of antennas (a diversity pair per sector is the minimum antenna requirement for any CDMA system) in each sector.

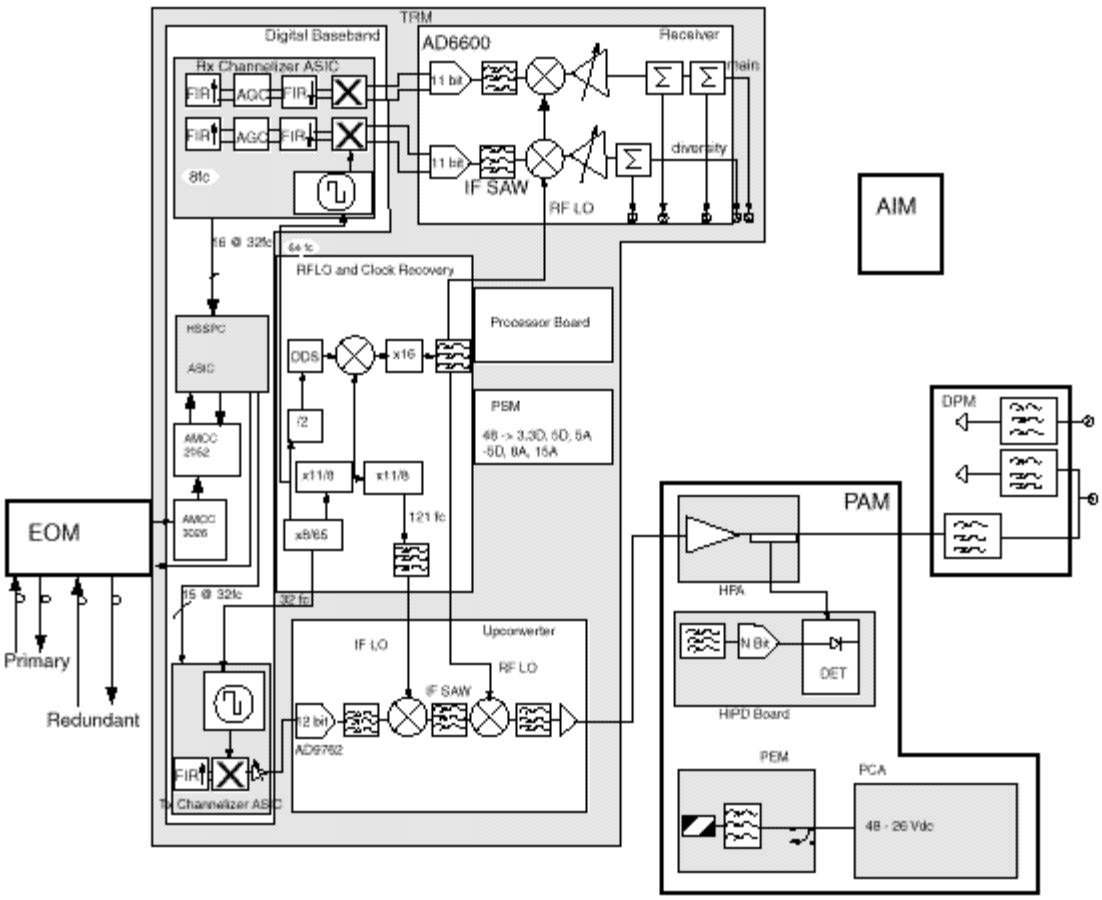
Within the receiver and upconverter many of the functions (E.G. filtering, Channelization, AGC) are performed digitally. Hence, the FRM interfaces to the digital enclosure are digital. The interface is implemented as a high speed serial digital optical link. The data transmitted over the optical link between the FRM and the CORE comprises Tx and Rx data , OA&M signalling, and frequency and timing reference signals.

The micro-controller and associated control circuitry within the FRM performs configuration, fault monitoring and several real time functions (mainly concerned with Tx sector power control) for the RF electronics.

The frequency reference recovery circuit recovers a frequency reference received over the optical interface with sufficient accuracy and low phase noise to meet ANSI J-STD-008 and IS-95 specifications.

A block diagram of the FRM is shown in Figure 3.

Figure 3: FRM Block Diagram



The FRM interfaces with the Configuration Resource (CORE) module within the digital enclosure (DE) via a completely digital optical link representing both the forward and reverse air interface, and OA&M information. DC power is supplied via a -48 volt cable. A minimum of two RF interfaces are required: one for main (Tx and Rx); and the other for diversity Rx. Additionally, internal and external RF interconnect is required to allow for multi-RFM per sector provisioning while minimizing antenna requirements.

Functionally, the 800 MHz FRM will convert a composite baseband digital input into a single carrier CDMA TX RF output signal. Similarly, it will convert main and diversity into digital baseband output. In addition to OA&M, blossom/wilting, TX output power control, and other system real-time control functions are implemented within the FRM via a micro-processor.

The FRM consists of the following modules:

- Transmit / Receive Module (TRM)

- Power Amplifier Module (PAM)
- Duplexer / LNA Preselector / LNA module (DPM)
- Electro-Optical Module (EOM)

Each of these modules is described in the following sections.

1.2.1 Transmit / Receive Module (TRM)

The TRM provides the RF interface between the transmit and receive FRM I/O blocks. It also provides all the necessary conversion and signal processing to digital baseband required by the optical interface.

The TRM interfaces with the following:

- Electro- Optical Module (EOM)
- Transmit upconverter output to the HPA
- Receiver (Main and Diversity) to the DPM
- Microprocessor board
- Power Supply Module (PSM), Power Entry Module (PEM) and Power Converter Module (PCA for DC voltages

Both the Main and Diversity signals (received from the antennas and passed through the LNA duplexer) are presented to the receiver for frequency translation and A/D conversion to digital baseband.

The transmit upconverter takes the digital baseband signal and upconverts it to the 800 MHz RF frequency and forwards this signal to the HPA.

Clock recovery is performed using the transmit high speed digital signaling. The recovered clock synchronizes the onboard Los used within the TRM board for frequency conversion and clock generation. These synthesized Los and clocks are necessary for proper frequency conversion and data processing within the various functional blocks.

The TRM utilizes two high speed digital interfaces; one for transmit and one for receive. The EOM interface is source/destination for these signals. They are fed via AMCC2052 interfce and the logical level shifting required for the HSSPC and clock recovery circuitry. Signal processing of the converted digital signal is performed by the Channelizer ASICs. These two functional blocks, transmit and receive channelizers, provide the digital baseband signal fed from and to the HSSPC.

The PSM is fed directly from the –48 Vdc main supply voltage (and/or from DE). It produces the following regulated DC voltages:

- +3.3 V, +5 V, and –5 V for the digital circuits
- +5 V, +8V, and +15 V for the analog circuits

1.2.2 Power Amplifier Module

The PAM contains the HPA, PCA, PEM and HIPD modules.

The HPA provide the final stage amplification for the Transmit signal. The amplifier has a maximum gain of 45 dB.

The PCA accepts nominal –48 V DC power and produces two regulated +26 V DC outputs; one for the HPA and one for auxiliary circuits (fused).

The PEM provides connector termination, surge protection, equipment grounding, EMI filtering and 15A circuit breaker protection for the -48V DC power input to the PCA and PSM.

The PAM also housed the HPA interface and power detector board (HIPD) which measures the RMS power of the transmitted CDMA signal. It communicates the measurement to the TRM processor via the inter-integrated circuit (IIC) bus. The HIPD also performs the following functions:

- controls the enable / disable state of the HPA.
- converts the status signals, HPA anxiety, HPA alarm, HPA fwd pwr, HPA rev pwr and HPA temp to digital information to be transferred to the TRM processor via the IIC bus.
- interfaces with the PCA and reports the status of the alarm to the TRM processor via the IIC bus.
- allows storage of data within an IIC addressable EEPROM which is used for manufacturing information and calibration data for the power detector.
- drives and powers the Fan Assembly Module.

1.2.3 Electro - Optical Module (EOM)

The EOM contains the circuitry and optical transceivers required to convert the optical to digital conversion for the CDMA forward channel and the digital to optical signal conversion for the CDMA reverse channel. The EOM provide thissignal conversion for both the primary and redundant signal paths.

1.2.4 Duplexer / LNA Preselector / LNA Module (DPM)

The duplexer component of the module provides two functions:

- provides isolation between the transmit and receive frequency bands thus facilitating the use of one antenna per diversity branch per sector
- provides filtering of the transmit and receive frequencies thus reducing interfering signals

The LNA component of the module provides a low noise amplification at the system front end thus reducing the overall effects of noise.

The 800MHz DPM operates within the Single Channel FRM (SFRM) framework of the 800 MHz CDMA base station. The DPM is the last stage in the transmit section of the SFRM preceding the antenna and lightning surge protectors; the DPM is the first stage in the receive section of the SFRM following the antenna and lightning surge protectors.

In the single carrier per sector case, the DPM must include a preselector / LNA that provides a conditioned antenna diversity signal to the receiver.

In the multicarrier per sector case, the DPM does not require the additional preselector / LNA to achieve antenna diversity.