



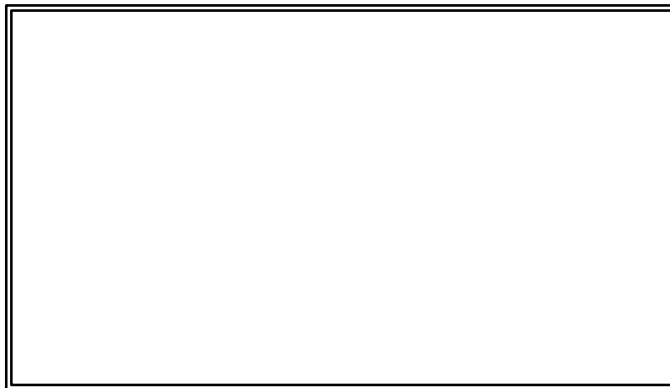
DATA STORM INC.

8334 FOOTHILL BLVD., SUNLAND, CALIFORNIA 91040
(818)352-4994 TEL.
(818)352-9794 FAX.

Engineering Specification

V-KEYFOB
Transmitter Duty Cycle Test

Data Storm/Mytek
Confidential





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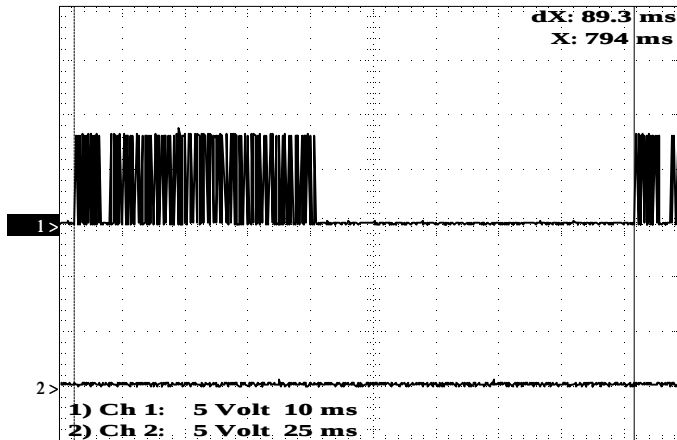
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V-Keyfob Duty Cycle

1. Transmission Time: 89.3mS per transmission



2. Code Format

FIGURE 4-1: CODE WORD TRANSMISSION FORMAT

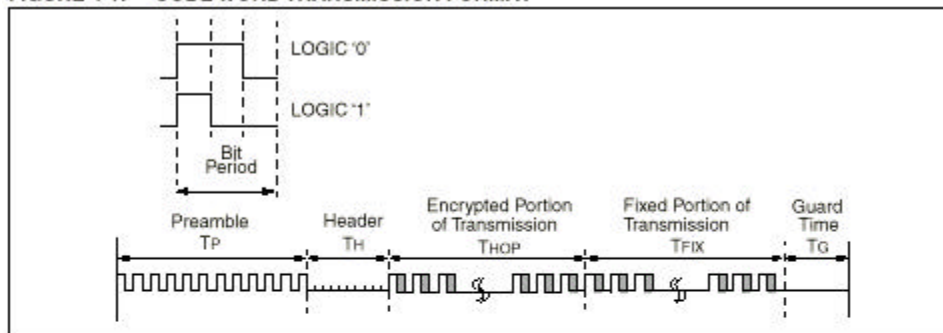
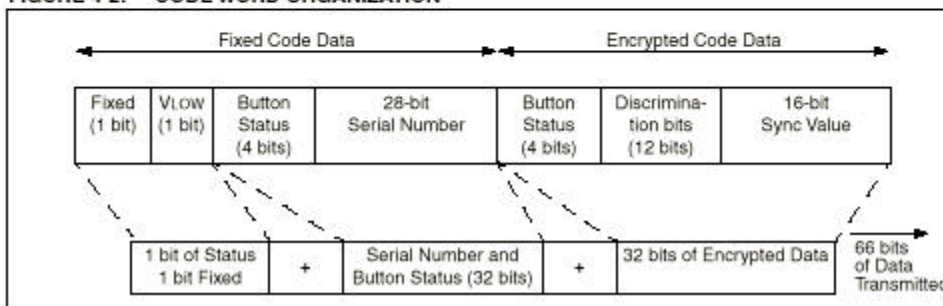


FIGURE 4-2: CODE WORD ORGANIZATION





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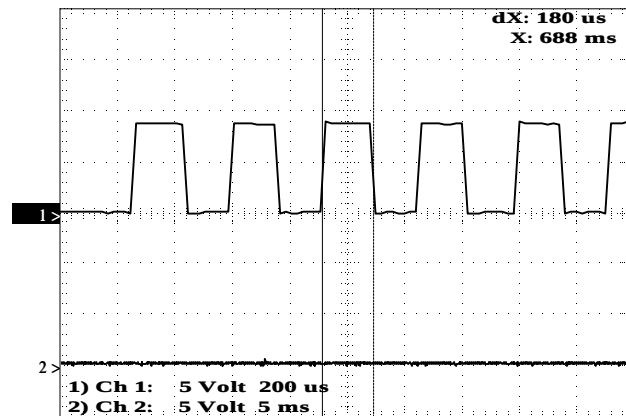
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VDD = +3.5 to 13.0V				
Commercial (C): Tamb = 0°C to +70°C				
Industrial (I): Tamb = -40°C to +85°C				
Symbol	Characteristic	Number of TE	Typ.	Units
TE	Basic pulse element	1	200	µs
TBP	PWM bit pulse width	3	600	µs
TP	Preamble duration	23	4.6	ms
TH	Header duration	10	2.0	ms
THOP	Hopping code duration	96	19.2	ms
TFIX	Fixed code duration	102	20.4	ms
TG	Guard Time	39	7.8	ms
—	Total Transmit Time	270	54.0	ms
—	PWM data rate	—	1667	bps

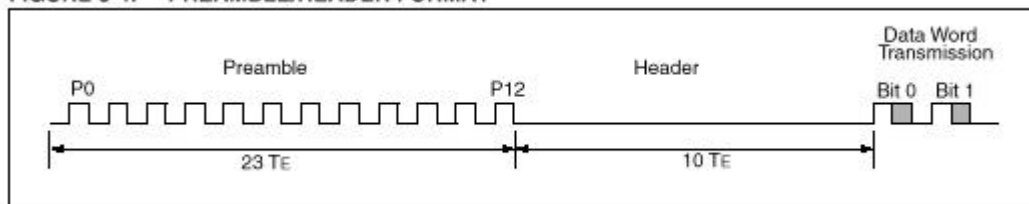
Measured TE: 180uS



3. Preamble (TP):

	Typical	Measured
TP	4.6mS	3.82mS
On Time	2.4mS	1.99mS
Off Time	2.2mS	1.83mS
Duty Cycle %	52%	52%

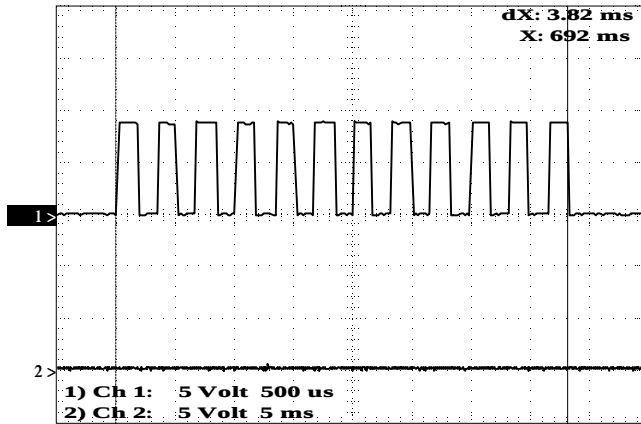
FIGURE 8-4: PREAMBLE/HEADER FORMAT





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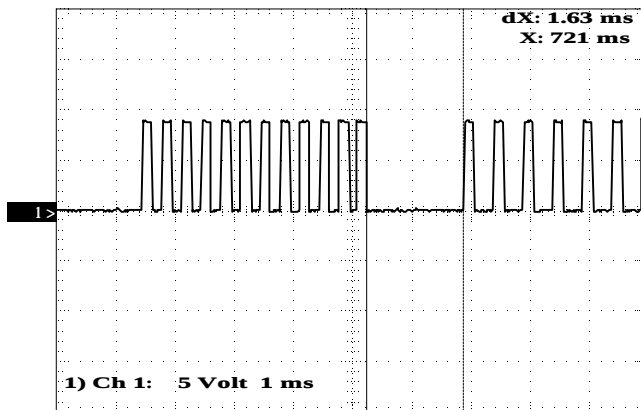
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4. Header (TH): 1.63mS

TH is typically 2.0mS.

	Typical	Measured
TH	2.0mS	1.63mS
On Time	0mS	0mS
Off Time	2.0mS	1.63mS
Duty Cycle %	-	-



5. Encrypted Portion of Transmission (THOP):

The Encrypted Data is generated from 3 button bits, 12 discrimination bits, and the 16-bit sync value. Total 32 bits. This data can't be all 0. Worst case will be estimated to be 28 logic 0 (87.5%)bits and 4 logic 1 bits (12.5%). Measured data was 00001 01101 11110 11101 11101 01110 11. There was 21 logic 1 (65%) and 11 logic 0 (35%).

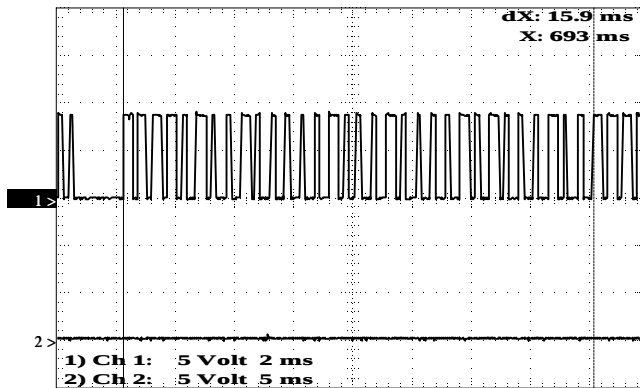
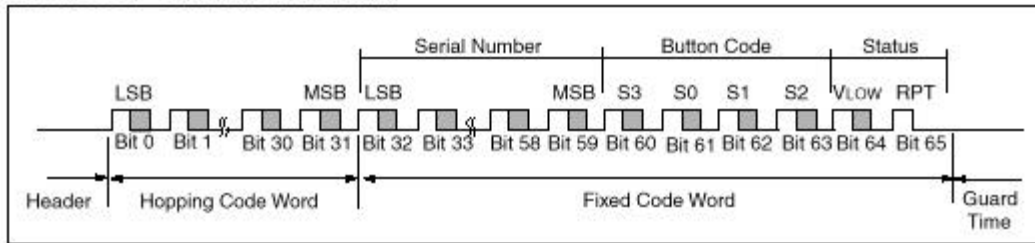
	Typical	Measured
THOP	19.2mS	15.9mS
On Time	12mS (28 logic 0 and 4 logic 1)	7.1mS (11 logic 0 and 21 logic 1)
Off Time	7.2mS	8.8mS
Duty Cycle %	62.5%	44.7%



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FIGURE 8-5: DATA WORD FORMAT



6. Fixed Portion of Transmission (TFIX):

The Fixed Code Data is made up from 1 status bit (Vlow), 1 fixed bit (logic 1), 4 button bits, and the 28-bit serial number. 4 button bit in worst case will be 3 logic 0 and 1 logic 1. Worst case for this transmission will be 28 serial data being 0 and button data being in worst case (3 logic 0) and Vlow bit being 0 will result in 32 logic 0 bits (94%) and 2 logic 1 bits (6%). Measured data was 00000 01101 01110 11111 11111 11001 0001. There was 14 logic 0 (41%) and 20 logic 1 (59%).

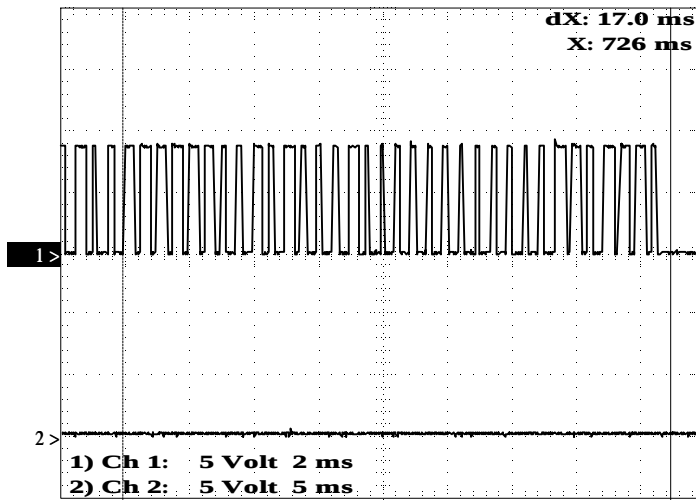
	Typical	Measured
TFIX	20.4mS	17.0mS
On Time	13.2mS (32 logic 0, and 2 logic 1)	8mS
Off Time	7.2mS	9mS
Duty Cycle %	64.7%	47%

	External			Internal			
	S2	S1	S0	S3	S2	S1	S0
Standby after CC	0	0	0	0	0	0	0
Hop	0	0	1	0	0	0	1
	0	1	0	0	0	1	0
	0	1	1	0	0	1	1
	1	0	0	1	1	0	0
	1	0	1	1	1	1	0
	1	1	0	1	1	1	0
Fixed	1	1	1	1	1	1	1



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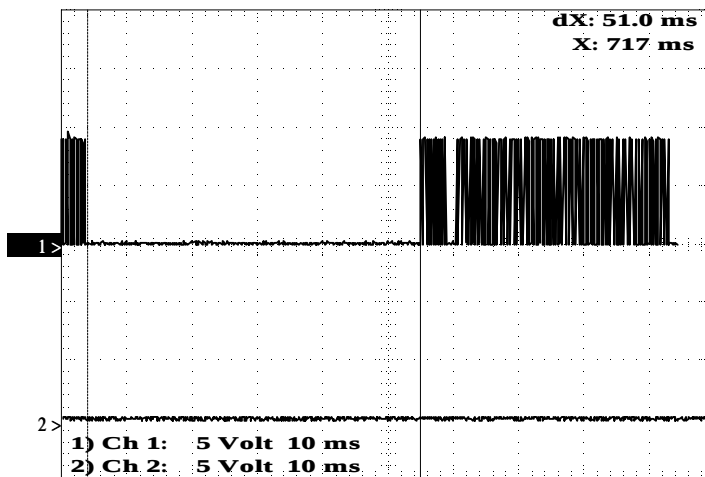
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7. Guard Time (TG) & Rest Time:

TG is 7.8mS Typical and rest time is 54mS.

	Typical	Measured
TG and Rest Time	54mS	51mS
On Time	0mS	0mS
Off Time	54mS	51mS
Duty Cycle %	-	-



8. Duty Cycle:

Duty cycle is calculated by Total On Time over Total Transmit Time or 100mS if Total Transmit Time is greater than 100mS. Therefore Duty Cycle is calculated as below:



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	Typical		Measured	
	On Time	Total Time	On Time	Total Time
TP On Time	2.4mS	4.6mS	1.99mS	3.82mS
TH On Time	0mS	2.0mS	0mS	1.63mS
THOP On Time	12mS	19.2mS	7.1mS	15.9mS
TFIX On Time	13.2mS	20.4mS	8mS	17.0mS
TG & Rest Time	0mS	54mS	0mS	51mS
Total Time	27.6mS	100.2mS	17.09mS	89.3mS
Duty Cycle	27.6%		19.14%	