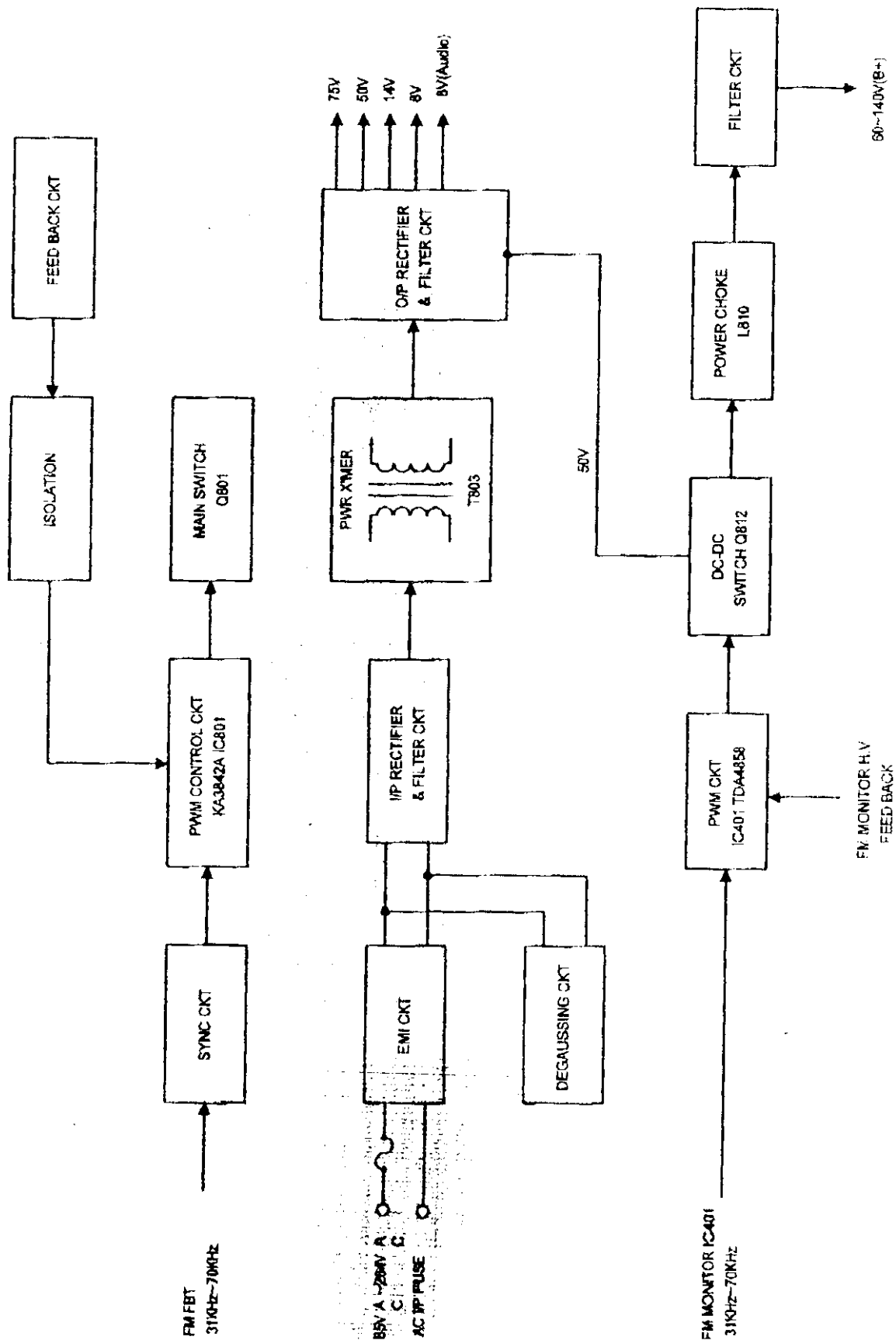


BLOCK DIAGRAM (SPS)



FCC ID: AMPJ51H

The diagram illustrates the internal architecture of the Philips 7446 television receiver, organized into three main functional areas:

- Signal Processing Section:**
 - Input:** An I/O CABLE provides SIGNAL R.G.B INPUT and HV SYNC INPUT to the system.
 - Pre-Processing:** The SIGNAL R.G.B INPUT goes to IC801 (VIDEO PRE-AMP TDA4885). The HV SYNC INPUT goes to IC101 (CPU MICRO CONTROL DDC1/DDC2B 68HC06BD7).
 - Processing:** IC801 outputs O-R, O-G, and O-B signals to IC804 (VIDEO OUTPUT LM2409T). IC101 is connected to an I²C BUS and also controls IC902 (OSD MTV016-10).
 - Output:** IC804 outputs R, G, and B signals to the CRT. IC902 outputs to the VERT. AMP (TDA4866 IC301).
- Control and Timing Section:**
 - Timing:** IC102 (E²PROM 24C08) is connected to IC101 via an I²C BUS.
 - Horizontal Sync:** IC101 outputs H-SIZE, H-PHASE, V-SIZE, V-POSITION, KEYSTONE, and PINK signals to IC401 (COMBINED HORIZONTAL & VERTICAL PROCESSOR TDA4868).
 - Vertical Sync:** IC401 outputs to the VERT. AMP (TDA4866 IC301).
- Power and Drive Section:**
 - Power Supply:** AC input goes to a SWITCHING POWER SUPPLY, which provides 76V, 50V, 14V, 6V, and 6V(Audio) rails. A REGULATOR (ZD802 OB15) provides a 5V rail. A POWER MANAGEMENT block controls the supply.
 - Driver:** The VERT. AMP (TDA4866 IC301) drives the H-DRIVER, which includes IC701, IC703, and IC704, IC713. This drives the H. OUTPUT TRANSISTOR (BU2520DF Q407) through a DRIVER TRANSFORMER (T401).
 - Deflection:** The H-DRIVER also drives the DEFLECTION YOKE. The VERT. AMP also drives the DEFLECTION YOKE.
 - Power Regulation:** A DC-DC CONVERTER (BU2520DF) is connected to the 50V rail and provides a 5V output to the HV REGULATOR.

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