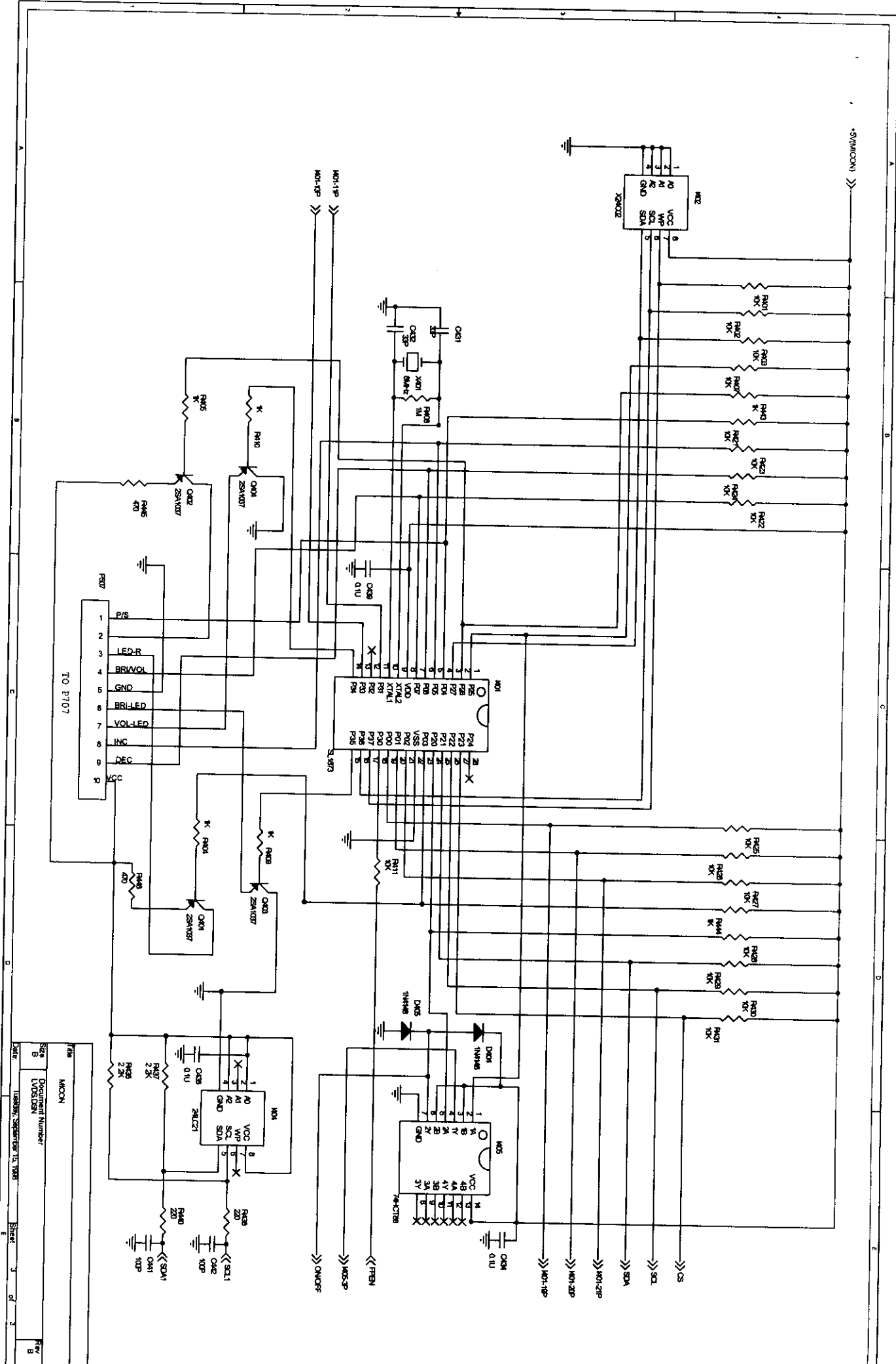
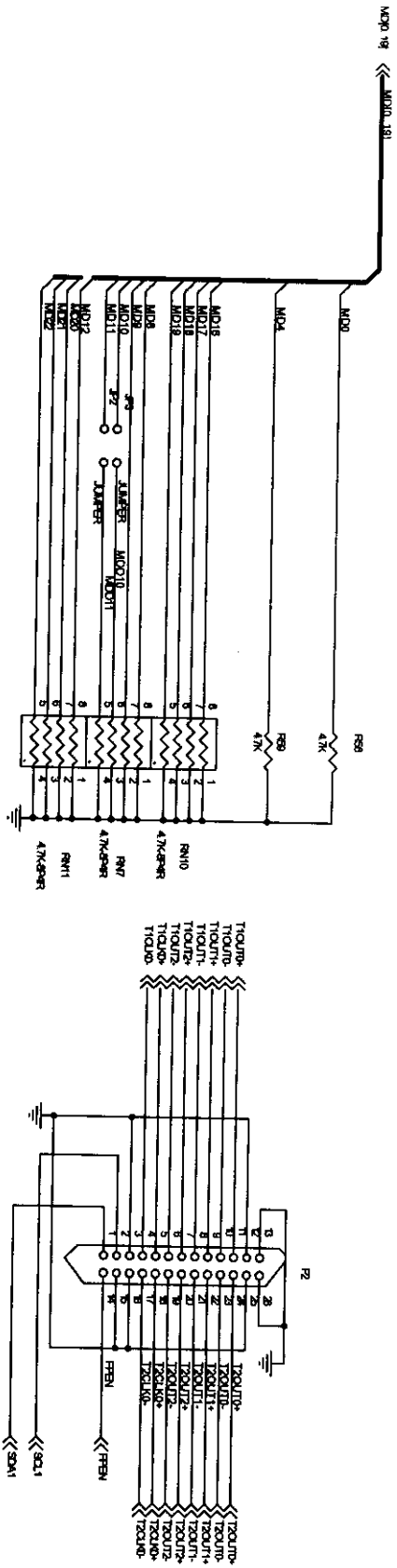






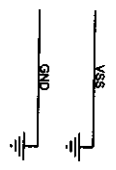
MD0 : 0=8MCLK
1=7MCLK
MD1 : 0=4MCLK
1=3MCLK Memory RAS to CAS Delay
MD2 : 0=1MB bank each
1=2MB bank each
MD3 : 0=4MCLK
1=3MCLK Memory Pre-charge time select

MD[5:4] : 10= 8-bit column address
11= 9-bit column address
0x= 10-bit column address
MD6 : 0= disable Block Write for Drawing Processor
1= Enable Block Write for Drawing Processor

MD7 : 0=EDO DRAM 1=SDRAM or SGRAM
MD8 : 0=Color TFT 1=Color STN
MD9 : 0=Normal 1=Inverted TFT FPCCLK select
MD[11:10] : 00= 640x480 LCD DISPLAY SIZE
01= 800x600
10= 1024x768
11= 1280x1024

MD[14:12] : 110= 36-bit (18+18-bit , 2 pixel/clock)
100= 24-bit (12+12-bit , 2 pixel/clock)
011= 24-bit , 8-bit per R,G,B
MD15 : 0=16-bit interface DSTN Interface type
1= 24-bit interface

JP3	JP2	
ON	ON	640X480
OFF	ON	800X600
ON	OFF	1024X768
OFF	OFF	1280X1024

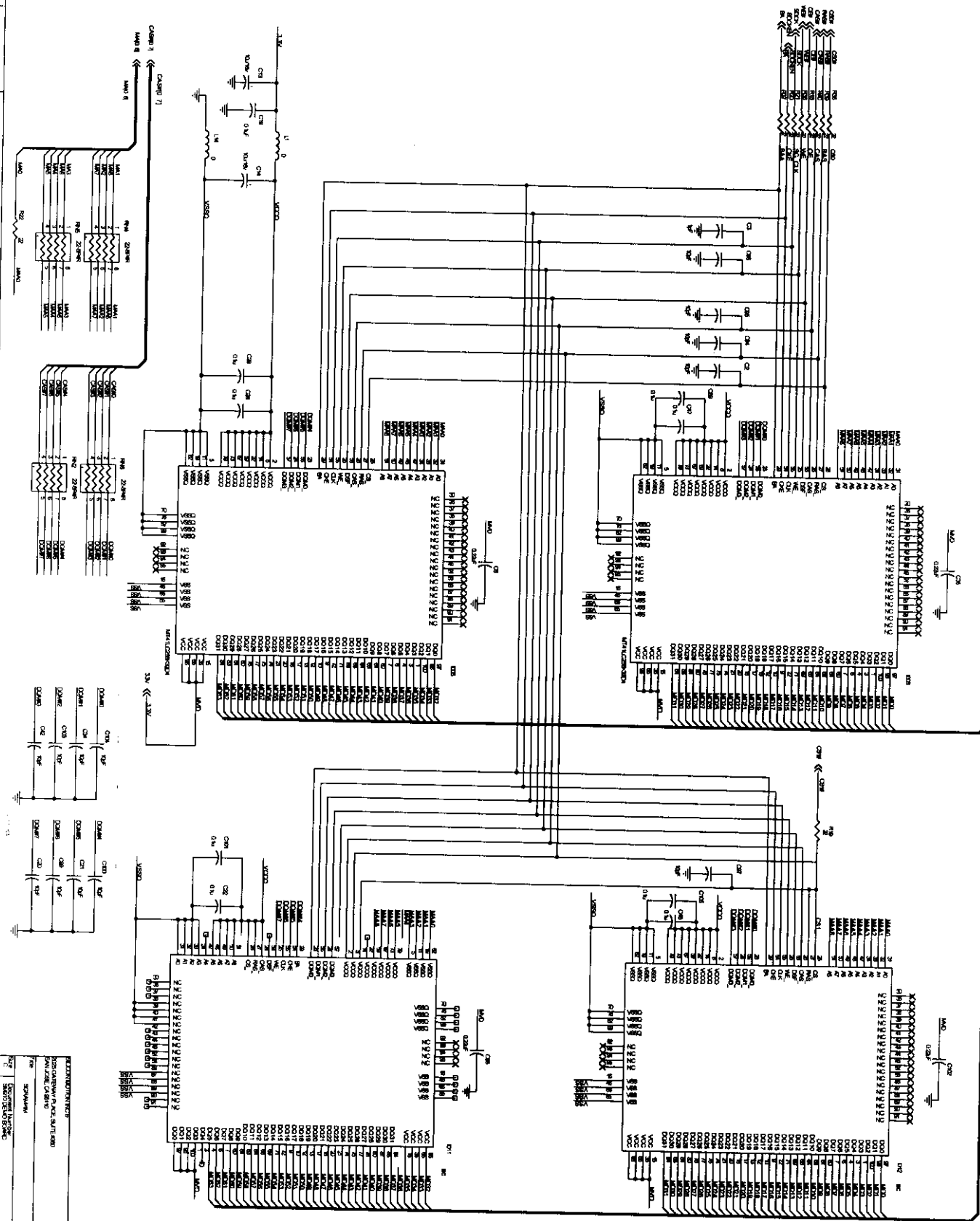


File	CONF & LCD PORT
Size	Document Number
B	CAUTION
Date	January, September 15, 1998
Sheet	1 of 7
Rev	A

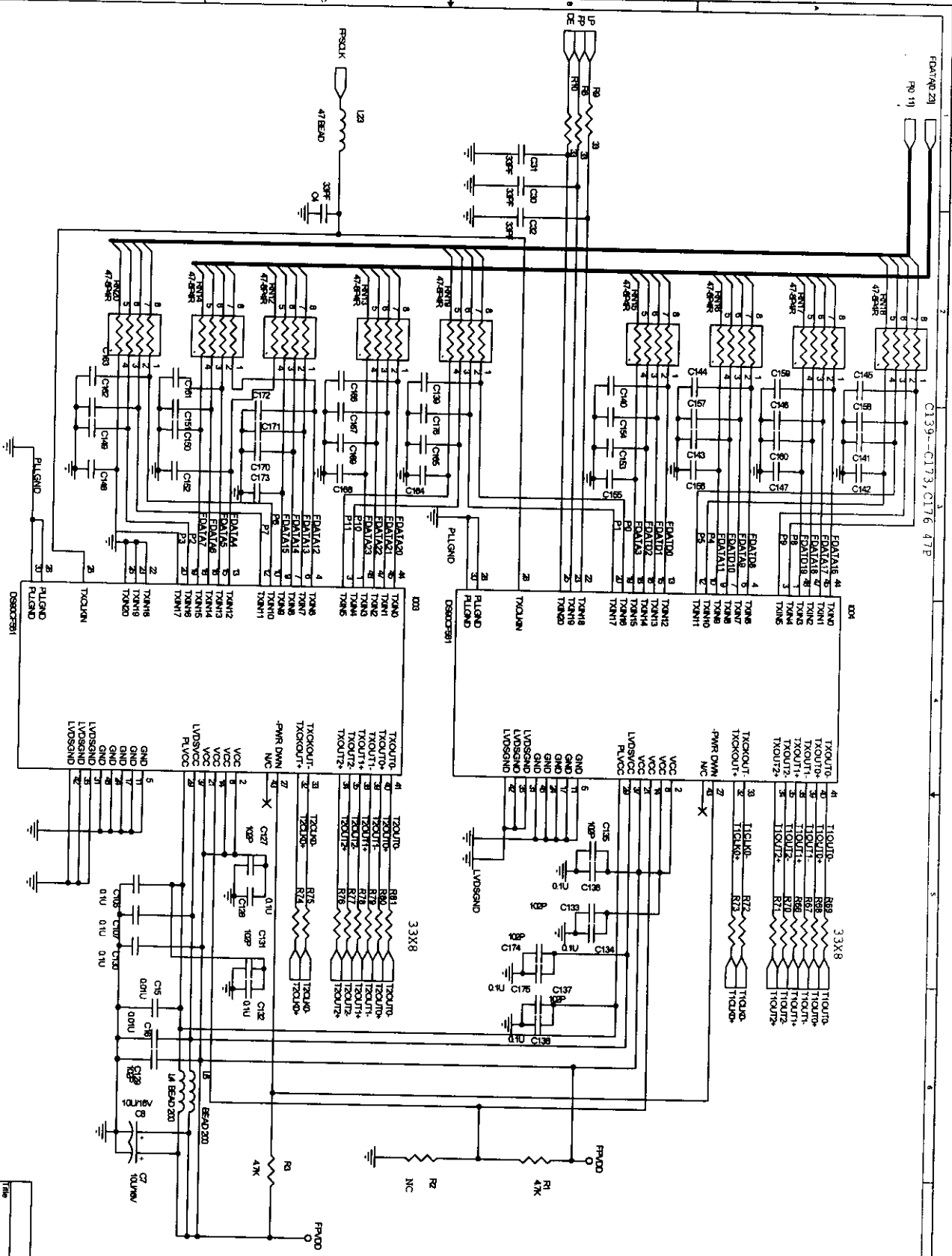
个面大

THE FIRST 2 MB

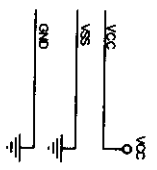
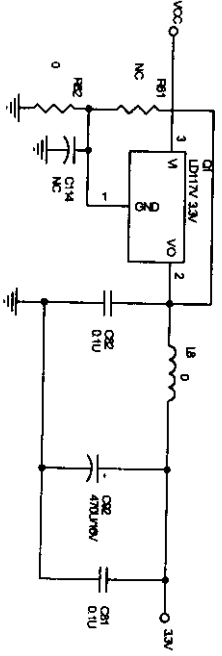
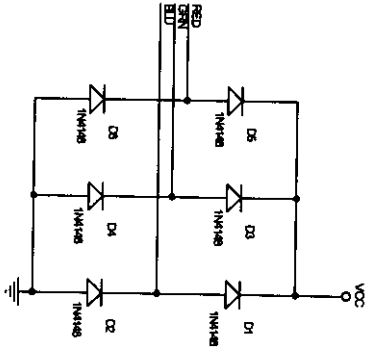
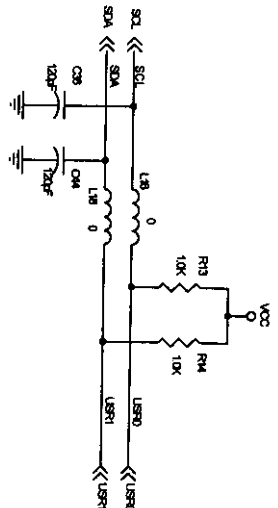
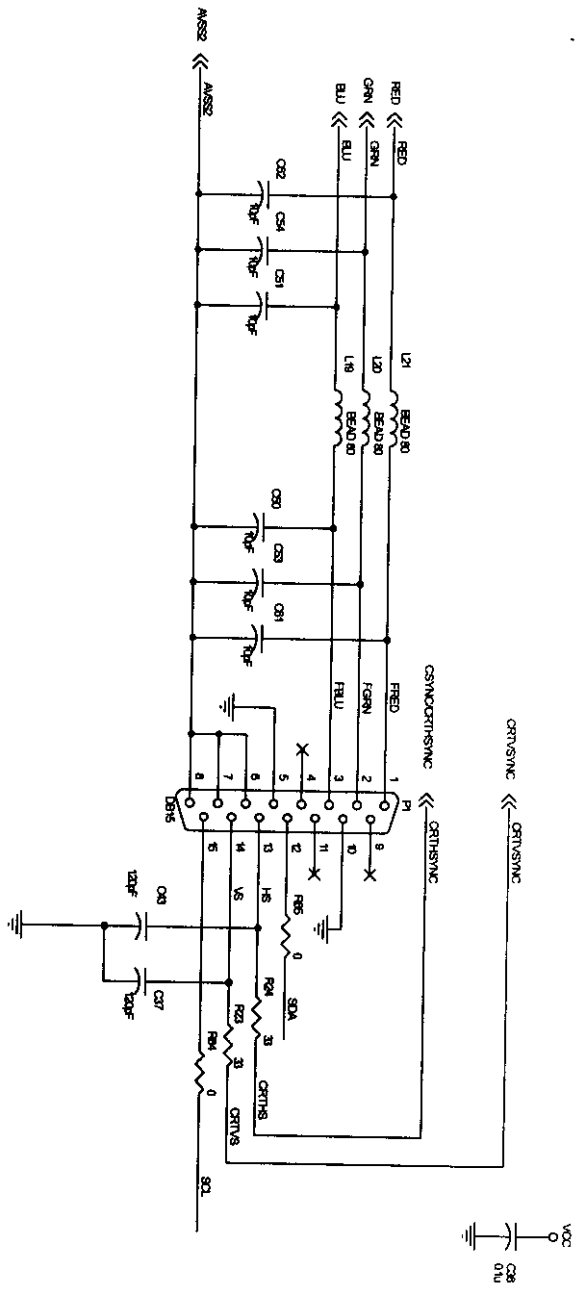
THE SECOND 2 MB



DATE	1980
DESIGNED BY	W. J. B. J.
CHECKED BY	W. J. B. J.
APPROVED BY	W. J. B. J.
REVISION	1
DESCRIPTION	2 MB DRAM ARRAY



File	LVDS18
Size	Document Number
B	03/15/2000
Date	Sheet 3 of 7



Saturday, September 18, 1998

File	CRT
Size	Document Number
B	Classification
Date	Friday, September 18, 1998
Sheet	4 of 7

