UH046Z(PCD2000A) Circuit Description

The transceiver unit employed the architecture where the receive synthesizer makes the channel selection and a second synthesizer generates a fixed transmit offset. This architecture is implemented using the "Receiver and Transmitter Interface" IC (IC20l) and the "Radio Interface and Twin Synthesizer" IC (IC202). IC201 is a VHF oscillator,up-converter and prescaler. IC202 is a combined radio interface circuit and twin synthesizer. Its radio interface section contains circuits to monitor and control levels such as transmit power, circuits to demodulate the frequency modulated signal to audio, and a frequency multiplier. The synthesizer section has the Main synthesizer used to select serve channel by generating the 1st local oscillator (LO) frequency. The fixed Auxiliary synthesizer is used for the transmit-receive offset and for modulation. IC202 also generates 8 . 064 MHz system clock for the "System Controller and DATA MODEM" IC (IC401).

1 RF

l.1 RF Receiver Section

RF inband signal enters the duplexer (FL101) of the transceiver through the external antenna system. This duplexer has a cutoff frequency of 869 - 894 MHz Where emissions outside of this band are well reduced to prevent interference caused by unwanted signals.

The received inband signal is then amplified by approximately 15dB by the low noise amplifier (LNA) Q101 to improve its Noise Figure. This LNA also works as buffer circuit to prevent antenna conducted emissions in the antenna circuit.

Then this amplified inband signal goes to the SAW bandpass filter which has cutoff frequency of 869 - 894 MHz. This filter futher rejects out of band interferences and reduces antenna conducted emissions.

After filtering, the signal is mixed with the 1st LO frequency by IC101 to provide the first IF at 45 MHz. At this stage, impedance matching for these signal sources are well achieved to isolate the signals from each other to prevent antenna conducted emissions from going toward the antenna.

The 1st LO is generated by the PLL synthesizer circuit which includes the combination of lC201, IC202 and VCO MO101. The frequency range for the VCO is from 914.04 to 938.97 MHz. The reference for the PLL circuit is generated from the 14.85 MHz VC-TCXO (MO202). This 14.85 MHz VC-TCXO is a5 PPM crystal oscillator but it is stablized well within2.5 PPM, in the temperature range of -30 deg C to +70 deg C, by the automatic frequency control (AFC) algorithm employed in the transceiver.

The 45 MHz 1st IF signal is filtered by the crystal filter FL103 which has bandwidth of 34 kHz. After the matching circuit, the 1st IF signal goes to the 2nd Mixer of IC102 which consists of an oscillator, a Mixer, a RSSI detector and an IF amplifier (2nd IF amplifier). Here it is mixed with the 44.55MHz second LO to generate 450KHz second (final) IF. This 2nd IF signal is filtered by FL104 which has bandwidth of 30KH~. After being amplified by the 2nd IF amplifier of IC102, the signal enters IC202 for demodulation.

The 44.55 MHz is generated by multiplying the crystal frequency 14.85 MHz by 3 by the multiplier of IC202.
Once the final IF enters the Radio Interface and Twin Synthesizer IC (IC202), it is amplified, Limited and then processed in two separate paths. One path samples the signal at 504 KHz. This

sampling gives a mixed-down output AFCOUT at 54 KHz when the input is at exactly 450 KHz and otherwise tracks the offset to allow estimation of the local oscillator error and the crystal error so that an AFC loop is used to adjust the crystal to exactly the correct frequency. Further details of the AFC loop is described in AFC section. The AFCOUT is also used by the MODEM in the System Controller and DATA MODEM IC (IC401) to receive signaling data.

The other path is the audio discriminator which is a purely digital implementation of the delay-and-multiply technique. The extracted audio signal then drives the speech and SAT path in Audio Processor IC (IC301).

l.2 RF Transmitter Section

A fixed frequency of 90 MHz offset is generated by the Auxiliary synthesizer in the Radio Interface and Twin Synthesizer IC (IC202). This 90 MHz Offset frequency is then mixed with the 1st LO frequency by the mixer of the Receiver and Transmiter Interface IC (IC201) to generate the transmit carrier frequency.

Modulating signal from Audio Processor (IC301) is added to the Auxiliary loop by bulling VCO tank circuit to provide modulation.

Modulated carrier signal is then amplified and buffered by driver amplifier (Q201) to prevent any affects caused by any incidental load change at TX power OK (IC204).

The amplified TX signal then goes to TX SAW filter (FL201) where the frequency cmponents other than 824-849 MHz are reduced to prevent the spurious emissions from the TX carrier.

As a final amplifier stage, the TX power OK(IC204) is used to amplify the +7dBm input signal to the required transmission power level. The amplified signal then enters the duplexer (FL101) where final filtering is provided to prevent harmonics and spurious emission of the transmitter.

The directional coupler (Y201) picks up the - 14 dBm down level of TX power and then it is detected by D201. The detected power level is compared with the logic system's voltage in order to obtained the required TX output power level. During production, comparator setting voltages are calibrated and stored in EEPROM for channel v.s. TX power. This corresponding voltage is then used to set the required output TX power.

On the other hand, TX +B switching transistor (Q202) is used to stop the regulated DC power to the TX circuit to prevent spurious emissions when the unit is not in TX mode.

Thus, the stabilized TX power is obtained with these circuitries.

1.3 Protection Against False Transmission, Autonomous Timeout

The transmitter has a protection circuit that is processor independent to turn the TX Power Amplifier off in case of component failure.

Within the System Controller and DATA MODEM IC (IC401), there is a Autonomous Timeout (ATO) supervising block. This block monitors the status of the signals RXCD (Received Carrier Detect) and TXPOW (Transmit Power). If there is no signal in from antenna (RXCD is low) and the transmitter is on (TXPOW is high) and this is true for more than 30 seconds, the ATO originates a hardware turn off. When this happens the signal XPlNH from IC401 goes low and turn switch Q202 off, which in turn cuts off the DC power to the Power Amplifier (IC204) and its driver transistor (Q201) along with the associated power control circuits. This function is and must be processor independent.

One second before the ATO initiates a hardware turn off, it generates an interrupt to the microprocessor. This gives the processor enough time to clean up before it is turned off.

The RXCD signal is generated from the Radio Interface and Twin Synthesizer IC (IC202). The detected RSSI signal from IC102 is input to the A-D converter of IC202, and it is compared with a factory calibrated threshold by the comparator within IC202. This comparator sets the RXCD output signal to "HIGH” when the detected RSSI level is above the threshold, and to "LOW” when the RSSI signal falls below the threshold .

The TXPOW signal is generated from the power detector circuit. Detected power level is compared against a hardware setting threshold (-60 dBm). When the detected power level is above this threshold, the comparator generate a CMOS logic "HIGH” to indicate transmit power is on. When the detected power level is below this threshold, the comparator generate a CMOS logic "LOW” to indicate transmit power is off

l.4 Automatic Frequency Control (AFC)

The AFC is a combination of hardware and software functions to control the 5 PPM VC-TCXO frequency to well within the 2.5 PPM requirement over the operating temperature -30 deg C to +70 deg C.

1.4.1 Theory of operation

In order to fine trim the crystal oscillator frequency to the correct value, the accurately held frequency of the base station is locked on and tracked by the transceiver. To implement this, the final intermediate frequency signal (normally at 450 KHz) is converted to a logic signal and then mixed down by the Radio Interface and Twin Synthesizer IC (IC202) to a low frequency output for counting in the microcontroller (IC401). The operation of this system can be explained with the used of the simplified block diagram of the receiver architecture as in figure 1.

The receiver runs the first mixer with a high-side local oscillator controlled by the Main synthesizer, so a positive crystal frequency error will give an increased first IF. This is then mixed down further by a low-side second oscillator, LO2 in the IC202, derived by multiplying the same crystal as used for the Main synthesizer. A positive frequency error would now give a reduced second IF if the error in the first I.F. is ignored, but the overall effect is an increase by an amount slightly smaller than the increase in the first IF.

The second IF signal AFClN at around 450 KHz drives the FM discriminator to recover the modulation and also feeds a third mixer where high-side injection is used to give a very low output frequency, around 54 KHz, and is output on AFCOUT for counting. This third mixer is driven by a clock derived from the crystal but at a much reduced frequency so the effect of the high-side mixing dominates to give an output which drops in frequency when the crystal has a positive error.

As a result of the chain of mixing stages the error in the first local oscillator due to the crystal frequency will give a similar frequency shift at the output of the third mixer which is then a large percentage change of AFCOUT so it is possible to measure AFCOUT against the crystal to determine the trim needed.

1.4.2 Implementation

The System Controller and DATA MODEM IC (IC401) has a hardware counter to count a predetermined number of periods of AFCOUT signal which has frequency of 54 kHz when the crystal is exactly on frequency. The number of periods counted can be selected to 256 or 2432, giving measuring times of about 5ms or 45ms respectively for 54 KHz Signal.

Another timer runs at 2.008 MHz is used to determine the time lapse between counts. The hardware on IC401 is set up such that when the hardware counter is enable, the next rising edge of AFCOUT will start the counter and the timer at the same time. When the requested number of periods (256 or 2432) has been counted, the next falling edge of AFCOUT will latch the value of the timer to an input capture register for calculation. When the frequency is exactly on (AFCOUT is 54 KHz), the capture register should read 9519 or 90434 for period counts of 256 and 2432 respespectively.

The VCTCXO is a 5PPM crystal over the operating temperature, this together with 2.5 PPM of frequency variation from the base station (worst case, most of the base stations have frequency stability well within1.5 PPM) give the maximum frequency variation of AFCOUT is 54 KHz6.7KHz. This number assumes the highest operating frequency of channel 799 (1st LO is 938.97 MHz), which is the worst case scenario .

During production, the crystal frequency is adjusted for exact frequency at room temperature. This data controls the crystal adjust DAC in IC202 and is stored in EEPROM. Up on power up, after the DAC is initiallied with the calibrated data, the cellular phone is scanning for Forward Control Channel. At this time an acquisition AFC algorithm is employed to quickly acquire the control channel. Calculations and experiments showed that with the worst case frequency offset of6.7 KHz, the crystal frequency can be brought to within 0.5 PPM in less than 1.5 seconds. After this, the slow tracking mode of AFC loop is employed to track base station frequency to within 0.1 PPM. Loop damping and slew rate limiting are used in the AFC loop to avoid overshoot or hunting.

2 Audio

Audio Processor (IC301) provides all the audio signal processing and Data/SAT tone filtering functions.

2.1.1 RX audio

The detected signal (Audio out) from Radio Interface and Twin Synthesizer (IC202) is fed to the Audio Processor (IC301) through the de-emphasis circuit.

Once entering IC301, an adjustable gain block provides gain adjustment to take up signal level tolerances in the receiver output. After that the signal is bandpass filtered to the speech bandwidth of 300 to 3400 Hz and then expanded by a 1:2 dB expander to restore the original signal.

2.1.2 TX Audio

Audio signal from the microphone is fed into Audio Processor (IC301). At first the signal goes through the soft limiter which atcs as an AGC to restrict signal level without clipping to the correct level for FM deviation. The soft limiter is controlled by the signal amplitude at the compressor input and the hard limiter output later in the signal processing path.

Microphone level tolerance is trimmed by the variable gain block INPSENSE following the soft limiter. After the signal is band limitted to speech bandwidth of 300 Hz - 3 .4 KHz, it is then fed into a 2:1 dB compressor to halve the transmit dynamic range as required. A pre-emphasis filter follows the compressor to boost the amplitude of higher audio frequency, then a hard limitter is followed to control the maximum deviation to ensure compliance.

The signal then goes to the splatter filter to confine the emission within the specified bandwidth. A final variable gain block is provided to adjust the output level to give the required FM deviation for speech.

Finally the audio signal is combined with TX data and TX SAT by the SUM amplifier within IC301 and forwarded to the modulation tank circuit of the Auxiliary synthesizer to modulate the TX carrier.

2.1.3 TX DTMF

TX DTMF is generated by the DTMF generator in IC301. When DTMF is generated, it is inputted to the variable gain block INPSENSE and followed the same path as TX audio.

2.1.4 RX DTMF Detector

There is a DTMF detector (IC407) to detect all 16 digits sent from the forward channel. Demodulated audio signal after being filtered by the audio bandpass filter of Audio Processor IC (IC301), is also routed to IC407 for DTMF detection. Detected DTMF digits are sent to the System Controller and DATA MODEM IC (IC401) for processing.

3 DATA, Signaling Tone and SAT

3.1.1 RX DATA

The received control data after being mixed down to 54 KHz (AFCOUT) in the Radio Interface and Twin Synthesizer (IC202) is fed to the System Controller and DATA MODEM IC (IC401). Here data is demodulated by the digital discriminator, following by a digital transition data tracking loop decoder and word synch detector.

3.1.2 TX DATA

Transmit data is generated by the System Controller and DATA MODEM IC (IC401), where dotting and word synch pattern as well as BCH encoding is implemented. The formatted data then sent to the audio processing (IC301) where data is filtered and then level adjusted for correct deviation. This filter is a 4th order Butterworth lowpass filter with nominal -3 dB point of 20 KHz. The level adjustment is provided by the variable gain block DATADEV.

10 KHz Signaling Tone (ST) is also generated by IC401. It follows the same path as Data through the Audio Processor (IC301).

Data and ST are combined with audio and SAT by the SUM amplifier inside IC301 and then sent to the modulator.

3.13 RX SAT

The detected signal (Audio out)from Radio Interface and Twin Synthesizer (IC202) is fed to the Audio Processor (IC301) through RSI input. Here the received SAT signal is passed through 6 KHz bandpass filter, the recovered SAT signal then passes through a 10 dB amplifier and then a Schmitt trigger to drive pin RSO with a logic version of the receive SAT. This logic signal SAT is input to the System Controller and DATA MODEM (IC401) for SAT detection.

3.1.4 TX SAT

The System Controller and DATA MODEM IC (IC401) provides an option for TX SAT to be locally generated by the SAT generator, or RX SAT to be transponded. This feature is under software control. In this transceiver, transponded SAT is always selected. The selected SAT is then sent to Audio Processing IC (IC301) for filtering and level adjustment before it is summed with audio and sent to the modulator.

4 System Controller

4.1 CPU

The major portion of CPU function consists of the System Controller and DATA MODEM (IC401), ROM (IC402) to store operational software, and EEPROM (IC403) to store basic operation parameter for cellular telephone and factory calibrated data. The core of lC401 is the popular 8-bit microprocessor 6303 family. Its system clock is the 8.064 MHz generated by the Radio Interface and Twin Synthesizer IC (IC202). Internally the CPU runs at 2.008 MHz When in turbo mode and 1.004 MHz when in power saving mode.

4.2 Keypad and LCD display

The process of the Key input and the LCD display are done by the System Controller and DATA MODEM IC (IC401).

When a key is depressed, IC401 detects its key assignment and appropriated actions are taken to control LCD display as well as LCD back light and keypad LEDs lighting.

4.3 Key Tone and Alert Tone

Key tone and Alert tone are generated by the BAR (Beep/Alarm/Ring) generator on the system Controller and DATA MODEM IC (IC401). These tones appear at the Ringer (SP401). Frequency and volume of these tones are controlled by changing the ON and OFF time of the BAR generator which changes the period and duty cycle of the output signal. All of these are under software control.

5 Voltage regulators

Two voltage regulators, IC404 and IC406 are used to provide power for digital and audio circuitry and RF circuitry respectively. Normally all of these voltage regulators are turned off. When the power ON/OFF key is depressed for more than 2 seconds, these voltage regulators are turned on by the battery power connected through power ON/OFF key. After the micro-controller is up, it would in turn keep the voltage regulators on after the power ON/OFF key is released .
During unfinished talk (in used icon is on), the unit shall not be turned off even if the power ON/OFF key is depressed.

TX Frequency Stability Measurement Procedure

1 Introduction

The transceiver used a 1 4.85 MHz VCTCXO as reference to generate all synthesizer frequencies and clocks for its operation. This VCTCXO has a 5 PPM stability over the operating temperature (-30 deg C to 60 deg C). In order to achieve the required 2.5 PPM frequency stability, the transceiver employed an Automatic Frequency Control algorithm described in details in the circuit description document. This algorithm tracks the well stabilized frequency of the base station whenever the transceiver is in operation to achieve frequency stability. Therefore it is a must to have the transceiver locked to a stable source while testing its frequency stability.

2 Recommended test setup and procedure

The recommended test setup is to use the HP 8920 as a source to generate Forward Control FSK data and also to monitor the handset's frequency stability. Figure below shows the set up.

The followings are itemized steps taken for measurement:

2.1 Set the HP 8920 to transmit FSK data by using the decoder menu on HP 8920 and select AMPS/TACS mode. Then select to send control data.

2.2 Assign frequency for channel 333 (as an example), 879.99 MHz for forward frequency (HP 8920 generated), 834.99 MHz for reverse channel (handset generated).

2.3 Place the handset inside the climate chamber. Connect the external connector to the handset and turn on power supply. Connect RF cable from HP 8920 output to the handset. Turn on the handset by depress power On/Off key for more than 2 seconds.

2.4 Use test mode command to setup the handset (please consult appendix A and B of PCD2000A Operation document for more details) as follows:

_ Enter program mode by pressing and holding the [*] and [#] keys for 4 seconds. All the icons and the display will turn on and the phone will wait for the user to enter the password.

_ Enter 8 digits password: [3][2][2][l][8][5][9][1].

_ After the "PROGRAM MODE" is displayed, press either [up] or [down] arrow keys to select "TEST MODE". Press the [SEND] key to select.

_ If done properly "OPCODE:" will now appears.

_ Enter 83 to select channel, then press [SEND] .

_ When "DATA:" appears, enter 333 for channel 333 in Decimal, then press [SEND] .

_ The display should show "SUCCESS" indicating the function is executed.

_ Enter 81 to turn on the TX carrier.

_ Enter 84 to adjust output power if necessary. Data entry for this is 0-7, for output power level

0 to 7 respectively.

The handset now should be locking to the forward control channel and it is ready for testing frequency stability.