

Legend GM2115 LCD CONTROLLER BOARD SCHEMATICS

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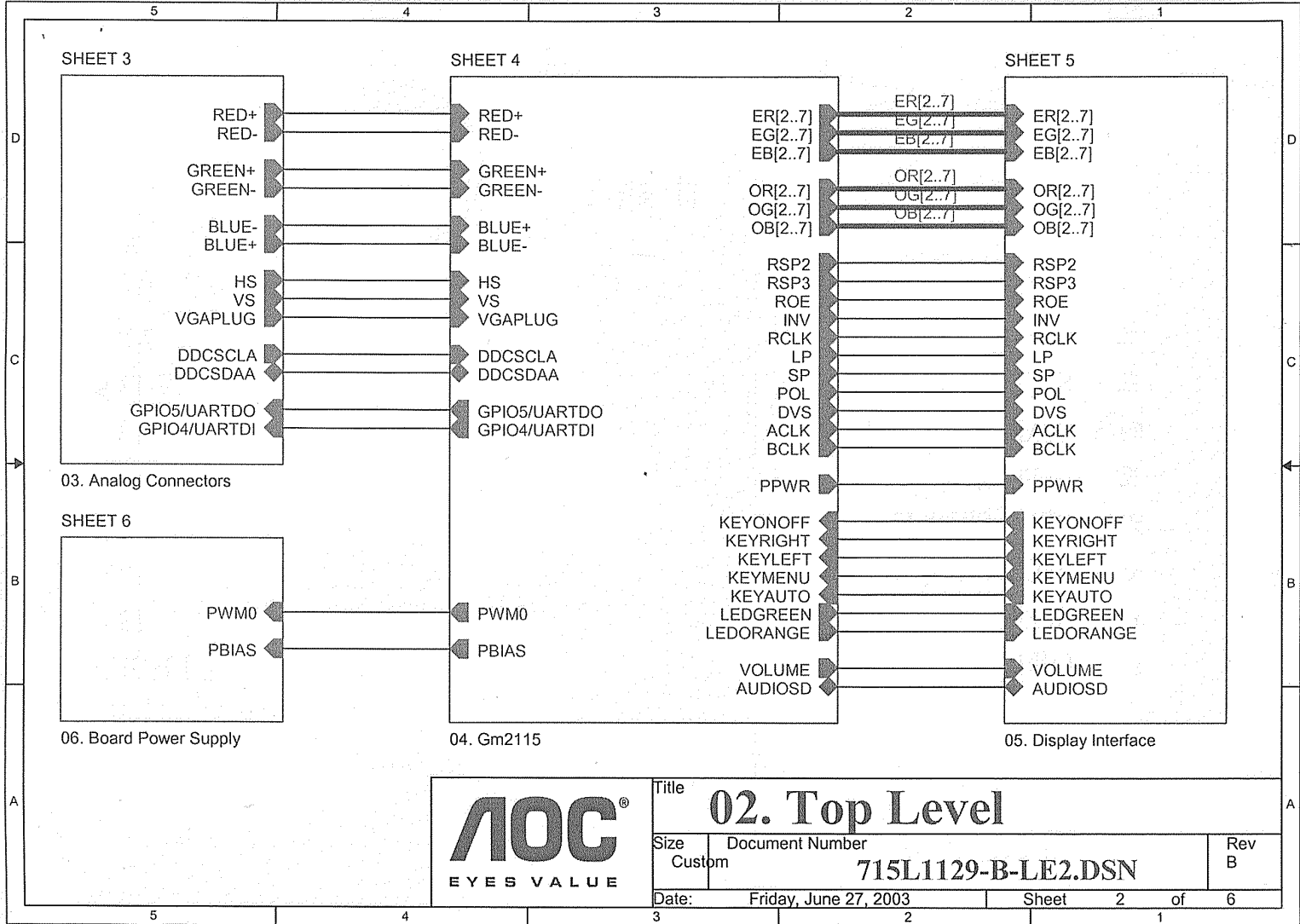
REVISION HISTORY

Date	Author	Ver	Comments
5/13/03	Rick	A	A. LED控制訊號反向 B. 7414 Power & Ground 未連線
5/19/03	Rick	B	

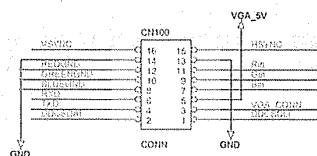
Approval	Organization	Signature	Date



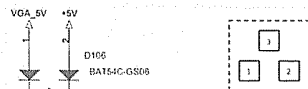
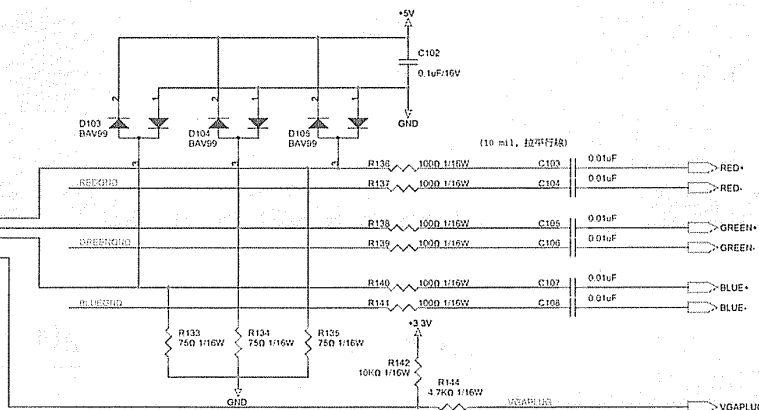
Title		01. Contents	
Size	Document Number	Rev	
A	715L1129-B-LE2.DSN	B	
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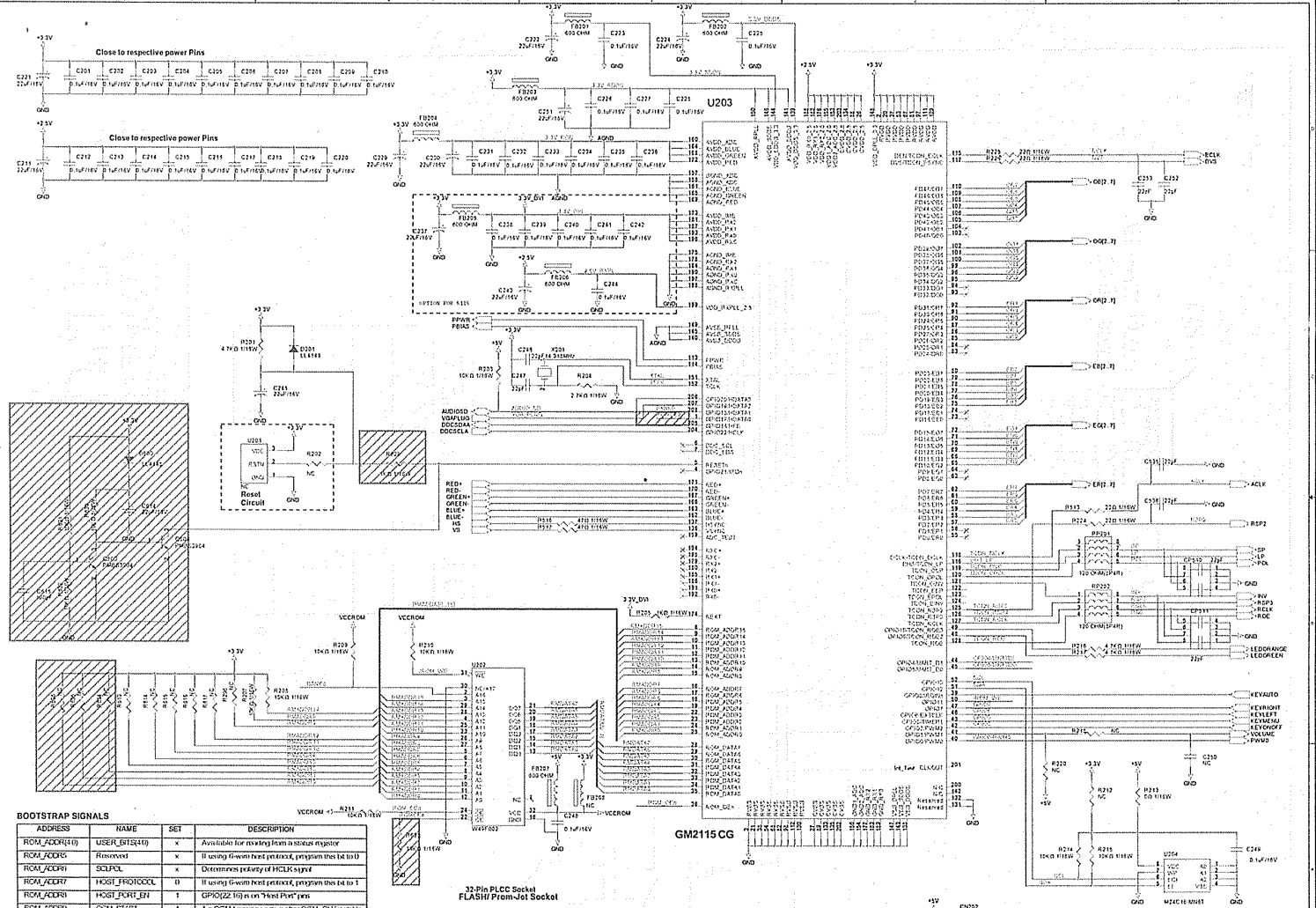


GPIO5:UARTD0 R104 470 1/16W 120
GPIO4:UARTD1 R103 470 1/16W R202

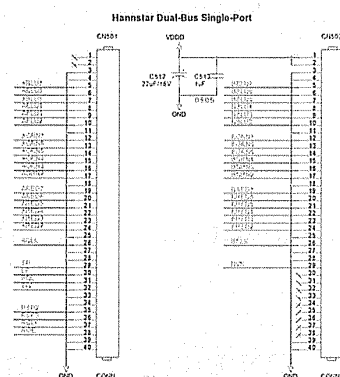
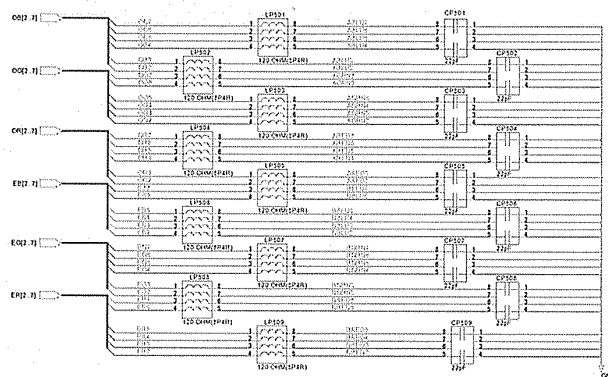
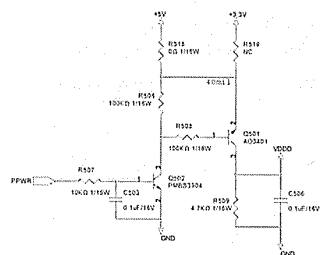
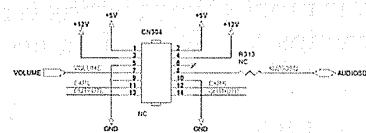


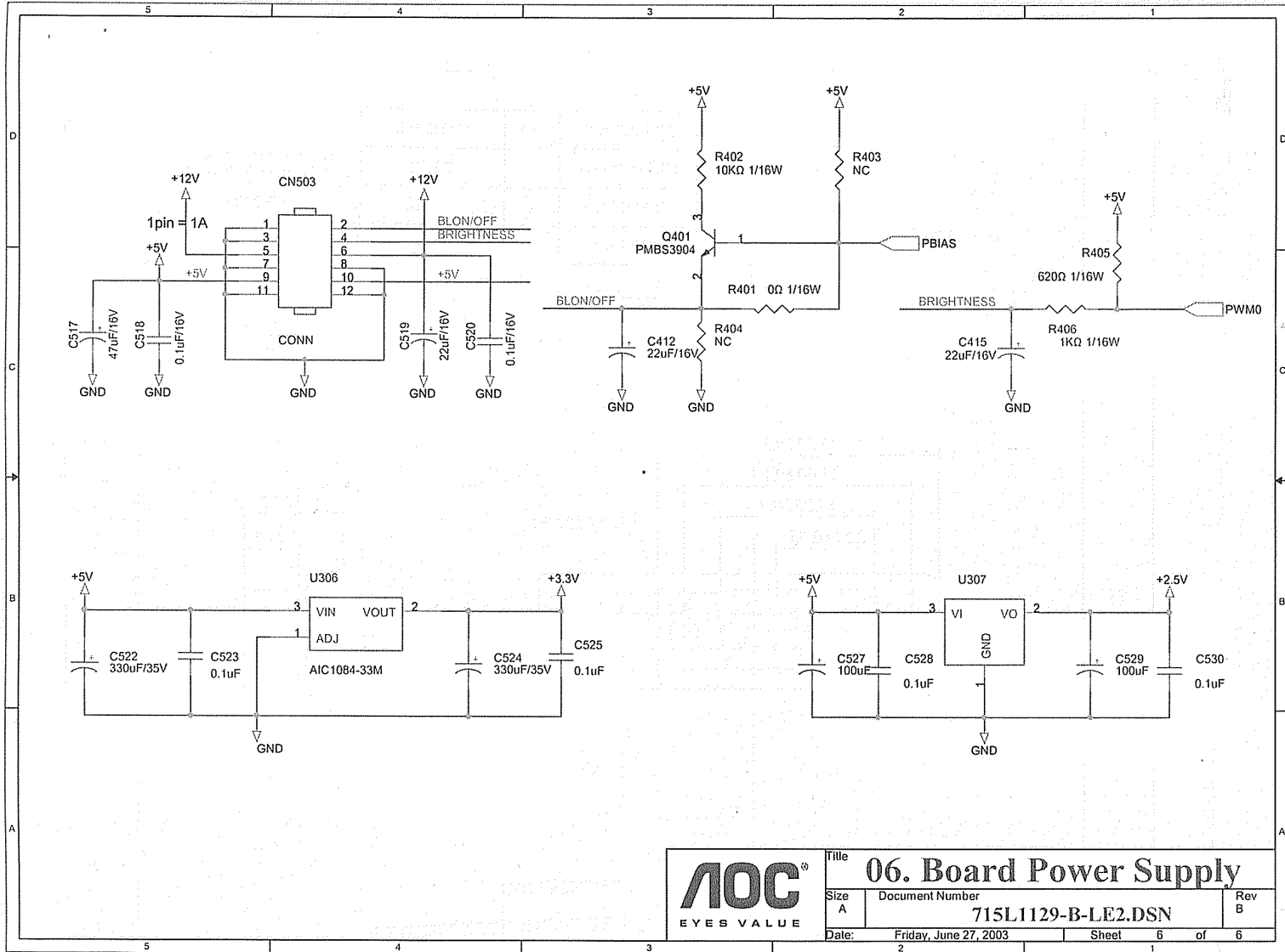
Pins 8/10/12 are R/G/B return lines resp.
75-ohm terminating resistor very close to the VGA conn.





ADDRESS	NAME	SET	DESCRIPTION
ROM_ADDR(4)	USER_RST(4)	x	Available for moving from a status register
ROM_ADDR5	Reserved	x	If using 6-word host protocol, program lines 14 to 19
ROM_ADDR6	SOLPOL	x	Determines polarity of HCLK signal
ROM_ADDR7	H0ST_PORT00L	0	If using 6-word host protocol, program lines 14 to 19
ROM_ADDR8	H0ST_PORT01	1	GPIO(22 to 23) as "Host Port" pins
ROM_ADDR9	OCM_START	1	1 = OCM becomes active after OCM_CLK is stable
ROM_ADDR(12 to 19)	USER_RST(5)	x	Available for moving from a status register
ROM_ADDR(1)	OSC_SEL	0	0 = XTAL and TCLK pins are connected
ROM_ADDR11	OCM_ROM_C00(1)	1	1 = At 48K of ROM is in external ROM

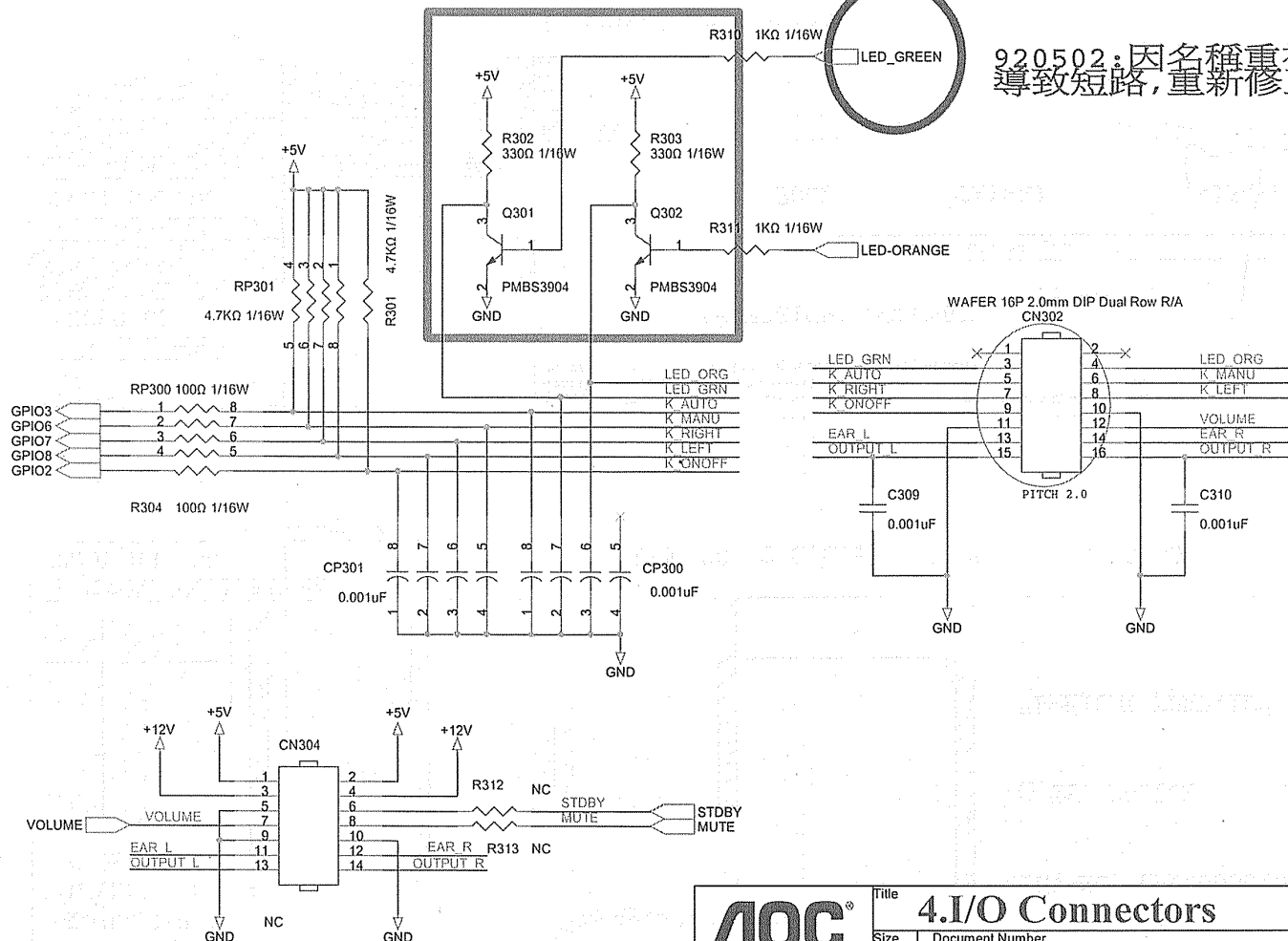
[illegible]



	Title				
	06. Board Power Supply				
	Size A	Document Number			Rev B
		715L1129-B-LE2.DSN			
	Date:	Friday, June 27, 2003	Sheet	6	of 6
		2		1	

920519: LED訊號腳反向

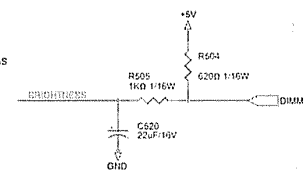
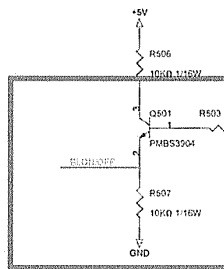
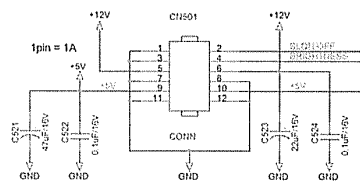
920502: 因名稱重複,
導致短路, 重新修正



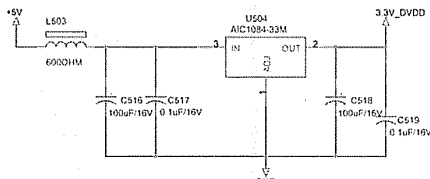
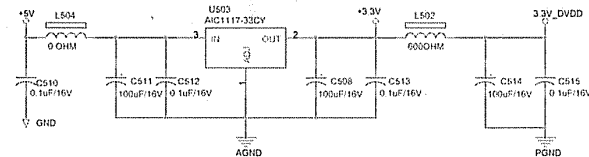
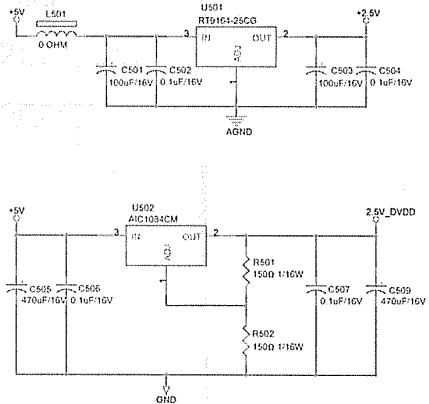
AOC
EYES VALUE

Title **4.I/O Connectors**

Size	Document Number	Rev
A	EAGLE17-715L1130-B-LEG.DSN	B
Date:	Monday, May 26, 2003	Sheet 5 of 6

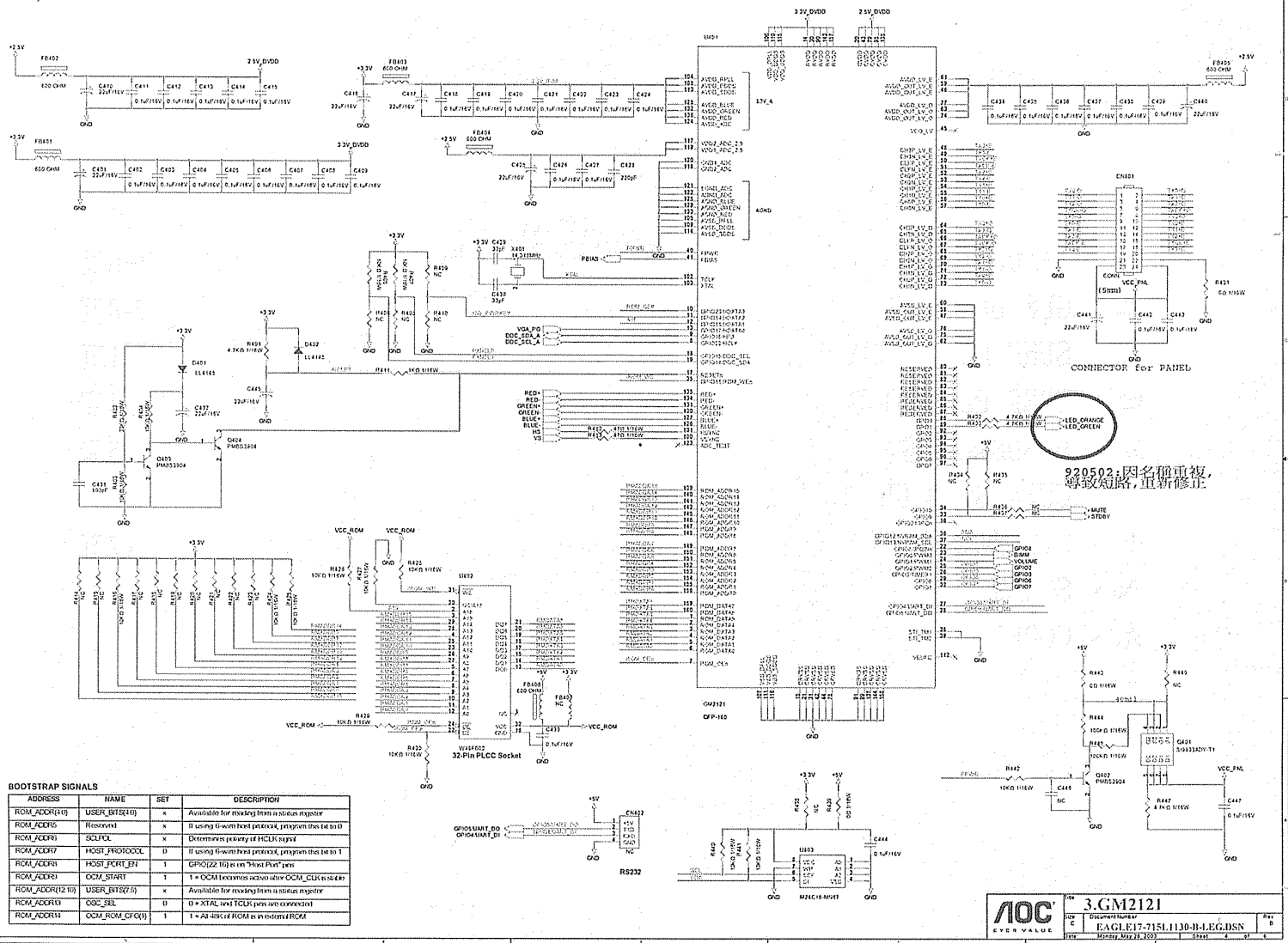


920519: Inverter 訊號腳反向



AOC EYES VALUE		5.Power	
Size	9	Document Number	EAGLE17-71SL1130-B-LEG.DSN
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Rev	B		

ADDRESS	NAME	SET	DESCRIPTION
ROM_ADDR(16)	USER_BITS(16)	x	Available for masking from a status register
ROM_ADDR5	Reserved	x	If using from host protocol, program the bit to 0
ROM_ADDR6	SCLPOL	x	Determines polarity of HCLK output
ROM_ADDR7	HOST_PROTOCOL	0	If using from host protocol, program the bit to 1
ROM_ADDR8	HOST_PORT_EN	1	GPIO(22:16) is on "Host Port" pins
ROM_ADDR9	OCM_START	1	1 = OCM becomes active after OCM_CLK is stable
ROM_ADDR(12:13)	USER_BITS(2)	x	Available for masking from a status register
ROM_ADDR10	OSC_SEL	0	0 = XTAL and TCLK pins are connected
ROM_ADDR14	OCM_ROM_CFG(1)	1	1 = All bits of ROM are in on-chip ROM



GPIO4_UART_DO R124 470 1/16W 100
GPIO4_UART_DI R103 470 1/16W 100

920507: 依聯想要求, 修正Connector

