CTN730/CTN732

NFC wireless charging transmitter controller

Rev. 3.0 — 11 January 2021 Product short data sheet
655130 COMPANY PUBLIC

1 General description

This 32-bit Arm Cortex-M0-based, all in one NFC wireless charging transmitter IC is designed to follow the NFC Forum Standard for Wireless Charging. This product is part of a solution offering from NXP for wireless charging and wireless power transfer for low-power application and small form factor devices.

NFC wireless charging solutions enable customers to remove plugs and cords from their product. This facilitates new design flexibility, can make products smaller and more compact in combination with completely new design options. The removal of plugs and pins is an important step to make a product waterproof and seal it hermetically, which in turn offers an unmatched level of quality and robustness.

In many customer applications, it is the combination of wireless charging with a fast, bidirectional data channel that makes the solution exciting.

In the figure below a typical NFC charging system is illustrated including CRN120 as communication and PCA9430 or PCA9431 as power receiver. A detailed system view can be found in the AN12639. AN12641 provides all needed system information from RF point of view.

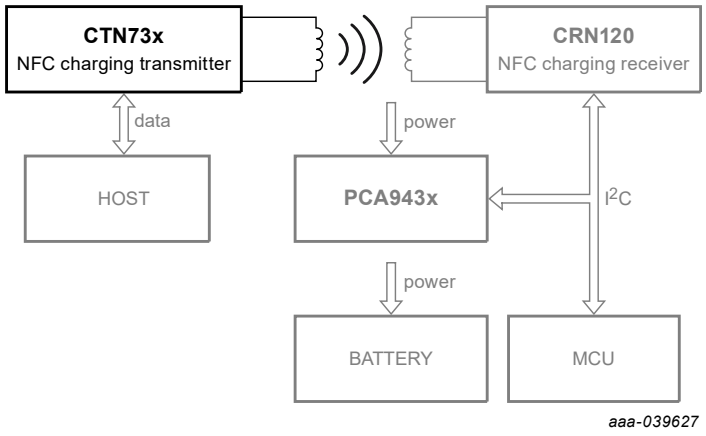

Figure 1. NFC wireless charging system

2 Features and benefits

2.1 Integrated NFC charging frontend

- 1.25 W output power frontend
- Supports reading and writing of NFC Forum tag types 2, 3, 4A, 4B and 5
- CTN730 Supports type 4A card emulation mode up to and including 848 kbit/s
- Low-power NFC charging RX device detection

Table 1. NFC transfer speed in [kbit/s]

NFC charging controller	Type 2 Tag	Type 3 Tag	Type 4A Tag	Type 4B Tag	Type 5 Tag
CTN730	106	212	up to 848	106	26
CTN732	106	212	106	106	26

2.2 Cortex-M0 microcontroller

- Processor core
  - Arm Cortex: 32-bit M0 processor
  - Built-in Nested Vectored Interrupt Controller (NVIC)
  - Non-maskable interrupt
  - 24-bit system tick timer
  - Running frequency of up to 20 MHz
  - Clock management to enable low power consumption
- Memory
  - Flash: 160 kB
  - SRAM: 12 kB
  - EEPROM: 4 kB
  - 40 kB boot ROM included, including USB mass storage primary boot loader for code download
- Debug option
  - Serial Wire Debug (SWD) interface
- Peripherals
  - Host interface:
    - USB 2.0 full speed with USB 3.0 hub connection capability
    - HSUART for serial communication, supporting standards speeds from 9600 bauds to 115200 bauds, and faster speed up to 1.288 Mbit/s
    - SPI with half-duplex and full duplex capability with speeds up to 7 Mbit/s
    - I^2C supporting standard mode, fast mode, and high-speed mode with multiple address supports
  - Master interface:
    - SPI with half-duplex capability from 1 Mbit/s to 6.78 Mbit/s
    - I^2C supporting standard mode, fast mode, fast mode plus, and clock stretching
- Up to 21 General-Purpose I/O (GPIO) with configurable pull-up/pull-down resistors
- GPIO1 to GPIO12 can be used as edge and level sensitive interrupt sources

- Power
  - Two reduced power modes: standby mode and hard power-down mode
  - Supports suspend mode for USB host interface
  - Processor wake-up from hard power-down mode, standby mode, suspend mode via host interface, GPIOs, NFC field detection
  - Integrated PMU to adjust internal regulators automatically, to minimize the power consumption during all possible power modes
  - Power-on reset
  - NFC supply: external, or using an integrated LDO (TX LDO, configurable with 3 V, 3.3 V, 3.6 V, 4.5 V, and 4.75 V)
  - Pad voltage supply: external 3.3 V or 1.8 V, or using an integrated LDO (3.3 V supply)
- Timers
  - Four general-purpose timers
  - Programmable Watchdog Timer (WDT)
- CRC coprocessor
- Random number generator
- Clocks
  - Crystal oscillator at 27.12 MHz
  - Dedicated PLL at 48 MHz for the USB
  - Integrated HFO 20 MHz and LFO 365 kHz
- General
  - VFBGA64 package
  - HVQFN64 package (CTN730 only)
  - Temperature range: -40 °C to +85 °C

3 Applications

Designed to follow the NFC Forum Standard for wireless charging, this product is part of a solution offering from NXP for wireless charging and wireless power transfer for low-power application and small form factor devices.

The solution supports wireless charging and power transfer of

- small battery powered devices with small form factors with a power level <1 W
- hearable and audio devices (earbuds, hearing aids)
- computer accessories (stylus pen)
- wearable devices (wrist bands, fitness trackers, rings, smart watches)
- industrial devices (wireless connectors, sensors)
- medical devices (sensor, waterproof small devices)

4 Quick reference data

Table 2. Quick reference data

Operating range: -40 °C to +85 °C unless specified; NFC interface: internal LDO not used

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DDP(VBUS)}$	power supply voltage on pin VBUS	CTN730 card emulation mode	2.3	-	5.5	V
		reader/writer charging mode	2.7	-	5.5	V
$V_{DD(PVDD)}$	PVDD supply voltage	1.8 V	1.65	1.8	1.95	V
		3.3 V[1]	3	3.3	3.6	V
$I_{DDP(VBUS)}$	power supply current on pin VBUS	in hard power-down mode; T = 25 °C; $V_{DDP(VBUS)}$ = 5.5 V; RST_N = 0	-	12	18	µA
		stand by mode; T = 25 °C; $V_{DDP(VBUS)}$ = 3.3 V; external PVDD LDO used	-	18	-	µA
		stand by mode; T = 25 °C; $V_{DDP(VBUS)}$ = 5.5 V; internal PVDD LDO used	-	55	-	µA
		suspend mode, USB interface; $V_{DDP(VBUS)}$ = 5.5 V; external PVDD supply; T = 25 °C	-	120	250	µA
$I_{DD(TVDD)}$	TVDD supply current	on pin TVDD_IN; maximum supported operating current by the NFC interface	-	-	250	mA
P_{max}	maximum power dissipation		-	-	1050	mW
T_{amb}	ambient temperature	JEDEC PCB	-40	-	+85	°C

[1] If the USB interface is used, PVDD_IN voltage must be between 3.0 V and 3.6 V, according to the USB specification.

5 Ordering information

The table below lists the ordering information of CTN73x.

Table 3. Ordering information

Orderable part number	Package		
	Name	Description	Version
CTN730EV/C101Y	VFBGA64	plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm; 4000 pcs. on 13" reel	SOT1307-2
CTN730EV/C101E	VFBGA64	plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm; 490 pcs. on tray	SOT1307-2
CTN730HN/C101Y	HVQFN64	plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; 9 × 9 × 0.85 mm; 1000 pcs. on 13" reel	SOT804-4
CTN732EV/C101Y	VFBGA64	plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm; 4000 pcs. on 13" reel	SOT1307-2

6 Block diagram

6.1 Block diagram CTN73x

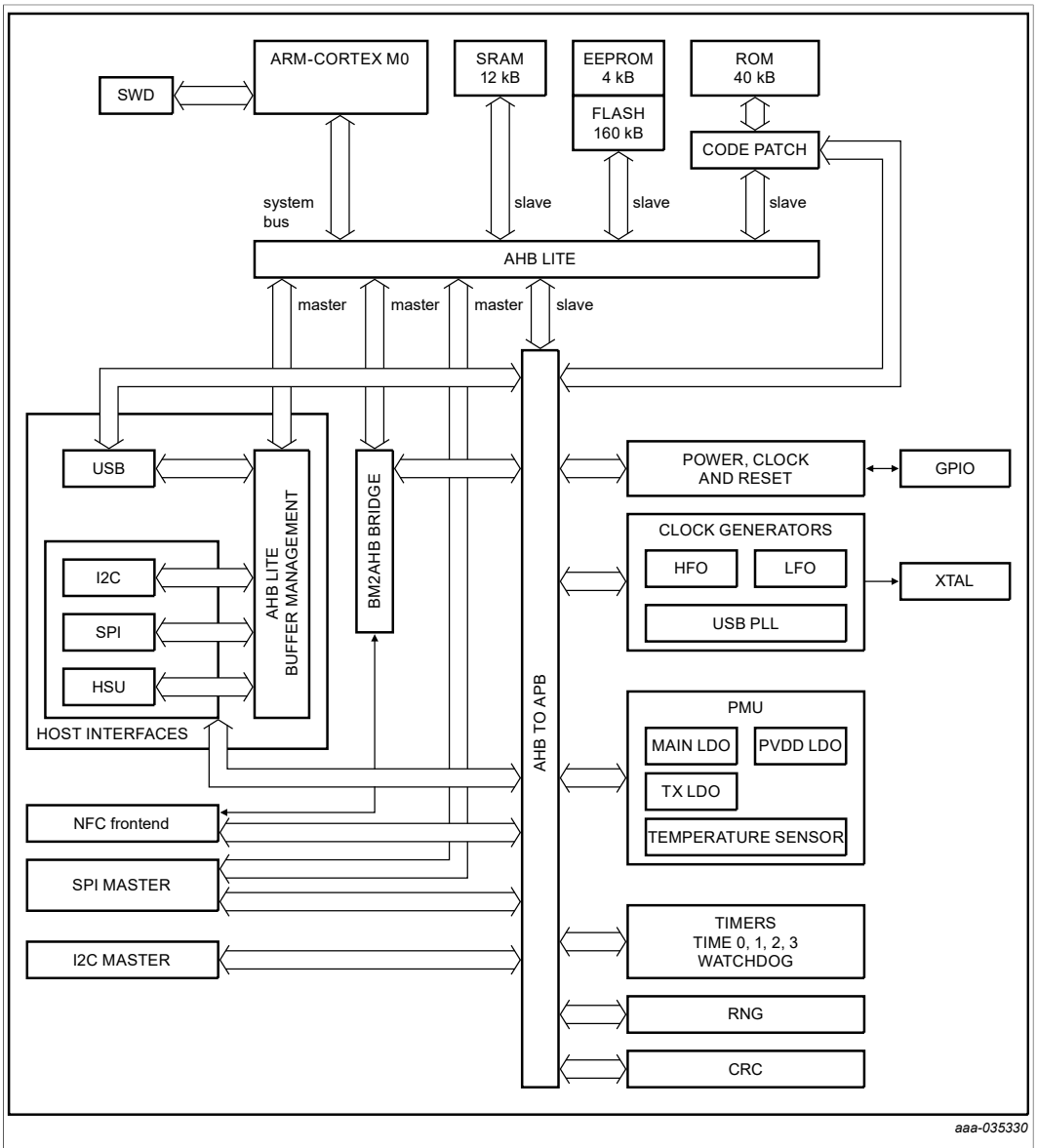

Figure 2. Block diagram

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	human body model (HBM)[1]				
		on all pins		-2	+2	kV
		charged device model (CDM)[2]				
		on all pins		-1	+1	kV
T_{stg}	storage temperature	non-operating		-55	+150	°C
$T_{j(max)}$	maximum junction temperature			-	+125	°C
P_{tot}	total power dissipation	reader mode; $V_{DDP(VBUS)}$ = 5.5 V		-	1050	mW

[1] According to ANSI/ESDA/JEDEC JS-001.
[2] According to ANSI/ESDA/JEDEC JS-002.

Table 5. Limiting values for GPIO1 to GPIO12

Symbol	Parameter	Conditions		Min	Max	Unit
V_i	input voltage			-0.3	4.2	V

Table 6. Limiting values for I^2C master pins (i2cm_sda, i2cm_scl)

Symbol	Parameter	Conditions		Min	Max	Unit
V_i	input voltage			-0.3	4.2	V

Table 7. Limiting values for SPI master pins (spim_nss, spim_miso, spim_mosi and spi_clk)

Symbol	Parameter	Conditions		Min	Max	Unit
V_i	input voltage			-0.3	4.2	V

Table 8. Limiting values for host interfaces atx_a, atx_b, atx_c, atx_d in all configurations (USB, HSUART, SPI and I^2C)

Symbol	Parameter	Conditions		Min	Max	Unit
V_i	input voltage			-0.3	4.2	V

Table 9. Limiting values for crystal oscillator

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{IH}	high-level input voltage	XTAL1, XTAL2		0	2.2	V

Table 10. Limiting values for power supply

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DDP(VBUS)}$	power supply voltage on pin VBUS		[1]	-0.3	7	V
$V_{DDP(VBUSP)}$	power supply voltage on pin VBUSP		[1]	-0.3	7	V
pin supply voltage for host interface and GPIOs (on pin PVDD_IN)						
$V_{DD(PVDD)}$	PVDD supply voltage	on pin PVDD_IN; power supply for host interfaces and GPIOs	[1]	-0.3	4.2	V
pin supply voltage for master interfaces (on pin PVDD_M_IN)						
$V_{DD(PVDD)}$	PVDD supply voltage	on pin PVDD_M_IN; power supply for master interfaces	[1]	-0.3	4.2	V
NFC interface LDO (pin VUP_TX)						
$V_{I(LDO)}$	LDO input voltage	for NFC interface LDO	[1]	-0.3	7	V
NFC transmitter (pin TVDD_IN)						
$V_{DD(TVDD)}$	TVDD supply voltage	for NFC interface transmitter	[1]	-0.3	7	V

[1] Maximum/minimum voltage above the maximum operating range and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter life time of the device.

Table 11. Limiting values for NFC interface

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_i	input voltage	on pins RXN and RXP	[1]	0	2.2	V

[1] Maximum/minimum voltage above the maximum operating range and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter life time of the device.

Table 12. Limiting values for USB interface

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DDP(USB\_VBUS)}$	Voltage on pin USB_VBUS		[1]	-0.3	7	V

[1] Maximum/minimum voltage above the maximum operating range and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter life time of the device.

8 Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards.

For assembly guidelines refer to AN1902.

9 References

[1] NFC Forum - Wireless Charging Technical Specification
https://nfc-forum.org/product-category/specification/

[2] UM10204 I^2C-bus specification and user manual
https://www.nxp.com/docs/en/user-guide/UM10204.pdf

[3] VFBGA64 - SOT1307-2 package and soldering information
https://www.nxp.com/docs/en/package-information/SOT1307-2.pdf

[4] HVQFN64 - SOT804-4 package and soldering information
https://www.nxp.com/docs/en/package-information/SOT804-4.pdf

[5] AN1902 Assembly guidelines for QFN and SON packages
https://www.nxp.com/docs/en/application-note/AN1902.pdf

[6] AN12639 NFC wireless charging system guide
https://www.docstore.nxp.com/products

[7] AN12641 NFC wireless charging hardware development and RF configuration
https://www.docstore.nxp.com/products

[8] PCA9430 NFC wireless charging power receiver data sheet
https://www.docstore.nxp.com/products

[9] PCA9431 NFC wireless charging power receiver data sheet
https://www.docstore.nxp.com/products

[10] CRN120 NFC wireless charging communication receiver frontend
https://www.docstore.nxp.com/products

10 Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Supersedes
CTN730_SDS v. 3.0	20210112	Product short data sheet	-
Modifications:	• First released "Product short data sheet"		

11 Legal information

11.1 Data sheet status

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Tables

Figures

Contents

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