

APPENDIX 4

PLL DATA SHEETS

From: M.P. Mok Total: 13 copies. CMOS LSI

SANYO

No. 4797A

LC72322

Single-Chip Microcontroller with PLL and LCD Driver

-55.34

Received

Overview

The LC72322 is a single-chip microcontroller for use in electronic tuning applications. It includes on chip both LCD drivers and a PLL circuit that can operate at up to 150 MHz. It features a large-capacity ROM, a highly efficient instruction set, and powerful hardware.

Functions

- Stack: Eight levels
- Fast programmable divider
- General-purpose counters: HCTR for frequency measurement and LCTR for frequency or period measurement
- LCD driver for displays with up to 56 segments (1/2 duty, 1/2 bias)
- Program memory (ROM): 4 k words by 16 bits
- Data memory (RAM): 256 4-bit digits
- All instructions are single-word instructions
- Cycle time: 2.67 μ s, 13.33 μ s, or 40.00 μ s (option)
- Unlock FF: 0.55 μ s detection, 1.1 μ s detection
- Timer FF: 1 ms, 5ms, 25ms, 125ms
- Input ports*: One dedicated key input port and one high-breakdown voltage port
- Output ports*: Two dedicated key output ports, one high-breakdown voltage open-drain port
Two CMOS output ports (of which one can be switched to be used as LCD driver outputs)
Seven CMOS output ports (mask option switchable to use as LCD ports)
- I/O ports*: One switchable between input and output in four-bit units and one switchable between input and output in one-bit units

Note: * Each port consists of four bits.

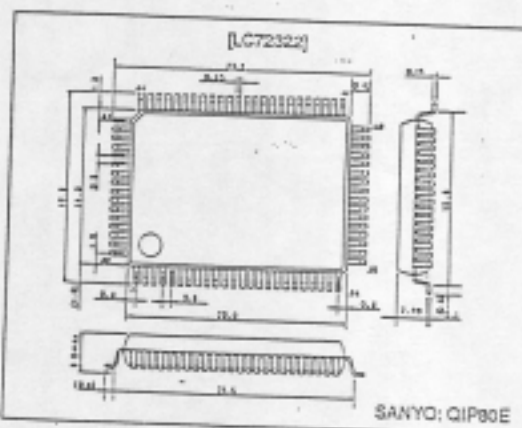
- Program runaway can be detected and a special address set (Programmable watchdog timer).
- Voltage detection type reset circuit
- One 6-bit A/D converter
- Two 8-bit D/A converters (PWM)
- One external interrupt
- Hold mode for RAM backup
- Sense FF for hot/cold startup determination
- PLL: 4.5 to 5.5 V
- CPU: 3.5 to 5.5 V
- RAM: 1.3 to 5.5 V

Package Dimensions

unit: mm

3174-QFP80E

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Sanyo 莫先生, 孫小姐
TEL: 2311 1198

Dash
June 22, 1998.

June 23, 1998.

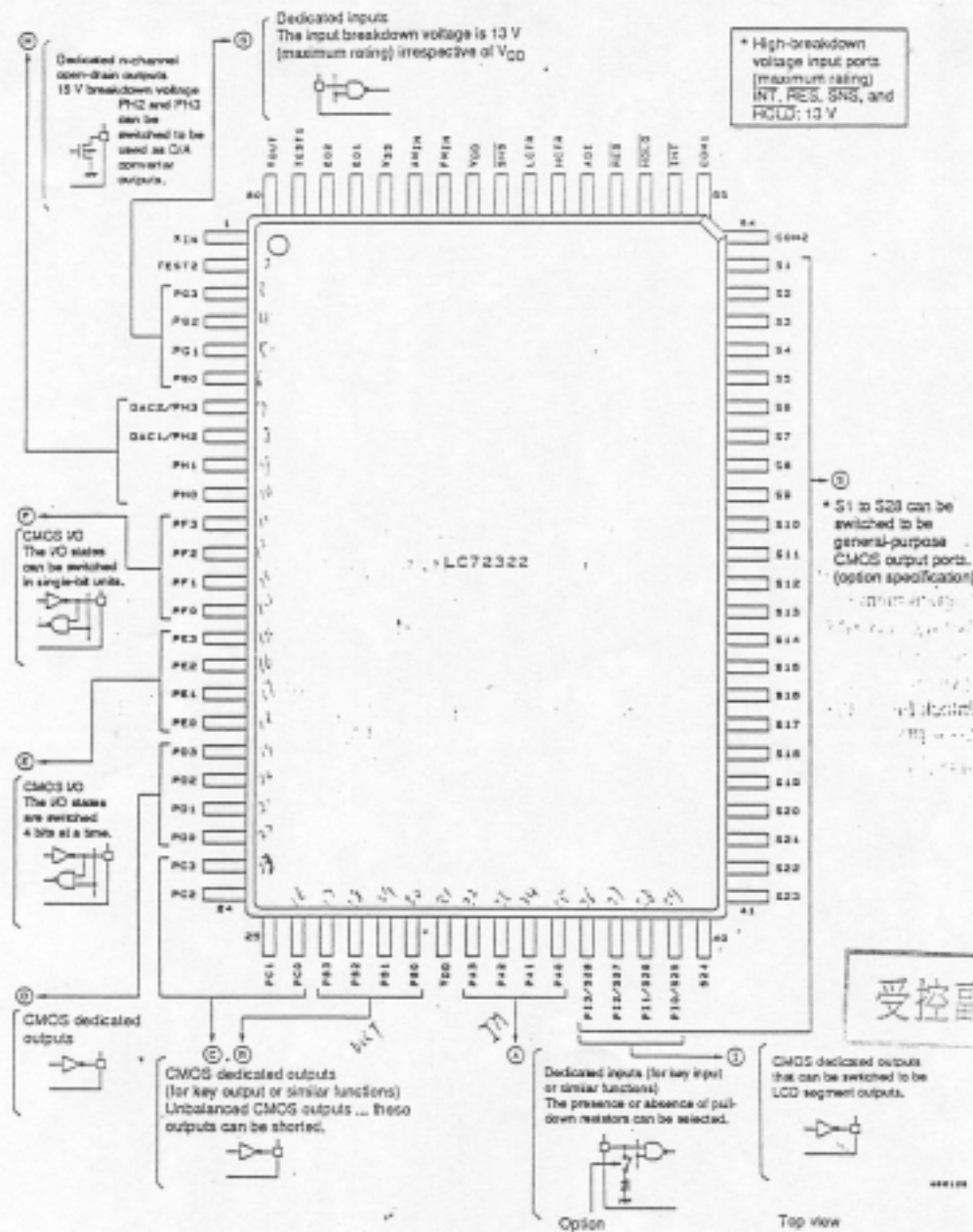
This LSI can easily use CCB that is SANYO's original bus format.



- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus

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Pin Assignment



Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$		-0.3 to +6.5	V
Input voltage	V_{IH1}	HOLD, INT, RES, ADI, SNS, and the G port	-0.3 to +13	V
	V_{IH2}	Inputs other than V_{IH1}	-0.3 to $V_{DD} + 0.3$	V
Output voltage	V_{OH1}	H port	-0.3 to +15	V
	V_{OH2}	Outputs other than V_{OH1}	-0.3 to $V_{DD} + 0.3$	V
Output current	I_{OH1}	All O and H port pins	0 to 5	mA
	I_{OH2}	All E and F port pins	0 to 3	mA
	I_{OH3}	All S and G port pins	0 to 1	mA
	I_{OH4}	S1 to S28 and all I port pins	0 to 1	mA
Allowable power dissipation	$P_d\text{ max}$	$T_a = -40\text{ to }+85^\circ\text{C}$	300	mW
Operating temperature	T_{opr}		-40 to +85	$^\circ\text{C}$
Storage temperature	T_{stg}		-45 to +125	$^\circ\text{C}$

Allowable Operating Ranges at $T_a = -40\text{ to }+85^\circ\text{C}$, $V_{DD} = 3.5\text{ to }5.5\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD1}	CPU and PLL operating	4.5		5.5	V
	V_{DD2}	CPU operating	3.5		5.5	V
	V_{DD3}	Memory retention voltage	1.3		5.5	V
Input high level voltage	V_{IH1}	G port	$0.7 V_{DD}$		8.0	V
	V_{IH2}	RES, INT, HOLD	$0.8 V_{DD}$		8.0	V
	V_{IH3}	SNS	2.5		8.0	V
	V_{IH4}	A port	$0.6 V_{DD}$		V_{DD}	V
	V_{IH5}	E, F port	$0.7 V_{DD}$		V_{DD}	V
	V_{IH6}	LCTR (period measurement), V_{DD1} , PE1, PE3	$0.8 V_{DD}$		V_{DD}	V
	V_{IH7}	AD0				V
Input low level voltage	V_{IL1}	G port	0		$0.3 V_{DD}$	V
	V_{IL2}	RES, INT, PE1, PE3	0		$0.2 V_{DD}$	V
	V_{IL3}	SNS	0		1.3	V
	V_{IL4}	A port	0		$0.2 V_{DD}$	V
	V_{IL5}	PE0, PE2, F port	0		$0.3 V_{DD}$	V
	V_{IL6}	LCTR (period measurement), V_{DD1}	0		$0.2 V_{DD}$	V
	V_{IL7}	AD0	0		$0.4 V_{DD}$	V
Input frequency	f_{IN1}	XIN	4.0	4.5	8.0	MHz
	f_{IN2}	FMIN, V_{IN2} , V_{DD1}	10		120	MHz
	f_{IN3}	FMIN, V_{IN2} , V_{DD1}	10		150	MHz
	f_{IN4}	AMIN (S1), V_{IN4} , V_{DD1}	0.5		10	MHz
	f_{IN5}	AMIN (H), V_{IN5} , V_{DD1}	2.0		40	MHz
	f_{IN6}	HCTR, V_{IN6} , V_{DD1}	0.4		12	MHz
	f_{IN7}	LCTR (frequency), V_{IN7} , V_{DD1}	100		500	kHz
	f_{IN8}	LCTR (frequency), V_{IN8} , V_{IN6} , V_{DD1}	1		20×10^3	Hz
Input amplitude	V_{IN1}	XIN	0.50		1.5	Vrms
	V_{IN2}	FMIN	0.10		1.5	Vrms
	V_{IN3}	FMIN	0.15		1.5	Vrms
	$V_{IN4, 5}$	AMIN	0.10		1.5	Vrms
	$V_{IN6, 7}$	LCTR, HCTR	0.10		1.5	Vrms
Input voltage range	V_{IN8}	AD0	0		V_{DD}	V

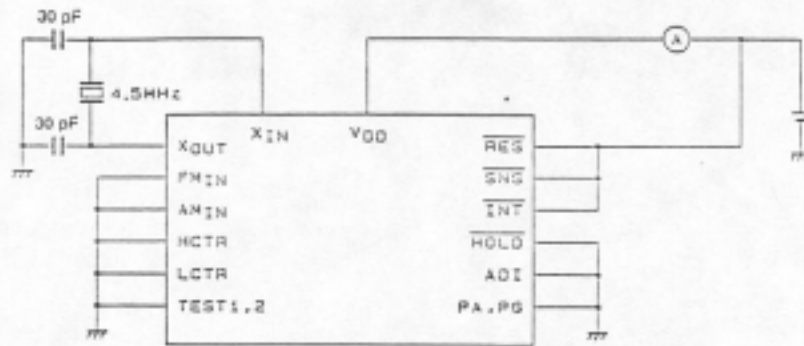
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Electrical Characteristics for the Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Hysteresis	V_H	LC7R (period), RES, INT, PE1, PE2	$0.1 V_{DD}$			V
Rejected pulse width	P_{REJ}	SNS			50	ns
Power-down detection voltage	V_{DET}		2.7	3.0	3.3	V
Input high level current	I_{IH1}	INT, HOLD, RES, AD1, SNS, and the G port: $V_I = 5.5$ V			3.0	μ A
	I_{IH2}	A, E, and F ports: E and F ports with outputs off, A port with no R_{PD} , $V_I = V_{DD}$			3.0	μ A
	I_{IH3}	XIN: $V_I = V_{DD} = 5.0$ V	2.0	5.0	15	μ A
	I_{IH4}	FMIN, AMIN, HGTR, LC7R: $V_I = V_{DD} = 5.0$ V	4.0	10	30	μ A
	I_{IH5}	A port: With an R_{PD} , $V_I = V_{DD} = 5.0$ V		50		μ A
Input low level current	I_{IL1}	INT, HOLD, RES, AD1, SNS, and the G port: $V_I = V_{SS}$			3.0	μ A
	I_{IL2}	A, E, and F ports: E and F ports with outputs off, A port with no R_{PD} , $V_I = V_{SS}$			3.0	μ A
	I_{IL3}	XIN: $V_I = V_{SS}$	2.0	5.0	15	μ A
	I_{IL4}	FMIN, AMIN, HGTR, LC7R: $V_I = V_{SS}$	4.0	10	30	μ A
Input floating voltage	V_{IF}	A port: With an R_{PD}			$0.05 V_{DD}$	V
Pull-down resistance	R_{PD}	A port: With an R_{PD} , $V_{DD} = 5.0$ V	75	100	200	k Ω
Output high level off leakage current	I_{OH1}	EO1, EO2: $V_O = V_{DD}$		0.01	10	nA
	I_{OH2}	B, C, D, E, F, and I ports: $V_O = V_{DD}$			3.0	μ A
	I_{OH3}	H port: $V_O = 13$ V			5.0	μ A
Output low level off leakage current	I_{OL1}	EO1, EO2: $V_O = V_{SS}$		0.01	10	nA
	I_{OL2}	B, C, D, E, F, and I ports: $V_O = V_{SS}$			3.0	μ A
Output high level voltage	V_{OH1}	B and C ports: $I_O = 1$ mA	$V_{DD} - 2.0$	$V_{DD} - 1.0$	$V_{DD} - 0.5$	V
	V_{OH2}	E and F ports: $I_O = 1$ mA	$V_{DD} - 1.0$			V
	V_{OH3}	EO1, EO2: $I_O = 500$ μ A	$V_{DD} - 1.0$			V
	V_{OH4}	XOUT: $I_O = 200$ μ A	$V_{DD} - 1.0$			V
	V_{OH5}	S1 to S28 and the I port: $I_O = -0.1$ mA	$V_{DD} - 1.0$			V
	V_{OH6}	D port: $I_O = 5$ mA	$V_{DD} - 1.0$			V
	V_{OH7}	COM1, COM2: $I_O = 25$ μ A	$V_{DD} - 0.75$	$V_{DD} - 0.5$	$V_{DD} - 0.3$	V
Output low level voltage	V_{OL1}	B and C ports: $I_O = 50$ μ A	0.5	1.0	2.0	V
	V_{OL2}	E and F ports: $I_O = 1$ mA			1.0	V
	V_{OL3}	EO1, EO2: $I_O = 500$ μ A			1.0	V
	V_{OL4}	XOUT: $I_O = 200$ μ A			1.0	V
	V_{OL5}	S1 to S28 and the I port: $I_O = 0.1$ mA			1.0	V
	V_{OL6}	D port: $I_O = 5$ mA			1.0	V
	V_{OL7}	COM1, COM2: $I_O = 25$ μ A	0.3	0.5	0.75	V
	V_{OL8}	H port: $I_O = 5$ mA, V_{DD1}	(150 Ω) 0.75		(400 Ω) 2.0	V
Output middle level voltage	V_M	COM1, COM2: $V_{DD} = 5.0$ V, $I_O = 25$ μ A	2.0	2.5	3.0	V
A/D conversion error		AD1: V_{DD1}	-1/2		1/2	LSB
Current drain	I_{DD1}	V_{DD1} , $f_{IN2} = 120$ MHz		15	20	mA
	I_{DD2}	V_{DD1} , PLL stopped, CT = 2.67 μ s (HOLD mode, Figure 1)		1.5		mA
	I_{DD3}	V_{DD1} , PLL stopped, CT = 13.33 μ s (HOLD mode, Figure 1)		1.0		mA
	I_{DD4}	V_{DD1} , PLL stopped, CT = 40.00 μ s (HOLD mode, Figure 1)		0.7		mA
	I_{DD5}	$V_{DD} = 5.5$ V, oscillator stopped, $T_a = 25^\circ$ C (BACK UP mode, Figure 2)			5	μ A
		$V_{DD} = 2.5$ V, oscillator stopped, $T_a = 25^\circ$ C (BACK UP mode, Figure 2)			1	μ A

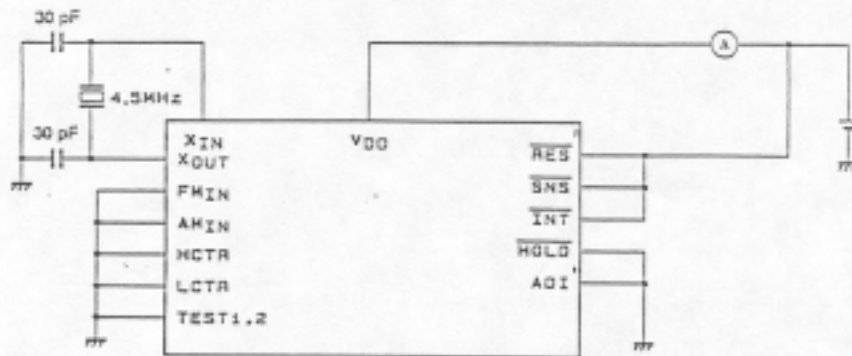
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Test Circuits



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Note: PB to PF, PH, and PI are all open. However, PE and PF are output selected.

Figure 1 I_{DD2} to I_{DD4} in HOLD Mode

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Note: PA to PI, S1 to S4, COM1, and COM2 are all open.

Figure 2 I_{DD5} in BACK UP Mode

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