



User Manual

Product Name: Wireless Audio Module

Model: WL2SB21

Brand: LG

Part No.: SWA52-L1

LG Electronics Inc.

222, LG-ro Jinwi-myeon Pyeongtaek-si, Gyeonggi-do, 17709, Republic of Korea

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General Description

Extended Range Mono/Stereo Wireless Audio System, based on the Skyworks AV5100

GeneralDescription

The WL2SB21 module is a member of a family of products representing a new level of system integration offering customers fast time to market with a point-to-point mono, or stereo, wireless connection. These modules are optimized for low-cost, high-quality and ease-of-use.

The module incorporates Skyworks's proprietary 5GHz wireless audio protocol, designed from the ground up specifically for audio. It features low fixed latency, uncompressed CD quality mono or stereo audio, superior interference immunity, and inherent coexistence with WiFi.

Extended range is enabled on WL2SB21 with an external RF power amplifier (PA), increasing typical transmit power to as much as 12dBm typical.

The WL2SB21 module integrates all features necessary to complete a wireless stereo or mono link, including AV5100 Wireless Audio Chip, printed diversity antennas, PA, shield can, flash memory, interface connector and all passive components. Just provide power and an I2S interface and you are ready to create a wireless audio link.

The module measures 35 x 35 x 2.7 mm and is provided with a 26 pin FPCconnector.

The module is certified to FCC and CE standards(TBD).

Applications

- ✓ Wireless Subwoofers
- ✓ Stereo Wireless RearSpeakers
- ✓ Soundbar / Audio Video Receiver /BluRay
- ✓ Mono/Stereo Audio ChannelTransmission

OrderingOptions

WL2SB21 TX: Transmit module with digital audio input

WL2SB21 RX: Receive module with digitalaudio output

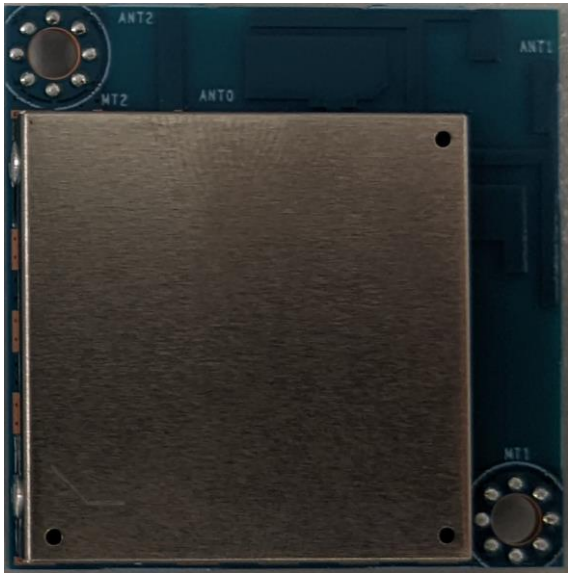
Features

- ✓ AudioInterfaces
 - ✓ I2S Digital Input / Output interfacewith >93dB end-to-end digital audio path
- ✓ Wireless Range(Typ)
 - ✓ > 50m Non Line Of Sight (NLOS)range
 - ✓ > 160m Line Of Sight (LOS) range
- ✓ Frequency range: 5.725-5.875 GHz, continuous dynamic channelselection
- ✓ Forward error correction coding,error detection, and audio-specific error concealment
- ✓ Dual printed PCB diversity antennas for multipath and fadingmitigation
- ✓ Auto-search/synch and dynamicchannel selection
- ✓ Low, fixedlatency
- ✓ 26 pin FPC or pin headerconnector
- ✓ Sample rate converter: Support for 32-96kHz input samplerates
- ✓ Customizable firmware for simple, low-cost, sub-woofer amplifierimplementations
- ✓ RF parts can-shielded, module meets FCC part 15 rules for emissions andsusceptibility.
- ✓ General purpose over-the-air (OTA)serial interface:
 - ✓ 11 kbps, bi-directional, fullduplex
 - ✓ Support for amplifier control data, meta-data, and remote controlcommands

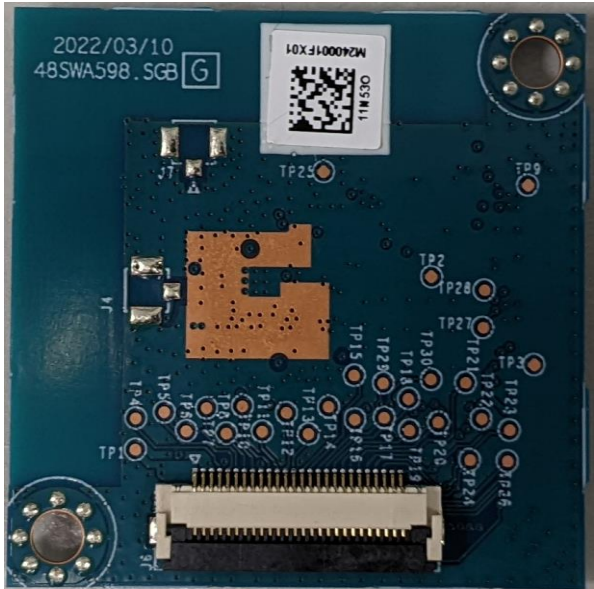
1 Product Photograph

WistronNeweb Corp.		
REG.DATE: 2022.03.15	SPECIFICATION	REV.NO :1.0
REV.DATE: 2022.03.15	MODEL NAME : 48SWA598.SGB	

Product Photograph Top View



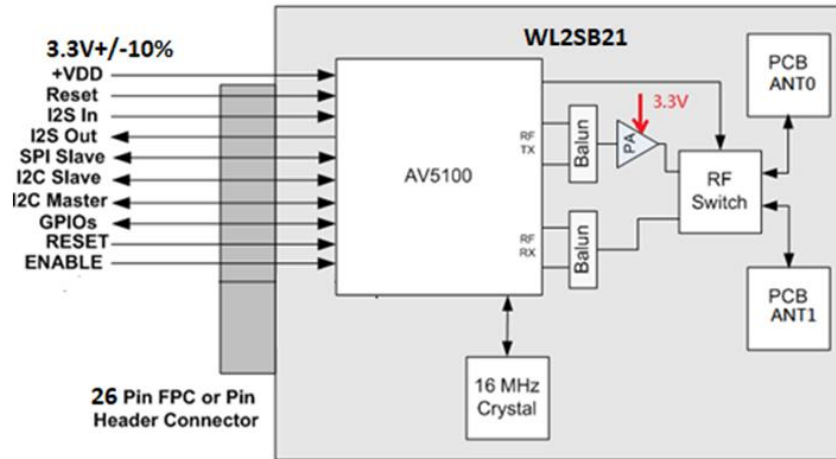
Product Photograph Bottom View



2 Standard Compliance

No	Pass Certificaton(TBD)	Certification number
1	북아(FCC)인증	BEJ-WL2SB21
2	IC	2703H-WL2SB21
3	CE	
4	UKCA	
5	KCC	
6	ANATEL	
7	RAMATEL	

3 WL2SB21 Functional Block Diagram and Functional Description



FCC frequency range: 5155.35-5247.35 & 5726.35-5848.35 & 5850.35-5874.35MHz
 IC frequency range: 5155.35-5247.35 & 5726.35-5848.35MHz
 EU / UKCA frequency range: 5728.35-5872.35MHz

Figure 1: WL2SB21 Module Block Diagram

The WL2SB21 module is available in 2 variations; digital input transmitter module or digital output receiver module.

There are three available I2S digital audio data inputs/outputs, each of these can be configured to operate as either a master or a slave - depending on the application, the I2S ports can operate simultaneously as either inputs or outputs. When configured as slaves, the I2S inputs/outputs can be independently clocked by up to two external masters. In addition, MCLK can be output from the module to provide a reference clock source to an external ADC or DAC. MCLK can also be input to the module to provide a reference clock from an external source.

Figure 1 shows the block diagram of the WL2SB21 module. The hardware for the audio input (transmit) and audio output (receive) versions of the module is identical and only the firmware loaded onto the module determines its function.

The highly integrated nature of the AV5100 transceiver IC results in few external components being required for the WL2SB21 module design. 2 printed PCB antennas are used to achieve increased range, and to achieve antenna spatial diversity. The extended-range RF path consists of the antennas, associated tuning components, shield can, the RF switch, RF power amplifier (PA) and two baluns, one connected to each of the RF input/output ports on the AV5100 IC.

A 16MHz crystal oscillator generates the AV5100 fundamental system clock used as the basis for all RF and digital audio clocks.

The AV5100 is able to boot from internal ROM upon first power up, which enables programming the flash chip with the application firmware through USB. In addition, Over-the-air Firmware upgrade capability can be enabled through the application firmware. The module can be controlled from an external host device via the I2C Slave or the SPI Slave data interfaces. The I2C master port allows the module to control other system audio devices such as a sub-woofer amplifier system without having to add another MCU to the product design. Up to 9 additional GPIOs are available on the WL2SB21 module (not including I2C and I2S signals) for implementing different UI features on the target application. The resources mentioned above can be leveraged to implement low cost sub-woofer designs as outlined below.

The firmware of the module has locked the set of the parameter, it's not allowed to adjust the parameter in any way. It's the same as the usual wireless mechanism, the transmission will be stopped automatically if the transmission information is missed/ lacked or failed.

3.1 Typical Sub-Woofer Implementation

A basic AV5100 Wireless Subwoofer system block Diagram is shown in Fig. 2.

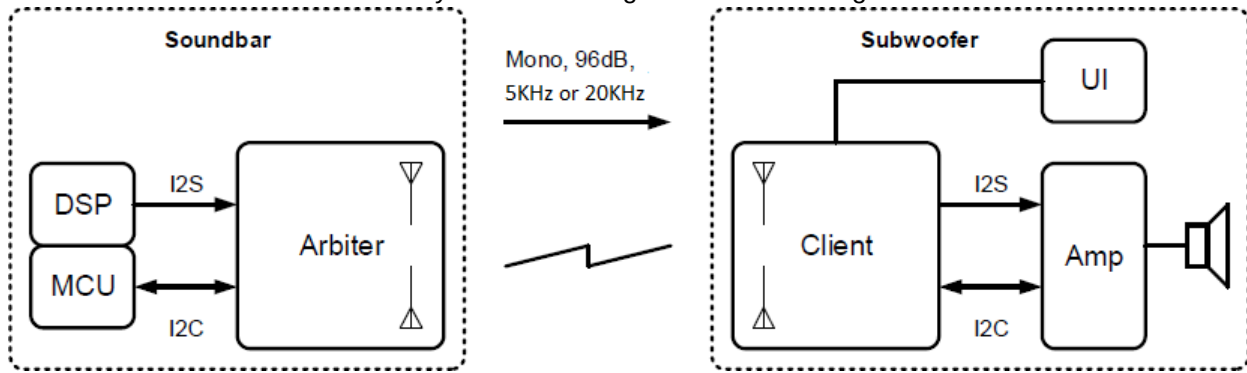


Figure 2: AV5100 Wireless Subwoofer Solution Block Diagram

A simple low cost implementation of sub-woofer design is shown in Figure 3. The sub amplifier consists of a PWM chip plus an output stage device, but no external MCU is required as the WL2SB21 RX module performs the control function using the I2C master communication port in conjunction with multiple GPIOs. The WL2SB21 module is configured to accept nominal 3.3V power from the main application board. An optional reset signal can be supplied to the WL2SB21 RX module and I2C or SPI slave communication can be used to control the module if required.

Several GPIOs can be used to drive LEDs, or to connect to UI buttons. Typically 2 LEDs may be used and 1 button for pairing purposes. Another button could be used, for example, to implement a “bass enhance” feature. Another GPIO can be used to control the power supply to external system blocks such as the PWM IC and the output stage. The WL2SB21 RX module can remain powered up during a standby or low power operating mode; however, a true power-down mode can be implemented by configuring pin 17 (GPIO15/ADAT2/CEN) to be used as a chip-enable pin that can be used to power down the AV5100. The WL2SB21 can also be completely powered down by turning off the main 3.3V supply.

If the wireless link is lost (ex. when the sound bar is powered down), the WL2SB21 RX module can, after a timeout period, power down the amplifier and output stage sections to conserve power and to help meet Energy Star requirements.

The I2C master port from the WL2SB21 RX module (pins 5 and 6 on the connector) can communicate, control, and initialize external audio ICs such as the PWM chip in this example. Other GPIOs can be used to detect fault conditions (over temperature etc) and notify the module. The audio is routed from the WL2SB21 RX module to the amplifier circuit with the I2S output port which can be configured as either a master or a slave as required. MCLK can also be generated from the WL2SB21 RX module as a 12.00 MHz clock if required.

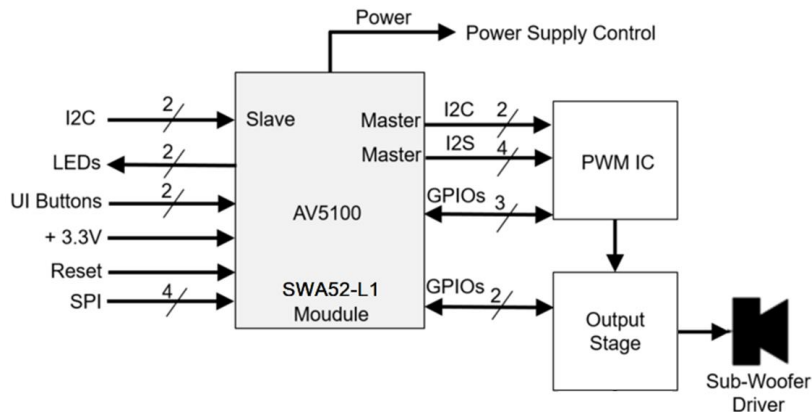


Figure 3: WL2SB21 Module Simple Sub-Woofer Implementation

3.2 WL2SB21 Module Connections and Interfaces

Signal Type	Description
+3.3V Supply	The WL2SB21 hardware is configured to accept a nominal +3.3V supply.
Reset	Active low reset input. This pin is driven from an open collector/drain device such that it can be pulled to ground for the active reset state but, when released, must go to a high impedance state. This pin should not be actively driven high, as the AV5100 internal reset circuit will not operate correctly.
I2S In Port	The I2S input port can be configured as a master or slave. Consequently BCLK and LRCK can be either inputs or outputs. In addition, MCLK can be sourced by the module on pin 16. Since the AV5100 IC contains a sample rate converter, MCLK is not required to be supplied to the module when it is an I2S slave. CMOS 3.3V logic levels are used for all I2S signals.
I2S Out Port	The I2S output port can be configured as a master or slave. Consequently BCLK and LRCK can be either inputs or outputs. In addition, MCLK can be sourced by the module on pin 16. Since the AV5100 IC contains a sample rate converter, MCLK is not required to be supplied to the module when it is an I2S slave. CMOS 3.3V logic levels are used for all I2S signals.
I2C Slave Port	The I2C slave port can be used for external host communication and for module testing. It is assumed that external pull up resistors are connected at the I2C master communicating with the module.
I2C Master Port	The I2C master port is used to communicate with external audio devices such as a sub-woofer amplifier. It is assumed that external pull up resistors are included on the application board.
GPIOs	3.3V CMOS logic level GPIOs available to connect to other devices, or to use as UI supporting GPIOs for LED and button support. All supported GPIOs can be configured as outputs or inputs with configurable pull-ups/pull-downs.

4 WL2SB21 Connector Information

Table 1: WL2SB21 Connector Information

No	Pin Name	Pin Type	AV5100 Pin	WL2SB21 TX Pin Description	WL2SB21 RX Pin Description
1	VDD	Supply Input	31	+3.3V input supply voltage	+3.3V input supply voltage
2	GND	GND	Paddle (57)	GND	GND
3	GND	GND	Paddle (57)	GND	GND
4	GPIO20/ Green_LED	Digital I/O	56	GPIO, or LINK_LEDOutput	GPIO, or LINK_LED Output
5	GPIO22/ Red_LED	Digital I/O	43	GPIO, or LINK_LEDOutput	GPIO, or LINK_LED Output
6	GPIO10/MCLK	Digital I/O	53	(default is NC pin for TX module)	(default is output of MCLK for RX module)
7	GPIO13/DATA_B	Digital I/O	50	GPIO or I2S Port 1 Audio Data	GPIO or I2S Port 1 Audio Data
8	GPIO13/DATA_A	Digital I/O	49	DIN_Rear_L	DOUT_Woofers or Rear
9	GND	GND	Paddle (57)	GND	GND
10	GPIO4/S_SCL/M_SCL	Digital I/O	9	GPIO, I2C Master Serial Clock	GPIO, I2C Master Serial Clock
11	GPIO5/S_SDA/M_SDA	Digital I/O	10	GPIO, I2C Master Serial Data	GPIO, I2C Master Serial Data
12	GPIO9/M_MISO	Digital I/O	5	GPIO, SPI Slave Data In	GPIO, SPI Master Data In
13	GPIO8/M_MOSI	Digital I/O	6	GPIO, SPI Slave Data In	GPIO, SPI Master Data In
14	GPIO7/M_SCLK	Digital I/O	7	GPIO or SPI Slave Serial Clock	GPIO or SPI Slave Serial Clock
15	GPIO6/S_SSB	Digital I/O	8	GPIO or SPI Slave Chip Select	GPIO or SPI Slave Chip Select
16	GPIO25/SPI_WP	Digital I/O	40	GPIO or SPI Slave Chip Select	GPIO or SPI Slave Chip Select
17	RESETN_EXT	Digital Input	37	RESET signal active low (4)	RESET signal active low (4)
18	GPIO15/PWR_SENSE	Digital I/O	48	Reserved	PWR_SENSE
19	GPIO24/PWR_CTRL	Digital I/O	41	Reserved	PWR_CTRL
20	GPIO23/PWM_RESET	Digital I/O	42	Reserved	PWM_RESET
21	GPIO18_RESET	Digital I/O	2	Reserved	AMP_RESET
22	GPIO19_AMP_SD/OTW	Digital I/O	1	Reserved	AMP_SD/OTW
23	GPIO21_PAIR	Digital I/O	55	GPIO, or input from PAIR Button	GPIO, or input from PAIR Button
24	GPIO11/BCLK	Digital I/O	52	GPIO or I2S Port 1 Bit Clock	GPIO or I2S Port 1 Bit Clock
25	GND	GND	Paddle (57)	GND	GND
26	GPIO12/LRCK	Digital I/O	51	GPIO or I2S Port 1 Word Clock	GPIO or I2S Port 1 Word Clock

5 WL2SB21 Mechanical Information

The mechanical design of the WL2SB21 is shown in Figure 4. The location of the 26 pin connector, locating slots, and mounting hole are dimensioned. The module features a shield can which height is 1.9mm above PCB. The top 27.8x 6mm area is consumed by the 2 PCB antennas. It is critical in product designs for the antenna part of the module to be located away from all metal objects and ideally away from close proximity to plastic.

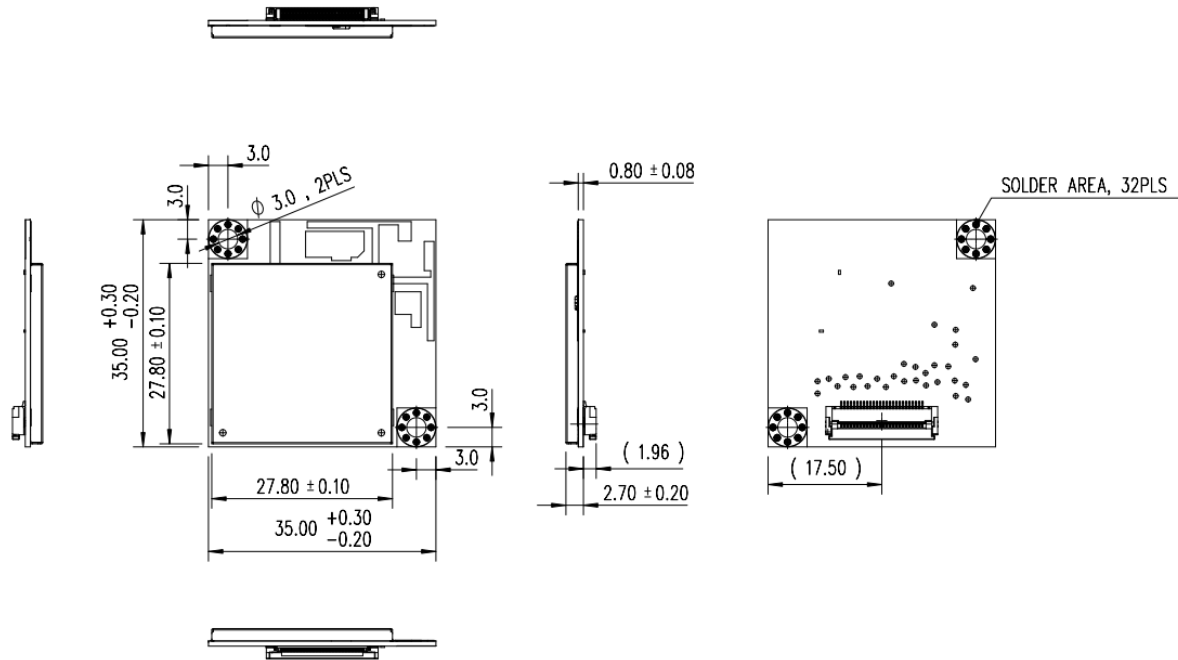


Figure 4 – WL2SB21 Module Outline and Mechanical Dimensions

- PCB thickness is 0.8mm
 - The top of shield is 1.9mm above PCB
 - The maximum height from the bottom of the PCB to the top of the shield can is 2.7mm.
- PCB thickness +/- 0.08mm tolerance is related to PCB production process variation.

6 Electrical, Audio and Timing Specifications

6.1 Absolute Maximum Ratings

Absolute Maximum Ratings (AMR) are stress ratings only. AMR corresponds to the maximum value that can be applied without leading to instantaneous or very short-term unrecoverable hard failure (destructive breakdown). Stresses beyond those listed under AMR may cause permanent damage to the device.

Functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Range” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may adversely affect device reliability.

Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

CONDITION	MIN	MAX
+3.3V Supply Voltage Input	3.0	3.6V
Input Voltage Range – Digital Inputs	-0.3V	3.6V
Input Voltage Range – Analog Inputs	-0.3V	3.6V
Operating Temperature	-40°C	+60°C
Storage Temperature	-40°C	+70°C
Static Discharge Voltage ¹	2kV	----

Notes:

1) HBM = ESD Human Body Model; C = 100pF, R = 1kΩ

6.2 Recommended Operating Range

PARAMETER	MIN	TYP	MAX	UNIT
VDD, +3.3V Supply pin voltage	3.0	3.3	3.6	V
Ambient Temperature (T _A)	0		55	°C
RESET pin hold time	10			msec
Power Supply Rise Time (to 3.0V)	0		10	msec

6.3 Electrical Characteristics – DC Characteristics

Operating Conditions: VDD = 3.0 to 3.6V, T_A = 0 °C to +55 °C, RF Freq = 5725-5875MHz, measured relative to the RF balun single-ended I/O. Typical specifications at T_A = 25 °C, VDD = 3.3V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current (IVDDA)	Shutdown (chip disabled)			1	uA
	Standby (also USB suspend)			2.5	mA
	RX mode (continuous RX)		89		mA
	TX mode (continuous TX); Pout=+12dBm		330		mA
CMOS I/O Logic Levels – 3.3V I/O					
Input Voltage Logic Low, VIL				0.6	V
Input Voltage Logic High, VIH		VDDIO-0.6			V
Output Voltage Logic Low, VOL				0.3	V
Output Voltage Logic High, VOH		VDDIO-0.3			V

***a** : This is DCRMS current consumption value. If customer want to implement OCP(over current protection) for SWA52-L1, please consult with WNC for proper setting and design.

6.4 Electrical Characteristics – RF RX Characteristics

Operating Conditions: VDD = 3.0 to 3.6V, T_A = 0 °C to +55 °C, RF Freq = 5725-5875MHz, measured relative to the RF balun single-ended I/O. Typical specifications at T_A = 25 °C, VDD = 3.3V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
RF Channel Frequency Range	Band1(lower band)	5150		5250	MHz
	Band3/4(Upper band)	5725		5875	MHz
RF I/O Impedance	ANT0,ANT1		50		ohm
RX Sensitivity	SSC (single sub-carrier)		-89 *b		dBm
Max input signal	LNA = low gain mode, min IF gain		-5		dBm
Out-of-band blocker level	<5150 MHz, >5850 MHz 2400-2483.5 MHz		-45		dBm
			-20		dBm
Spurious RF outputs	5150-5850 MHz		-55		dBm
	<5150 MHz		-63		dBm
	>5850 MHz		-63		dBm

***b** : The sensitivity been defined with BER <= 0.002

6.5 Electrical Characteristics – RF TX Characteristics

Operating Conditions: VDD = 3.0 to 3.6V, T_A = 0 °C to +55 °C, RF Freq = 5725-5875MHz, measured relative to the RF balun single-ended I/O. Typical specifications at T_A = 25 °C, VDD = 3.3V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
RF Channel Frequency Range	Band1(lower band)	5150		5250	MHz
	Band3/4(Upper band)	5725		5875	MHz
RF I/O Impedance	ANT0,ANT1		50		ohm
TX Output power	SSC (single sub-carrier)	11.3	13.3	15.3	dBm
LO leakage			-20		dBc

6.5.1 Measured at the worst performing frequency

6.6 Electrical Characteristics – Audio C/CS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Response (-3dB)	16 bit audio, 11KSps over-the-air sample rate	20		5K	Hz
	16 bit audio, 14.8KSps over-the- air sample rate	20		6.5K	Hz
	16 bit audio, 22KSps over-the-air sample rate	20		10K	Hz
	16 bit audio, 29.6KSps over-the- air sample rate	20		13K	Hz
	16 bit audio, 44KSps over-the-air sample rate	20		20K	Hz
Gain Flatness ¹	0dB Input / Output Gain		±0.2		dB
SNR	I2S Input / Output	93 ⁽¹⁾			dB
THD+N			94		dB

Notes

1- 16-bit audio, all OTA sample rates. OTA 12-bit path for voice is possible, but will limit the SNR to 72dB.

6.7 AV5100 Rate Converter Characteristics

SRC Block	Input Rates	Output Rates	SNR (dB)	SRC BW (-3dB)
SRC 0 (Audio)	<u>I2S</u> 32-96K <u>USB</u> 8k – 48K, <u>ECU (TX)</u> “11K” “14.8k” “22k” “29.6k” “44k”	<u>I2S</u> Master: 48k Slave: 44.1K-96K <u>ECU (TX)</u> “11K” “14.8k” “22k” “29.6k” “44k”	All rates support 16bit, >93dB	Actual bandwidth is dependent on the lower of the input or output rates. <u>Output BW vs OTA</u> “11k” = 5kHz “14.8k” = 6.5kHz “22k” = 10kHz “29.6k” = 13kHz “44k” = 20kHz
SRC 1 (LFE)	<u>I2S</u> 32-96K <u>USB</u> 8k – 48K, <u>ECU (TX)</u> “11K” “14.8k” “22k” “29.6k” “44k”	<u>I2S</u> Master: 48k Slave: 44.1K-96K <u>ECU (TX)</u> “11K” “14.8k” “22k” “29.6k” “44k”	All rates support 16bit, >93dB	Actual bandwidth is dependent on the lower of the input or output rates. <u>Output BW vs OTA</u> “11k” = 5kHz “14.8k” = 6.5kHz “22k” = 10kHz “29.6k” = 13kHz “44k” = 20kHz
SRC 2 (Voice)	<u>I2S</u> 32-96K <u>USB</u> 8k – 48K, <u>ECU (TX)</u> “14.8k”	<u>I2S</u> Master: 48k Slave: 44.1K-96K <u>USB</u> 8k – 48K, <u>ECU (RX)</u> “14.8k”	All rates support 16bit, >93dB, but the OTA 12bit path will limit SNR to 72dB	Actual bandwidth is dependent on the lower of the input or output rates. <u>Output BW vs OTA</u> “11k” = 5kHz “14.8k” = 6.5kHz “22k” = 10kHz “29.6k” = 13kHz “44k” = 20kHz

6.8 I2C Master/Slave Communication Interface Timing (S_SCL, S_SDA)

The SWA52-L1 has both I2C slave and master interfaces available with their respective pins S_SCL, S_SDA and M_SCL, M_SDA. The interfaces operate in I2C fast-mode and can receive and transmit at up to 400 kbit/s.

Bytes are 8 bits long and are transferred with the most significant bit (MSB) first. Each byte has to be followed by an acknowledge bit. The SWA52-L1 will apply clock-stopping (by holding the clock line S_SCL LOW to force the master into a wait state) if necessary due to internal high-priority tasks.

The slave/master interface can be used both for writing (e.g. sending commands) or reading (e.g. requesting status). An additional GPIO pin on the SWA52-L1 (Ex. GPIO24), can be used to notify the I2C master when a pending message is ready to be sent.

The SWA52-L1 slave interface responds to the 7-bit slave address 1000000 (0x40) as shown in Figure 1 below.

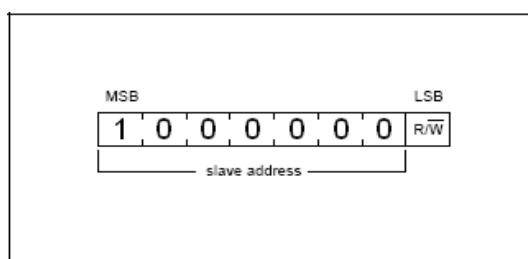


Figure 5: First Byte after the START Procedure

ELECTRICAL SPECIFICATIONS AND TIMING

Table 3: Characteristics of the S_SDA and S_SCL I/Os

PARAMETER	SYMBOL	FAST-MODE		UNIT
		MIN.	MAX.	
LOW level input voltage	VIL	-0.3	0.8	V
HIGH level input voltage	VIH	2.0	3.6	V
LOW level output voltage (open drain or open collector) at 1 mA sink current:	VOL	0	0.4	V
Output fall time from VIHmin to VILmax with a bus capacitance from 10 pF to 400 pF	tof	0	250	ns
Pulse width of spikes which must be suppressed by the input filter	tsp	0	50	ns
S_SCL clock frequency	fSCL	0	400	kHz
LOW period of the S_SCL clock	tLOW	1.3	–	μs
HIGH period of the S_SCL clock	tHIGH	0.6	–	μs
Data hold time	tHD;DAT	100	–	ns
Data set-up time	tSU;DAT	100	–	ns

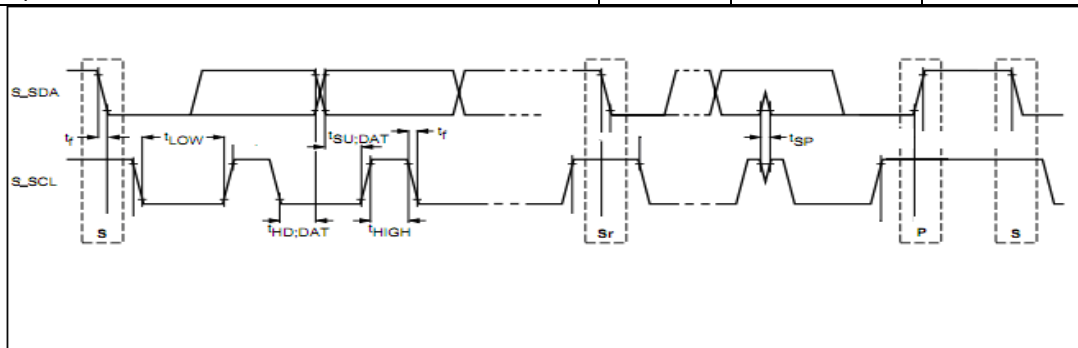
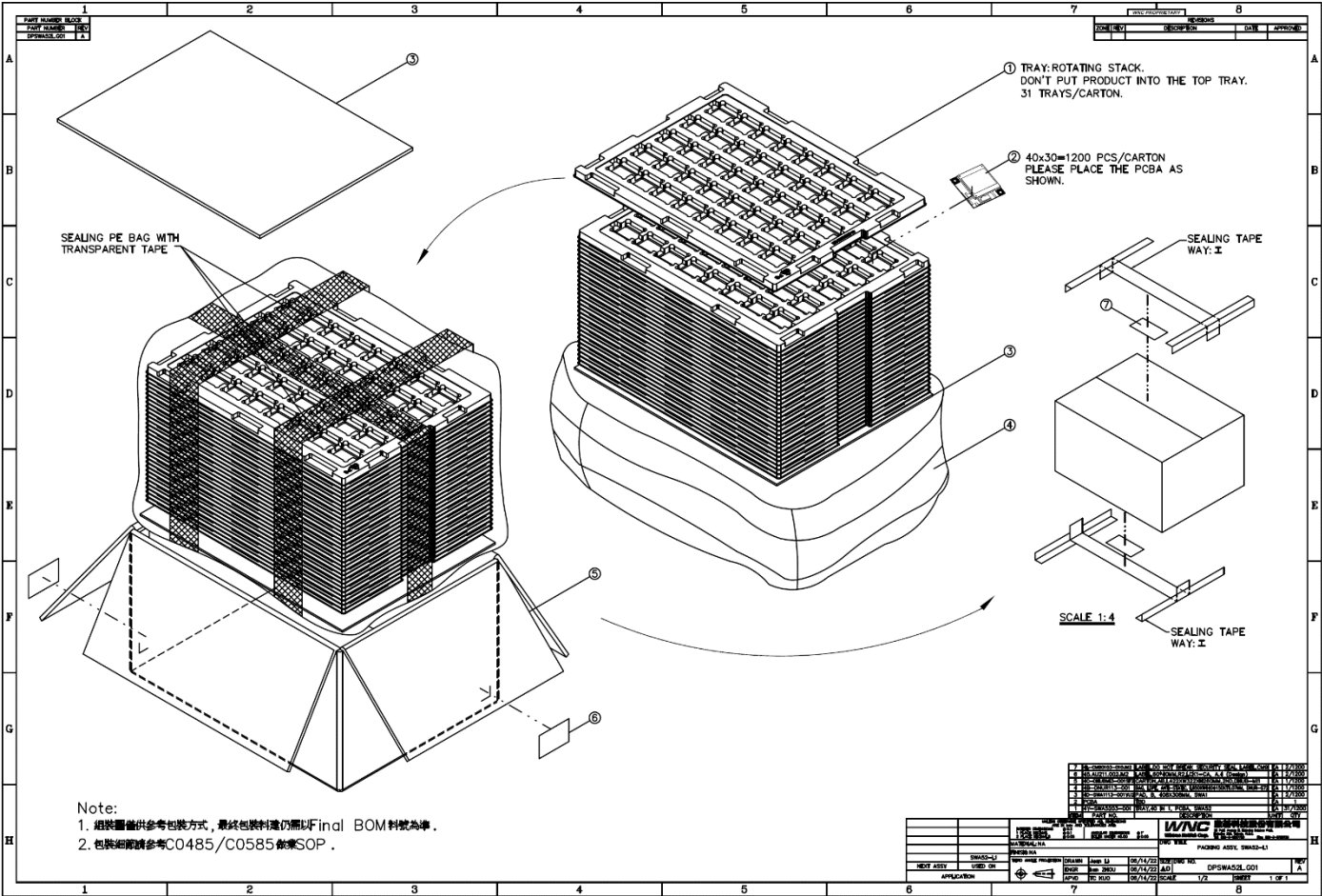
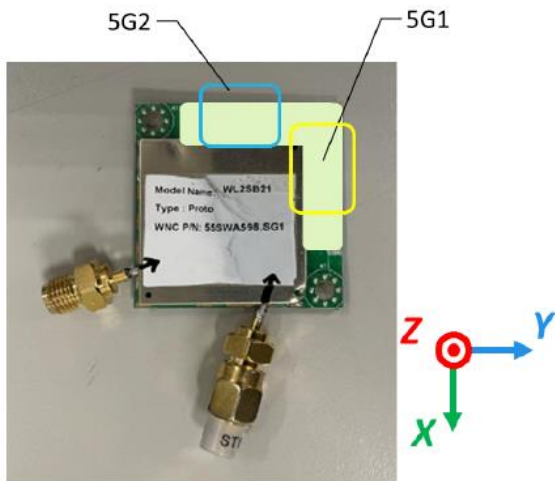


Figure 6: Definition of Timing for F/S-Mode Devices on the I²C-Bus

6.9 Packaging

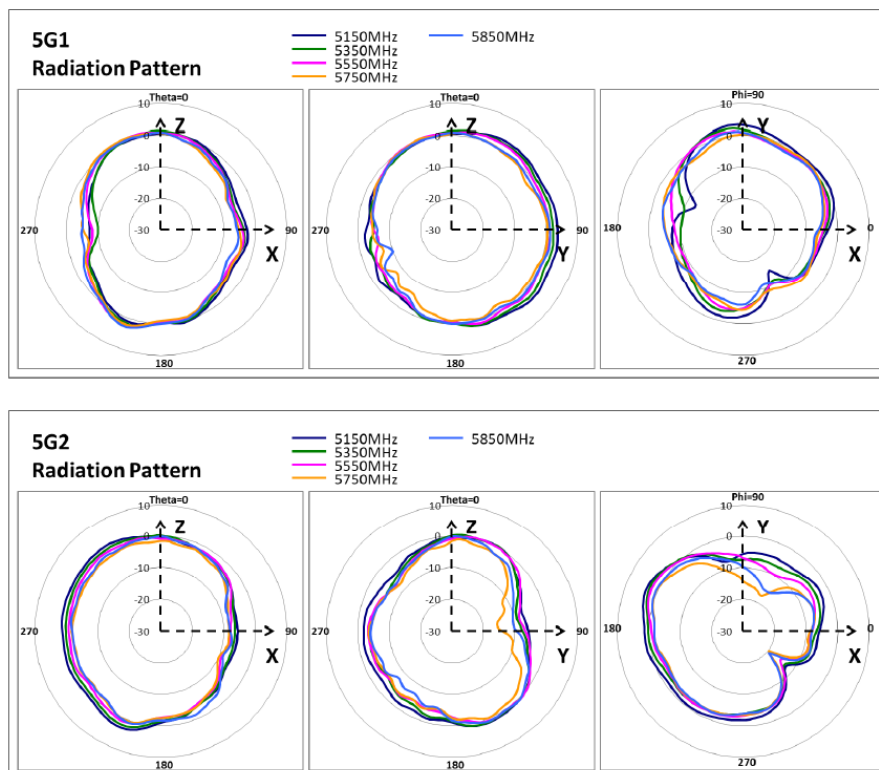


7 Antenna specification



	Frequency	5150	5350	5550	5750	5850	Avg.
5G1	Efficiency	71%	72%	68%	61%	62%	67%
	Average Gain	-1.50	-1.45	-1.65	-2.16	-2.06	
	Peak Gain	3.43	2.86	2.90	2.84	3.18	
5G2	Efficiency	70%	68%	60%	63%	64%	65%
	Average Gain	-1.53	-1.70	-2.23	-2.03	-1.94	
	Peak Gain	3.26	3.40	2.78	2.91	2.47	

Radiation Pattern for 5GHz



8 Ordering Information

FCC Statement

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference, and
- (2) This device must accept any interference received, including interference that may cause undesired operation.

Manufacturers integrating the Radio Module into other devices should note the following:

The device is compliant with part 15.407 of Title 47 of the FCC rules. If the Link Module is integrated into a new host product, the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device uses various test mode programs for test set up which operate separate from production firmware. Host integrators should contact the grantee for assistance with test modes needed for module/host compliance test requirements.

IC Statement

This Class B digital apparatus complies with Canadian ICES-003.

5150-5250MHz is limited to use indoor only

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions:

- (1) this device may not cause interference, and
- (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil est conforme aux normes CNR exemptes de licence d'Industrie Canada. Le fonctionnement est soumis aux deux conditions suivantes :

- (1) cet appareil ne doit pas provoquer d'interférences et
- (2) cet appareil doit accepter toute interférence, y compris celles susceptibles de provoquer un fonctionnement non souhaité de l'appareil.

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.

-Label and Compliance Information

The final end product must be labeled in a visible area with the following:

" Contains FCC ID: BEJ-WL2SB21". "Contains IC: 2703H-WL2SB21"

The grantee's FCC ID can be used only when all FCC/ IC compliance requirements are met.

-RF exposure

The module will install into mobile device such as Sound Bar

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

Information on test modes and additional testing requirements

-OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, additional transmitter in the host, etc.).