

LG-KS.WT0601



1. System Descriptions

The LG-KS.WT0601 module high-end digital wireless audio solution is a concept combination with system module, and main board.

The system module is a complete design, which includes all parts of RFIC, IA8 IC, optional audio I/O chip and connector in the single board.

(1) Clock generation

1. Use a 44MHz clock signal as reference clock of internal **programmable PLL** circuit to generate the audio system clock to the external ADC. Audio clock: SYS_CLK: 12.288MHz (512Fs), BCK: 3.072MHz, LRCK: 48 KHz
2. LG-KS.WT0601 have the internal PLL is configured as output frequency being 24/25 of reference clock (44MHz). Then, the output clock frequency is $44\text{MHz} \times \frac{24}{25} = 42.24\text{MHz}$. This clock is used as Base Band chip IA8's operating clock signal for audio sampling clock being 48KHz

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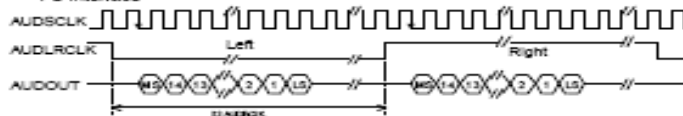


(2) External Audio ADC and Internal DAC Clock generation

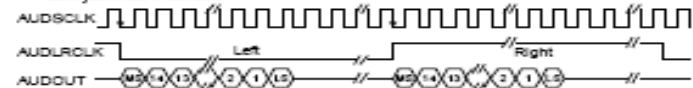
Audio ADC/DAC interface provides a high quality multi resolution(16/18/20/24-bit) digital audio connection to external audio devices. ADI interface supports I2S audio format as well as optional left-justified or right-justified audio format. ADI interface produces one 64-bit frame at the audio sample frequency using a bit clock and frame sync signal. ADI interface supports 32KHz, 44.1KHz or 48KHz audio sampling frequency, of which 256 or 384 times main clock can be generated from on-chip audio clock oscillator or external clock signal by interface mode programming.

Pin Name	I/O	Type	Description
AUD_MCLK	programmable	clock	audio oversampled clock This clock can be programmed 256 or 384 times AUDLRCLK
AUD_SCLK	programmable	clock	audio serial data bit clock This clock is fixed at 64 times AUDLRCLK
AUD_LRCLK	programmable	clock	audio frame synchronization clock This clock can be programmed 32KHz, 44.1KHz or 48KHz
AUD_DATA	programmable	serial data	audio serial data used for sending playback data to DAC and receiving data from ADC 16-bit data format with I2C, left-justified or right-justified interface

• PS Interface



• Left-justified Interface



• Right-justified Interface



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(3) Pin configuration

Pin No.	Pin definition	Pin No.	Pin definition
1	VCCIO	2	MIC_IN
3	NCS_CPU	4	AIR
5	SYS_CLK	6	UGND
7	PGND	8	AIL
9	RED LED	10	DGND
11	Blue LED	12	CH_ID
13	SCLK_CPU	14	SDA_CPU
15	REQ_CPU	16	SDI_ADC
17	LRCK_IN	18	SDI_I2S
19	SPDIF	20	BCK_IN
21	TEST1	22	TEST2
23	BCK_OUT	24	LRCK_OUT