

TWN-5213

R00C.5_0222

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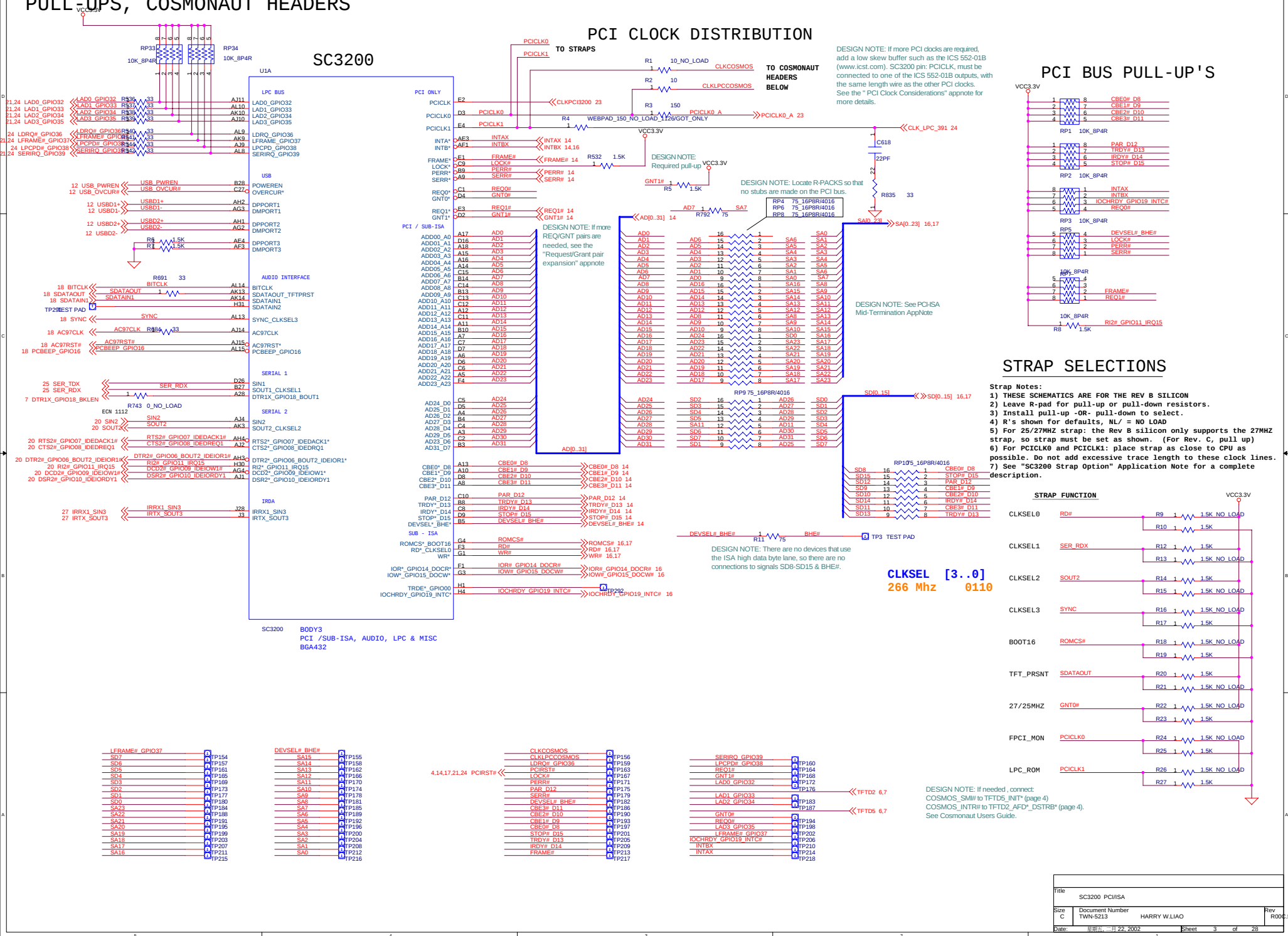
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HARRY W.LIAO
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HARRY W.LIAO
HARRY W.LIAO

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SC3200 INTERFACES: PCI/SUB-ISA, LPC, AUDIO, DOC, PCI CLOCKS; STRAP OPTIONS, PCI BUS PULL-UPS, COSMONAUT HEADERS

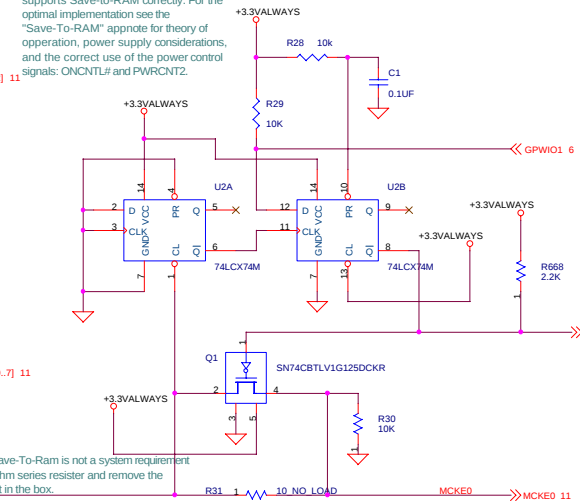


SC3200 INTERFACES: MEMORY, 32KHZ AND 27MHZ OSCILLATORS

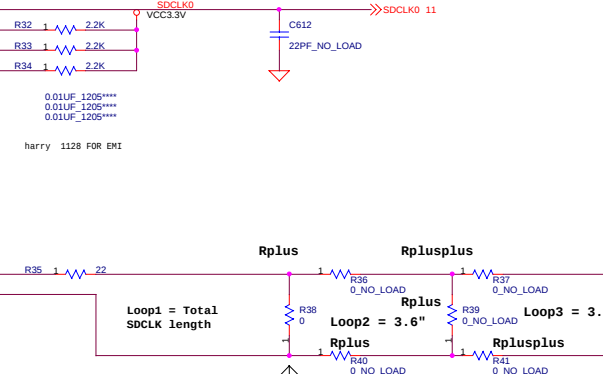
DESIGN NOTE: GPWIO0 and GPWIO1 are also connected to the Ethernet controller and the Compact Flash connector respectively. These GPWIO's are not expected to be shared. If Save-To-Ram is being used and either the Ethernet controller and the Compact Flash connector is also being used this conflict must be resolved. Contact your field service representative if your design has this issue.

SAVE-TO-RAM

DESIGN NOTE: This schematic does not have the power supply implementation that supports Save-to-RAM correctly. For the optimal implementation see the "Save-To-RAM" appnote for theory of operation, power supply considerations, and the correct use of the power control signals: ONCNTL# and PWRCNT2.



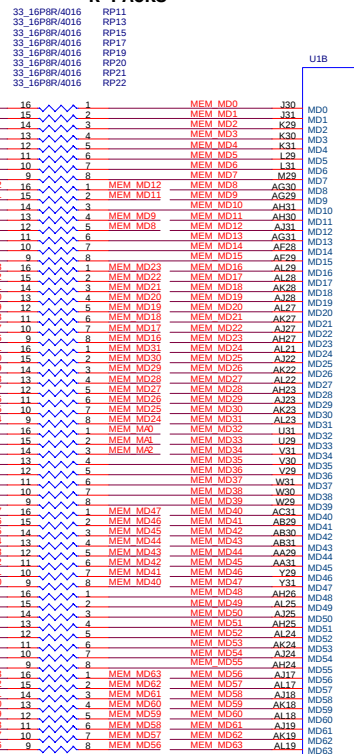
DESIGN NOTE: If Save-To-Ram is not a system requirement then install the 10 ohm series resistor and remove the Save-To-Ram circuit in the box.



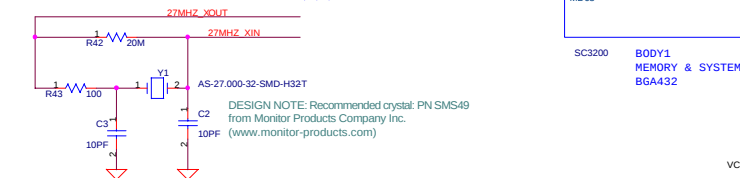
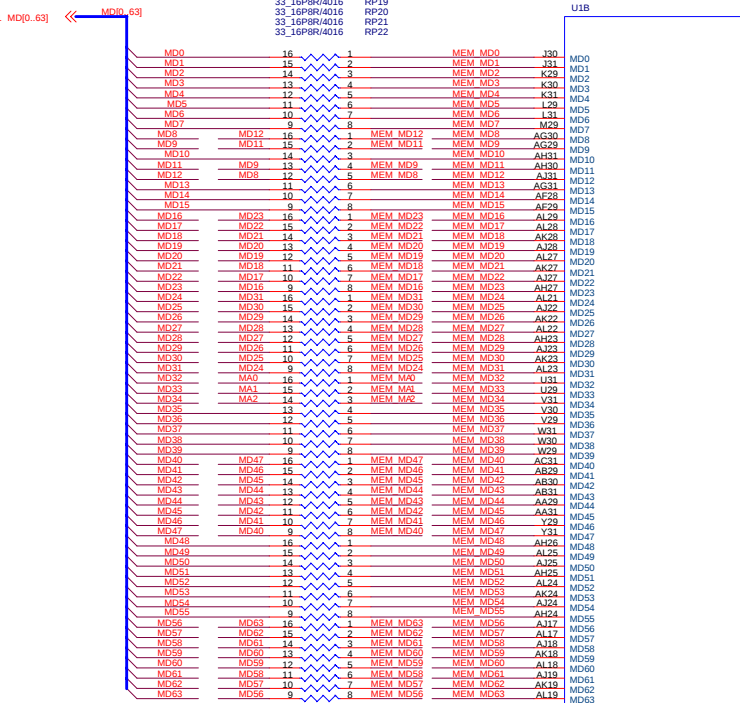
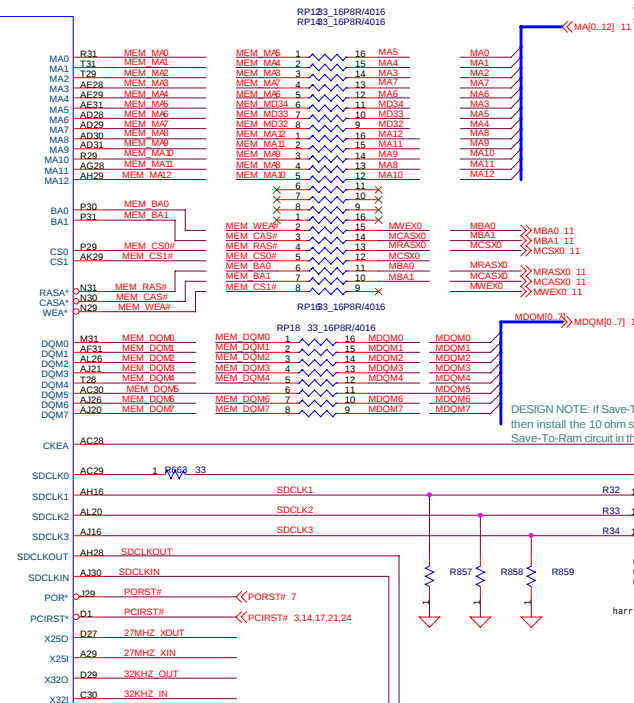
DESIGN NOTE: For more information regarding SDC routing see the "Layout Guidelines" appnote.

SODIMM total loop length is $SDCLK + 2.5''$
 DIMM total loop length is $SDCLK + 3.1''$
 On Board memory total loop length is $SDCLK + 0''$

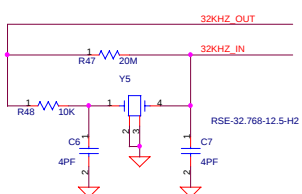
```
-DEFAULT IS TOTAL SDCLK LENGTH
-TO ADD~500ps TO LOOP TIME:
  REMOVE DEFAULT RESISTOR AND
  POPULATE THE "Rplus" RESISTORS.
-TO ADD ~1000ps TO LOOP TIME:
  REMOVE DEFAULT RESISTOR AND
  POPULATE "Rplusplus" RESISTORS.
```



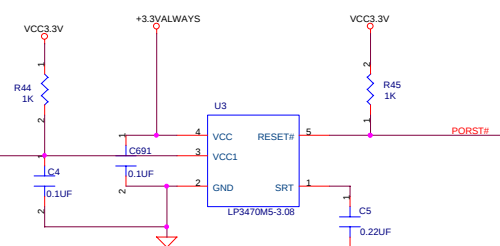
SC3200



27MHZ OSCILLATOR

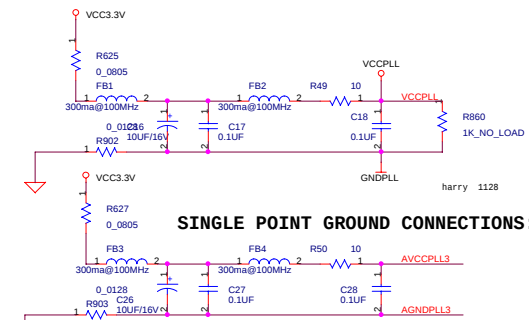


32KHZ OSCILLATOR

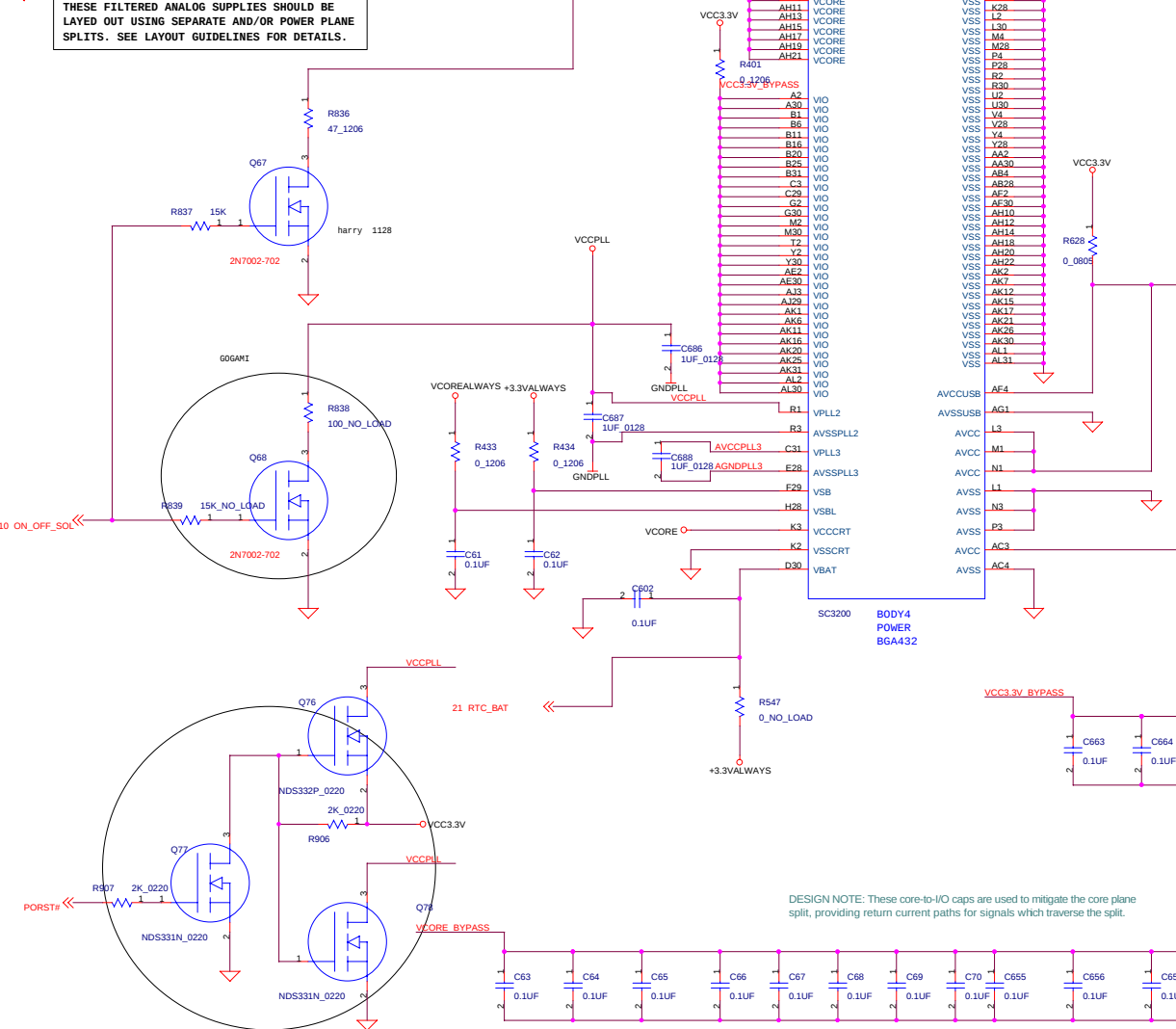


Title				
SDRAM				
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SC3200 INTERFACES: POWER; DECOUPLING CAPS, BATTERY HEADER

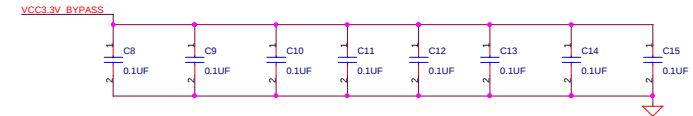


THESE FILTERED ANALOG SUPPLIES SHOULD BE LAYED OUT USING SEPARATE AND/OR POWER PLANE SPLITS. SEE LAYOUT GUIDELINES FOR DETAILS.

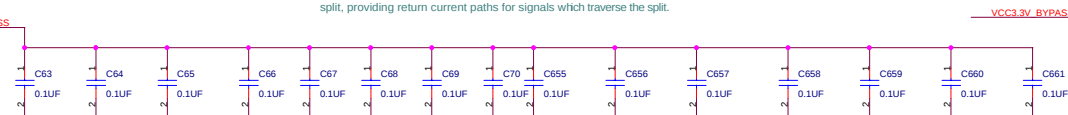
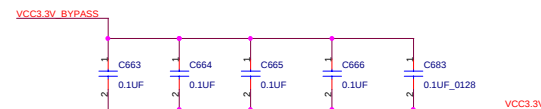
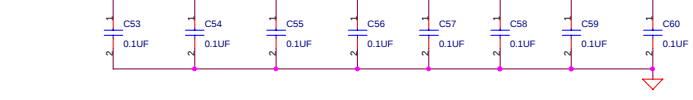
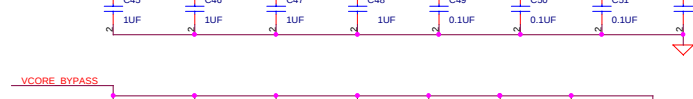
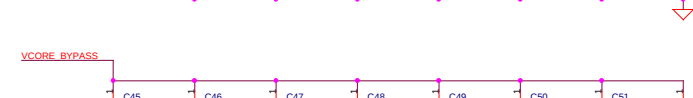
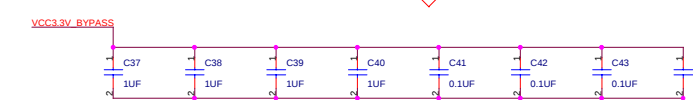
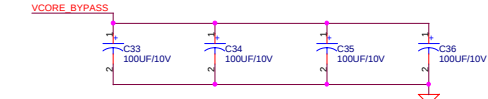
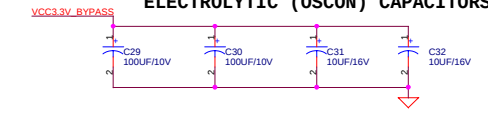
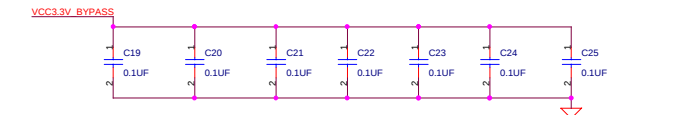


DESIGN NOTE: These core-to-I/O caps are used to mitigate the core plane split, providing return current paths for signals which traverse the split.

USE TANTALUM OR LOW-ESR ELECTROLYTIC (OSCON) CAPACITORS
SEE LAYOUT GUIDELINES FOR DECOUPLING CAPACITOR PLACEMENT

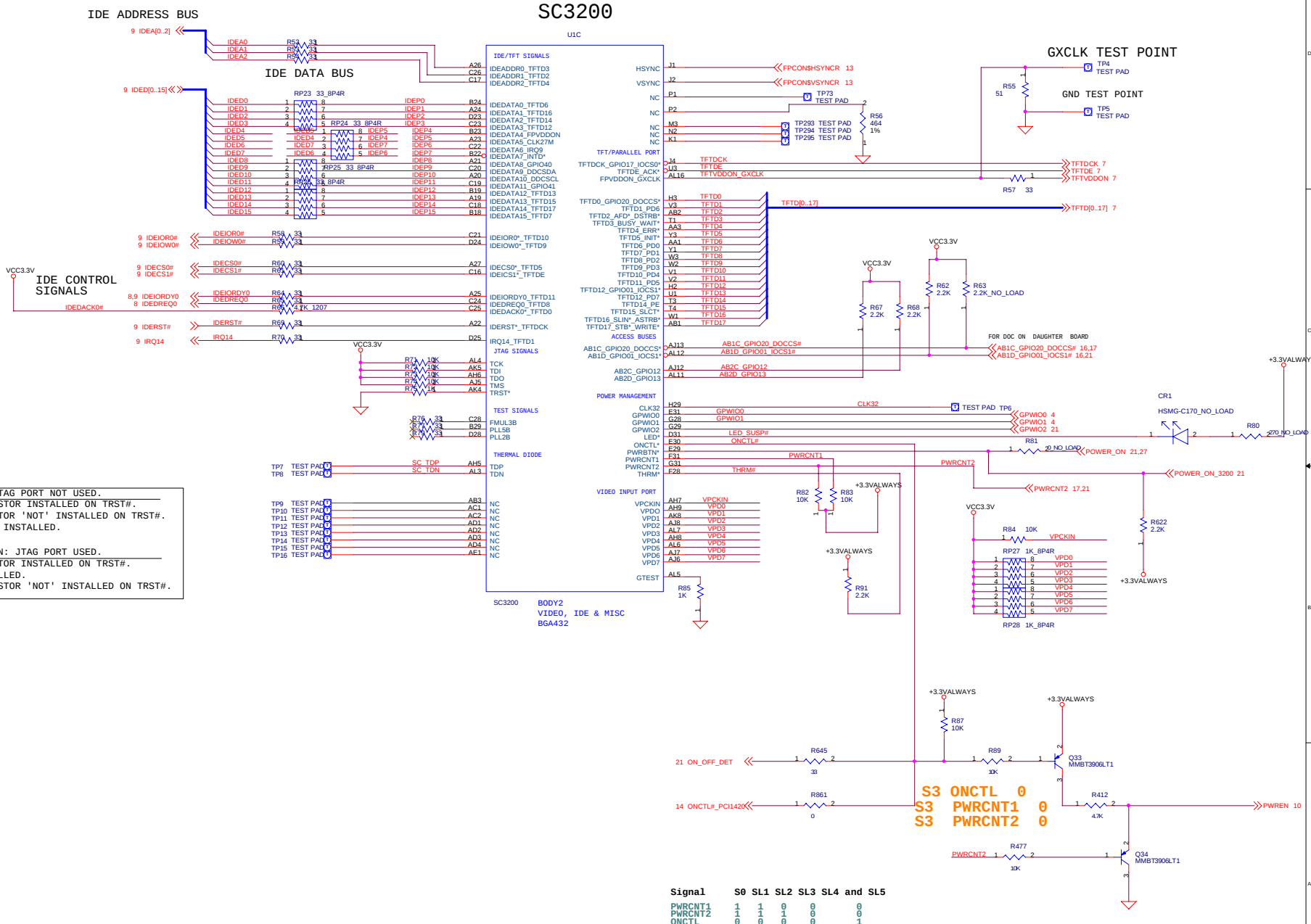


**USE TANTALUM OR LOW-ESR
ELECTROLYTIC (OSCON) CAPACITORS**



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SC3200 INTERFACES: TFT (NO PARALLEL), IDE, POWER MANAGEMENT, JTAG (WITH
HEADER), ACCESS BUS 1/2, CRT; TEMP SENSOR



SL3 Sleep State
In this state, SC3200 places the SDRAM in self-refresh mode, and then deasserts the PWCNT1 pin and the PWCNT2 pin. As a result, most of the system is powered off (except for the SDRAM).

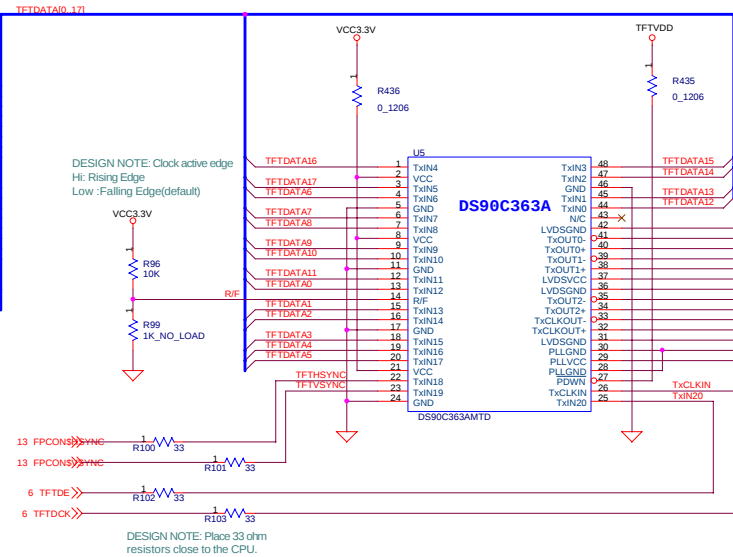
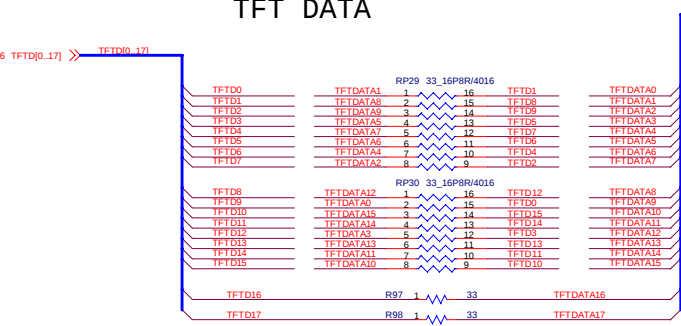
Title			
SC3200 TFT LCD I/F & IDE			
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LVDS TFT: CONTROLLER, INVERTER, AND CONNECTOR.

TFT DATA BUS LINES/CONNECTIONS	
TFTDATA[17..12]	: RS..R0 : TxIN[5..0]
TFTDATA[11..6]	: GS..G0 : TxIN[11..6]
TFTDATA[5..0]	: BS..B0 : TxIN[17..12]

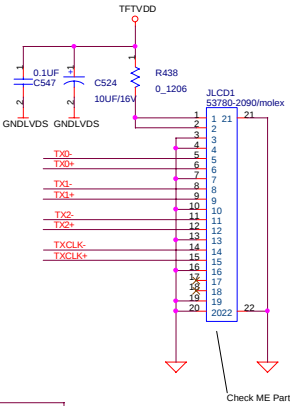
LVDS TFT CONVERTER/TRANSMITTER

TFT DATA



Single point connection.

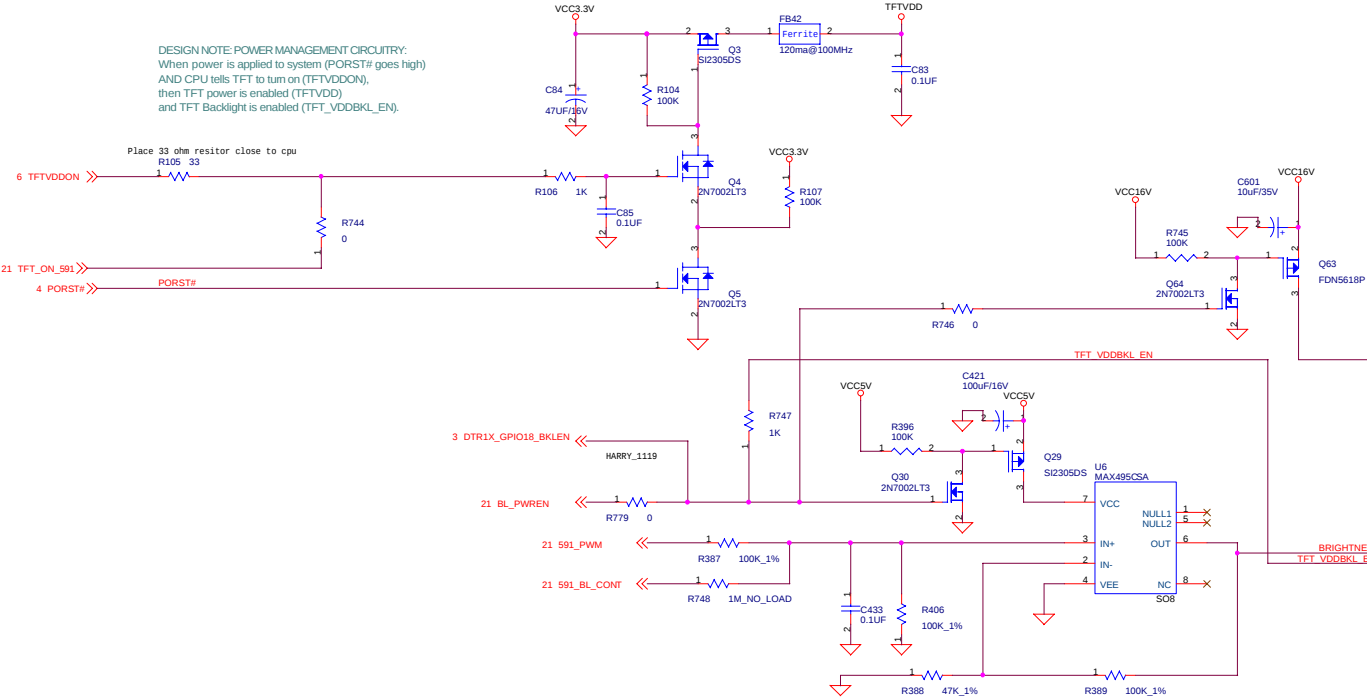
GENERIC TFT LVDS CONNECTOR



INVERTER CONNECTOR

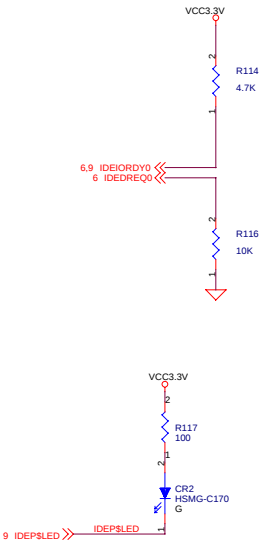
BACKLIGHT INVERTER CIRCUIT

DESIGN NOTE: POWER MANAGEMENT CIRCUITRY:
When power is applied to system (PORST# goes high)
AND CPU tells TFT to turn on (TFTVDDON),
then TFT power is enabled (TFTVDD),
and TFT Backlight is enabled (TFTVDDBLK_EN).



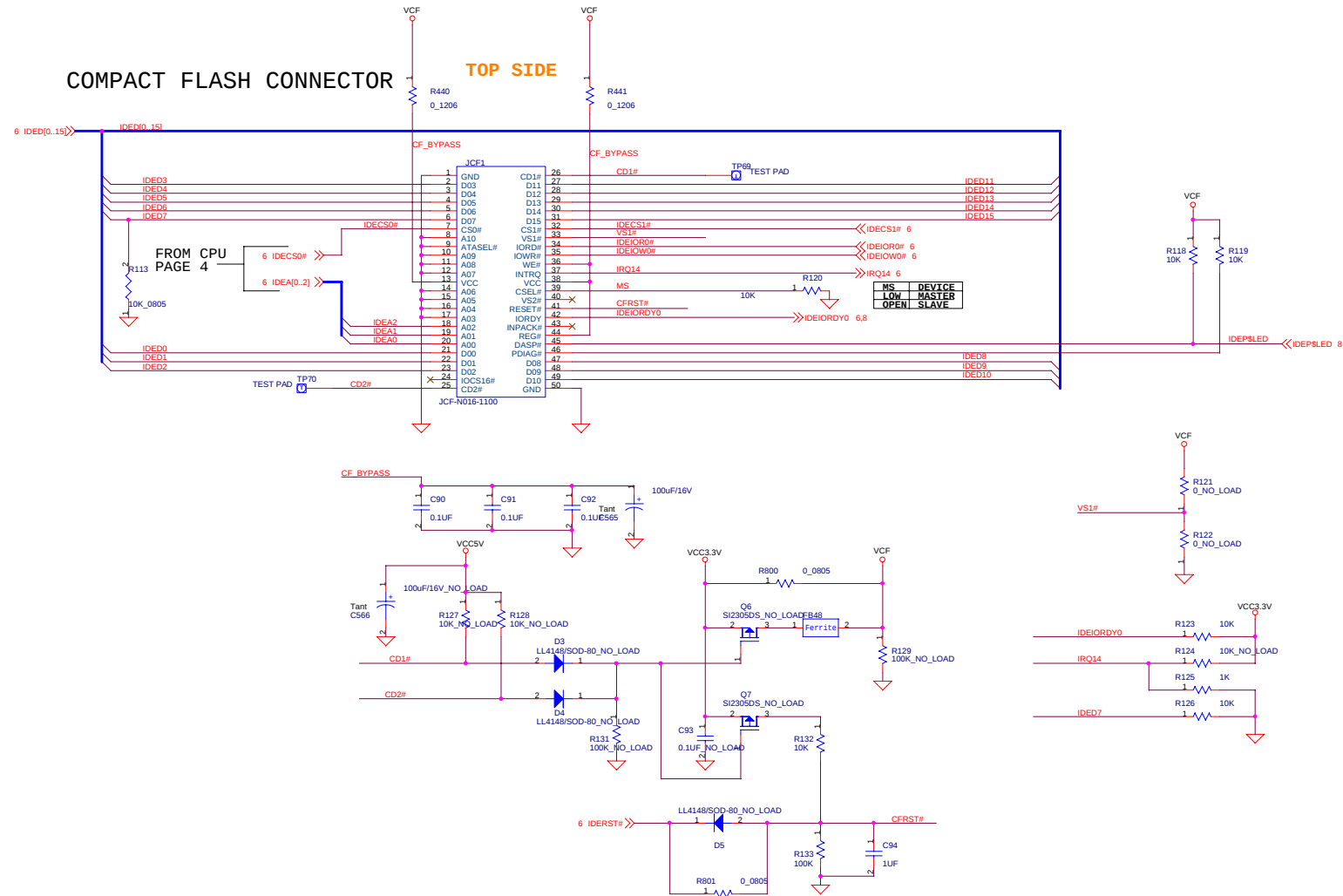
Title		LVDS & BACKLIGHT
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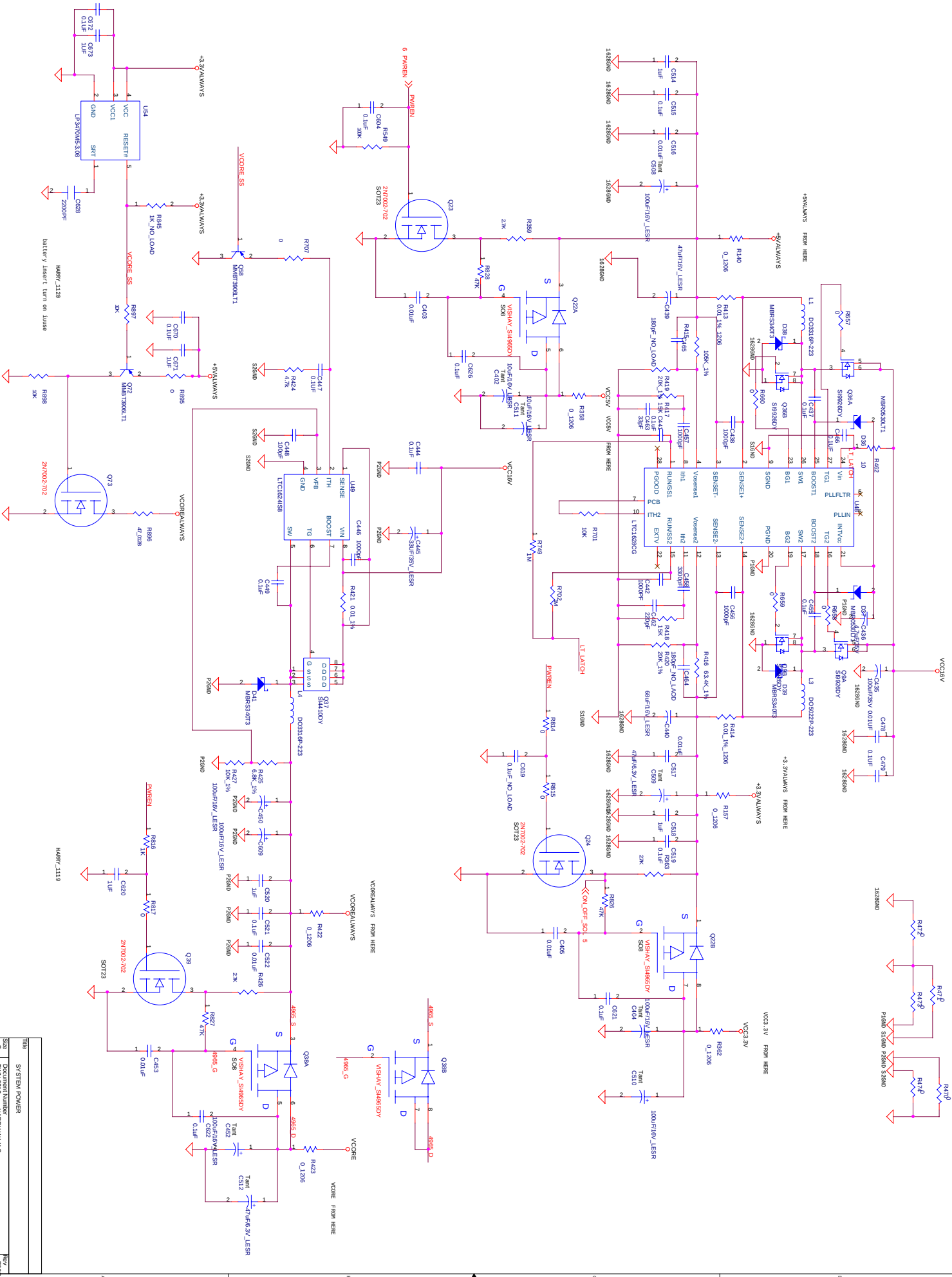
IDE: IDE INTERFACE AND CONNECTORS.



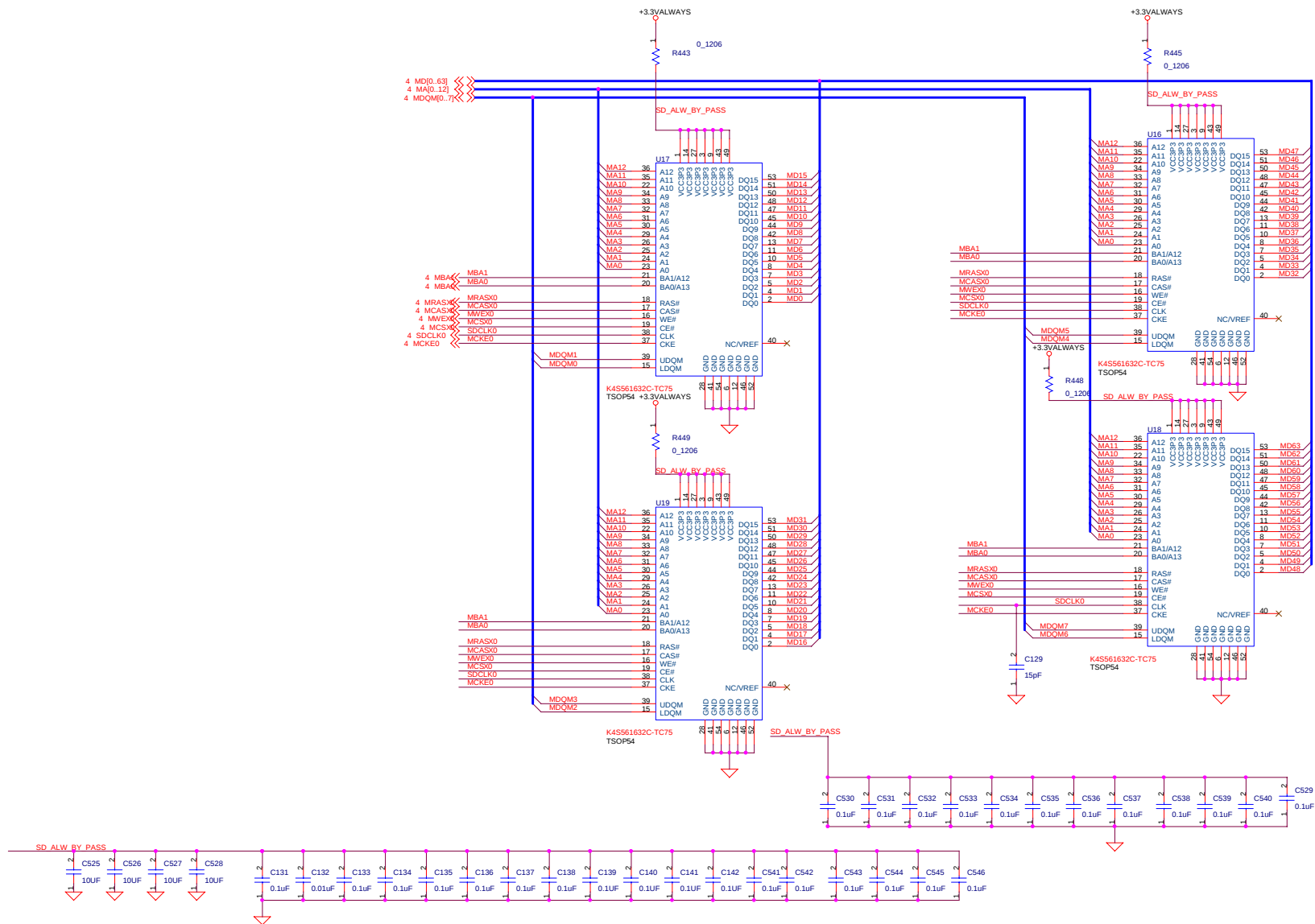
Title			
IDE I/F FOR DEBUG			
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COMPACT FLASH:





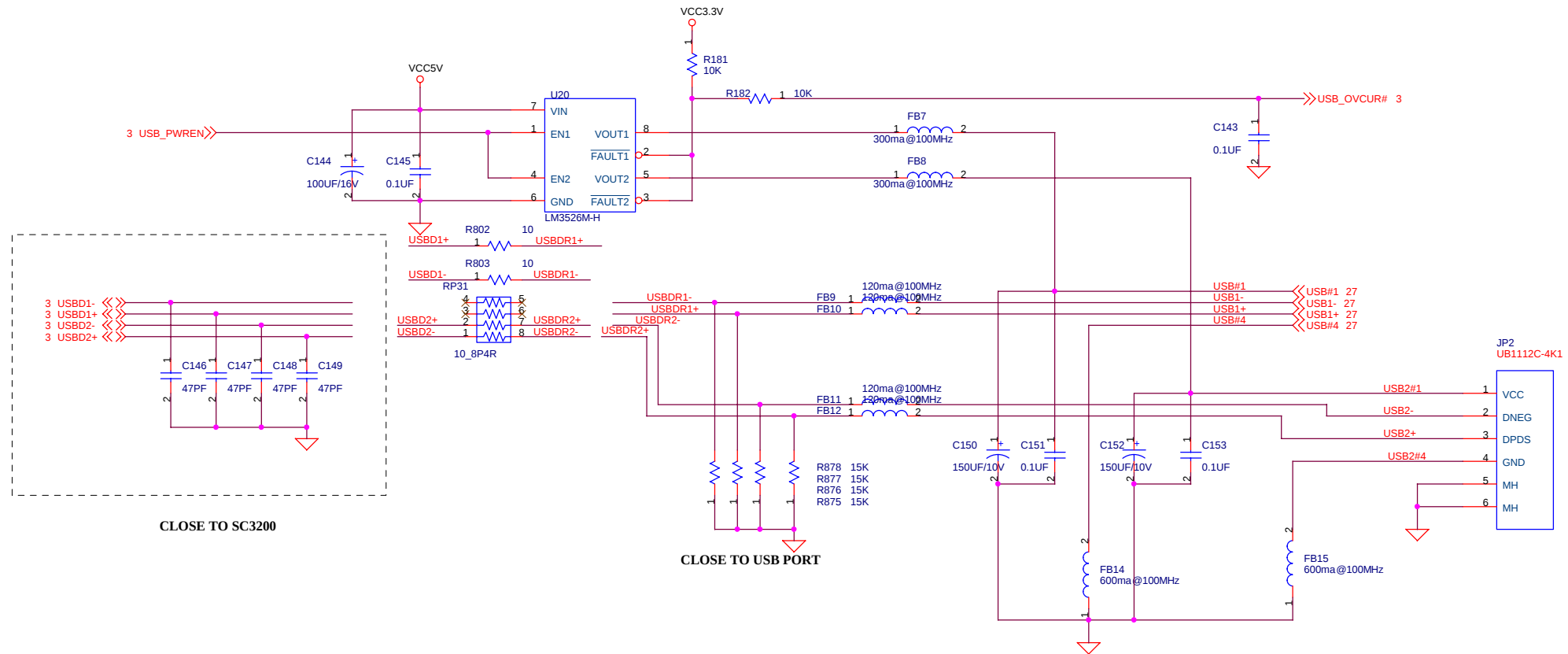
WEBCAD 16X16 K4S561632C-TC75



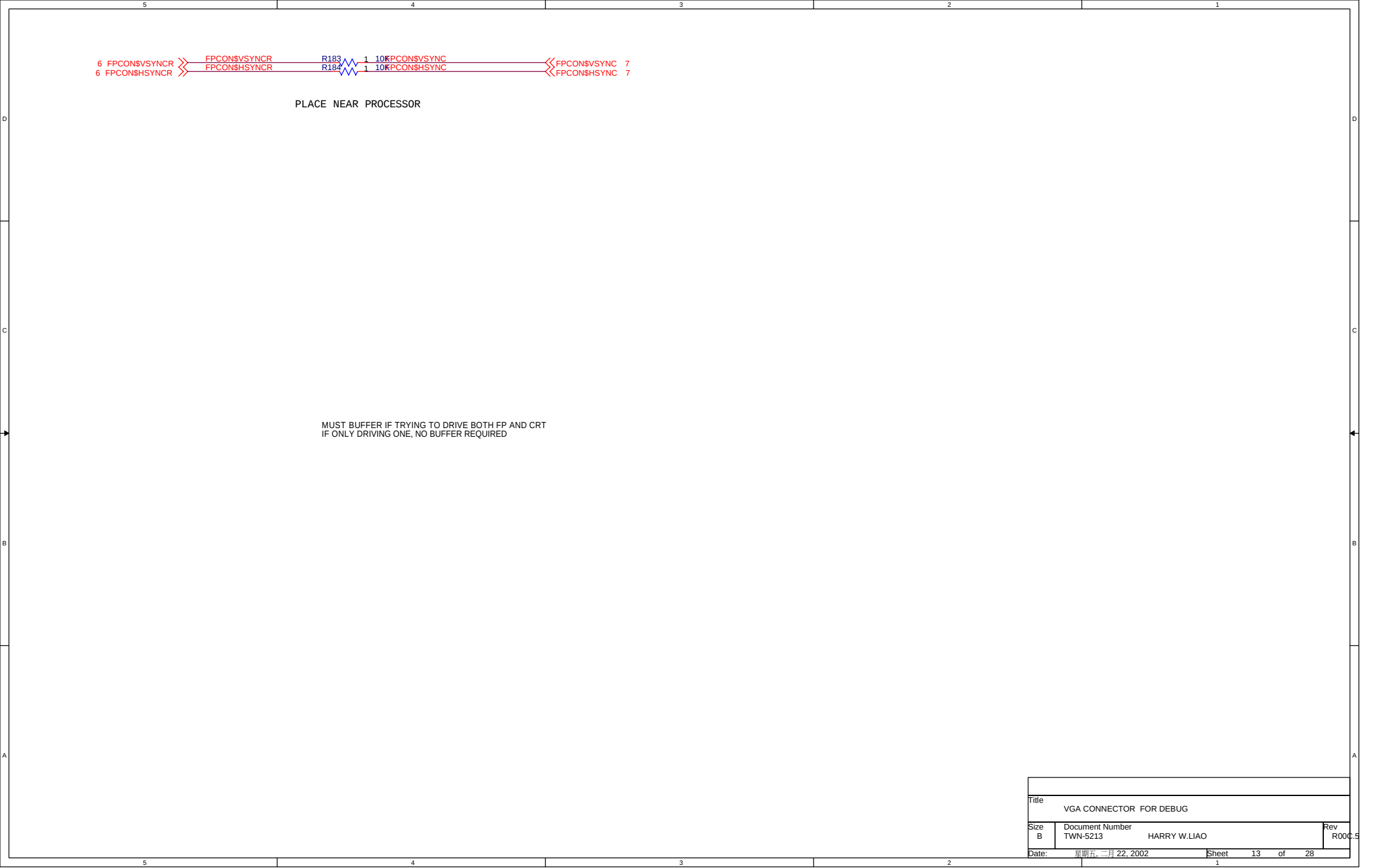
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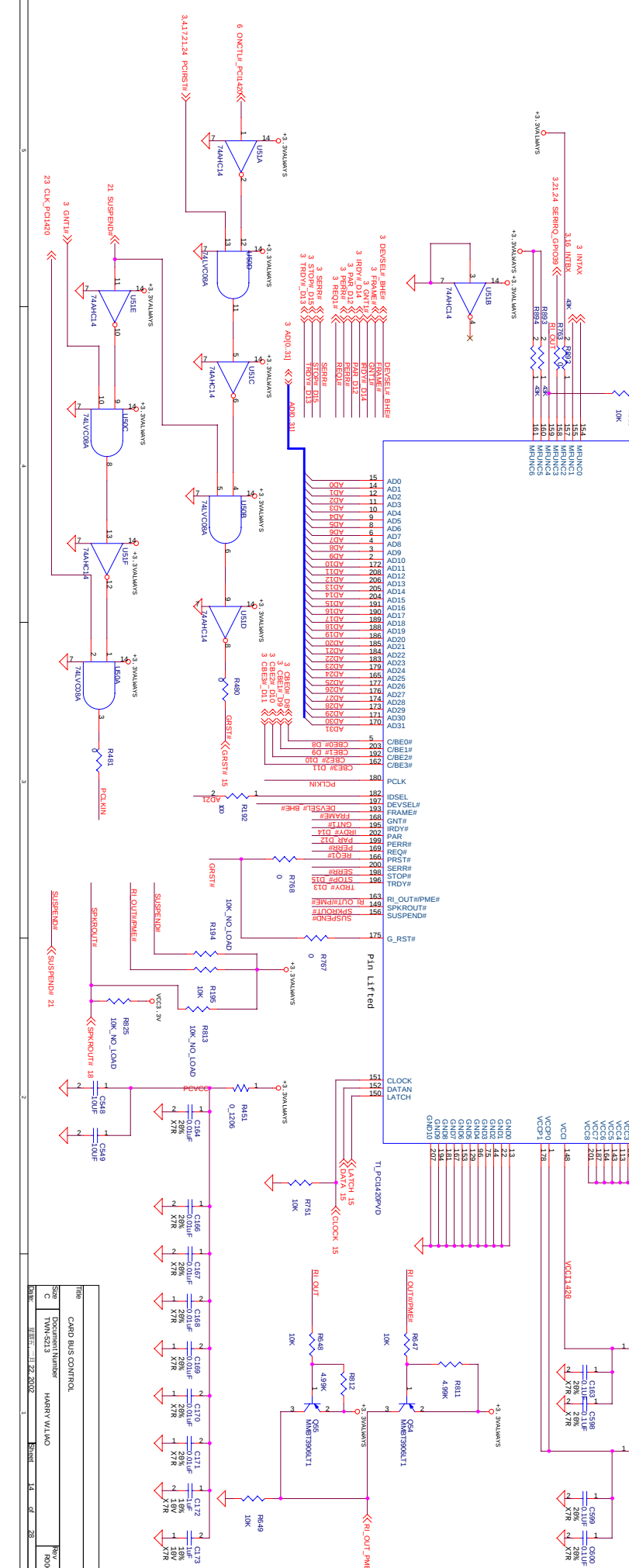
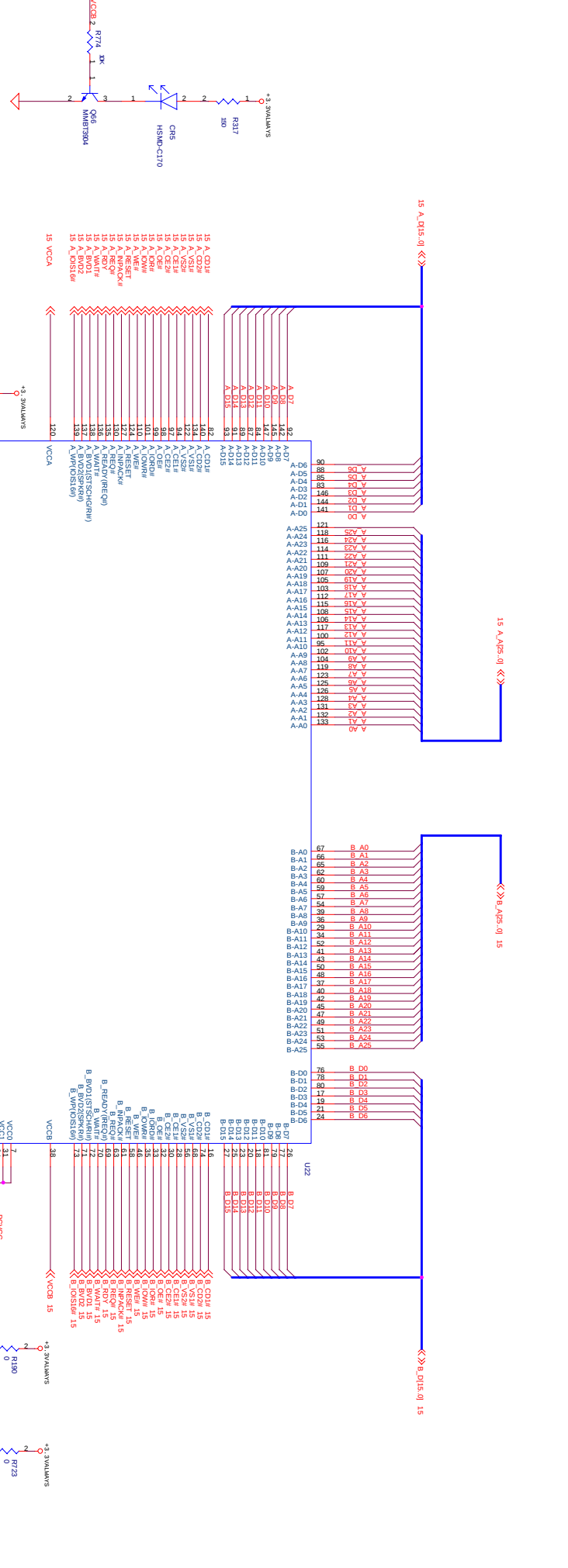
USB: INTERFACE AND CONNECTOR

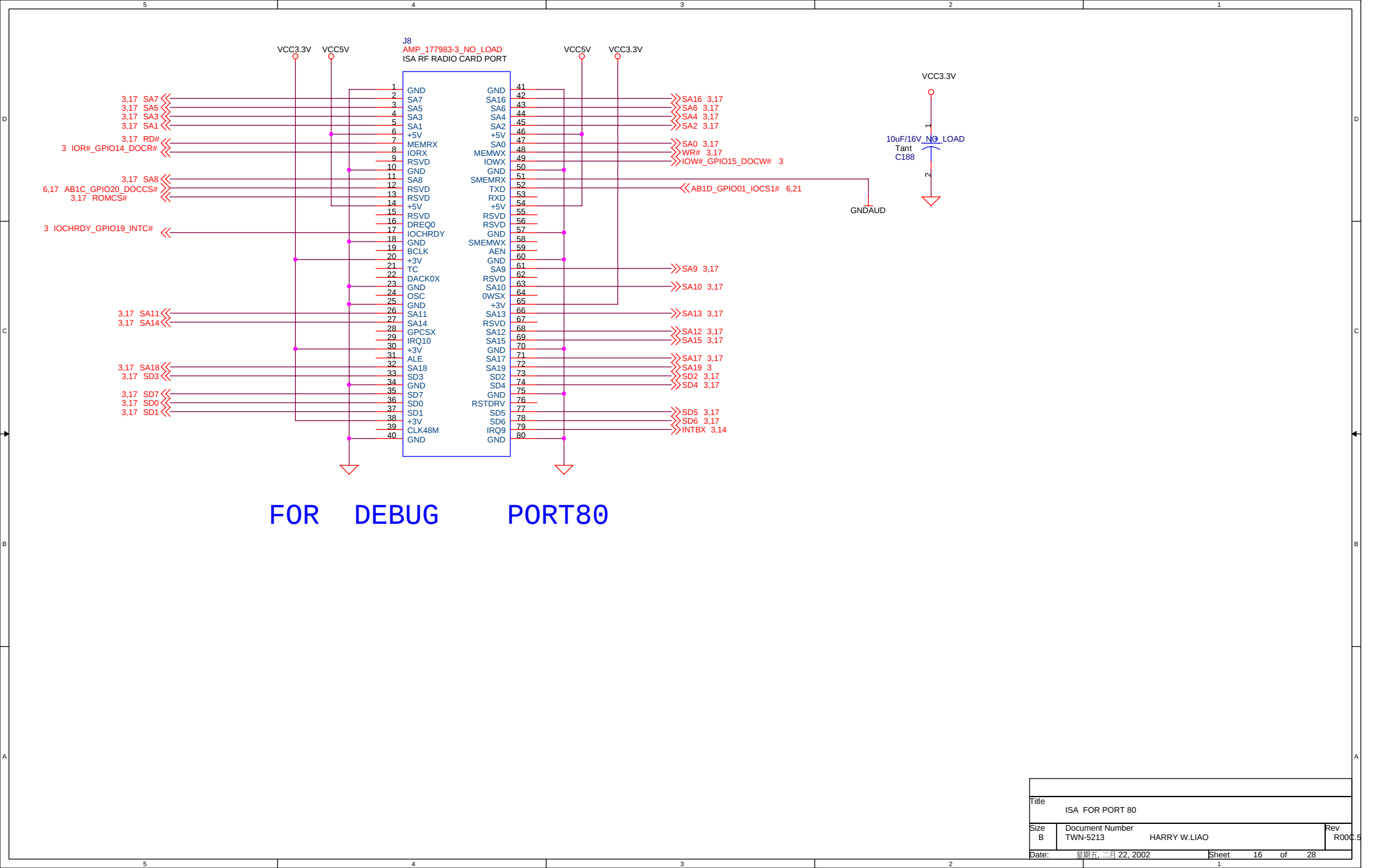
USB INTERFACE



Title			
USB PORT			
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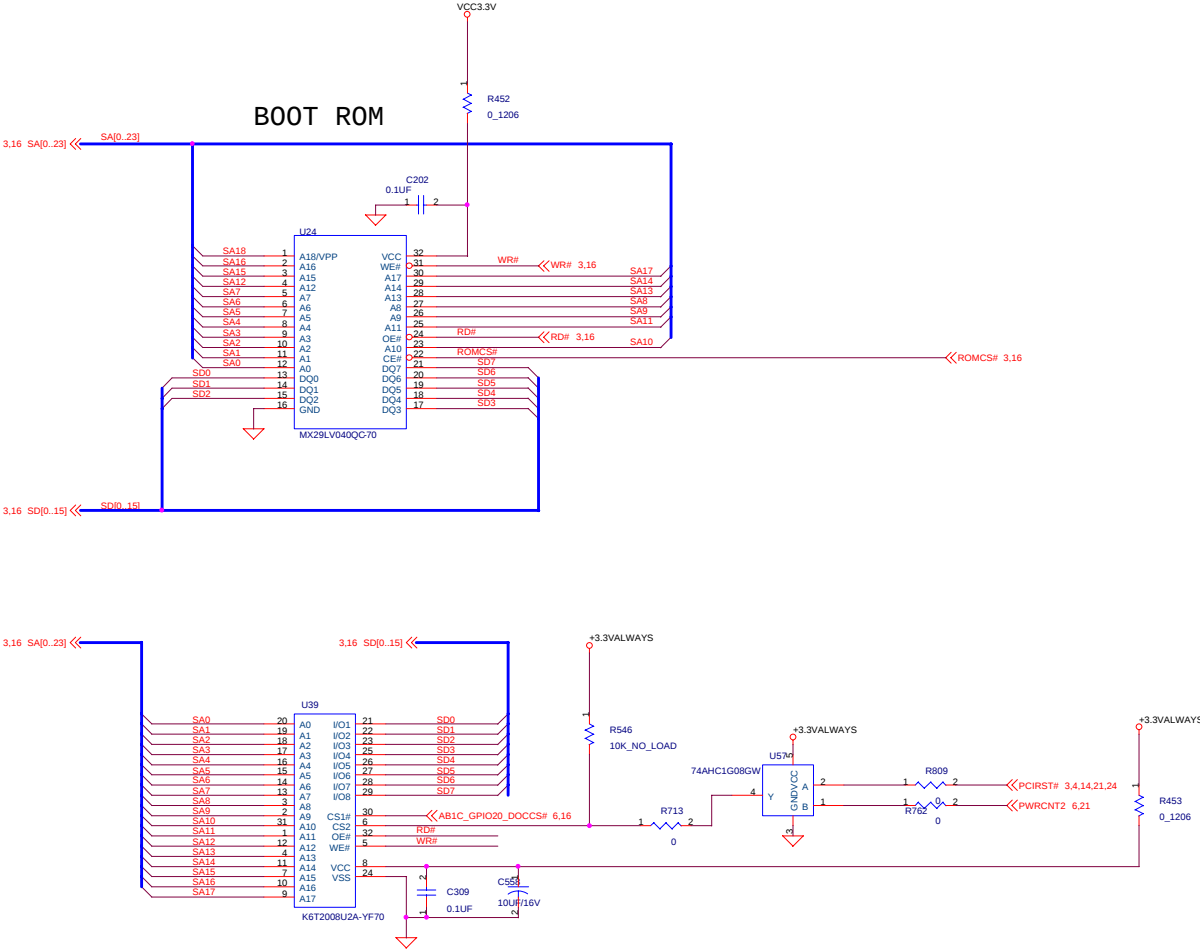


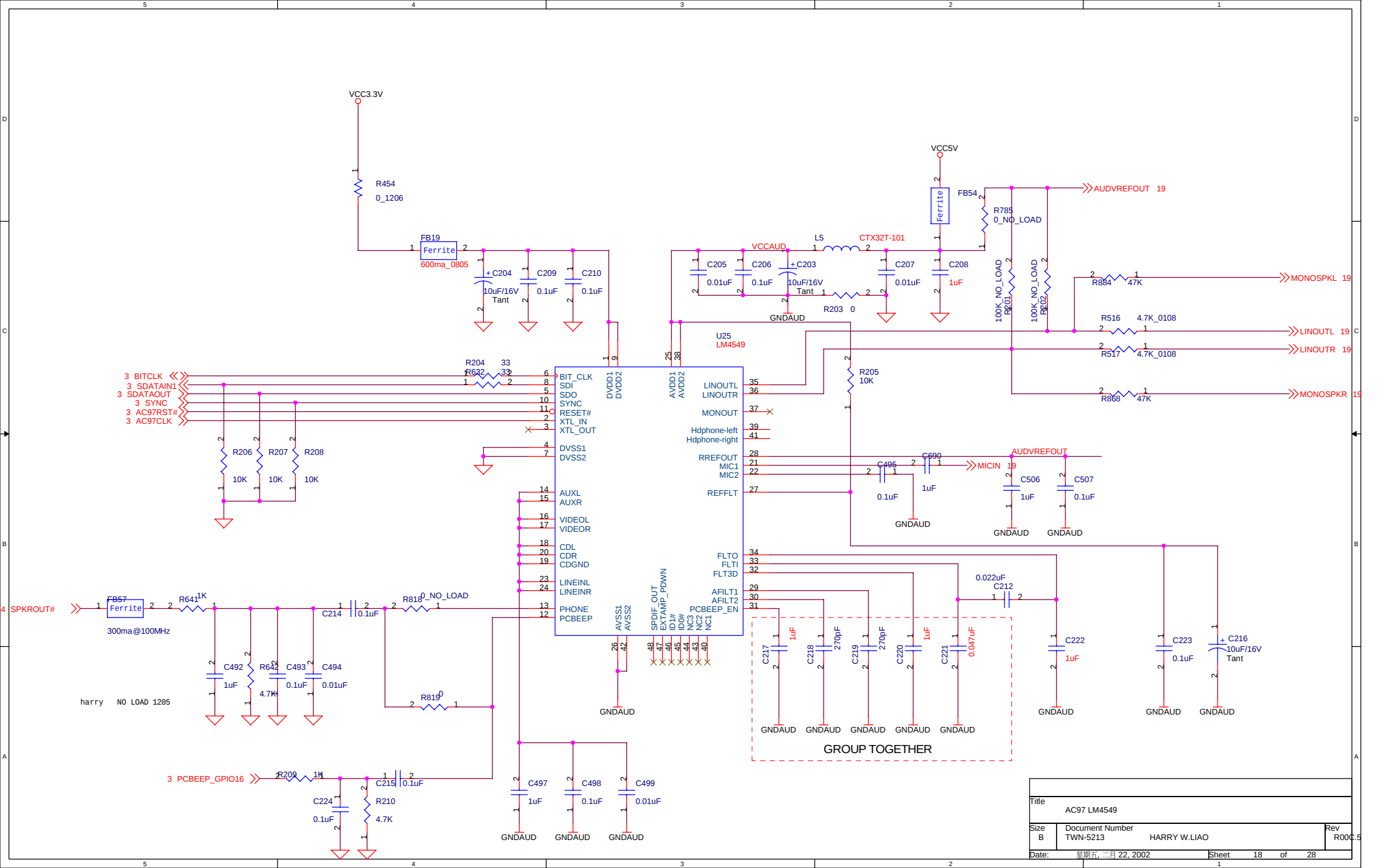




Title		
ISA FOR PORT 80		
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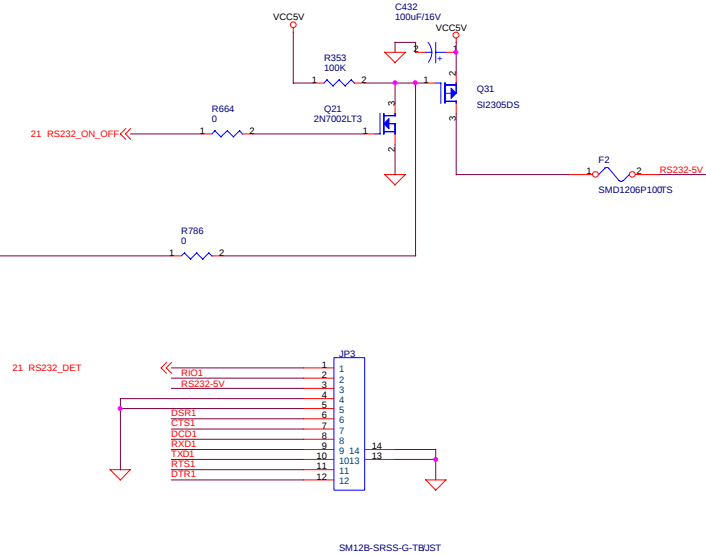
BOOT ROM + D.O.C.: ISA BOOT ROM AND DOC DEVICES, DOWSER HEADER, POLARIS HEADER





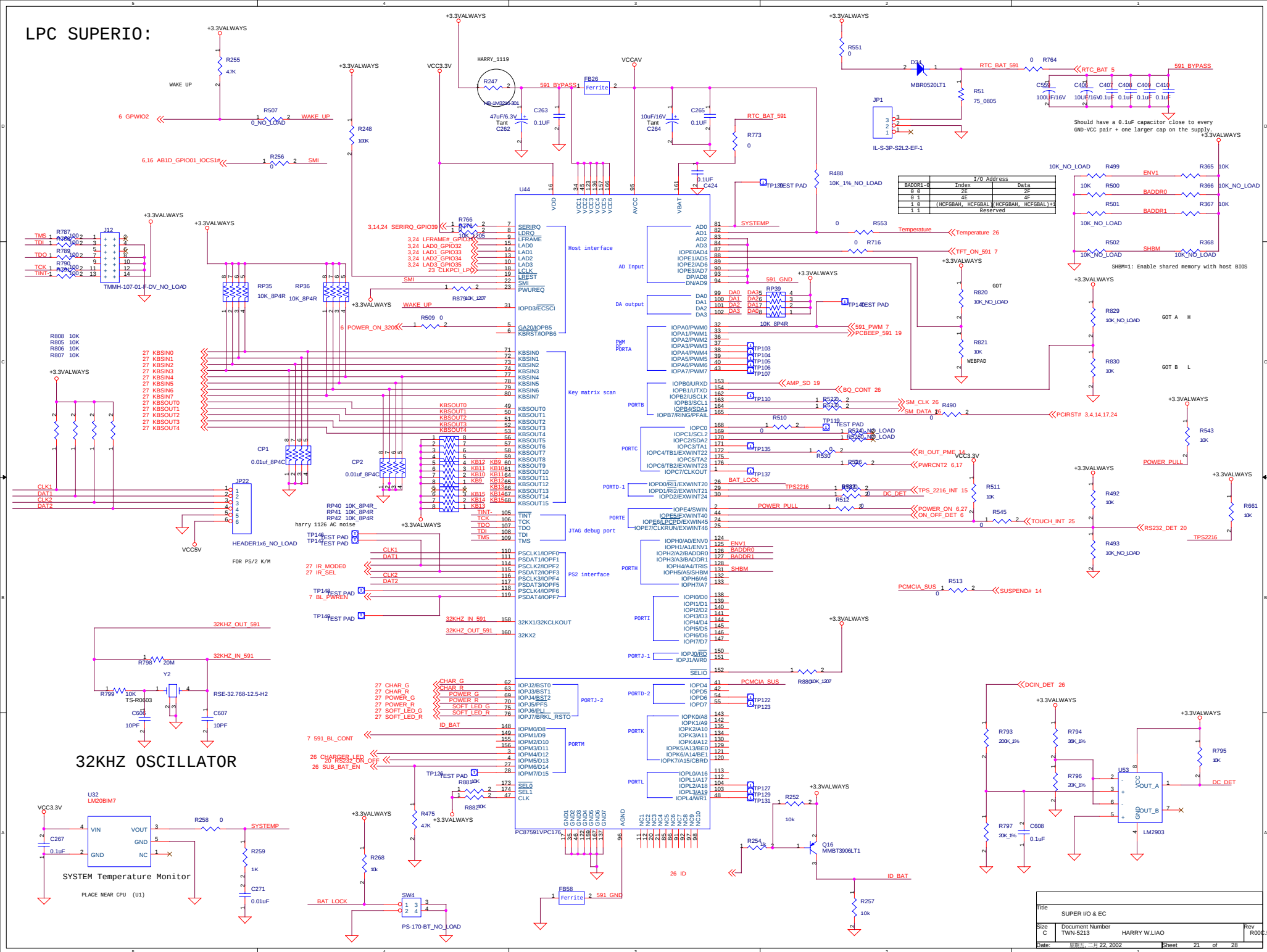
Title AC97 LM4549			
Size B	Document Number TWN-5213		Rev R000.5
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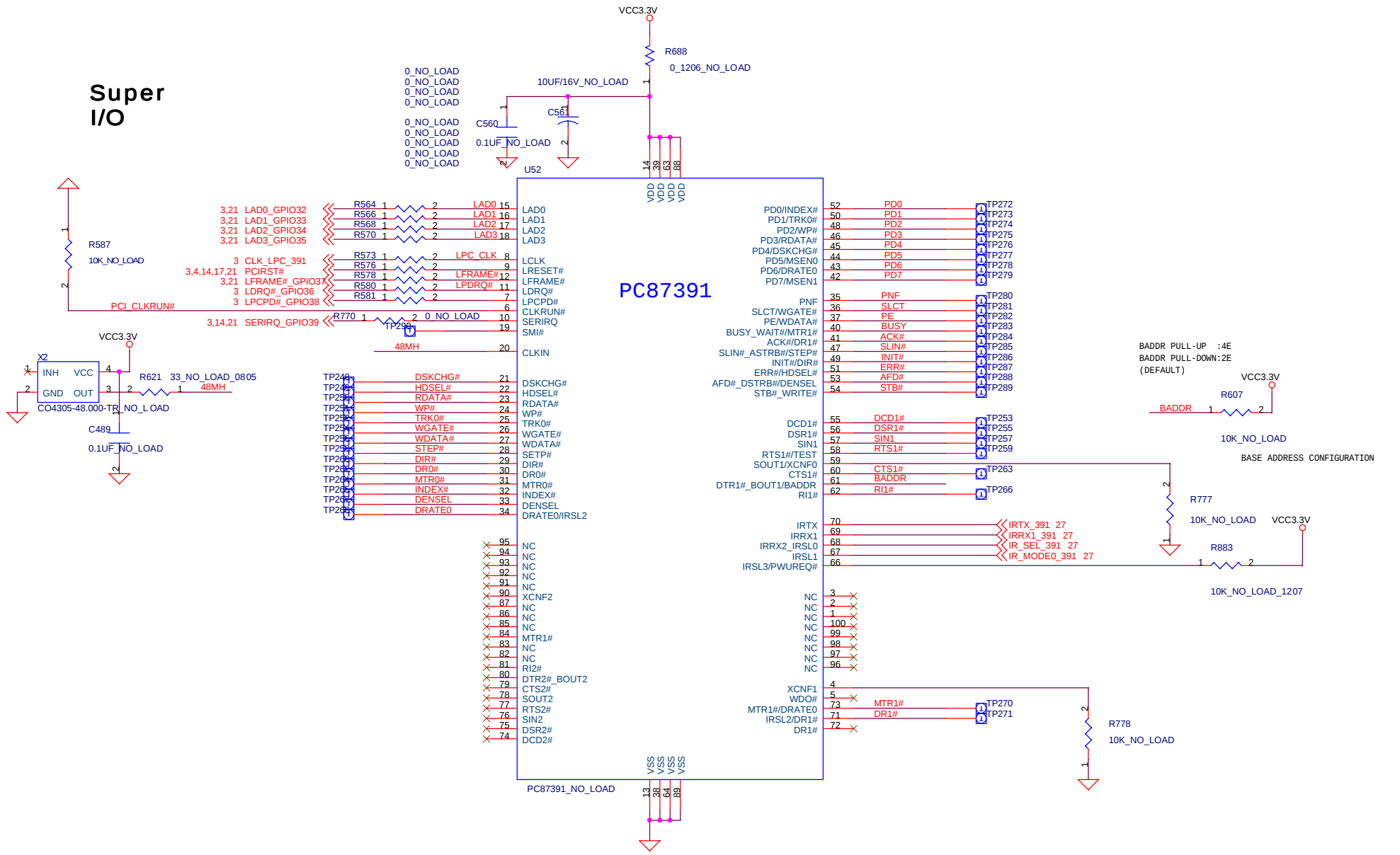
[illegible]

Title SERIAL PORT			
Size C	Document Number HARRY W.LIAO		Rev 900C.5
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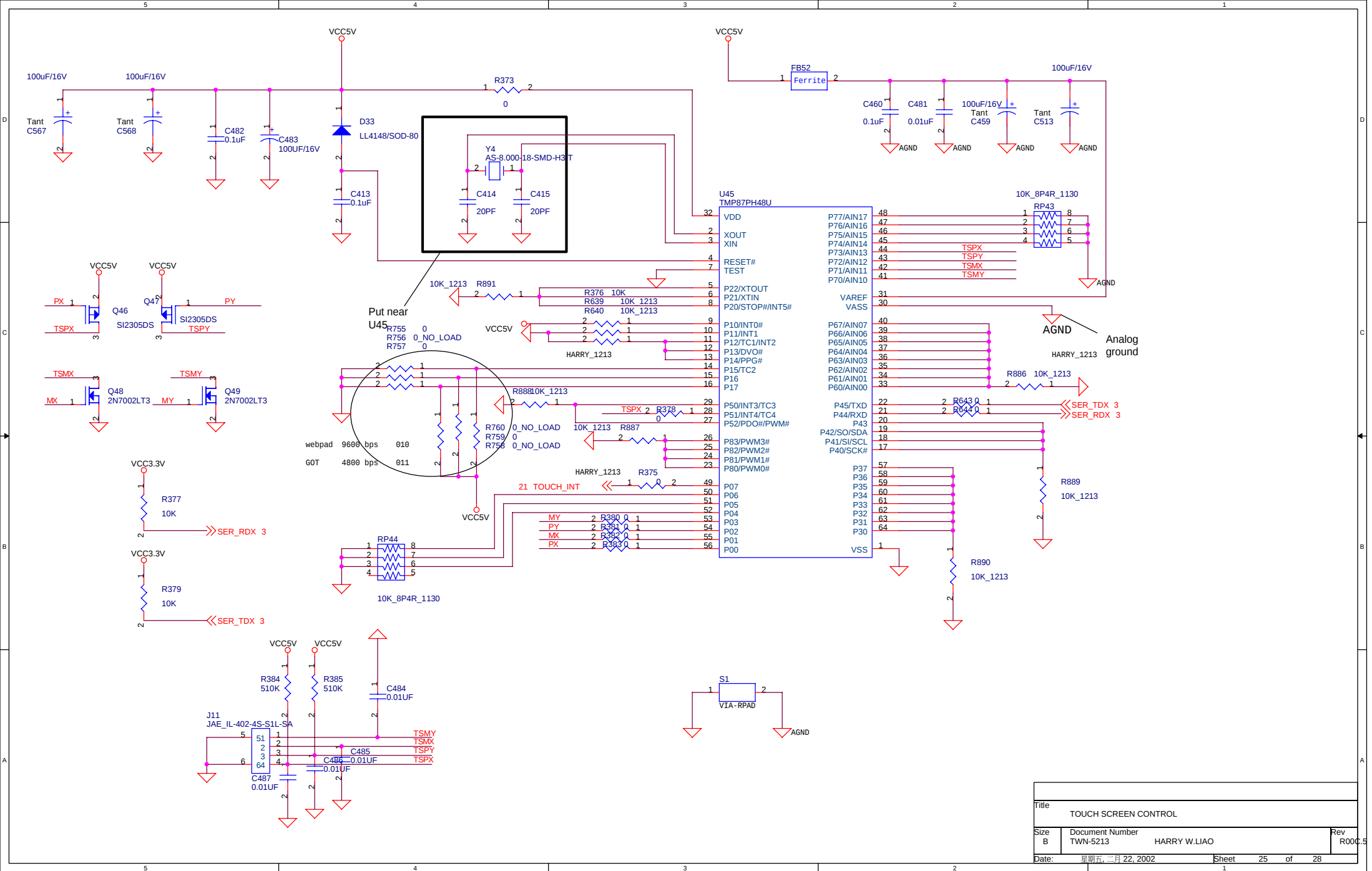
LPC SUPERIO:

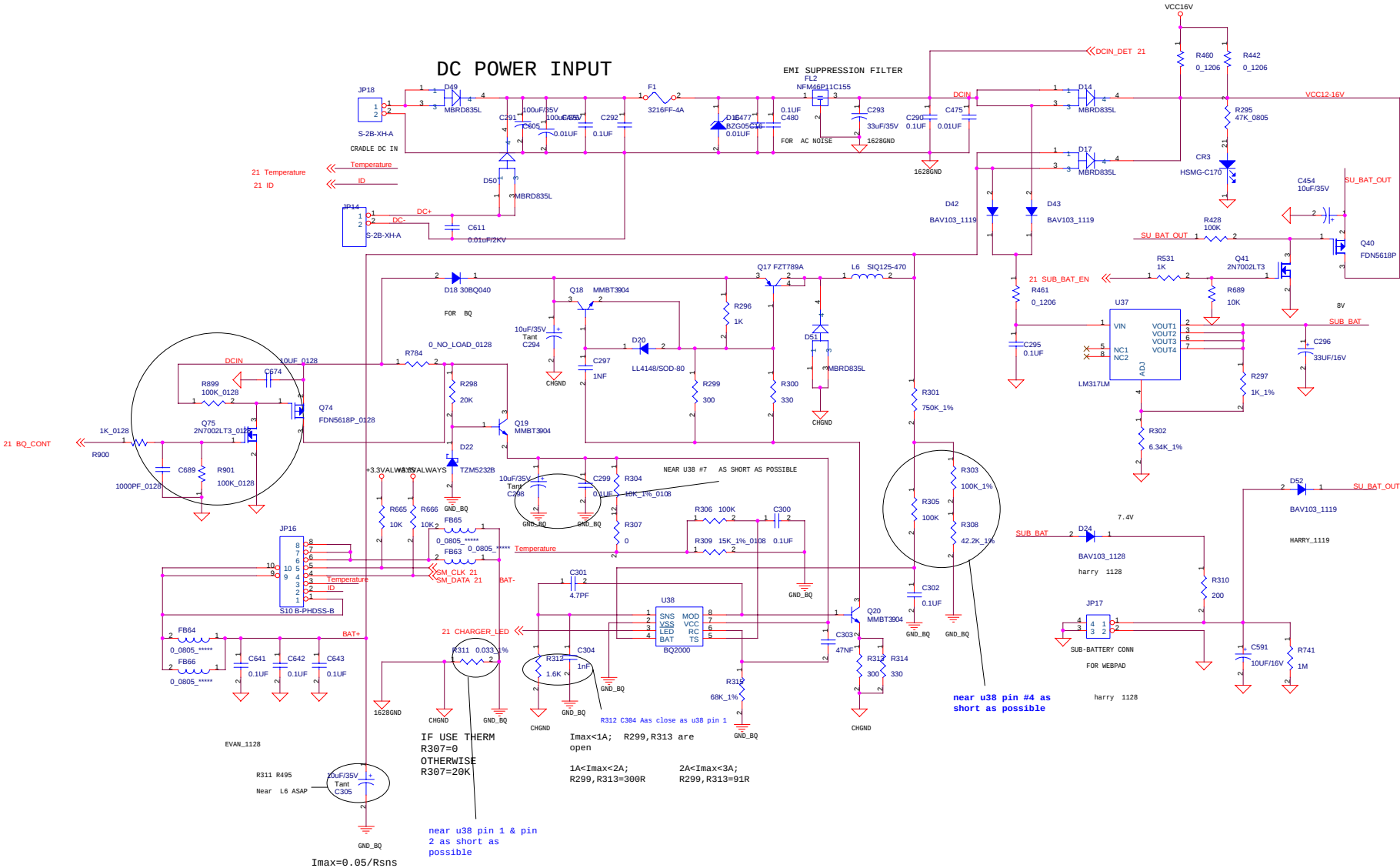


Super I/O

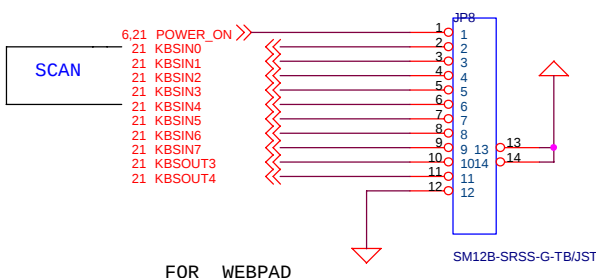


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PC87391 SUPER I/O				
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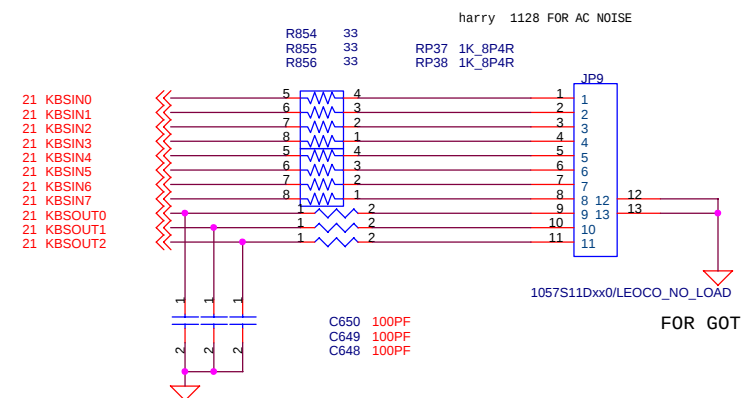


Title			
DC IN & CHARGER			
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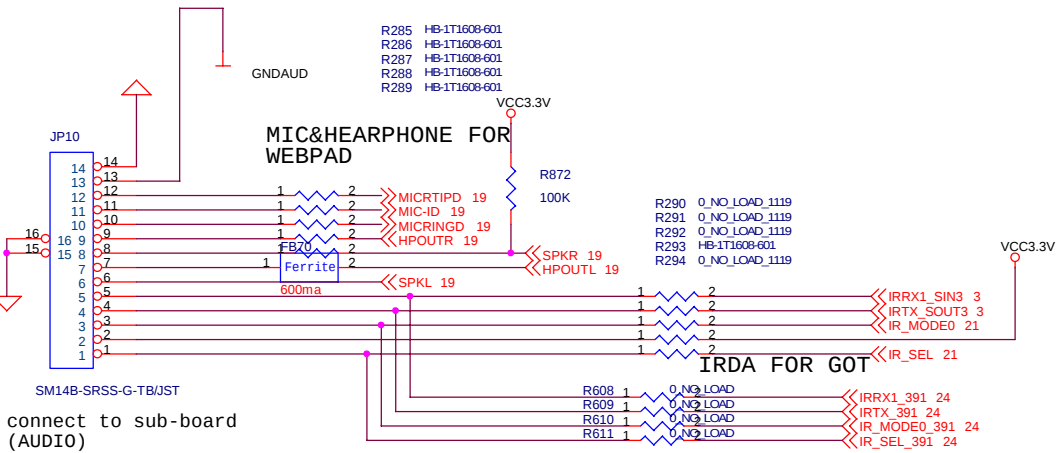


FOR WEBPAD

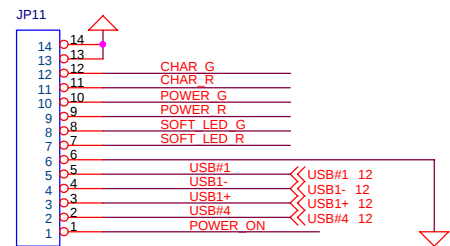
connect to sub-board
(key board)



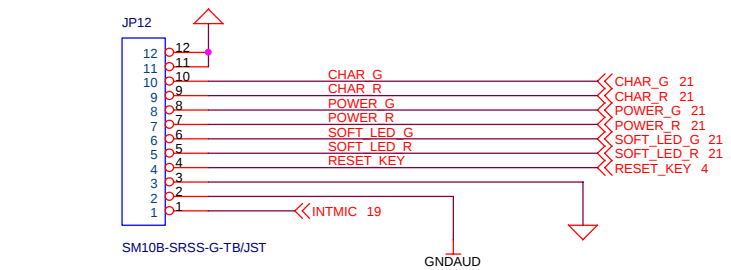
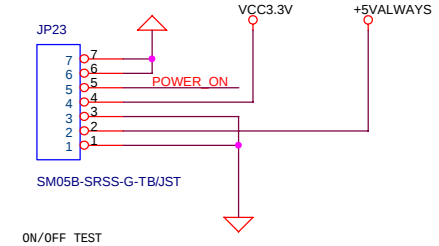
FOR GOT



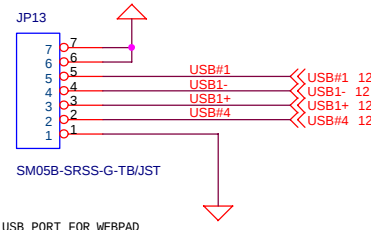
connect to sub-board
(AUDIO)



SM12B-SRSS-G-TB/JST_NO_LOAD
LED FOR GOT



connect to sub-board
(RESET \$ LED)



Title			
CONNECT FOR WEBPAD & GOT			
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	-----R00C-----		-----R00D-----1011		
	PAGE 3: Add R684,R691(33_0603); R743 (0_0603) PAGE 4: Modify R48(120k==>10k),C6,C7(12PF==>4PF) PAGE 4: Add R668(2.2k_0603) PAGE 5: Del R624,R626,R398,R400,R629(0_NL_0603) PAGE 5: Modify R547(0_0603==>0_NL) PAGE 5: Add C602(0.1uf_0603) PAGE 6: Del R623(10k_NL_0603);R503(10k_0603) PAGE 6: Del R653,R646(10k_0603);Q51(MMBT3906) PAGE 6: Modify R645 (0_0603==>33_0603) PAGE 7: Add R744,746 (0_0603);R406 (100K_0603) PAGE 7: Add R779(0_NL_0603) PAGE 7: Add R748(1M_NL_0603) PAGE 7 AddR745(100k_0603);C601(10uf/35V_CC7343) PAGE 7: Add Q64 2N7002 ,Q63 SI2305DS PAGE 7: Change LCD connect 53780-2090/molex PAGE 8: Modify U7,U8,U9 (SN74CBTD3861 ==>NL) PAGE 8: Modify C562,C563,C564(100UF/16V==>NL) PAGE 8: Modify C87,C88,C89(0.1UF==>NL);J4==>NL PAGE 9: Modify C556(100UF/16V==>NL);C93(0.1UF==>NL) PAGE 9: Modify R127,R128(10K==>NL) PAGE 9: Modify D3,D4(LL4148==>NL);R131,R129(100K==>NL) PAGE 9: Modify Q6,Q7(SI2305==>NL) PAGE 9: Add R800 ,R801(0_0805) PAGE 10 Add C604(0.1uf_0603);R707(0_NL);R708(10K_NL) PAGE 10 Add Q58(MMBT3906_NL);R701(10K_0603);R702,R749(1M_0603) PAGE 10 Add R706(0_1206) PAGE 10 Modify R421(0.01_1%==>0.033_1%_1206) PAGE 10 Del Q27(SI4965ADY);D44,D45 (LL4148);R533(100),R534(100K) PAGE 10 Modify C458 (1000PF==>3300PF);C462(33PF==>220PF) PAGE 10 Del D40(MBR0530);R550;R548(100K) PAGE 12 Add R802,R803 (10_0603); PAGE 14 Modify R194 (10K_0603==>NL);U51(74LVC04A==>74AHC14) PAGE 14 Add R763(0_0603),R709(100K_1%_NL),C596(0.1UF_0603_NL) PAGE 14 Add D48(LL4148_NL);R804(0_0603_NL);R768,R767(0_0603_NL) PAGE 14 Modify R317(270==>150); PAGE 14 Add R774(10K_0603),Q56(MMBT3904);R811,R812(4.99K_0603) PAGE 14 Add R723(0_0603);C599,C600(0.1UF_0603) PAGE 14 Del R193(10K_0603) PAGE 15 Add R731,R732(0_0805); PAGE 17 Modify R546(10K_0603==>NL) PAGE 17 Add R713,R809,R762(0_0603) PAGE 18 Add R785(0_NO_LOAD_0603) PAGE 19 Add R753,754(10K_0603) PAGE 19 Modify R520(10K_NO_LOAD==>10K) PAGE 19 Del R630,C490,C491,R631,Q50 PAGE 20 Add R786(0_0603) PAGE 21 Add R805,R806R807,R808(10K_0603) PAGE 21 Add R787,R788,R789,R790,R791 (0_0603) PAGE 21 Add U53(LM2903);R797,R796(20K_1%_0603) PAGE 21 Add R793(200K_1%_0603);R794(36K_1%_0603) PAGE 21 Add C608(0.1UF_0603);R795(10K_0603) PAGE 25 Add R755,R756,R758(0_NO_LOAD_0603) PAGE 25 Add R757,R759,R760(0_0603) PAGE 25 Modify FB49==>VIA-RPAD PAGE 26 Modify D49,D50,D51(MBRS340T3==>MBRD835L) PAGE 26 Modify F1(RLD30P250U==>3216FF_4A) PAGE 26 DEL D21(LL4148);ADD R784(0_0603);D23(MBRD835L) PAGE 26 ADD R689(10K_0603);R810(47K_0603) PAGE 26 DEL C454(100UF/16V_7343)		PAGE 4 Add c612 22PF_0603_NO_LOAD FOR EMI PAGE 6 CR1 HSMG-C170==>NO_LOAD,R80 270==>NO_LOAD PAGE 8 Modify R112 470_0805==>NO_LOAD PAGE 10 Add R814,R816 47K_0603;R815,R817 0_0603;C620,C619 0.1UF_0603;Modify R421 0.033=>0.01_1%_1206;ADD C609 100UF/16V_LESR PAGE 10 Modify C405 0.01UF==>0.1UF_0603;R707 0_NO_LOAD==>0_0603;R708 10K_NO_LOAD==>10K_0603; PAGE 10 Modify Q58MMBT3906_NO_LOAD==>MMBT3906;C442 0.1UF==>1000PF_0603;C447 560PF==>0.1UF_0603 PAGE 10 Modify R512 10uf/16v_3528==>47uf/6.3v_LESR_3528 PAGE 10 Add C621,C622 47UF/16V_LESR CC6032;Modify C452, 10UF/16V_LESR==>100UF/16V_LESR CC7043 PAGE 11 DEL R444,R446,R447,R450 0.05_1%_1206;Del C130,C552C553,C554,C555 100UF/16V CC7343 PAGE 11 Modify R443,R445,R449,R448 0.05_1%_1206==>0_1206 PAGE 12 Modify RP31 27==>10_8P4R PAGE 13 D10,D11,D12 BAV99==>NO_LOAD;FB16,FB17,FB18 HB-1T2012-121==>NO_LOAD;J5 MMT-106-02-S-H==>NO_LOAD PAGE 13 C157,C158,C159,C160,C161,C162 33PF_0603==>NO_LOAD;R185,R186 33_0603==>NO_LOAD PAGE 13 Q13,Q14 2N7002==>NO_LOAD;C155,C156 100PF_0603==>NO_LOAD;R187,R188,R189 75_0603==>NO_LOAD PAGE 14 Add R813,R825 10K_0603_NO_LOAD PAGE 16 Modify C188,C195 10UF/16V_CC3528==>NO_LOAD;C189,C190,C191,C192,C196,C197,C198,C199 0.1UF_0602==>NO_LOAD, PAGE 16 Modify C193,C200 0.01UF_0603==>NO_LOAD;C194,C201 1NF_0603==>NO_LOAD PAGE 19 Add R818 0_0603_NO_LOAD ,R819 0_0603 PAGE 19 Modify R520 10K_0603==>NO_LAOD,R411 10K_0603==>100; PAGE 20 ADD C610 0.47UF_0603 ; PAGE 23 Add R820 10K_0603 ,R821 10K_0603_NO_LOAD PAGE 23 ADD C613 10PF_0603;C614,C615,C616,C617==>10PF_0603 PAGE 23 Add R822,R823,R824 10K_0603_NO_LOAD;C623,C624,C625 10PF_0603_NO_LOAD PAGE 23 Add FB59 300Ma@100MHz HB-1T2012-601 PAGE 26 ADD D18 30BQ040;C454 10UF/35V_7343;D52 LL4148; PAGE 26 DEL R810 47K_0603 PAGE 26 Modify T1 CTX0_47_2P==>FL2 NFM46P11C155		
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			Title UPDATE NOTE		
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