

FRS Circuit Description

Model: 1050

Transmitter Section

RF Power Amplifier and Spurious Suppression

RF signal is amplified by FET transistor Q5. The max. power is fed to antenna through the low pass filter (C68, C69, L16, C72, L17 and C73). The spurious will be suppressed by the low pass filter.

PLL circuit

There is a voltage controlled oscillator (VCO) that is generated by RF transistors Q2 & Q3 as the transmit frequency. This VCO frequency is locked and controlled via a phase lock loop (PLL) circuit of U1.

Modulation

Frequency modulation (FM) of the transmit VCO is accomplished by superimposing the incoming audio signal on the PLL control voltage. IC U304c amplifies the audio signal as a pre-amplifier.

Maximum Modulation Limiter

The voltage limiter of U301b will amplify the audio signal from pre-amplifier and keep the output deviation less than 2.2KHz and then the audio signal will be fed to VCO through the low pass filter U301a.

Receiver circuit

The receiver adopts a double conversion super-heterodyne architecture with a first IF of 21.7MHz and a second IF of 450KHz. A signal transistor (Q10) circuit is used as LNA amplifier and first mixer (Q7). In order to enhance selectivity and FM demodulation this first IF signal is passed through the crystal filter (F2) and then is mixed down to the second IF. The second mixer, second local oscillator (X1, U1-pin9, C43), all IF amplification, demodulator (T1) and squelch (D1) function are provided by the IC U2.

Volume Control

There are 8 stages audio signal level can be adjusted (R352, R353 and R354) by key button and controlled by MCU (U300).

Power Audio Amplifier

The FM demodulation signal will be input to power amplifier U302 and converted to voice through speaker.