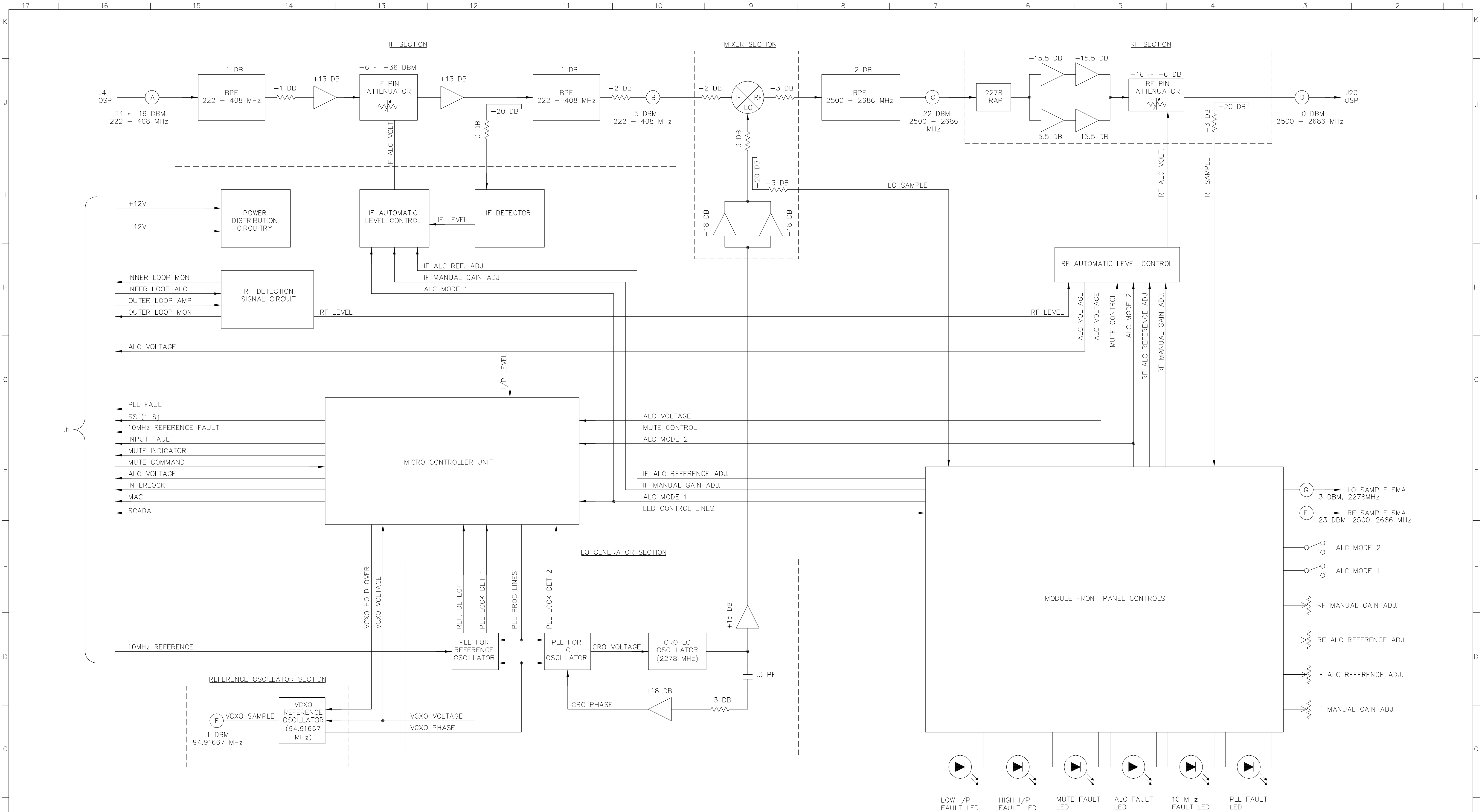


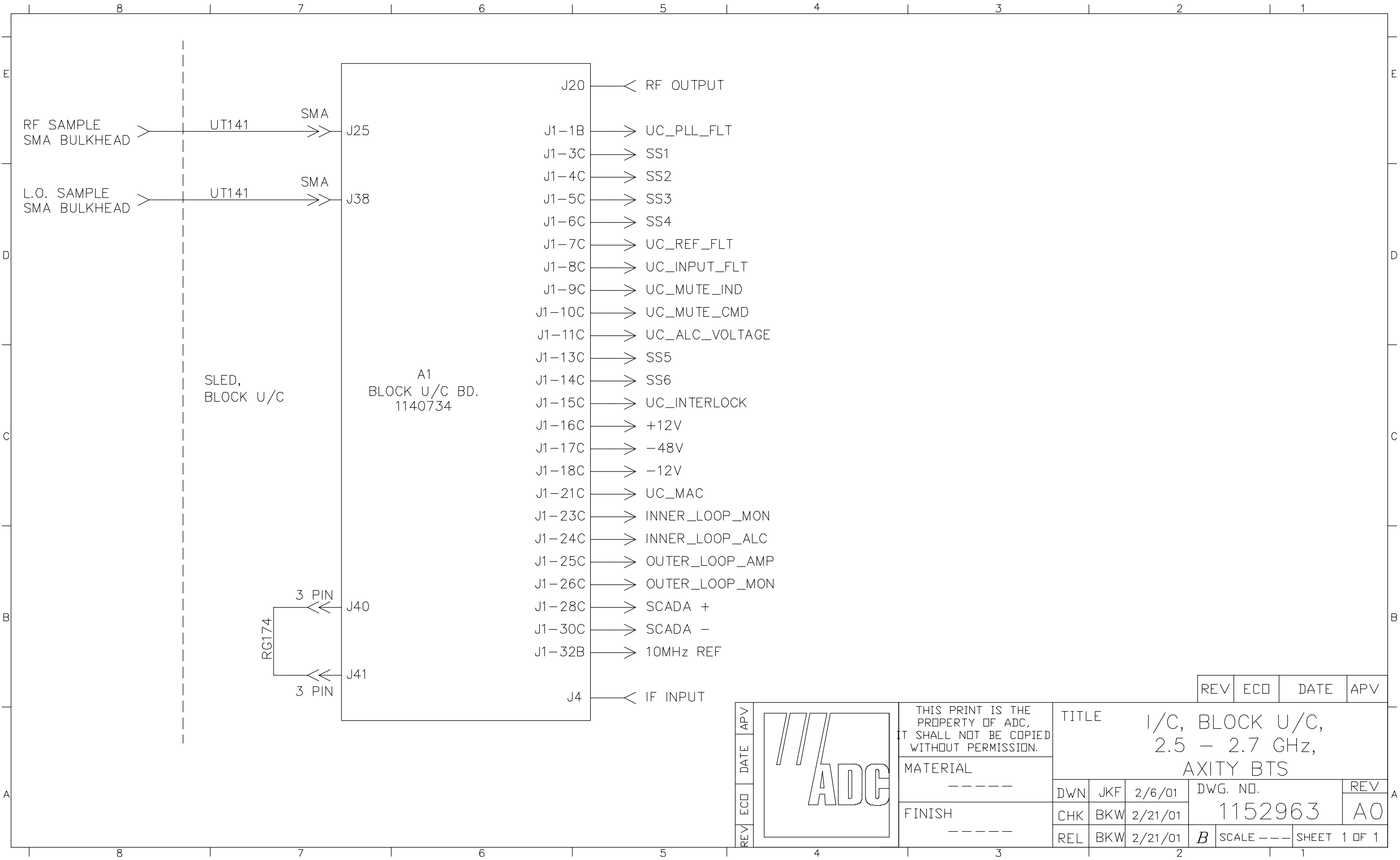
ADC

TELECOMMUNICATIONS

EXHIBIT VIII

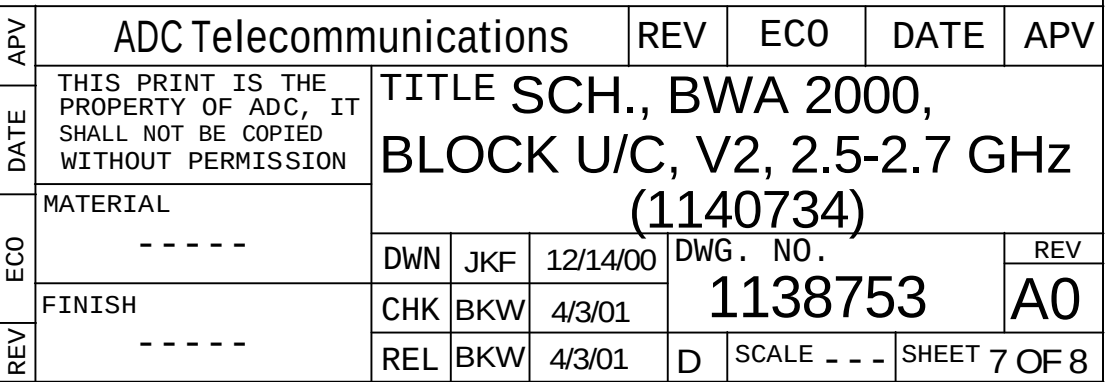
SCHEMATICS Part 2 of 2 BTS-7010

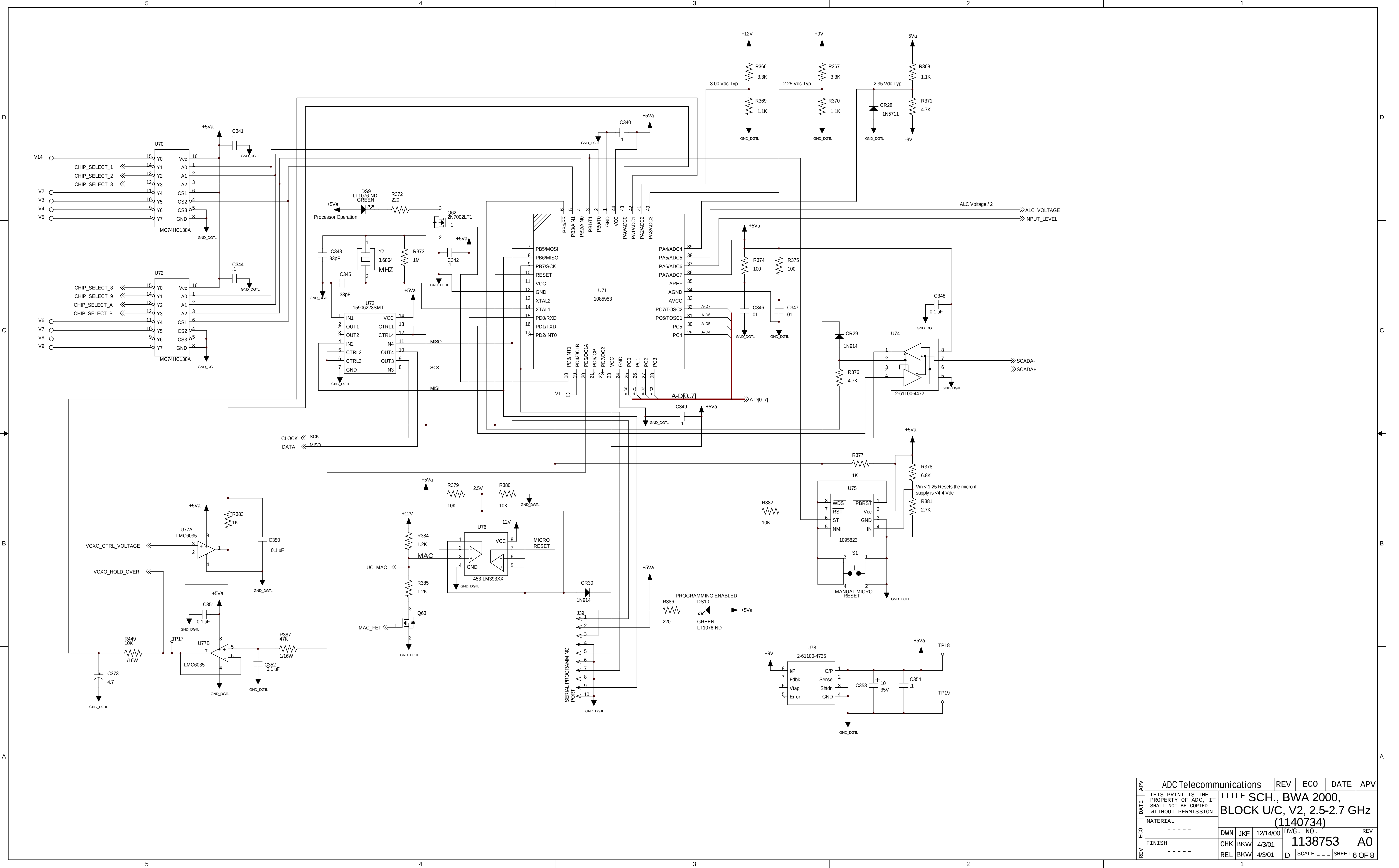




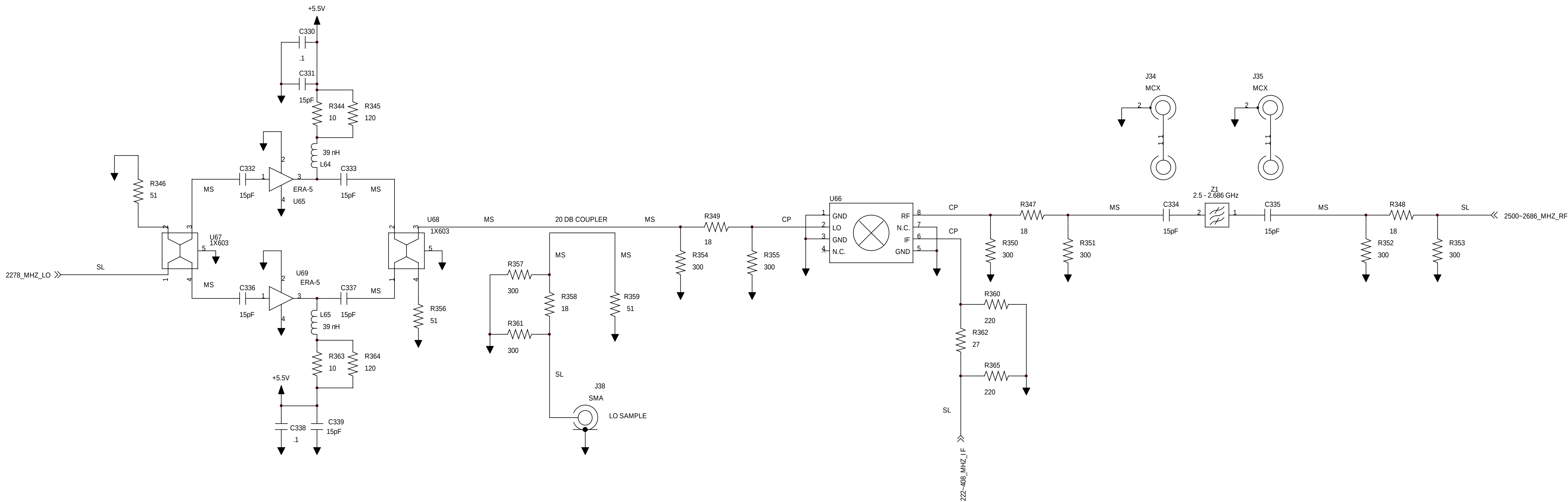
REV	ECD	DATE	APV
APV	DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION.	TITLE
ECD	REV	MATERIAL	I/C, BLOCK U/C, 2.5 - 2.7 GHz, AXITY BTS
REV	APV	FINISH	DWN JKF 2/6/01 DWG. NO. 1152963
APV	DATE	REL BKW 2/21/01	SCALE --- SHEET 1 OF 1

</

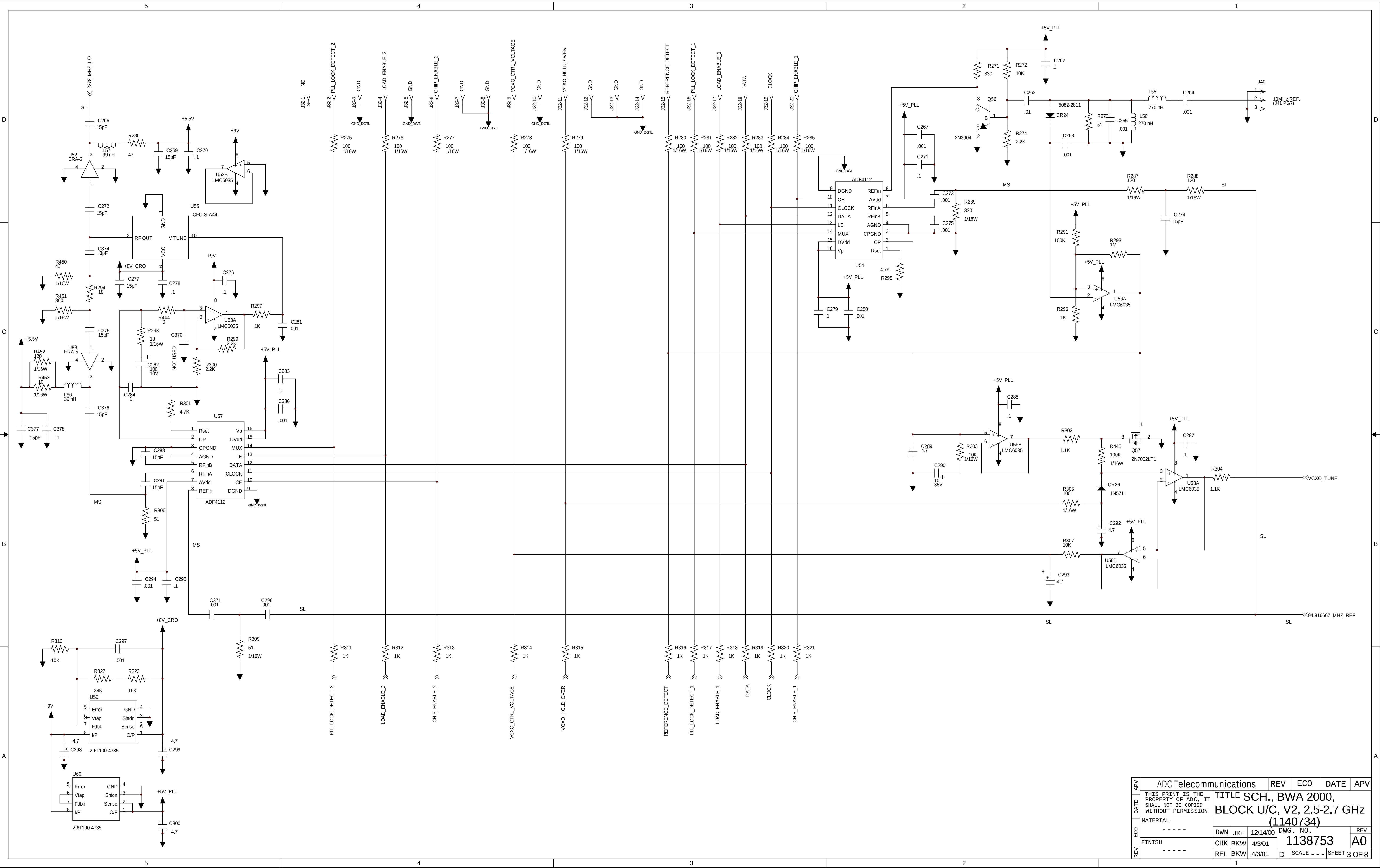




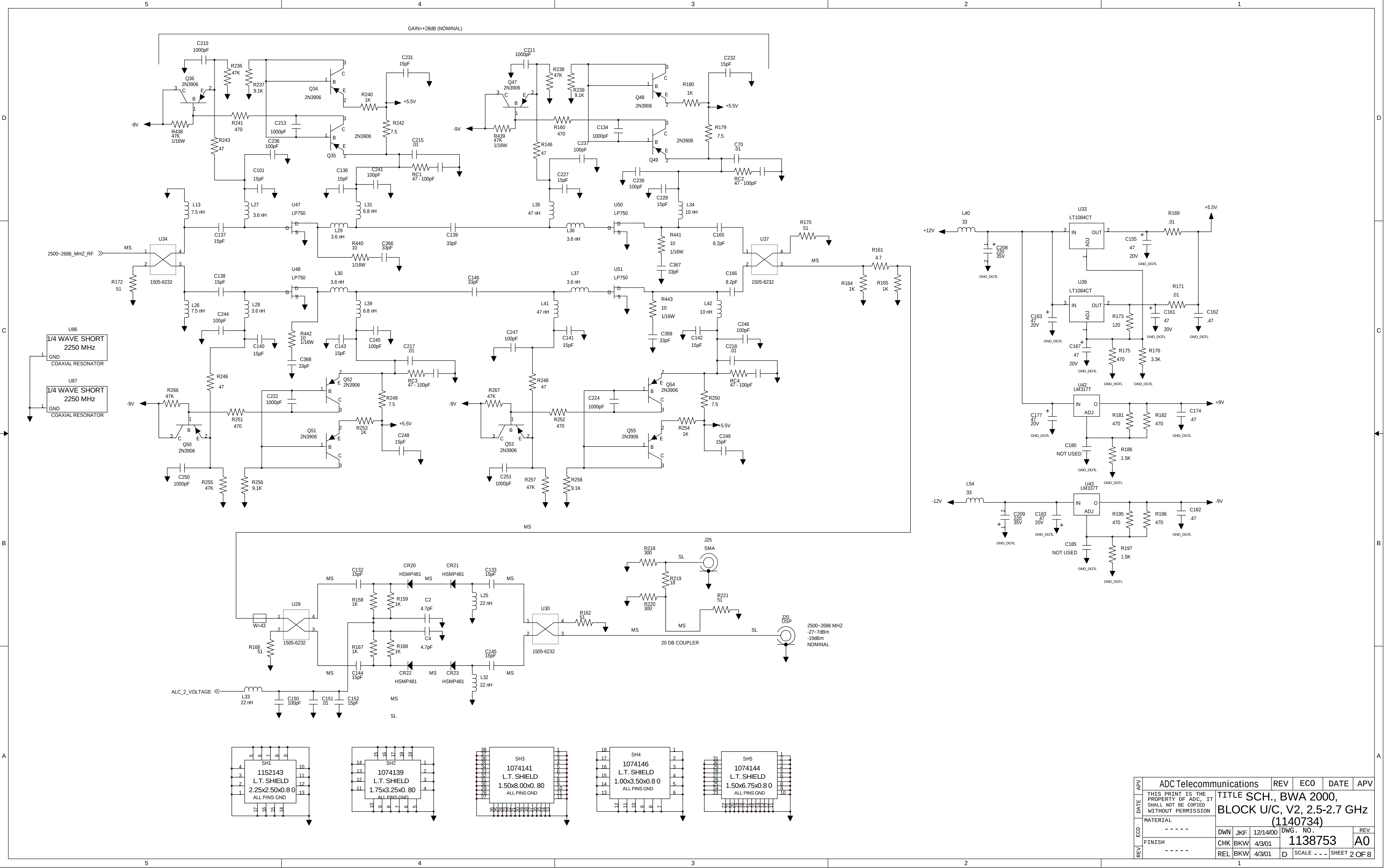
APV	ADC Telecommunications		REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION		TITLE SCH., BWA 2000, BLOCK U/C, V2, 2.5-2.7 GHz (1140734)			
ECO	MATERIAL		DWN	JKF	12/14/00	DWG. NO.
REV	FINISH		CHK	BKW	4/3/01	1138753
			REL	BKW	4/3/01	A0
				SCALE	---	SHEET 6 OF 8



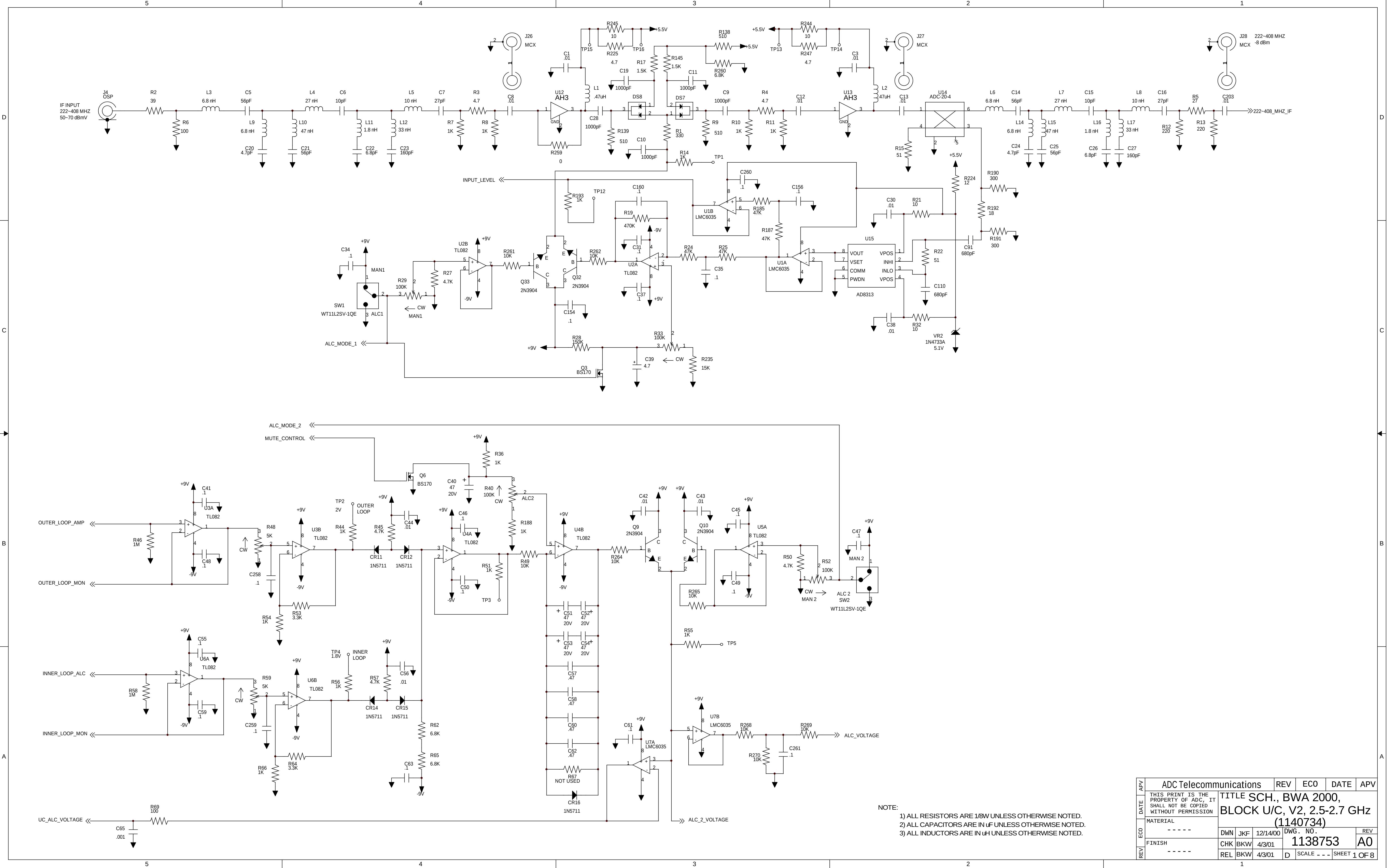
APV	ADC Telecommunications				REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION				TITLE SCH., BWA 2000, BLOCK U/C, V2, 2.5-2.7 GHz (1140734)			
ECO	MATERIAL				DWN JKF 12/14/00 DWG. NO. 1138753			
REV	FINISH				CHK BKW 4/3/01	REL BKW 4/3/01	D	SCALE --- SHEET 5 OF 8



APV	ADC Telecommunications		REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC. IT SHALL NOT BE COPIED WITHOUT PERMISSION		TITLE SCH., BWA 2000, BLOCK U/C, V2, 2.5-2.7 GHz (1140734)			
ECO	MATERIAL		DWN	JKF	DWG. NO.	REV
FINISH	-----		CHK	BKW	4/3/01	1138753 A0
REV	-----		REL	BKW	4/3/01	D SCALE - - - SHEET 3 OF 8

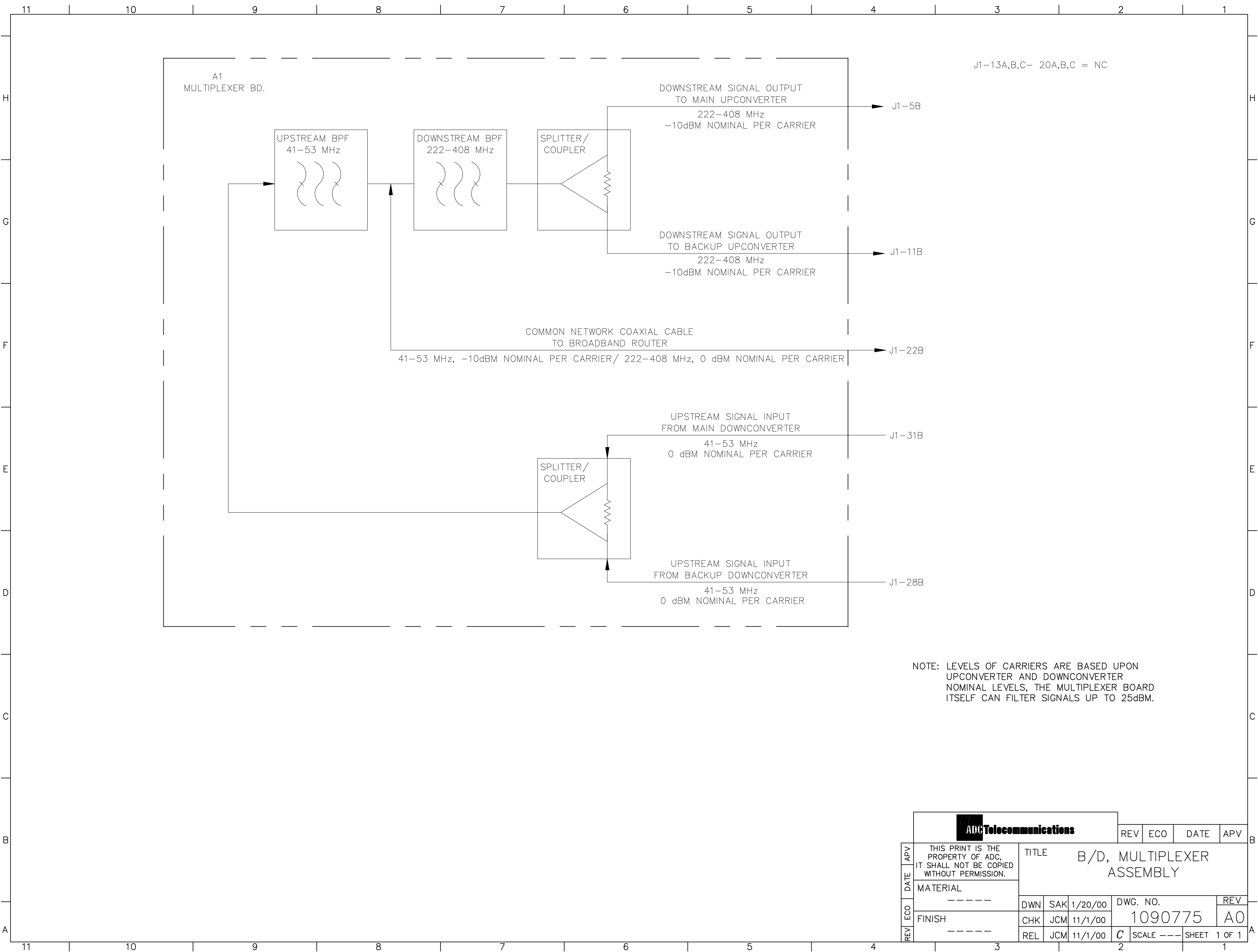


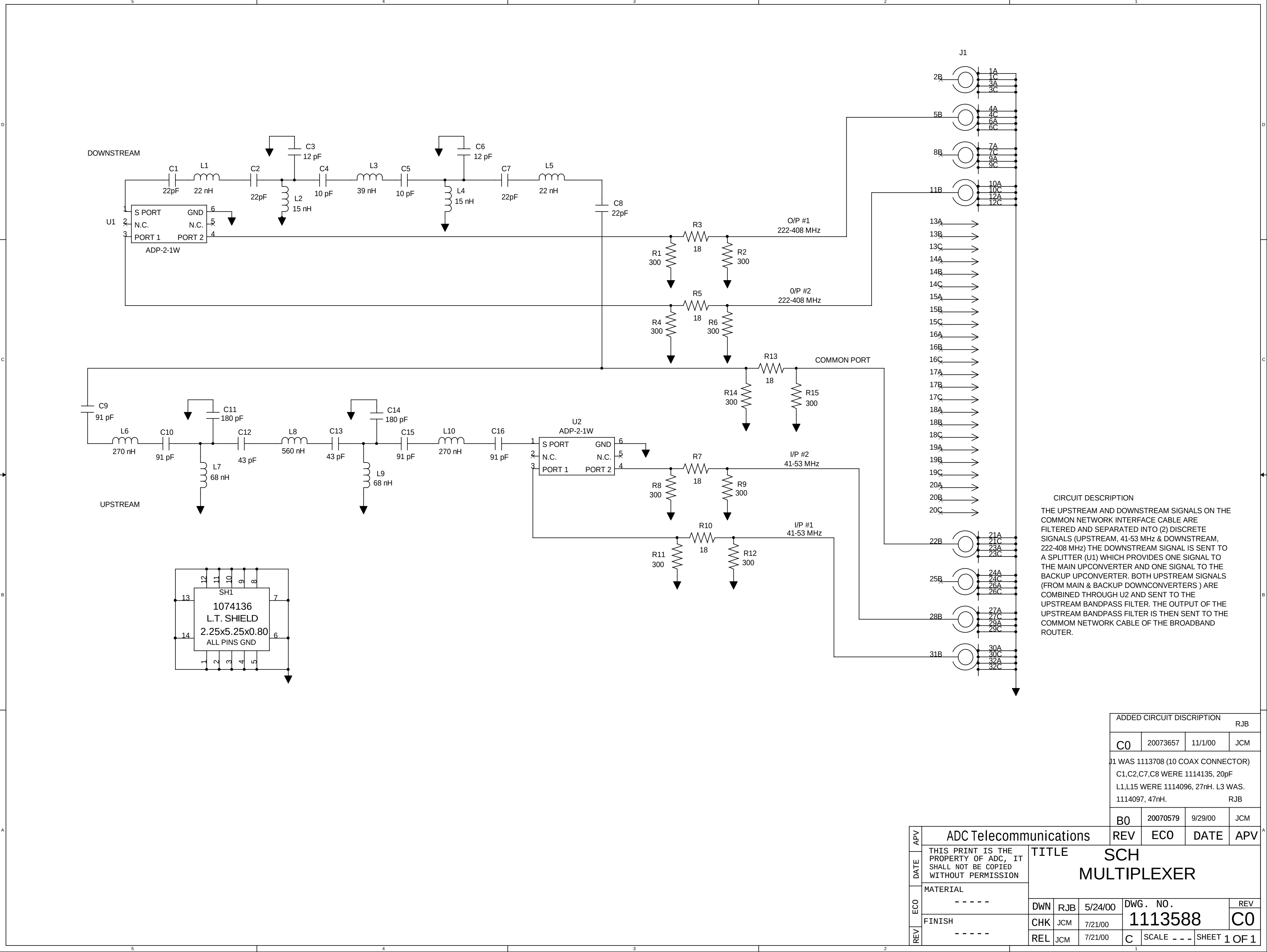
APV	ADC Telecommunications				REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION				TITLE SCH., BWA 2000, BLOCK U/C, V2, 2.5-2.7 GHz (1140734)			
MATERIAL	-----				DWN	JKF	12/14/00	DWG. NO.
FINISH	-----				CHK	BKW	4/3/01	1138753
REV	-----				REL	BKW	4/3/01	A0
					SCALE	---	SHEET 2 OF 8	



APV	ADC Telecommunications			REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION			TITLE SCH., BWA 2000, BLOCK U/C, V2, 2.5-2.7 GHz (1140734)			
ECO	MATERIAL			DWN	JKF	12/14/00	DWG. NO.
REV	FINISH			CHK	BKW	4/3/01	1138753
				REL	BKW	4/3/01	A0
				D	SCALE	---	SHEET 1 OF 8



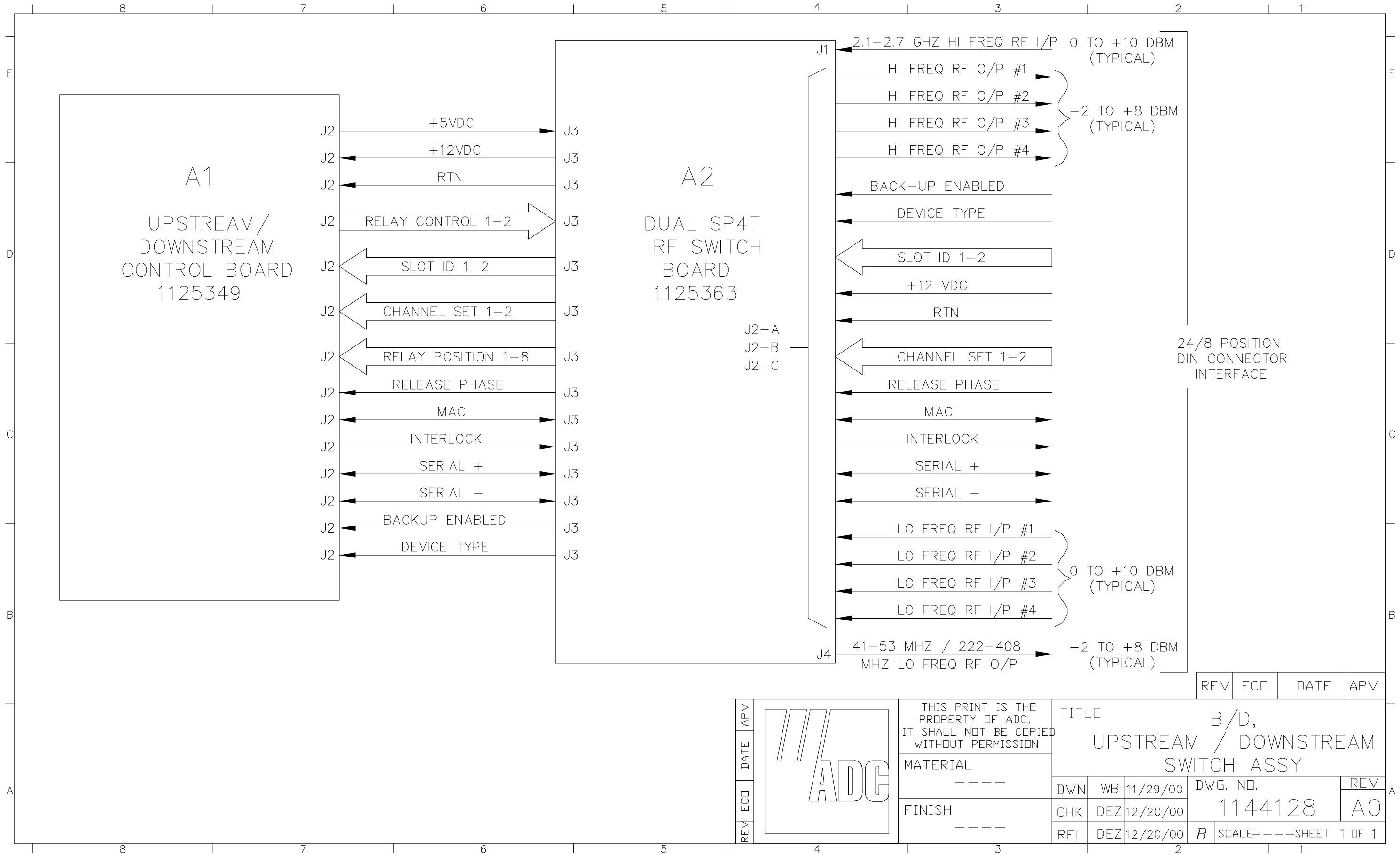




ADDED CIRCUIT DISCRPTION			
RJB			
C0	20073657	11/1/00	JCM
J1 WAS 1113708 (10 COAX CONNECTOR) C1,C2,C7,C8 WERE 1114135, 20pF L1,L15 WERE 1114096, 27nH. L3 WAS. 1114097, 47nH.			
RJB			
B0	20070579	9/29/00	JCM

ADC Telecommunications				REV	ECO	DATE	APV
THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION		TITLE SCH MULTIPLEXER					
MATERIAL -----							
FINISH -----		DWN	RJB	5/24/00	DWG. NO. 1113588		REV C0
		REL	JCM	7/21/00	C	SCALE ---	SHEET 1 OF 1

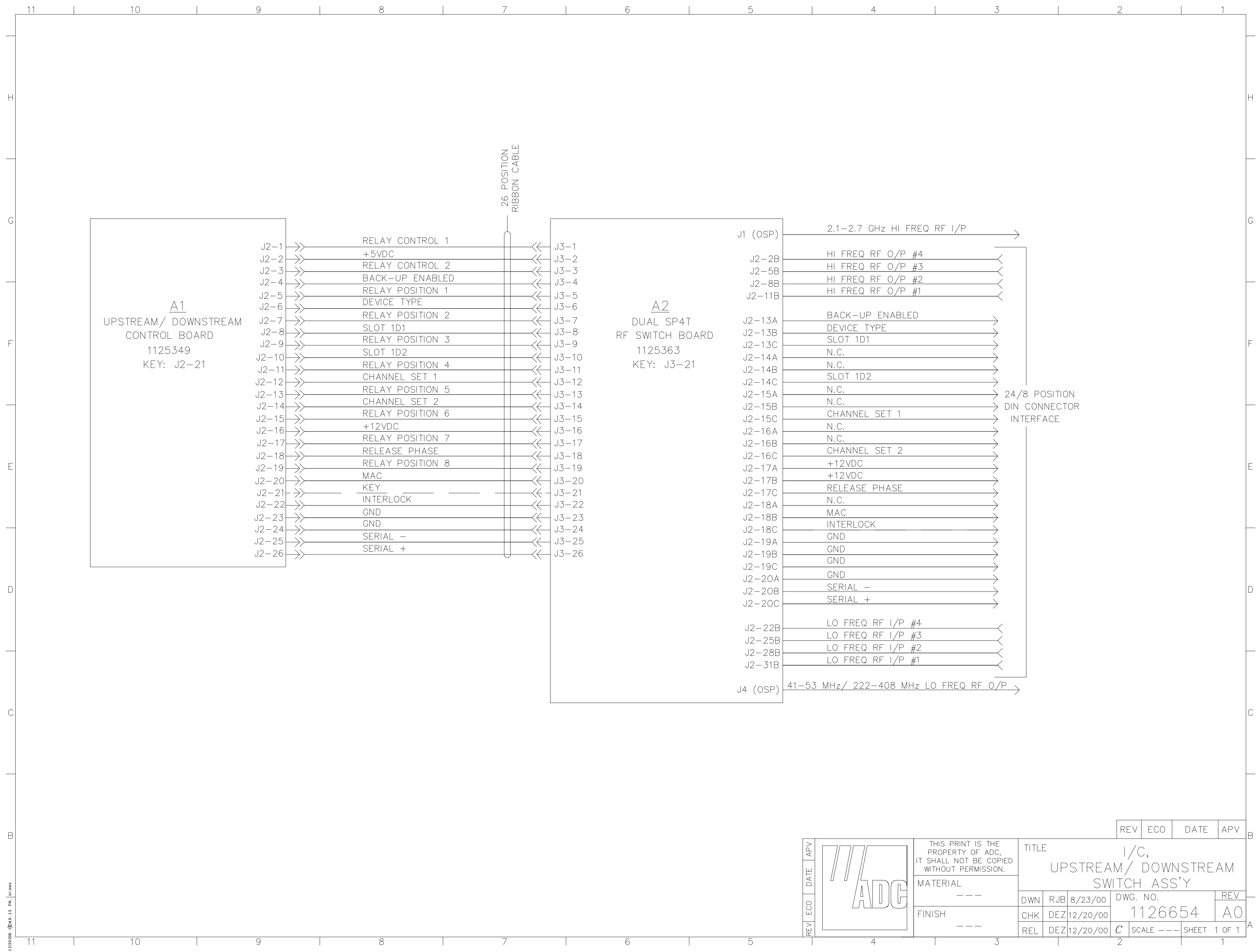
12/20/200 03:12:20 PM, k1zhes

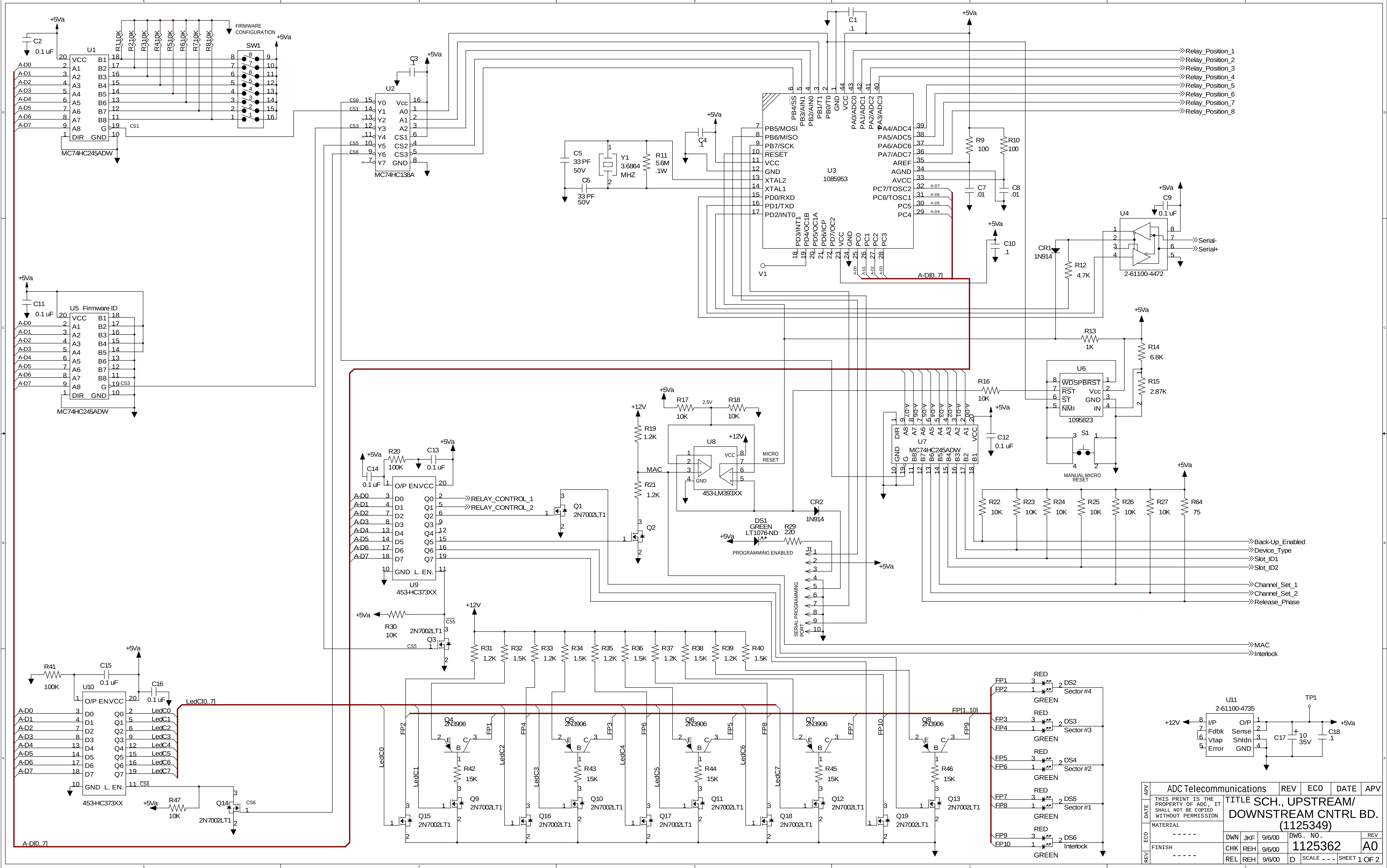


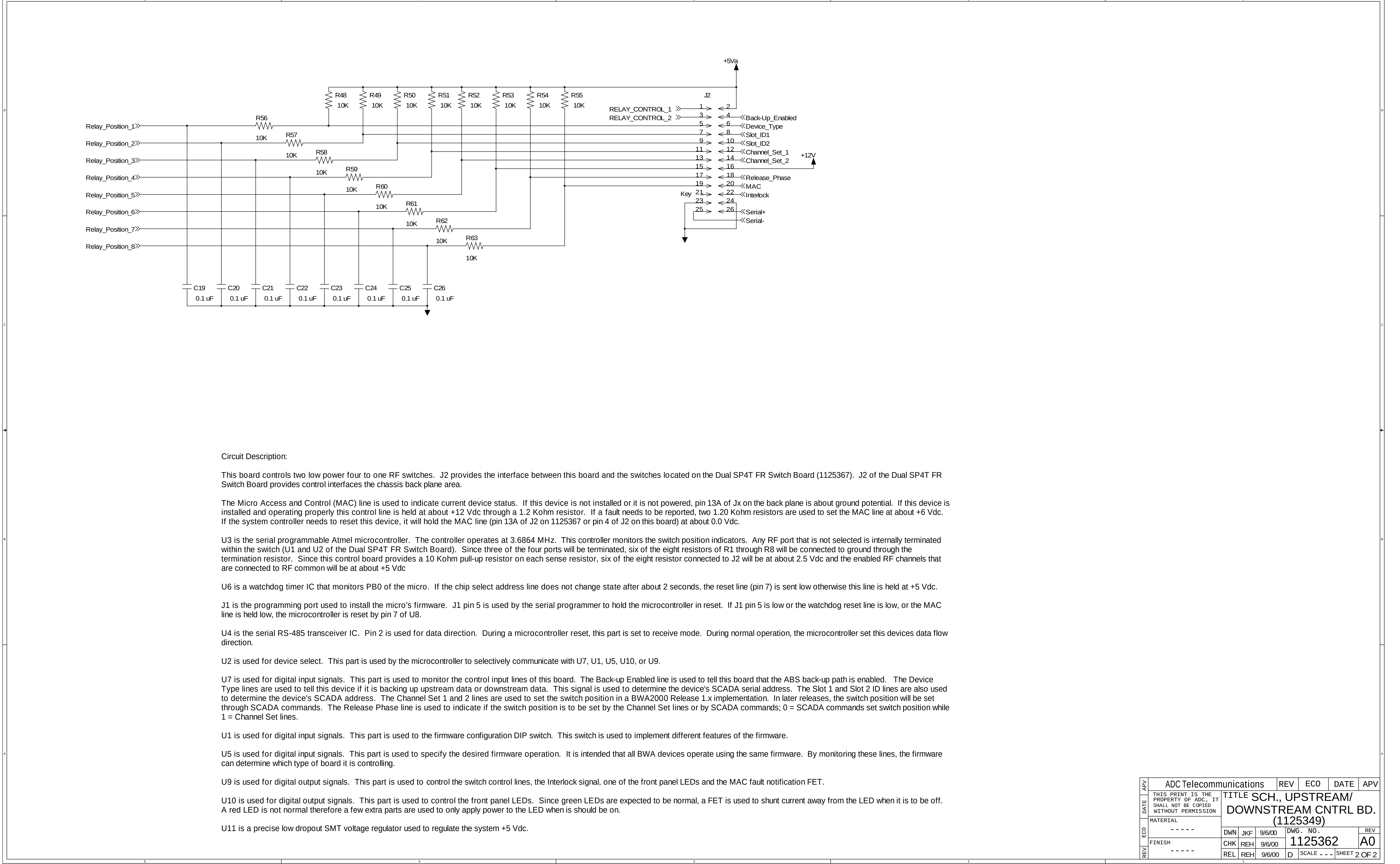
REV	ECO	DATE	APV
APV	DATE	ECO	REV
ECO	DATE	ECO	REV
REV	ECO	DATE	APV

THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION.				TITLE			
MATERIAL				B/D, UPSTREAM / DOWNSTREAM SWITCH ASSY			
FINISH				DWG. NO.			
---				1144128			
---				SCALE---			
---				SHEET 1 OF 1			

DWN	WB	11/29/00	REV
CHK	DEZ	12/20/00	A0
REL	DEZ	12/20/00	B







Circuit Description:

This board controls two low power four to one RF switches. J2 provides the interface between this board and the switches located on the Dual SP4T FR Switch Board (1125367). J2 of the Dual SP4T FR Switch Board provides control interfaces the chassis back plane area.

The Micro Access and Control (MAC) line is used to indicate current device status. If this device is not installed or it is not powered, pin 13A of Jx on the back plane is about ground potential. If this device is installed and operating properly this control line is held at about +12 Vdc through a 1.2 Kohm resistor. If a fault needs to be reported, two 1.20 Kohm resistors are used to set the MAC line at about +6 Vdc. If the system controller needs to reset this device, it will hold the MAC line (pin 13A of J2 on 1125367 or pin 4 of J2 on this board) at about 0.0 Vdc.

U3 is the serial programmable Atmel microcontroller. The controller operates at 3.6864 MHz. This controller monitors the switch position indicators. Any RF port that is not selected is internally terminated within the switch (U1 and U2 of the Dual SP4T FR Switch Board). Since three of the four ports will be terminated, six of the eight resistors of R1 through R8 will be connected to ground through the termination resistor. Since this control board provides a 10 Kohm pull-up resistor on each sense resistor, six of the eight resistor connected to J2 will be at about 2.5 Vdc and the enabled RF channels that are connected to RF common will be at about +5 Vdc

U6 is a watchdog timer IC that monitors PB0 of the micro. If the chip select address line does not change state after about 2 seconds, the reset line (pin 7) is sent low otherwise this line is held at +5 Vdc.

J1 is the programming port used to install the micro's firmware. J1 pin 5 is used by the serial programmer to hold the microcontroller in reset. If J1 pin 5 is low or the watchdog reset line is low, or the MAC line is held low, the microcontroller is reset by pin 7 of U8.

U4 is the serial RS-485 transceiver IC. Pin 2 is used for data direction. During a microcontroller reset, this part is set to receive mode. During normal operation, the microcontroller set this devices data flow direction.

U2 is used for device select. This part is used by the microcontroller to selectively communicate with U7, U1, U5, U10, or U9.

U7 is used for digital input signals. This part is used to monitor the control input lines of this board. The Back-up Enabled line is used to tell this board that the ABS back-up path is enabled. The Device Type lines are used to tell this device if it is backing up upstream data or downstream data. This signal is used to determine the device's SCADA serial address. The Slot 1 and Slot 2 ID lines are also used to determine the device's SCADA address. The Channel Set 1 and 2 lines are used to set the switch position in a BWA2000 Release 1.x implementation. In later releases, the switch position will be set through SCADA commands. The Release Phase line is used to indicate if the switch position is to be set by the Channel Set lines or by SCADA commands; 0 = SCADA commands set switch position while 1 = Channel Set lines.

U1 is used for digital input signals. This part is used to the firmware configuration DIP switch. This switch is used to implement different features of the firmware.

U5 is used for digital input signals. This part is used to specify the desired firmware operation. It is intended that all BWA devices operate using the same firmware. By monitoring these lines, the firmware can determine which type of board it is controlling.

U9 is used for digital output signals. This part is used to control the switch control lines, the Interlock signal, one of the front panel LEDs and the MAC fault notification FET.

U10 is used for digital output signals. This part is used to control the front panel LEDs. Since green LEDs are expected to be normal, a FET is used to shunt current away from the LED when it is to be off. A red LED is not normal therefore a few extra parts are used to only apply power to the LED when is should be on.

U11 is a precise low dropout SMT voltage regulator used to regulate the system +5 Vdc.

APV	ADC Telecommunications				REV	ECO	DATE	APV	
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION				TITLE SCH., UPSTREAM/ DOWNSTREAM CNTRL BD. (1125349)				
MATERIAL									
ECO	-----				DWN	JKF	9/6/00	DWG. NO.	REV
REV	FINISH				CHK	REH	9/6/00	1125362	A0
	-----				REL	REH	9/6/00	D SCALE - - -	SHEET 2 OF 2

Circuit Description:

This board contains two low power four to one RF relays. J3 provides the interface between this board and the upstream/downstream switch control board (1125362). J1, J2, and J4 provide the interface between this board and the chassis backplane area.

U1 is a SP4T RF switch. Control pins 9 and 10 are used to select which position is connected to RF common (pin 1). Any RF port that is not selected is internally terminated within U1. Since the switch can not pass DC current, there is no easy way of detecting if a specified path is really engaged.

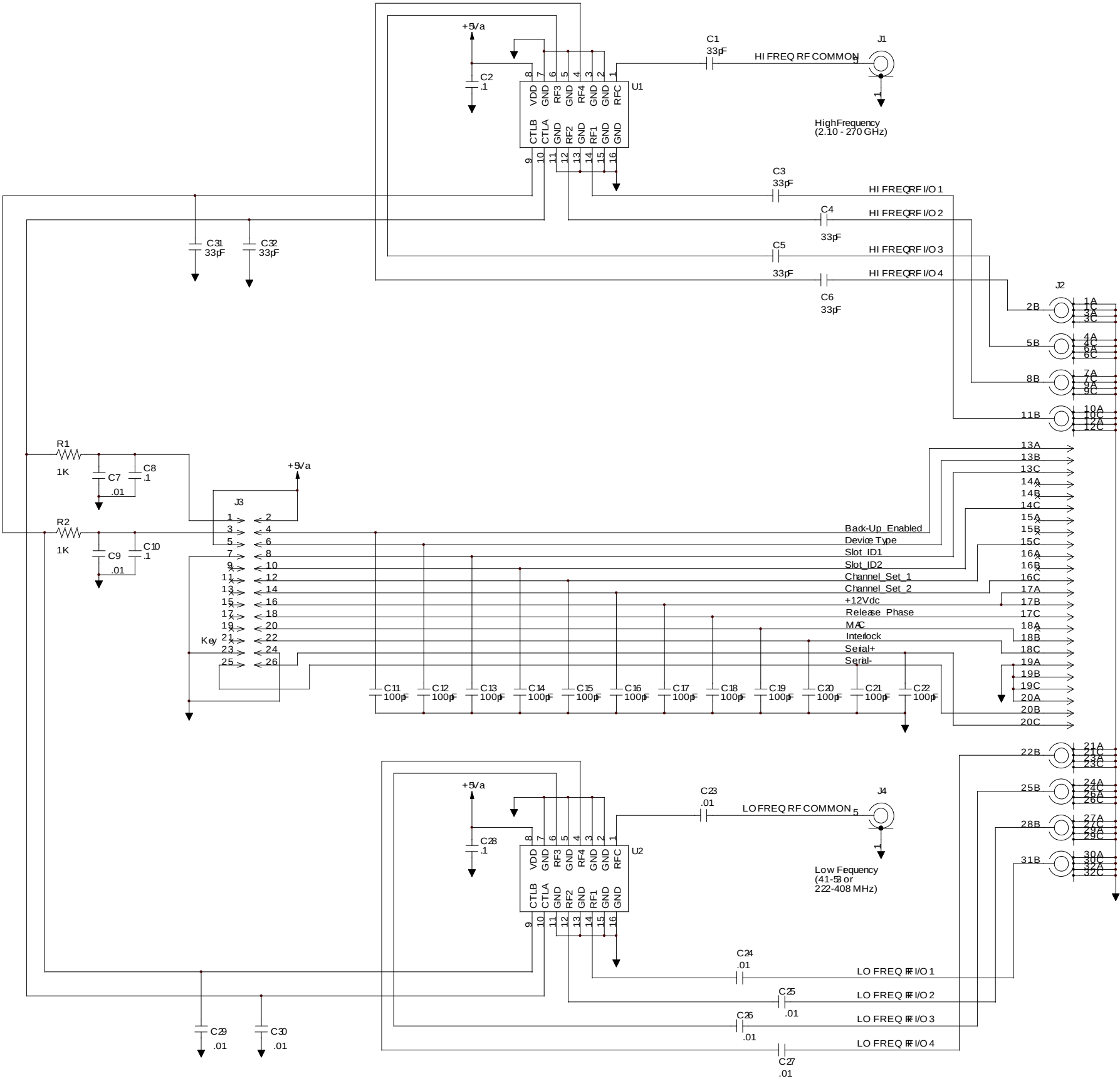
U2 is a second SP4T RF switch. Control pins 9 and 10 are used to select which position is connected to RF common (pin 1). Any RF port that is not selected is internally terminated within U2.

C1, C3 through C6 are DC blocking capacitors. Their values are selected to pass the high frequency (2.150 - 2.162 GHz) RF signals. C23 through C27 are DC blocking capacitors. Values are selected to pass the lower frequency (41 - 53 MHz or 222 - 408 MHz) RF signals.

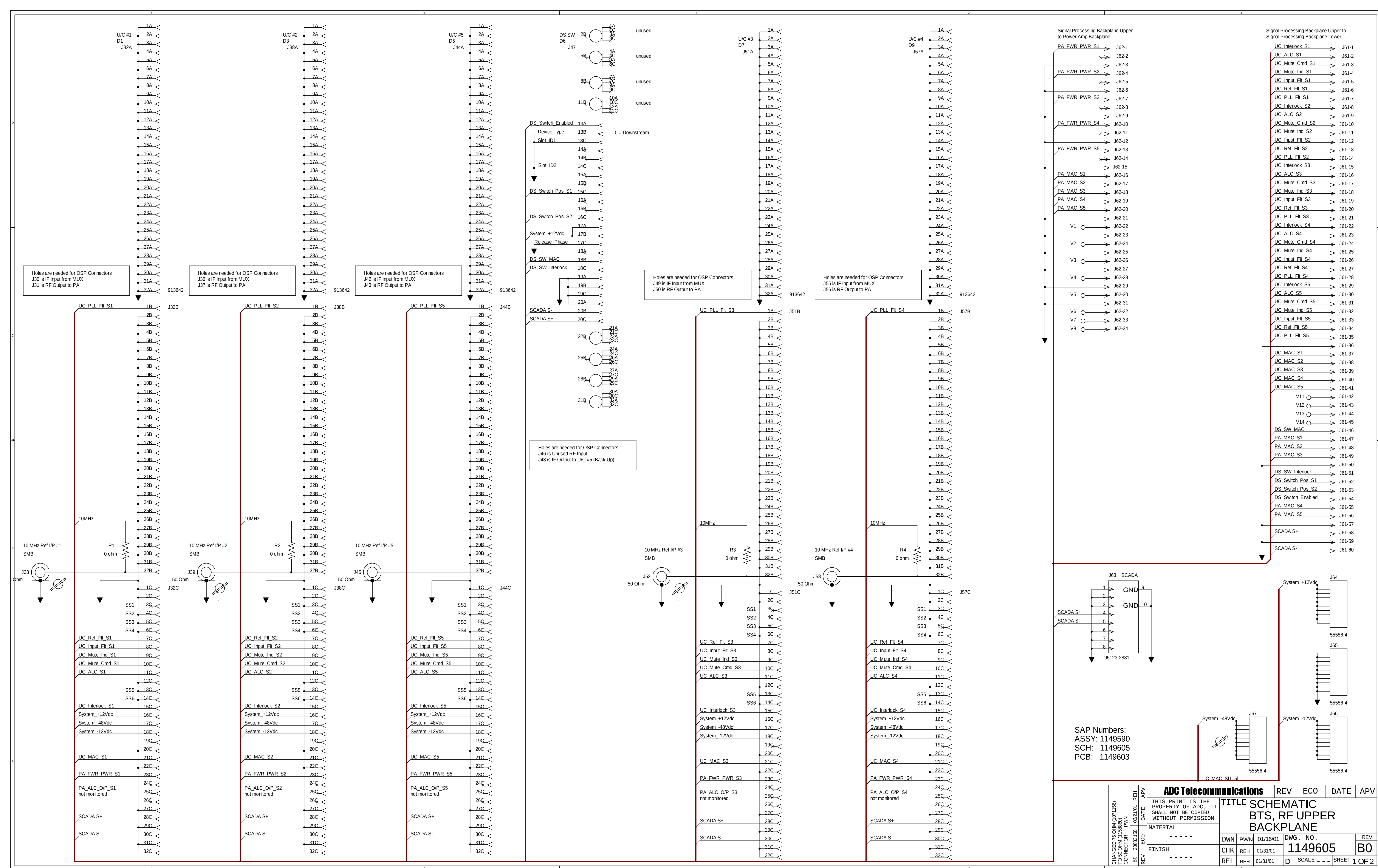
C2, C11 through C22, and C28 through C32 are RF bypass capacitors which remove unwanted RF signals from DC biaslines. R1 & R2 along with C7 through C10 perform a similar function as low pass filters.

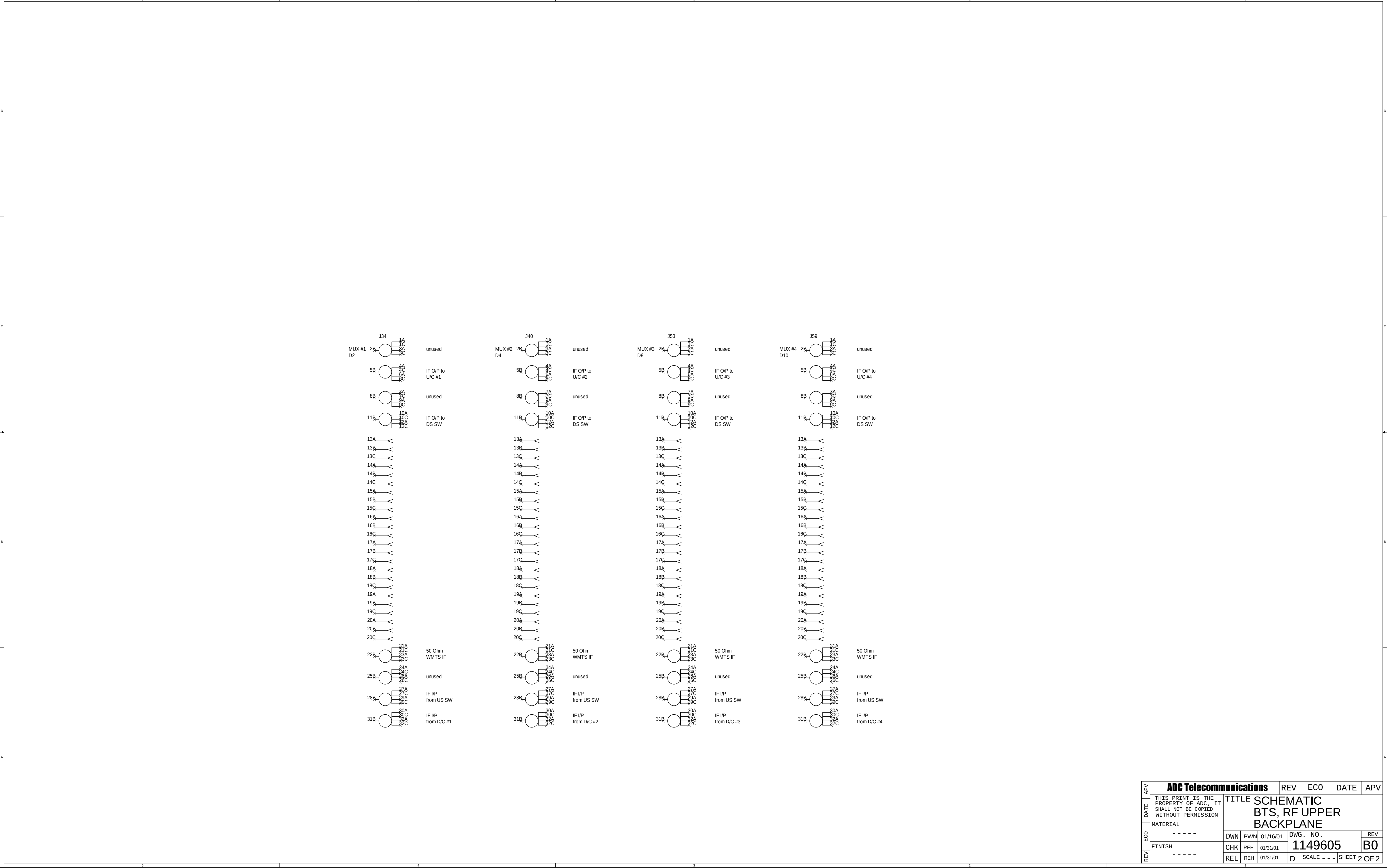
The control lines of J2 pins 13A through 20C are passed on to the upstream/downstream switch controlboard (1125362) and are described on that board's circuit description.

Pins 5 and 7 of J3 are wired to allow the upstream/downstream switch control board (1125362) determine which board it is controlling. The upstream/downstream switch control board (1125362) may also be used to control the redundant low noise amplifier RF section of a BWA2000 LNA.

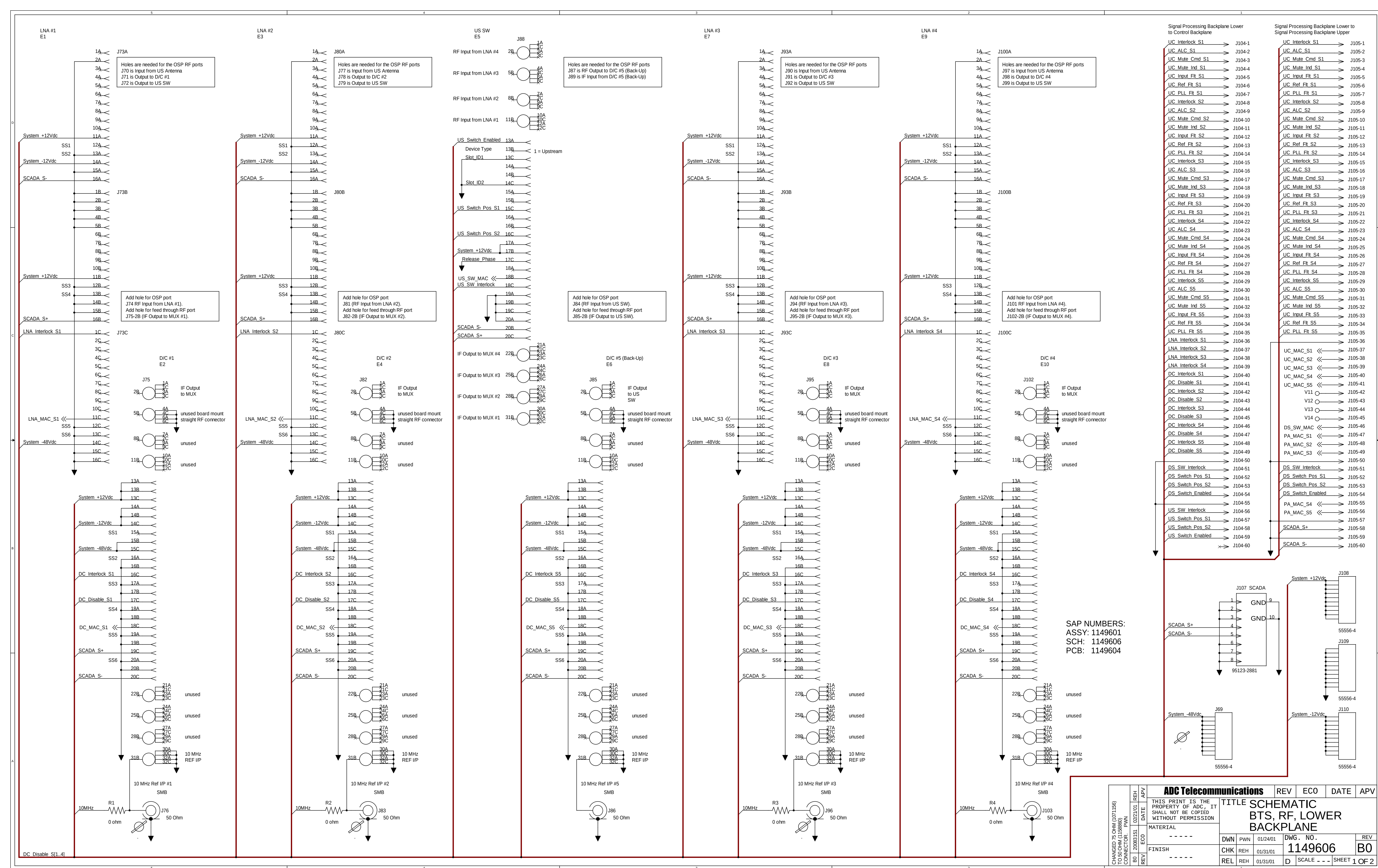


CHANGED ALL 15PF CAPS TO 33PF.	JKF	DEZ	APV	ADC Telecommunications				REV	ECO	DATE	APV			
	B0	2007042	12/00	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION				TITLE SCH., DUAL SP4T RF SWITCH BOARD (1125363)						
	REV	ECO	DATE					DWG. NO.						
	FINISH							-----	-----	CHK	REH	9/22/00	REV	
								REL	REH	9/22/00	D	SCALE ---	SHEET 1 OF 1	

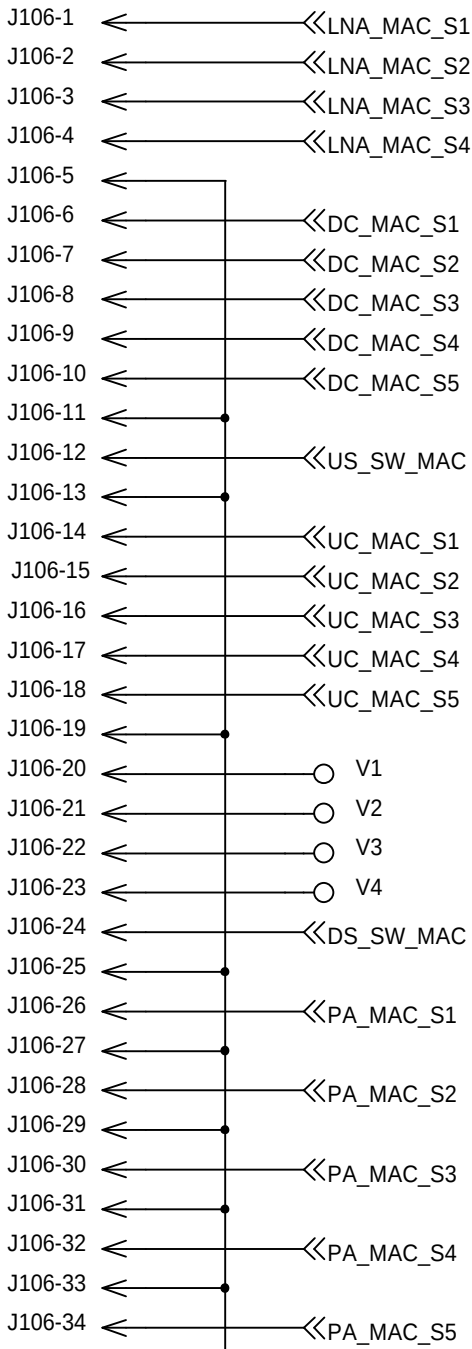




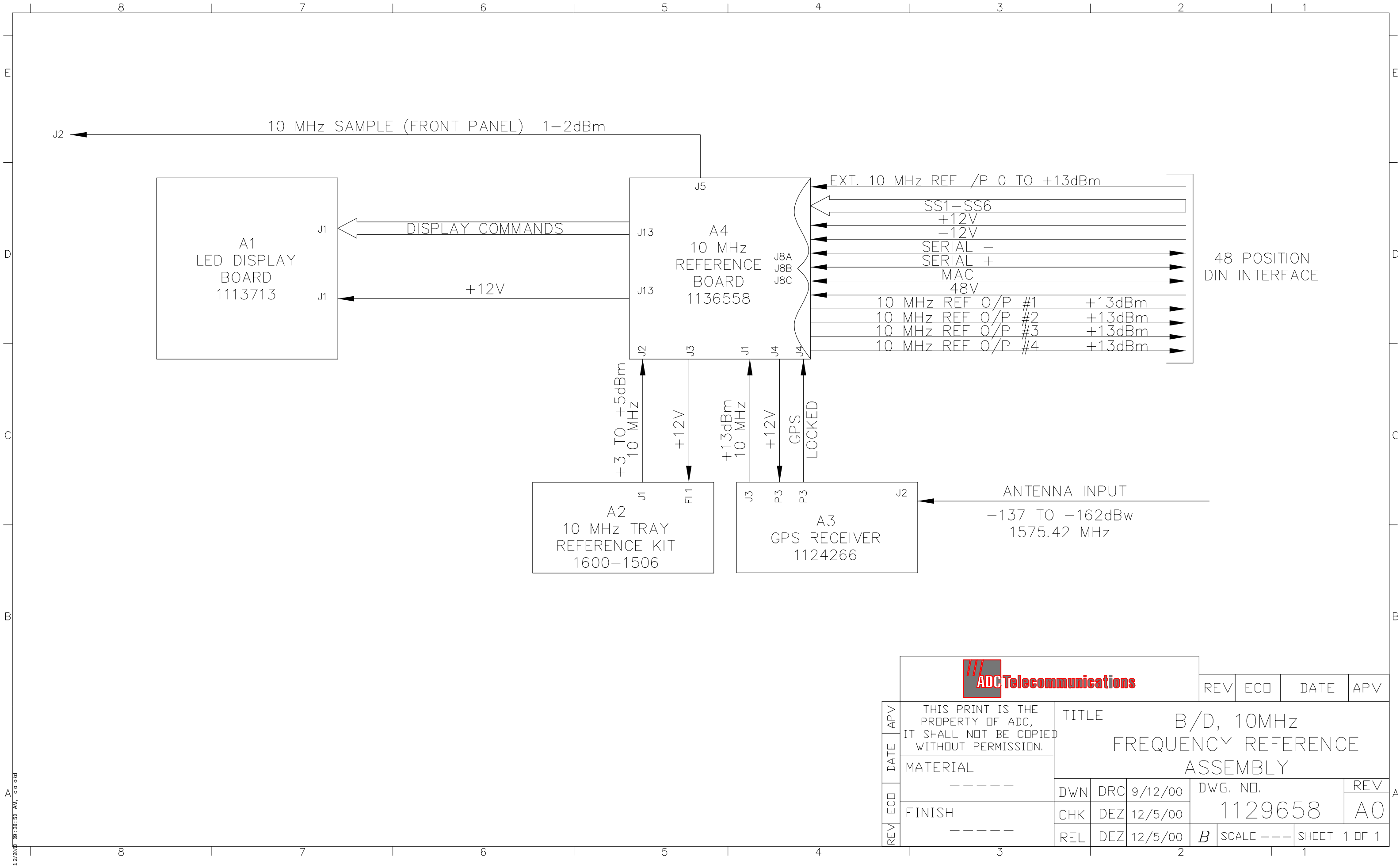
APV	ADC Telecommunications						REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION				TITLE SCHEMATIC BTS, RF UPPER BACKPLANE					
ECO	MATERIAL									
FINISH	-----				DWN	PWN	01/16/01		DWG. NO.	REV
REV	-----				CHK	REH	01/31/01		1149605	B0
					REL	REH	01/31/01		D	SCALE --- SHEET 2 OF 2



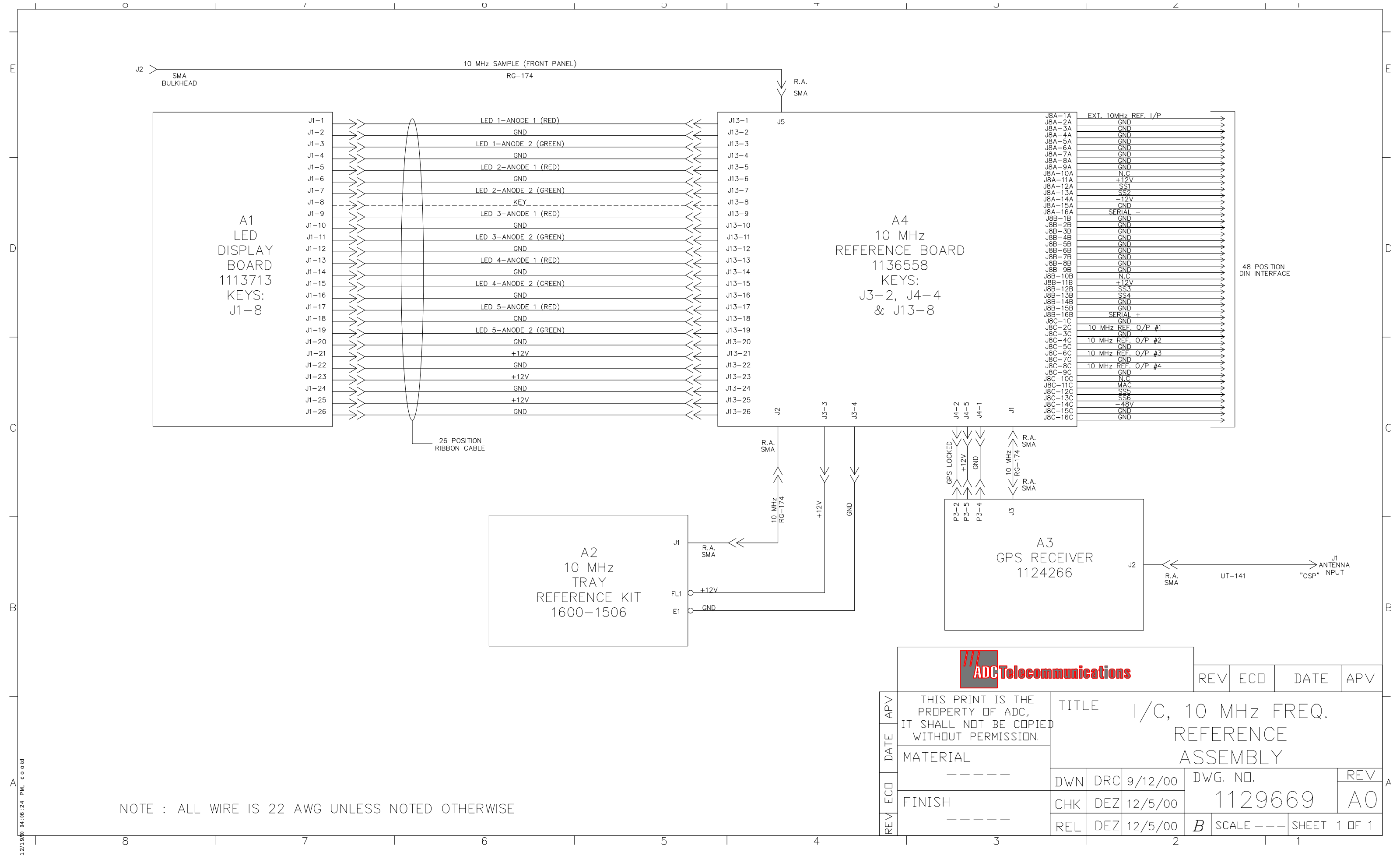
Signal Processing Backplane Lower
to CAM Controller



APV	ADC Telecommunications				REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION				TITLE SCHEMATIC BTS, RF, LOWER BACKPLANE			
ECO								
REV	FINISH				DWN	PWN	01/24/01	DWG. NO.
					CHK	REH	01/31/01	1149606
					REL	REH	01/31/01	D
								SCALE - - -
								SHEET 2 OF 2



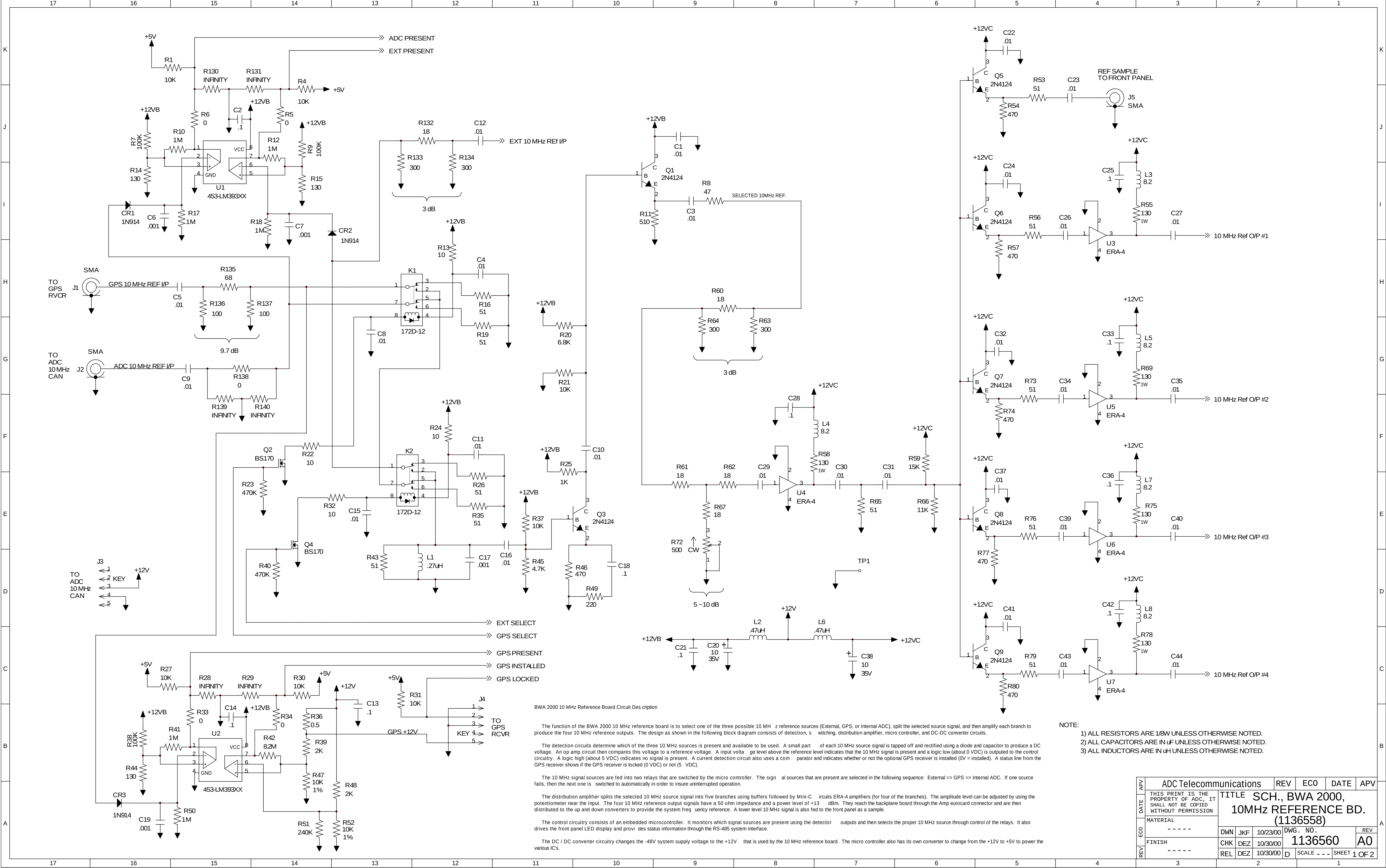
ADC Telecommunications												REV		ECO		DATE		APV	
APV		THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION.				TITLE B/D, 10MHz FREQUENCY REFERENCE ASSEMBLY													
DATE																			
ECO		MATERIAL				DWN		DRC		9/12/00		DWG. NO.		REV					
REV		FINISH				CHK		DEZ		12/5/00		1129658		A0					
		-----				REL		DEZ		12/5/00		B		SCALE --- SHEET 1 OF 1					



12/19/00 04:06:24 PM, c o o l d

NOTE : ALL WIRE IS 22 AWG UNLESS NOTED OTHERWISE

REV		ECO		DATE		APV	
		DWN		DRC		9/12/00	
		CHK		DEZ		12/5/00	
		REL		DEZ		12/5/00	
TITLE		I/C, 10 MHz FREQ.		REFERENCE		ASSEMBLY	
MATERIAL		DWN		DRC		9/12/00	
FINISH		CHK		DEZ		12/5/00	
REV		ECO		DATE		APV	
DWN		DRC		9/12/00		1129669	
REL		DEZ		12/5/00		A0	
SCALE		SHEET		1 OF 1			



BWA 2000 10 MHz Reference Board Circuit Description

The function of the BWA 2000 10 MHz reference board is to select one of the three possible 10 MHz reference sources (External, GPS, or Internal ADC), split the selected source signal, and then amplify each branch to produce the four 10 MHz reference outputs. The design as shown in the following block diagram consists of detection, switching, distribution amplifier, micro controller, and DC-DC converter circuits.

The detection circuits determine which of the three 10 MHz sources is present and available to be used. A small part of each 10 MHz source signal is tapped off and rectified using a diode and capacitor to produce a DC voltage. An op amp circuit then compares this voltage to a reference voltage. A input voltage level above the reference level indicates that the 10 MHz signal is present and a logic low (about 0 VDC) is output to the control circuitry. A logic high (about 5 VDC) indicates no signal is present. A current detection circuit also uses a comparator and indicates whether or not the optional GPS receiver is installed. A status line from the GPS receiver shows if the GPS receiver is locked (0 VDC) or not (5 VDC).

The 10 MHz signal sources are fed into two relays that are switched by the micro controller. The signal sources that are present are selected in the following sequence: External => GPS => Internal ADC. If one source fails, then the next one is switched to automatically in order to insure uninterrupted operation.

The distribution amplifier splits the selected 10 MHz source signal into five branches using buffers followed by Mini-Circuits ERA-4 amplifiers (for four of the branches). The amplitude level can be adjusted by using the potentiometer near the input. The four 10 MHz reference output signals have a 50 ohm impedance and a power level of +13 dBm. They reach the backplane board through the Ampuro card connector and are then distributed to the up and down converters to provide the system frequency reference. A lower level 10 MHz signal is also fed to the front panel as a sample.

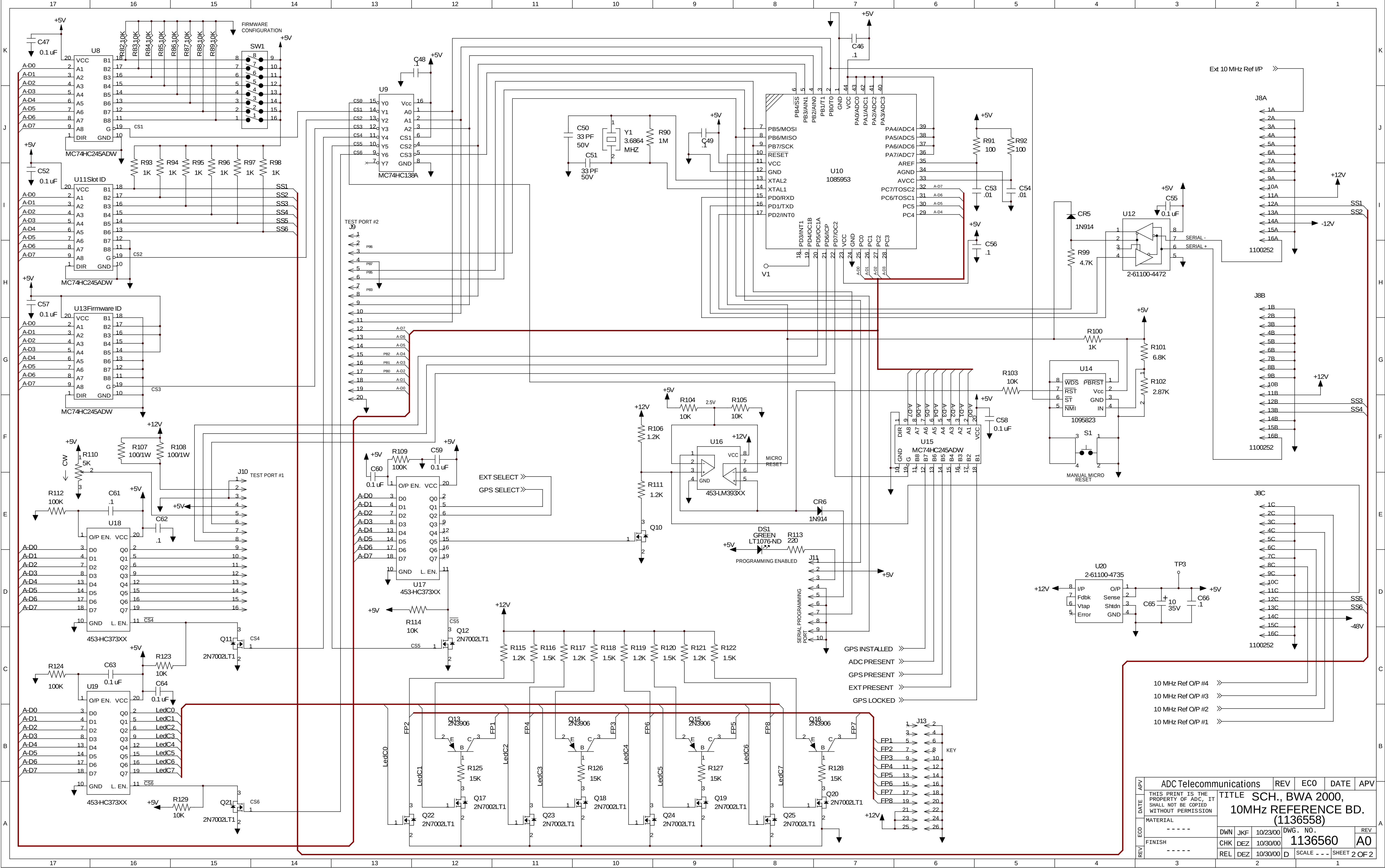
The control circuitry consists of an embedded microcontroller. It monitors which signal sources are present using the detector outputs and then selects the proper 10 MHz source through control of the relays. It also drives the front panel LED display and provides status information through the RS-485 system interface.

The DC / DC converter circuitry changes the -48V system supply voltage to the +12V that is used by the 10 MHz reference board. The micro controller also has its own converter to change from the +12V to +5V to power the various ICs.

NOTE:

- 1) ALL RESISTORS ARE 1/8W UNLESS OTHERWISE NOTED.
- 2) ALL CAPACITORS ARE IN uF UNLESS OTHERWISE NOTED.
- 3) ALL INDUCTORS ARE IN uH UNLESS OTHERWISE NOTED.

APV	ADC Telecommunications		REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC. IT SHALL NOT BE COPIED WITHOUT PERMISSION		TITLE SCH., BWA 2000, 10MHz REFERENCE BD. (1136558)			REV
MATERIAL			DWN	JKF	10/23/00	
ECO	FINISH	CHK	DEZ	10/30/00	1136560	A0
REV	REL	DEZ	10/30/00	D	SCALE - - -	SHEET 1 OF 2



APV	ADC Telecommunications			REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION			TITLE SCH., BWA 2000, 10MHz REFERENCE BD. (1136558)			
ECO	MATERIAL			DWN	JKF	10/23/00	DWG. NO.
FINISH	-----			CHK	DEZ	10/30/00	1136560
REV	-----			REL	DEZ	10/30/00	D SCALE - - - SHEET 2 OF 2



Model 87-664

GPS-XL Time and Frequency Module

TrueTime, Inc. Santa Rosa, CA USA
Phone 707-528-1230 Fax 707-527-6640
www.truetime.com Email truetime@truetime.com

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DETAIL-A

TABLE 5

PIN	DESCRIPTION
1	ALARM (OPEN COLLECTOR)
2	NC
3	GND
4	GND
5	+12V (9-18VDC)

MATING CONNECTION

MOLEX P/N 22-01-3057

CONTRACT NO.	APPROVALS	DATE
	DRAWN BY INNR	07/10
	CHECKED BY	
	APPROVED BY <i>[Signature]</i>	7/10
	NEXT ASSY	

FILENAME: \P7\87-264

DATE: 07-19-00

SCALE NONE

SHEET 1 OF 2

SHEET 1 OF 2

1-31 PHYSICAL SPECIFICATIONS

1-32 The GPS-XL is a board level product with the following physical specifications:

GPS-XL Module Size: 3.94 in. x 6.30 in. x .91 in.
(10 cm. x 16 cm. x 2.31 cm.)

Antenna Size: 2.625 in. dia. x 1.5 in.
(6.67 cm. dia x 3.81 cm.)

Antenna/DownConverter Size: 2.625 in. dia. x 8.6 in.
(Optional) (6.67 cm. dia. x 21.84 cm.)

Note: Antenna and Antenna/DownConverter Units are mounted on a 12 in. long PVC nipple with 3/4" Male Pipe Thread (MPT) on both ends. The above specified overall lengths of the Antenna and Antenna/DownConverter Units are therefore increased by approximately 11.25 in. when the mounting nipple is included.

GPS-XL Module Weight: .4 lb max. (.186 Kg)

Antenna Weight: 0.70 lb (.318 Kg)
(Including mtg. nipple)

Antenna/DownConverter Weight: 2.35 lb (1.067 Kg)
(Including mtg. nipple)
(Optional)

Antenna Cable, RG-59: Standard length = 50 ft.
1.2 lb (.545 Kg)

Antenna/DownConverter Cable, RG-58: Standard length = 200 ft.
(Optional) 5.4 lb (2.452 Kg)

1-33 ENVIRONMENTAL SPECIFICATIONS

1-34 The environmental specifications are:

Operating Temperature:

Antenna or Antenna/DownConverter: -40° to +70° C (-40° to +158° F)

GPS-XL Module: 0° to +60° C (+32° to +140° F)

Storage Temperature:

Antenna or Antenna/DownConverter: -55° to +85° C (-67° to +185° F)

GPS-XL Module: -40° to +85° C (-40° to +185° F)

Humidity:

Antenna or Antenna/DownConverter: 100%, condensing

GPS-XL Module: 95%, non-condensing

1-35 POWER INPUT SPECIFICATIONS

SUPPLY OPTION	VOLTAGE	RIPPLE+NOISE	POWER
<u>Standard Antenna:</u>			
12 VDC & 5 VDC (STANDARD)	+/- 5%	< 75 mV, 100 KHz BW	1.00 W @ 12V 3.75 W @ 5V
12 VDC (OPTION)	+/- 5%	< 75 mV, 100 KHz BW	6.00 W
12 VDC (Batt.) (OPTION)	8-16.5 VDC	< 1 V, 100 KHz BW	6.25 W
24 VDC (Batt.) (OPTION)	16-32 VDC	< 1 V, 100 KHz BW	6.25 W
<u>Antenna/DownConverter Option:</u>			
12 VDC & 5 VDC (STANDARD)	+/- 5%	< 75 mV, 100 KHz BW	3.00 W @ 12V 3.75 W @ 5V
12 VDC (OPTION)	+/- 5%	< 75 mV, 100 KHz BW	8.00 W
12 VDC (Batt.) (OPTION)	8-16.5 VDC	< 1 V, 100 KHz BW	8.75 W
24 VDC (Batt.) (OPTION)	16-32 VDC	< 1 V, 100 KHz BW	8.75 W

1-36 BATTERY SPECIFICATIONS

The battery provides standby power to the GPS-XL memory.

Battery type: Lithium, 3.5 Volt

Battery life: 15000 hours standby, shelf life 10 years

1-37 TIMING/FREQUENCY PERFORMANCE SPECIFICATIONS

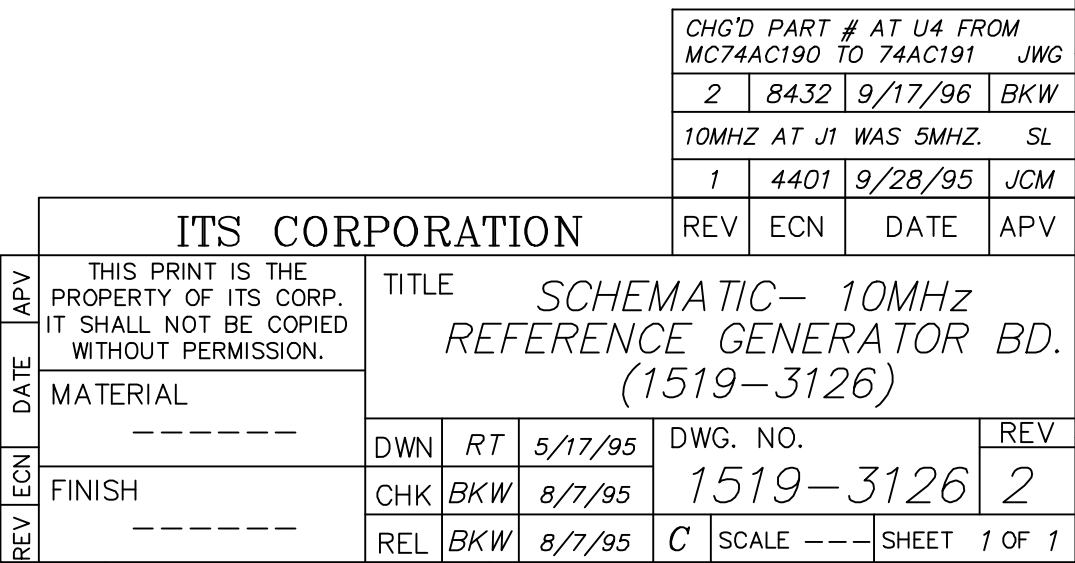
1-38 All performance specifications are valid when the antenna's geodetic position is known within 10 m in WGS-84 and four or more satellites are being tracked under the current conditions of Selective Availability (SA) as experienced at product release in March of 1994. In addition, in order to achieve the stated stability specifications, the GPS-XL must be mounted in an enclosure which will eliminate exposure of the internal oscillator to rapid temperature fluctuations due to air currents. During periods without SA, timing performance is improved to the +/- 100 nS level.

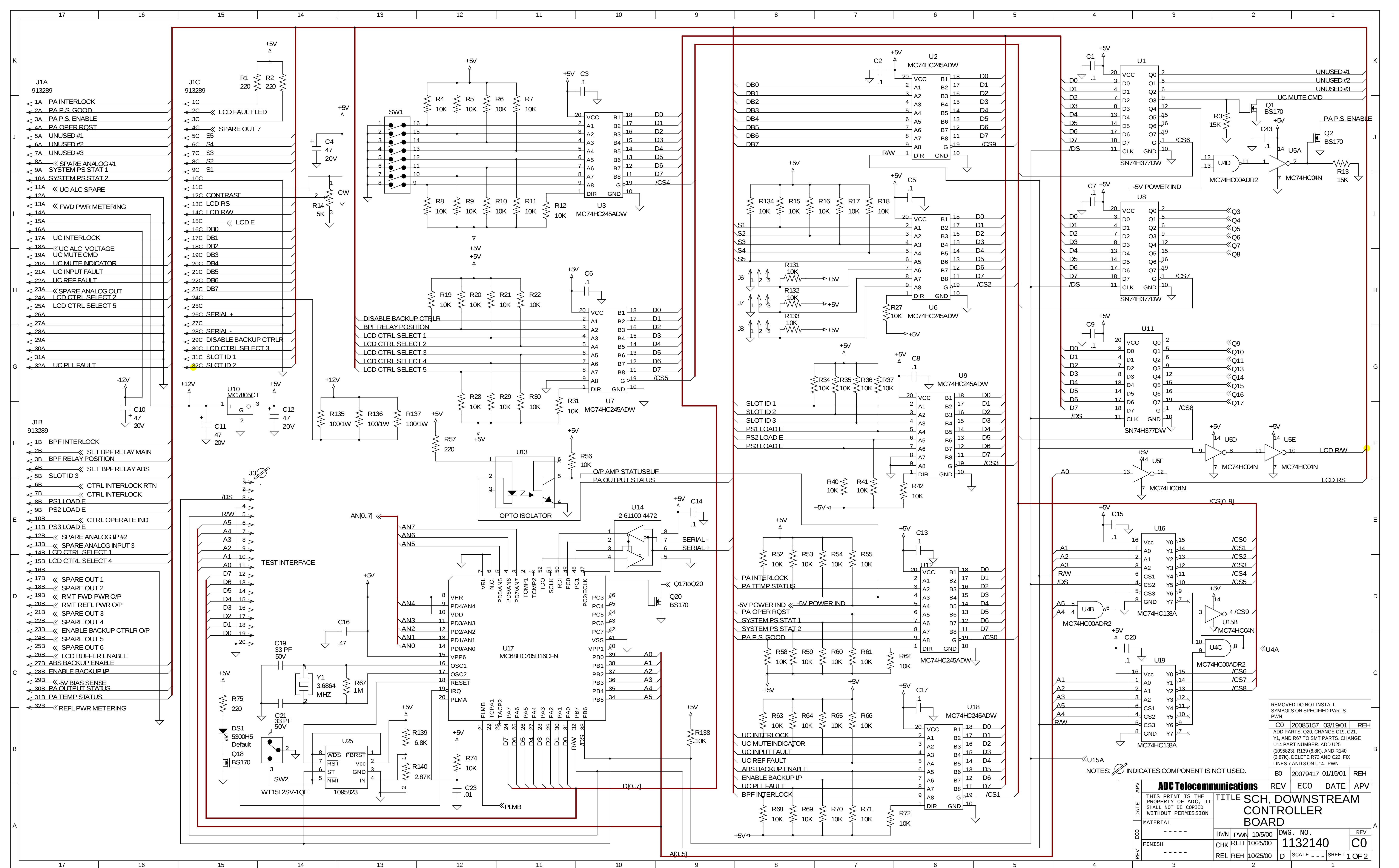
The GPS-XL core receiver specifications are:

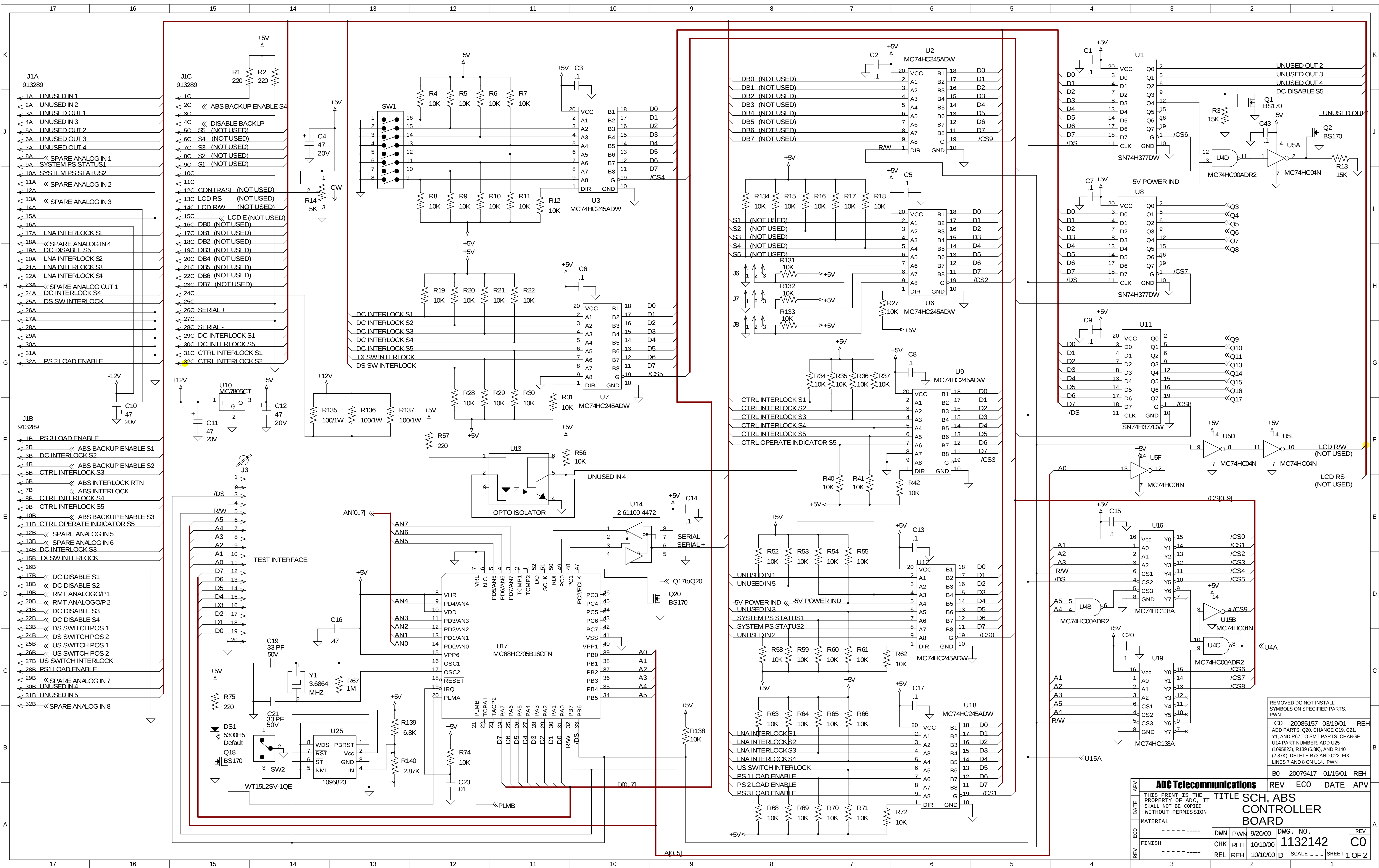
Frequency:	1575.42 MHz (L1 signal).
Code:	Coarse Acquisition (C/A) code.
Tracking:	Up to six satellites.
Acquisition Time:	Less than 2 min if satellites visible, position correct within 100 km. Position errors greater than 100 km may require 15 min or longer, with satellites visible. See Section III.
Single Fix Position Accuracy:	Within 25 m (SEP) referred to WGS84 when sequentially tracking four (4) or more satellites with a PDOP $\leq$ 6. 100 meters (2 dRMS) if SA is enabled.
24 Hour Averaged Position Accuracy:	< 10 m.

The GPS-XL timing and frequency specifications are:

1PPS Output Accuracy:	GPS Time +/- 150 nS. UTC-USNO +/- 150 nS.
Frequency Output Accuracy:	< 3×10^{-12}
Frequency/Timing Stability:	Allan Deviation, 1×10^{-9} @ 1 sec 3×10^{-10} @ 10 sec 3×10^{-10} @ 100 sec 3×10^{-12} @ 1 day
Oscillator Stability:	2×10^{-6} , over 0°C to 50°C when not tracking satellites.
IRIG B Amp. Mod. Output (STANDARD): Accuracy:	10 uS to UTC



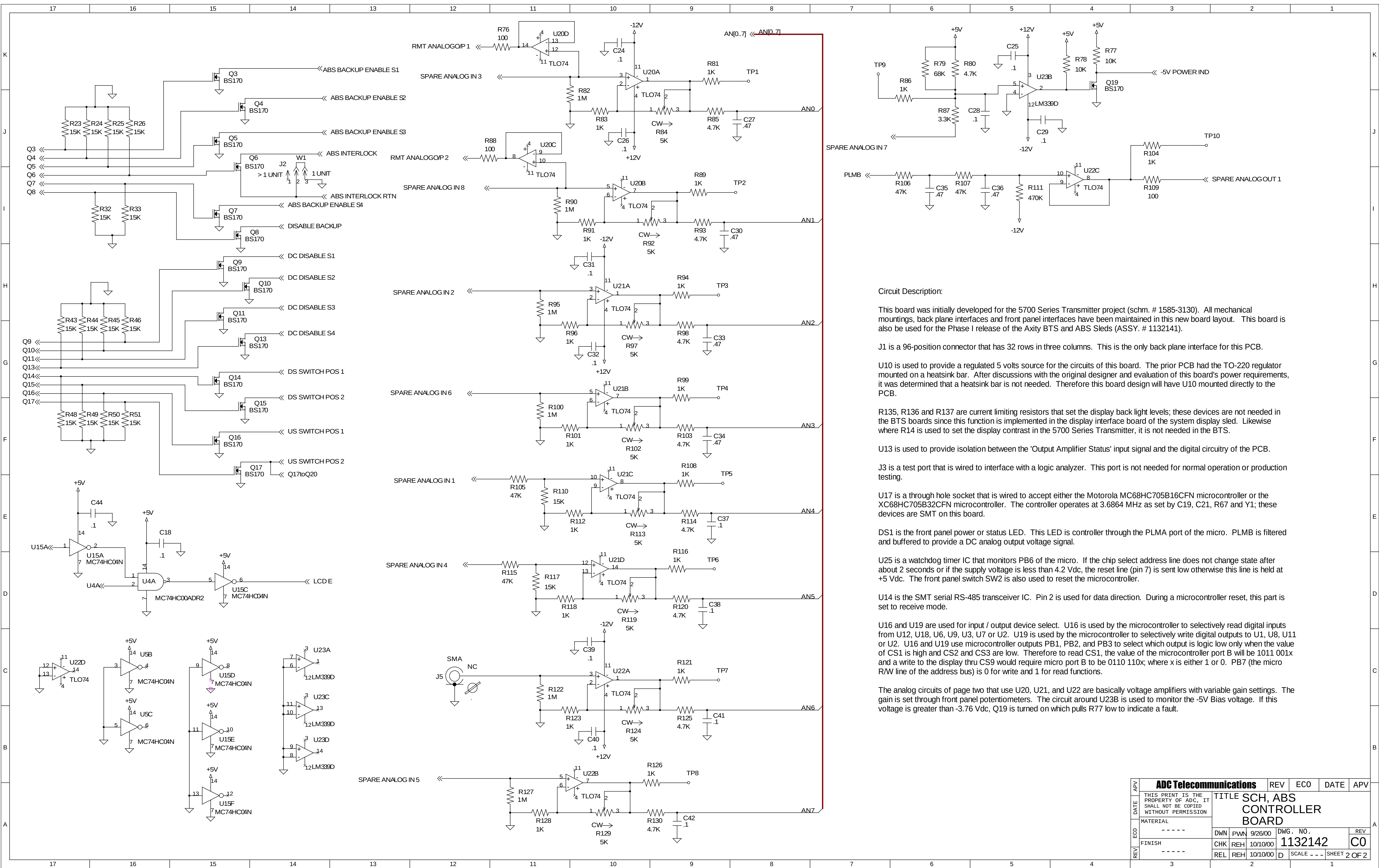




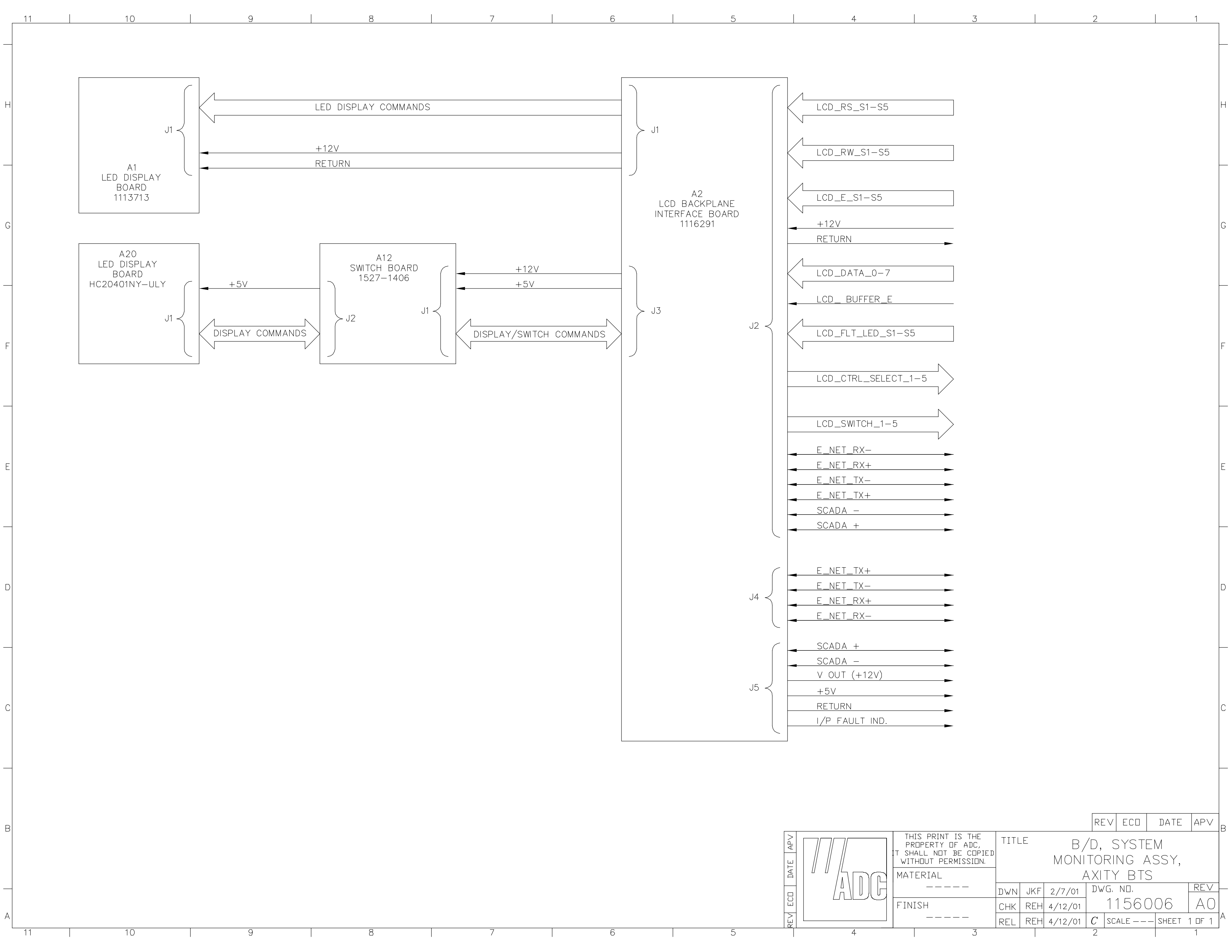
REMOVED DO NOT INSTALL
SYMBOLS ON SPECIFIED PARTS.
PWN

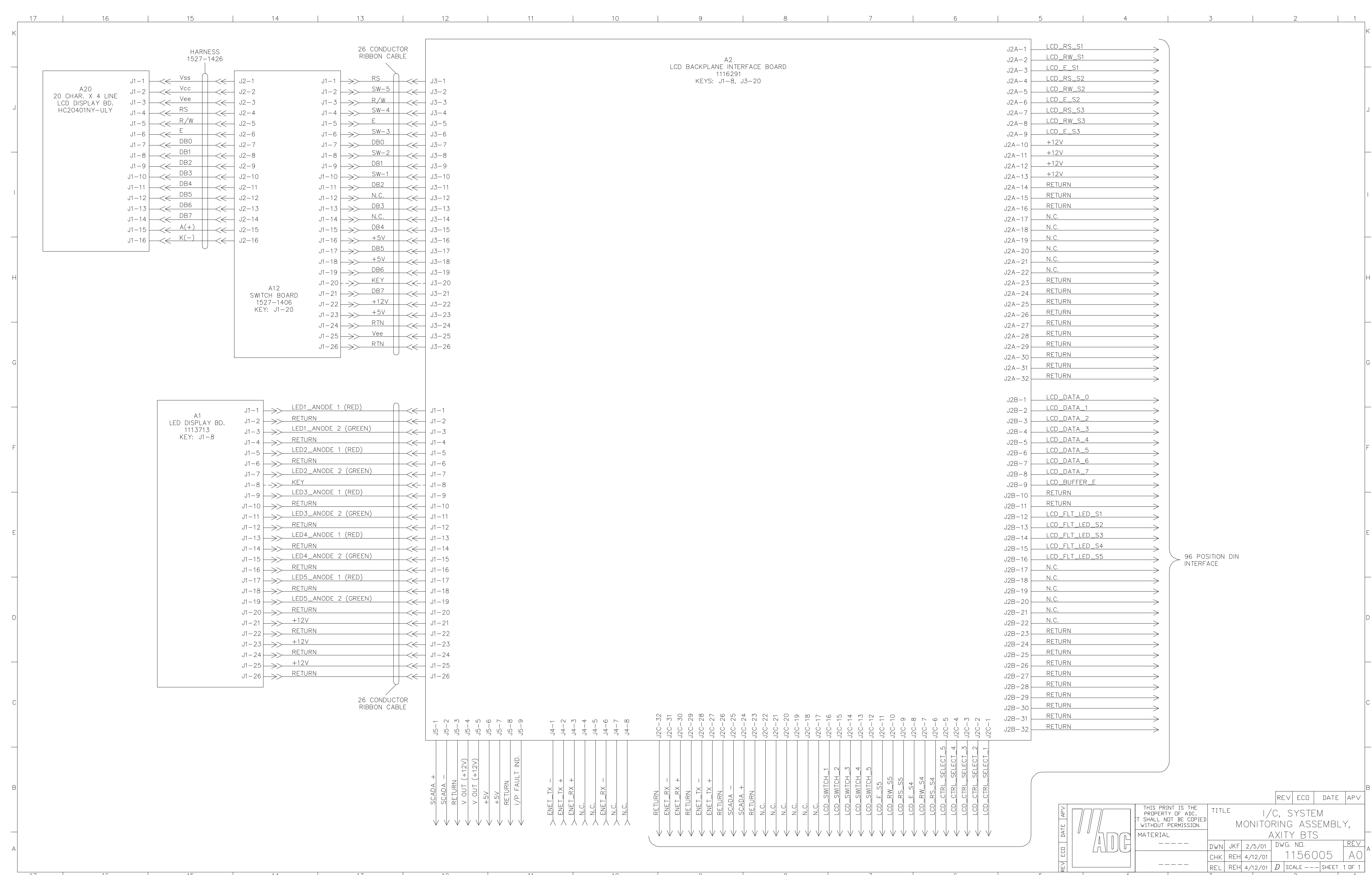
C0	20085157	03/19/01	REH
ADD PARTS: Q20, CHANGE C19, C21, Y1, AND R67 TO SMT PARTS. CHANGE U14 PART NUMBER. ADD U25 (1095823), R139 (6.8K), AND R140 (2.87K). DELETE R73 AND C22. FIX LINES 7 AND 8 ON U14. PWN			
B0	20079417	01/15/01	REH

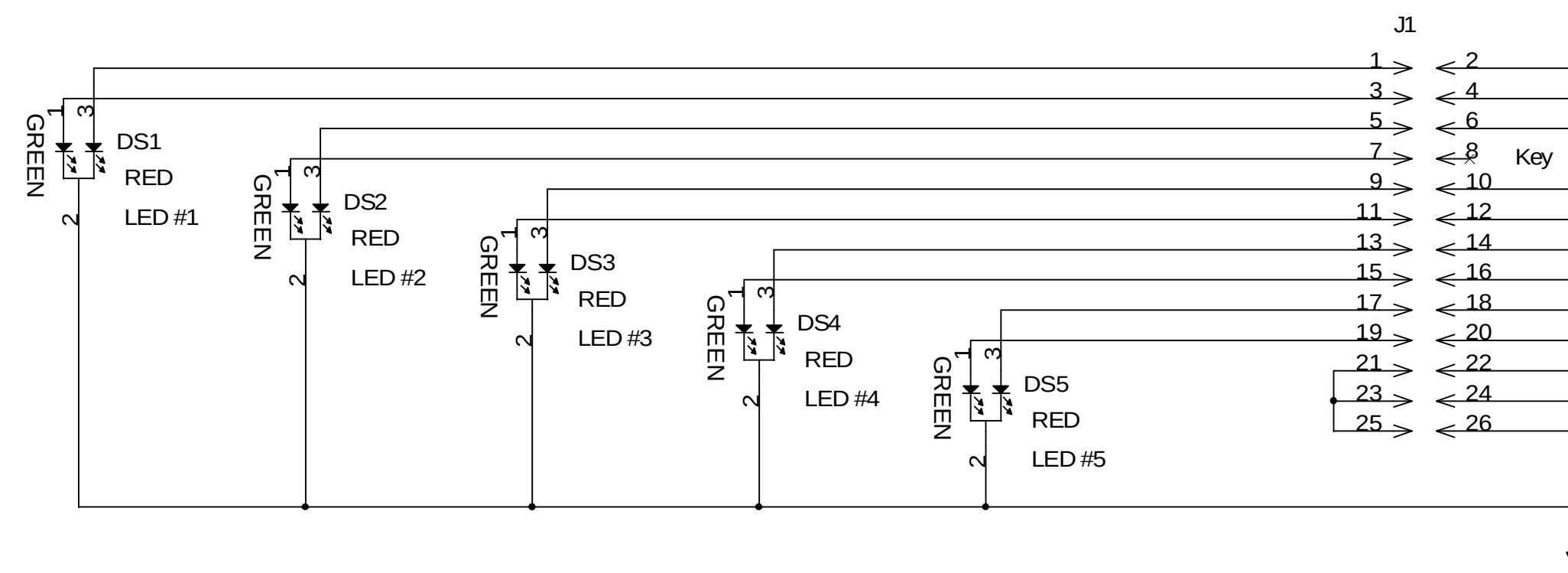
APV				REV			
DATE				ECO			
MATERIAL				FINISH			
-----				-----			
DWN				CHK			
PWN				REL			
9/26/00				10/10/00			
DWG. NO.				SCALE			
1132142				SHEET 1 OF 2			
REV				C0			



APV	ADC Telecommunications				REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION				TITLE SCH, ABS CONTROLLER BOARD			
ECO	MATERIAL				DWN	PWN	DWG. NO.	REV
REV	FINISH				CHK	REH	10/10/00	1132142
					REL	REH	10/10/00	C0
					D	SCALE	---	SHEET 2 OF 2







APV	ADC Telecommunications				REV	ECO	DATE	APV
DATE	THIS PRINT IS THE PROPERTY OF ADC, IT SHALL NOT BE COPIED WITHOUT PERMISSION		TITLE SCH., BWA 2000 FRONT PANEL BD. {1113713}					
ECO	MATERIAL		DWN PWN 6/9/00 DWG. NO.					REV
REV	FINISH		CHK REH 6/9/00		1113710		A0	
	-----		REL REH 6/9/00		D SCALE ---		SHEET 1 OF 1	

