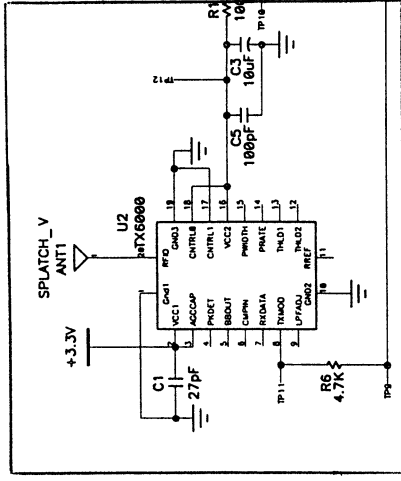
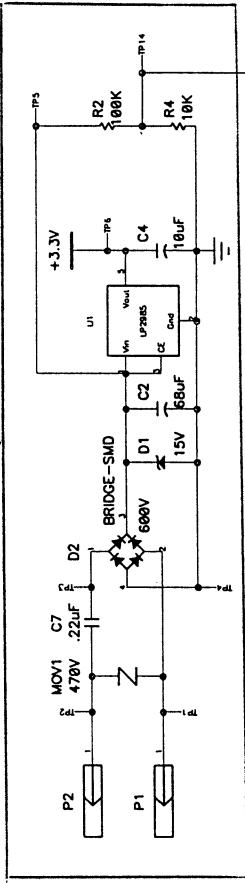


BLOCK DIAGRAM

REVISIONS			
ECO #	REV	DESCRIPTION	DATE
None	0	Prototype	05/09/00
370	1	Production Release	01/10/01

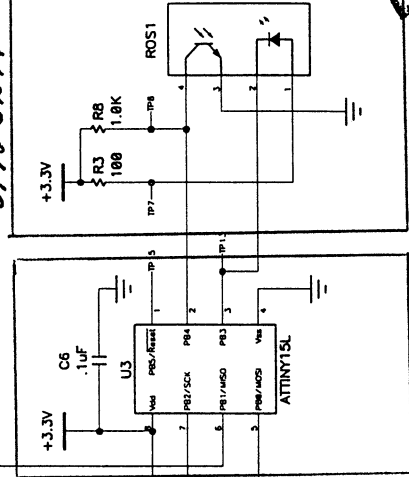
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PWR SPLY



Revision Notes
Rev 1 Changed from Transceiver to Transmitter only. Changed processor for one with internal EEPROM, LVI and voltage comparator.

OPTO INTF



ENCR/CNTR

Test Points TP4, TP6, TP9, TP10, TP14, and TP15 are used for In System Programming of the processor. These should be located in a clear area of the board for easy access.

- TP4 - Gnd
- TP6 - 3.3 VDC
- TP9 - MOSI
- TP10 - SCK
- TP14 - MISO
- TP15 - Reset

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Contract No.	Approvals	DATE	Title		
	Drawn	D. Davis	01/10/01	Schematic, RF OPI	
	Checked	D. Campos			
	Engr	D. Davis			
	Test Engr	R. Brown			
	Q.A.	M. Devine			
Size			CAGE Code	Drawing Number	Rev
A			07LJ5	303056-000	1
Scale: None			File: wopi.SCH	Sheet	1 of 1