

The figure displays 16 timing diagrams for various HDI signals. Each diagram shows a signal trace with a 10P8R-56 time scale. The signals are:

- HDI#50, HDI#61, HDI#56, HDI#62, HDI#54, HDI#53, HDI#58, HDI#60, HDI#24, HDI#21, HDI#23, HDI#16, HDI#20, HDI#11, HDI#7, HDI#30, HDI#38, HDI#36, HDI#37, HDI#39, HDI#28, HDI#22, HDI#34, HDI#43, HDI#9, HDI#3, HDI#16, HDI#13, HDI#12, HDI#5, HDI#15, HDI#28, HDI#63, HDI#57, HDI#55, HDI#46, HDI#40, HDI#52, HDI#48, HDI#59, HDI#19, HDI#29, HDI#32, HDI#31, HDI#26, HDI#25, HDI#33, HDI#35, HDI#2, HDI#14, HDI#3, HDI#13, HDI#10, HDI#12, HDI#9, HDI#18, HDI#51, HDI#49, HDI#41, HDI#47, HDI#45, HDI#44, HDI#42, HDI#48, HDI#27, HDI#1, HDI#5, HDI#8, HDI#4, HDI#6, HDI#7, HDI#15, HDI#4, HDI#17, HDI#15, HDI#4, HDI#6, HDI#7, HDI#15, HDI#4.

	VCCP	SDRAM11	SDRAM17	SDRAM19
D1	B26	VCC1		
D2	C0	VCC2		
D3	AE2	VCC3		
D4	AE2	VCC4		
D5	AB2	VCC5		
D6	J2	VCC6		
D7	K2	VCC7		
D8	F4	VCC8		
D9	F4	VCC9		
D10	F5	VCC10		
D11	AE4	VCC11		
D12	AE5	VCC12		
D13	AA5	VCC13		
D14	W5	VCC14		
D15	NS5	VCC15		
D16	NS5	VCC16		
D17	J5	VCC17		
D18	F3	VCC18		
D19	NS5	VCC19		
D20	B6	VCC20		
D21	AM8	VCC21		
D22	AM8	VCC22		
D23	F3	VCC23		
D24	B10	VCC24		
D25	B10	VCC25		
D26	AM12	VCC26		
D27	AM13	VCC27		
D28	F13	VCC28		
D29	B14	VCC29		
D30	AM16	VCC30		
D31	AM17	VCC31		
D32	B18	VCC32		
D33	AM20	VCC33		
D34	AM20	VCC34		
D35	AM21	VCC35		
D36	F22	VCC36		
D37	AM24	VCC37		
D38	AM24	VCC38		
D39	AM25	VCC39		
D40	F26	VCC40		
D41	F26	VCC41		
D42	AM28	VCC42		
D43	AM28	VCC43		
D44	AK34	VCC44		
D45	F30	VCC45		
D46	F30	VCC46		
D47	B30	VCC47		
D48	AM32	VCC48		
D49	AM32	VCC49		
D50	Z32	VCC50		
D51	V32	VCC51		

PCI Routing

PCI1 : AD25 PIRQ#A
 PCI2 : AD26 PIRQ#B
 PCI3 : AD27 PIRQ#C
 PCI4 : AD28 PIRQ#D
 PCI5 : AD29 PIRQ#B
 AGP1 PIRQ#A
 CT5880:AD23 PIRQ#C
 USB : AD23 PIRQ#D

81E : INSTALL
 81B : DON'T INSTALL

R65

0

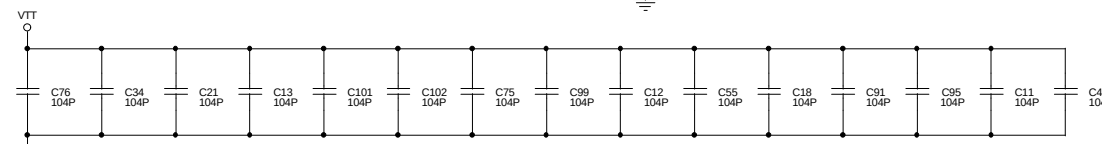
VTT

VCC3

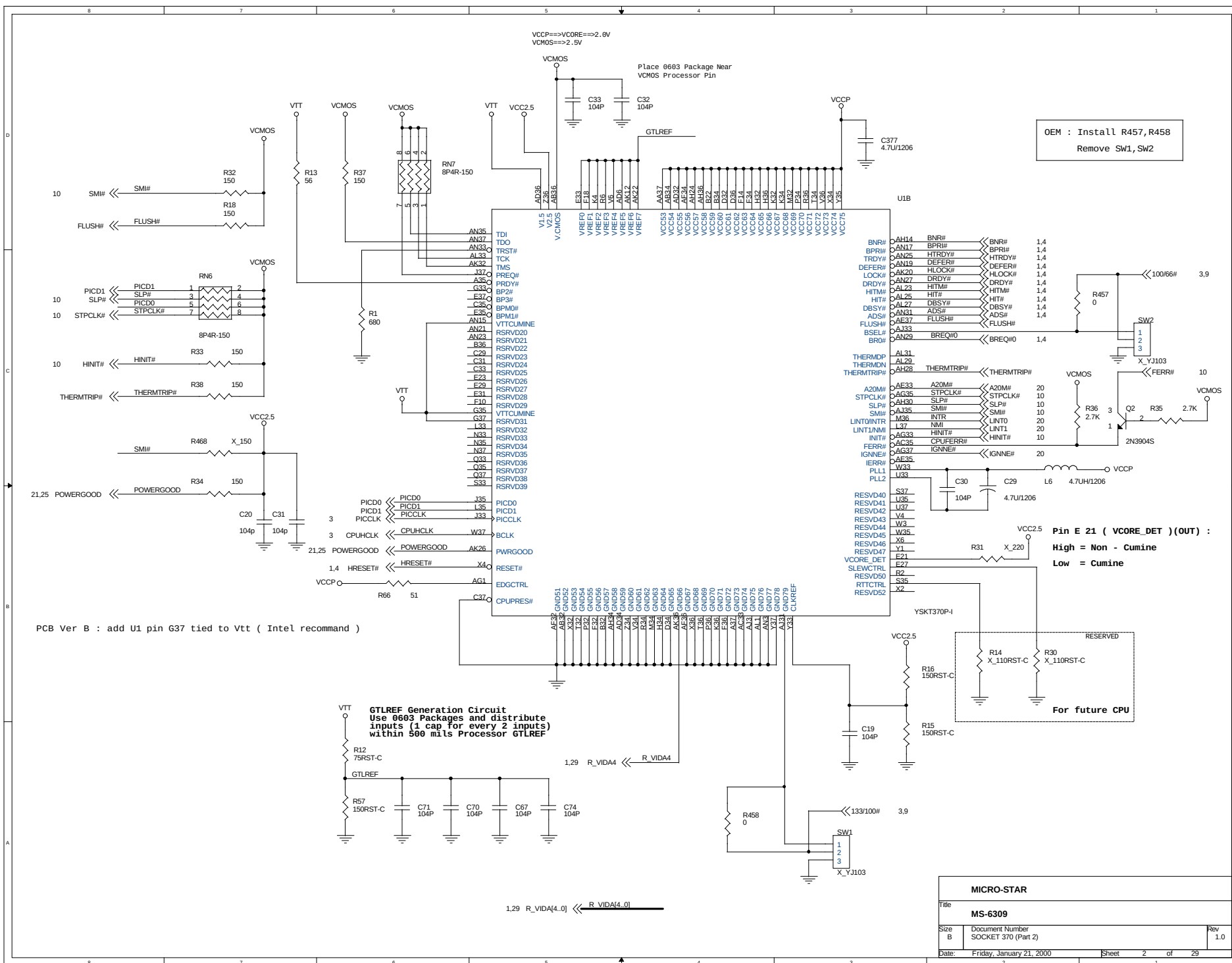
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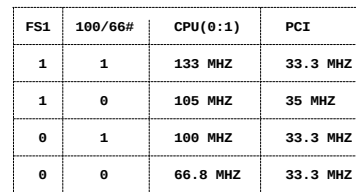
PC11 : AD25 PIRQ#A
PC12 : AD26 PIRQ#B
PC13 : AD27 PIRQ#C
PC14 : AD28 PIRQ#D
PC15 : AD29 PIRQ#B
AGP1  PIRQ#A
CT5880:AD23 PIRQ#C
USB   : AD23 PIRQ#D

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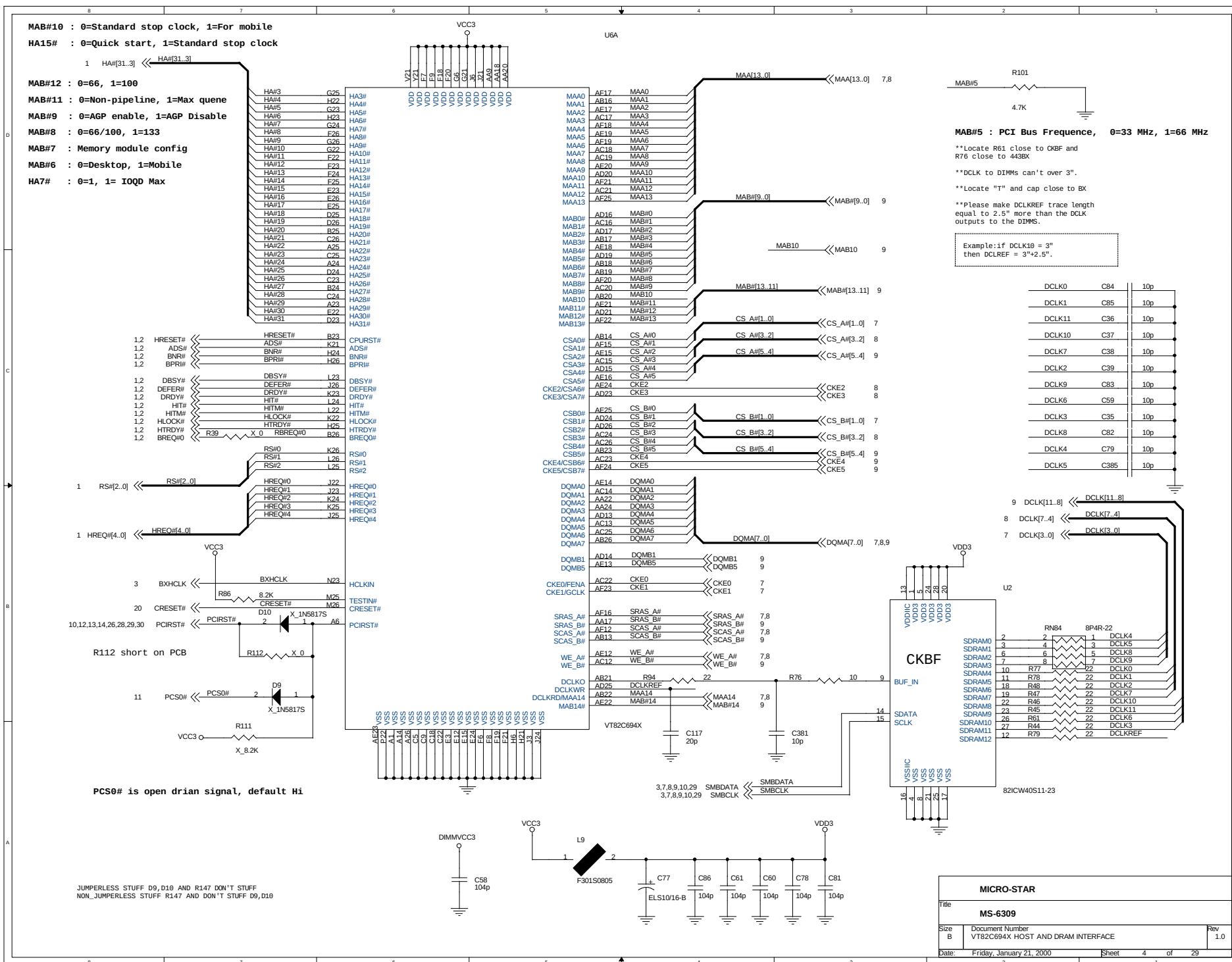


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B	SOCKET 370 (Part 1)	1.0	
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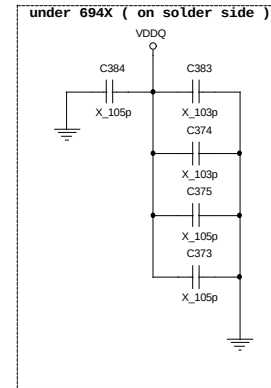
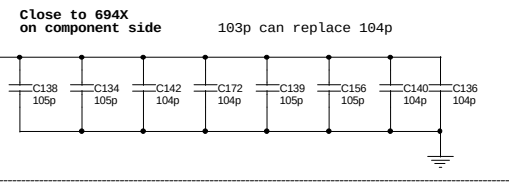
NET	TRACE	MIN	MAX
R193 CPU	H	1.0 ⁿ	9.0 ⁿ
R194 U7	H+3.25 ⁿ	1.0 ⁿ	12.0 ⁿ
R225 PC11	H+4.0 ⁿ	1.0 ⁿ	12.5 ⁿ
R224 PC12	H+4.0 ⁿ	1.0 ⁿ	12.5 ⁿ
R223 PC13	H+4.0 ⁿ	1.0 ⁿ	12.5 ⁿ
R226 PC14	H+7.3 ⁿ	1.0 ⁿ	12.5 ⁿ
R221 U7	H+7.5 ⁿ	1.0 ⁿ	15.0 ⁿ
R220 U18	H+7.5 ⁿ	1.0 ⁿ	15.0 ⁿ



NOTE : AGP LAYOUT LENGTH LIMITATION.

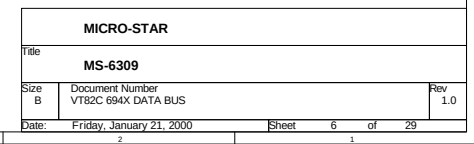
440BX TO AGP SLOT LENGTH : Min = 1", Max = 9".

Stuffing option to enable and test
the POS state.

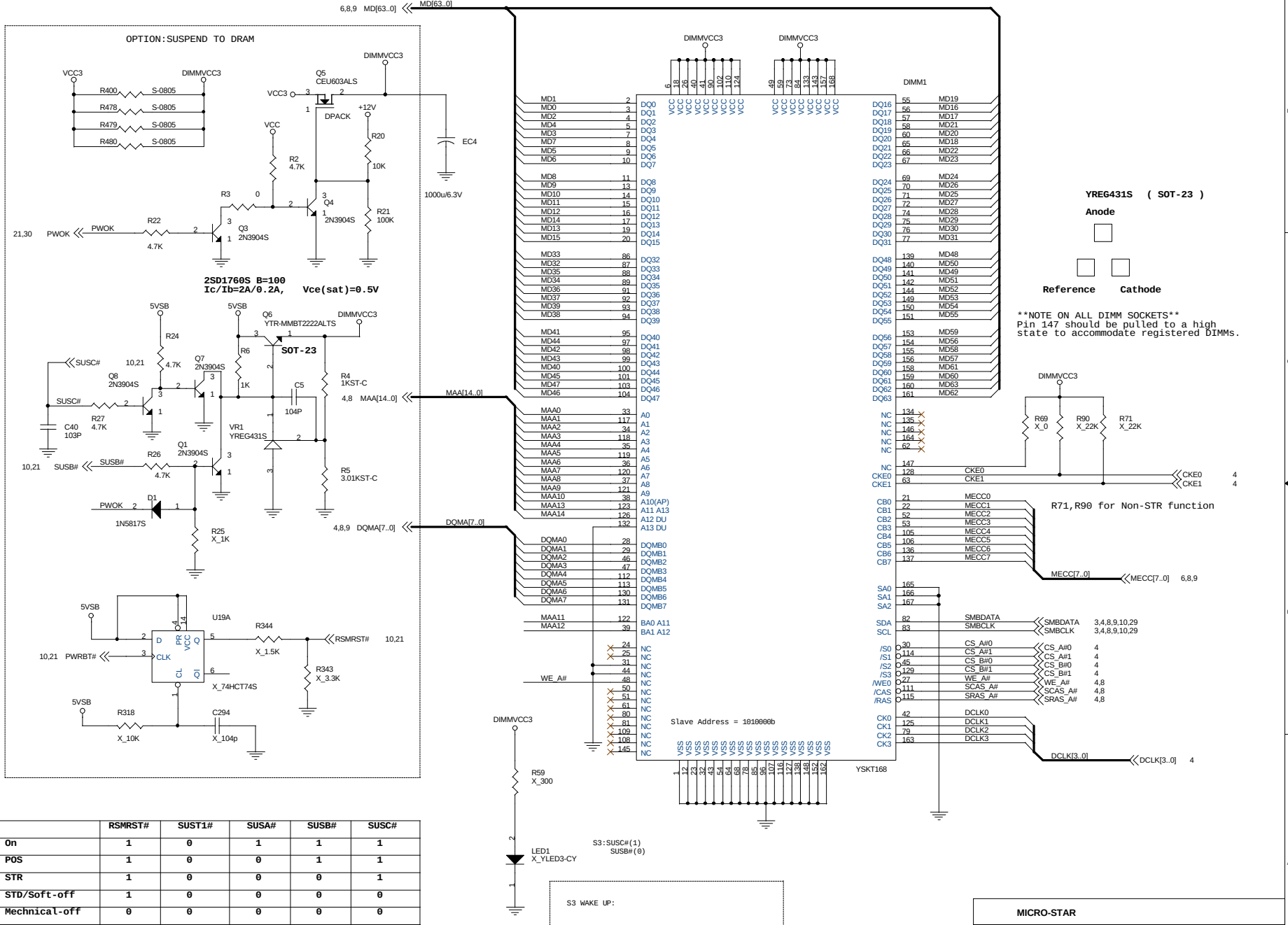


R44 & R46 must to closed VT82C694X
GCLKI = GCLKOUT + 3000 mils
Stub to tee should be 1" MAX.

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B	VT82C694X PCI AND AGP INTERFACE	1.0
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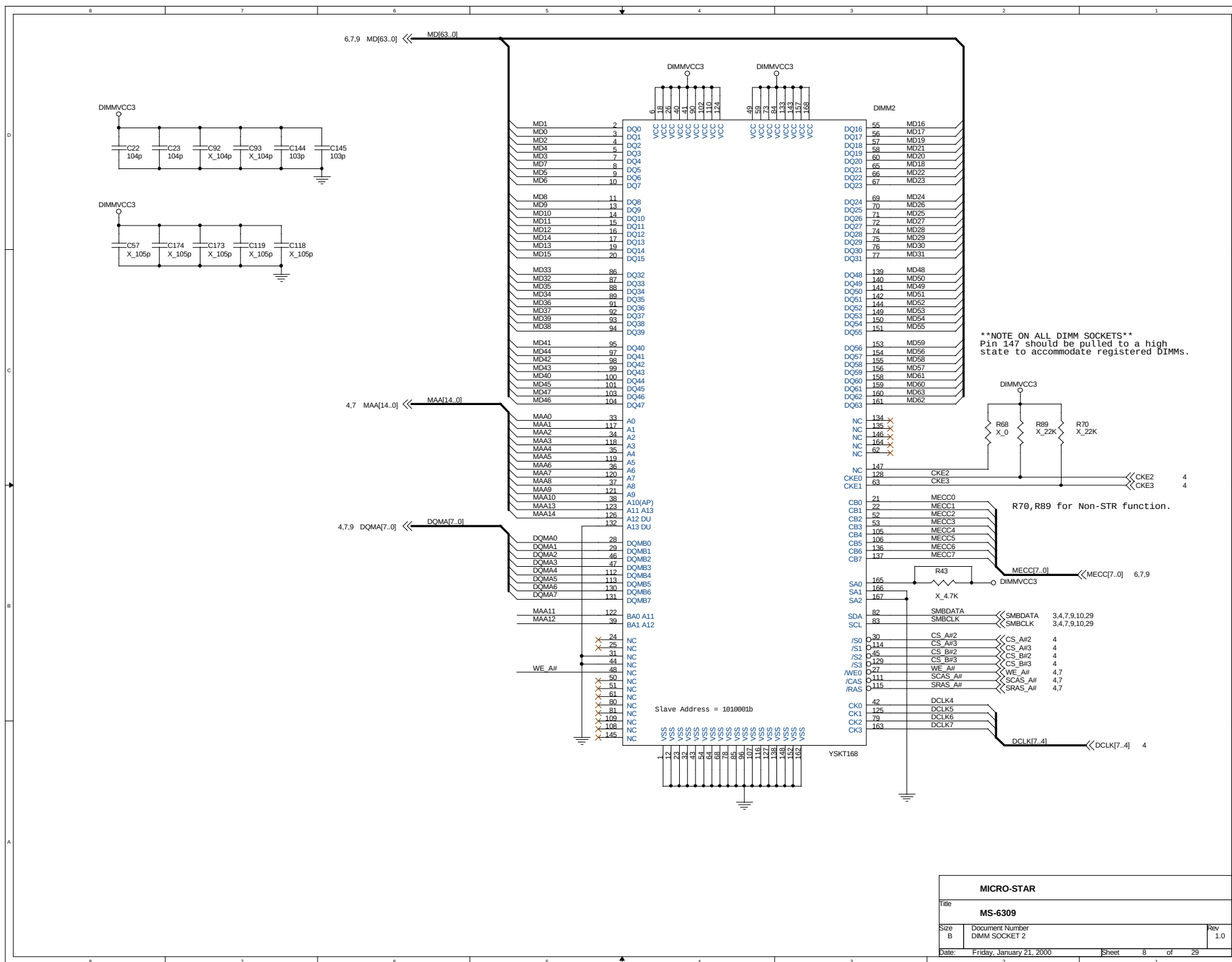


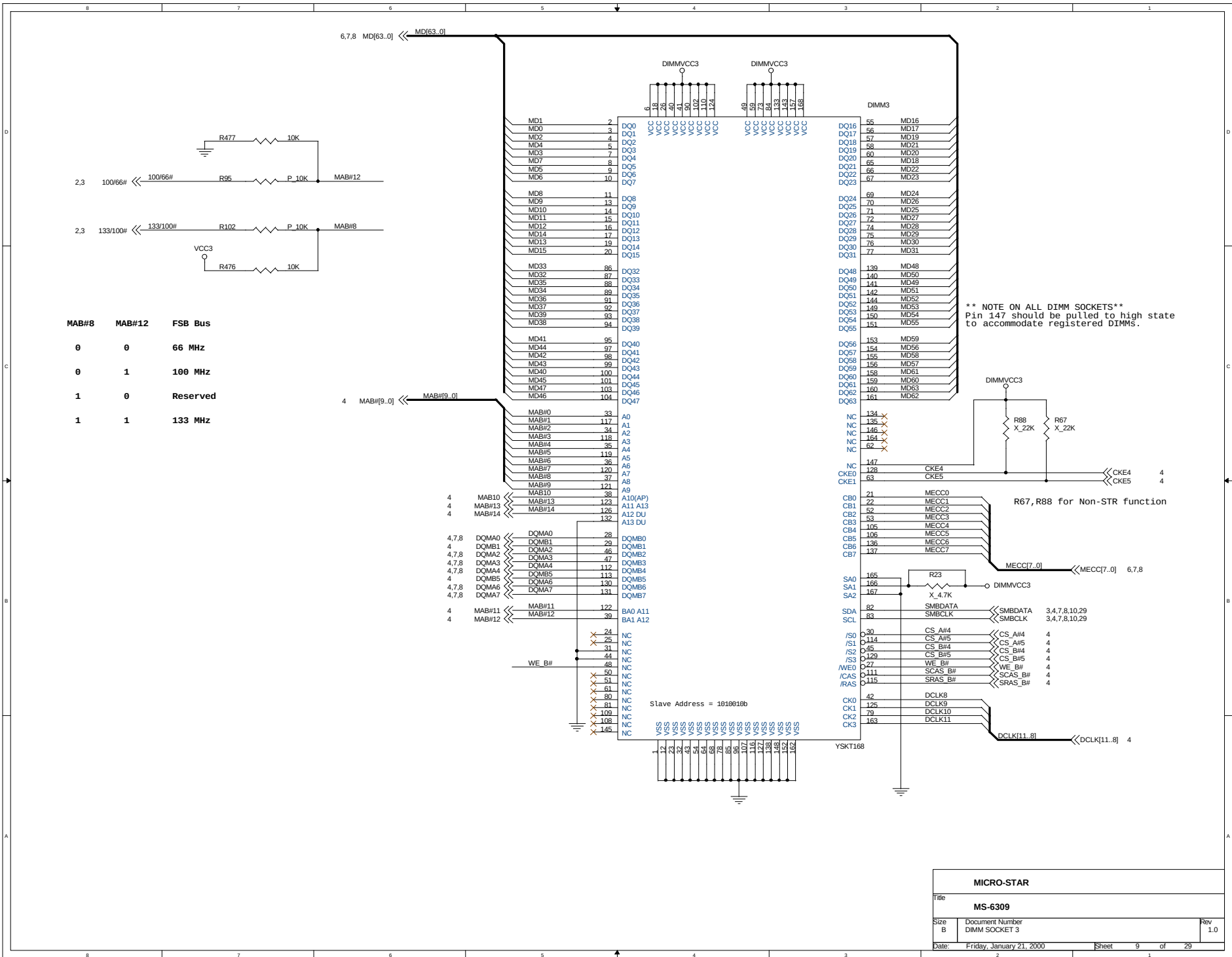
IF ENABLE SUSPEND TO DRAM JDIM1 AND JDIM2 SHORT

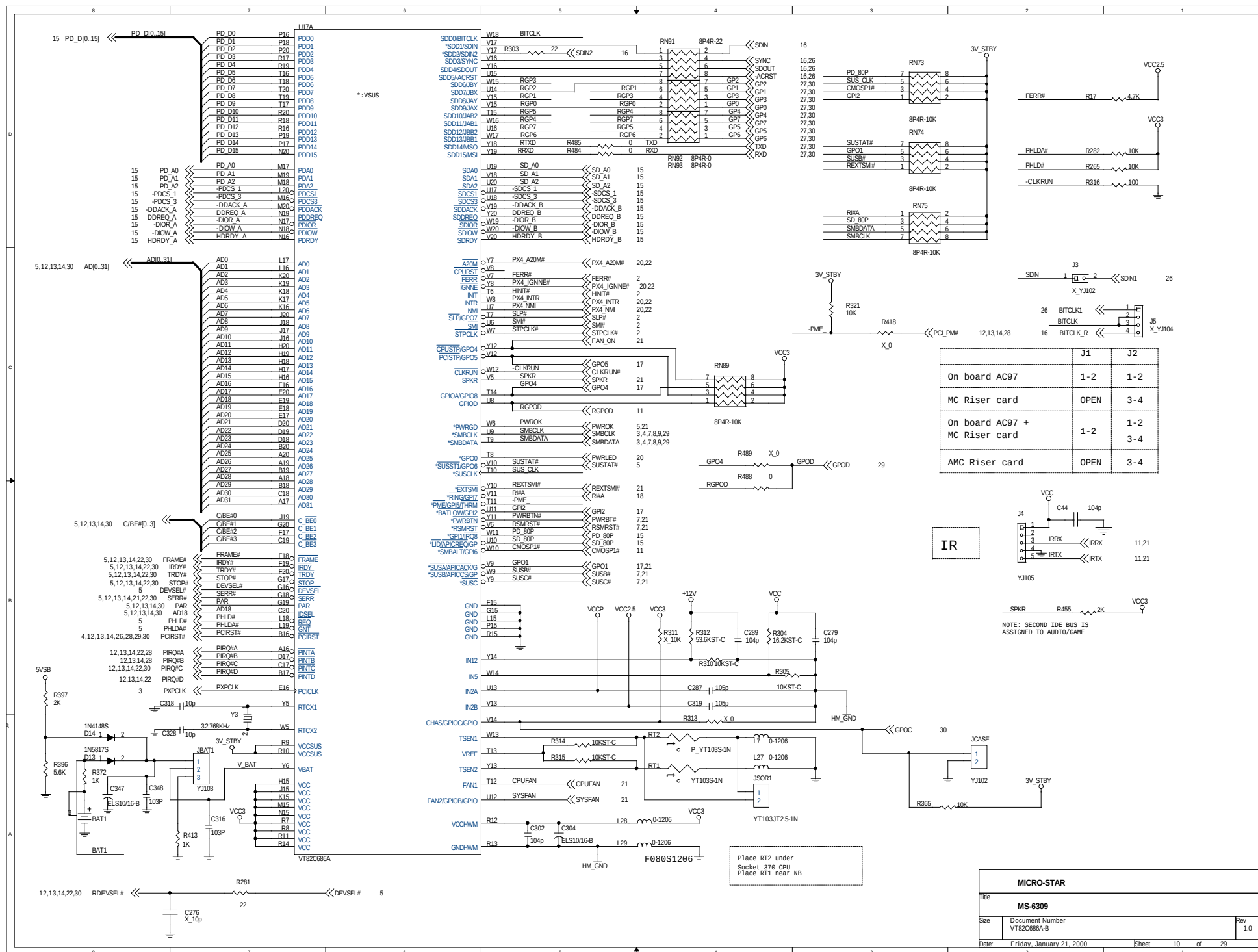


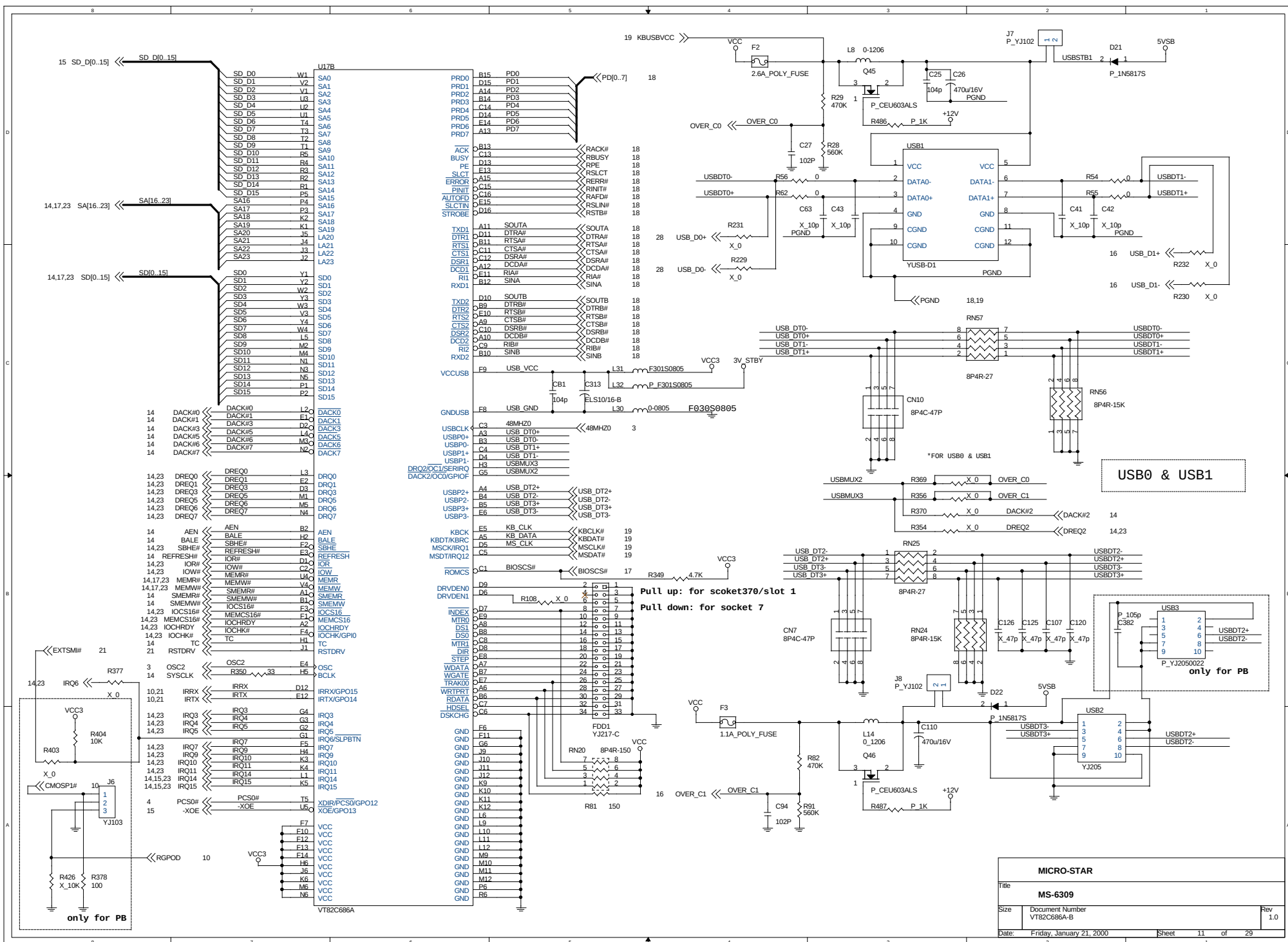
MICRO-STAR

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DIMM SOCKET 1		
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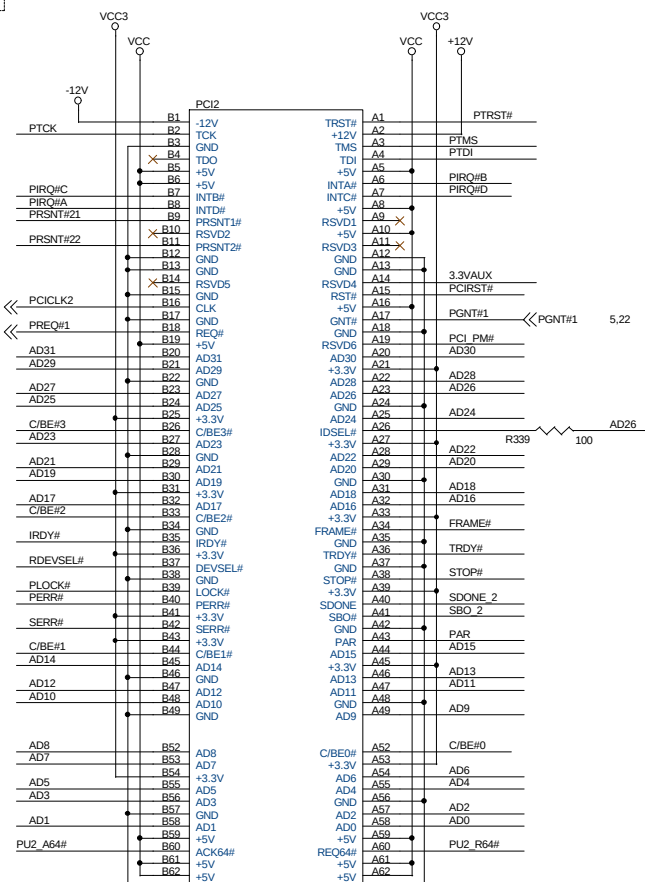
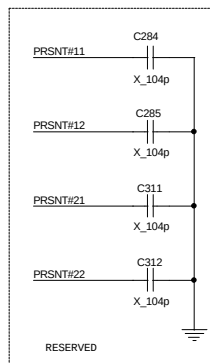
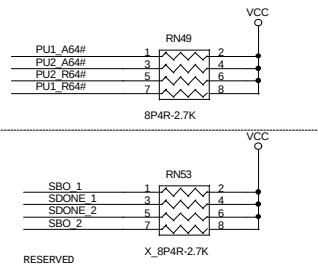
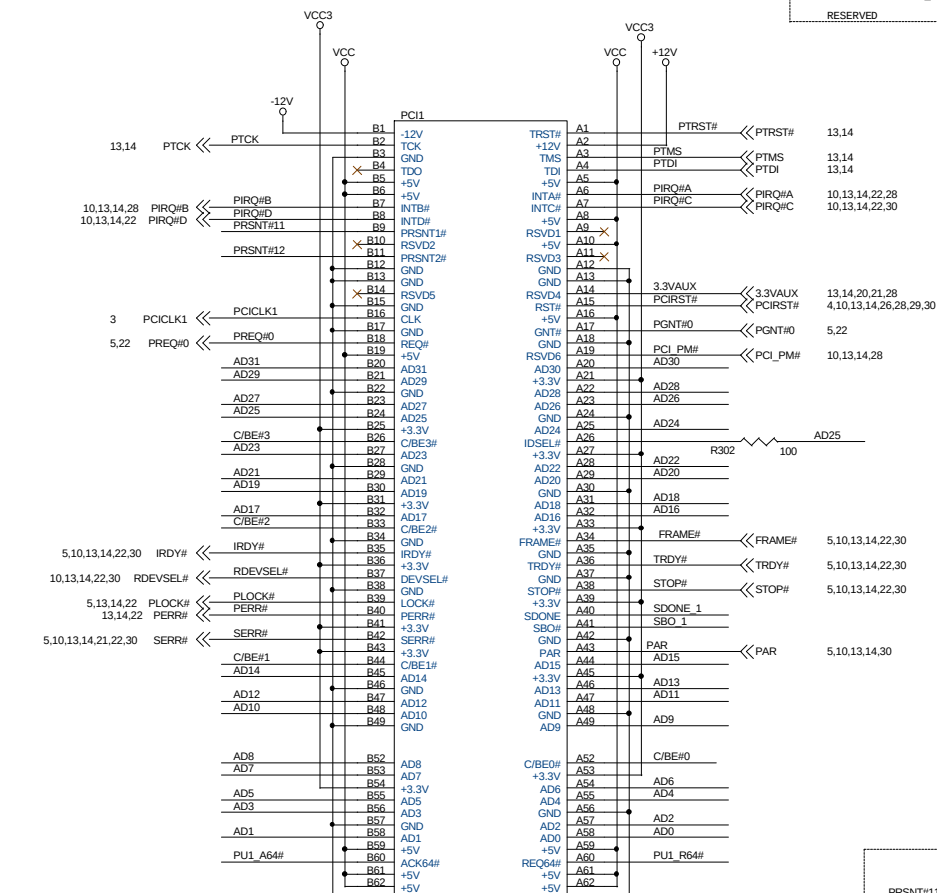
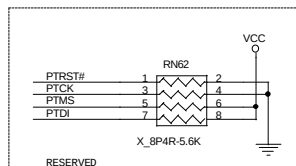




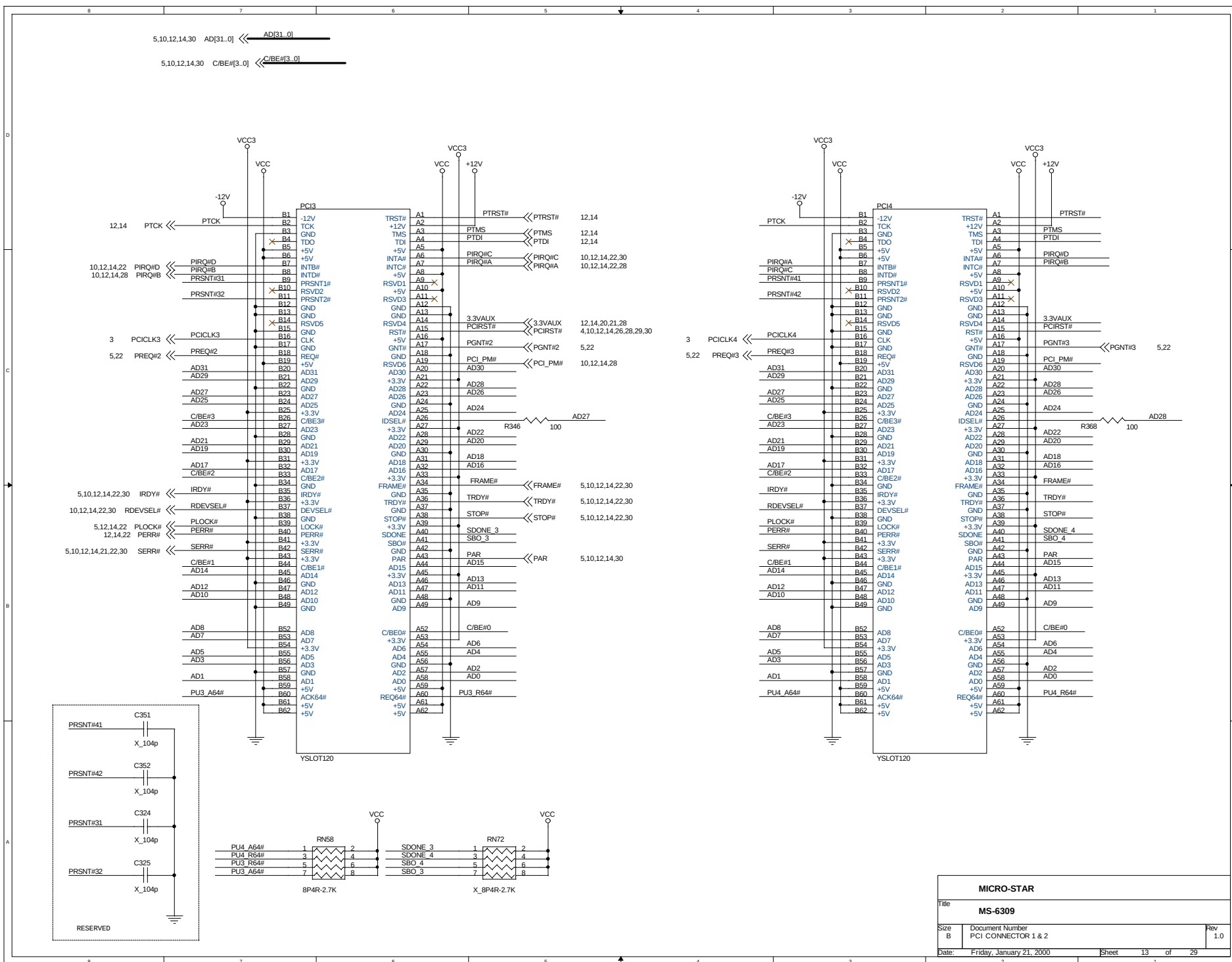


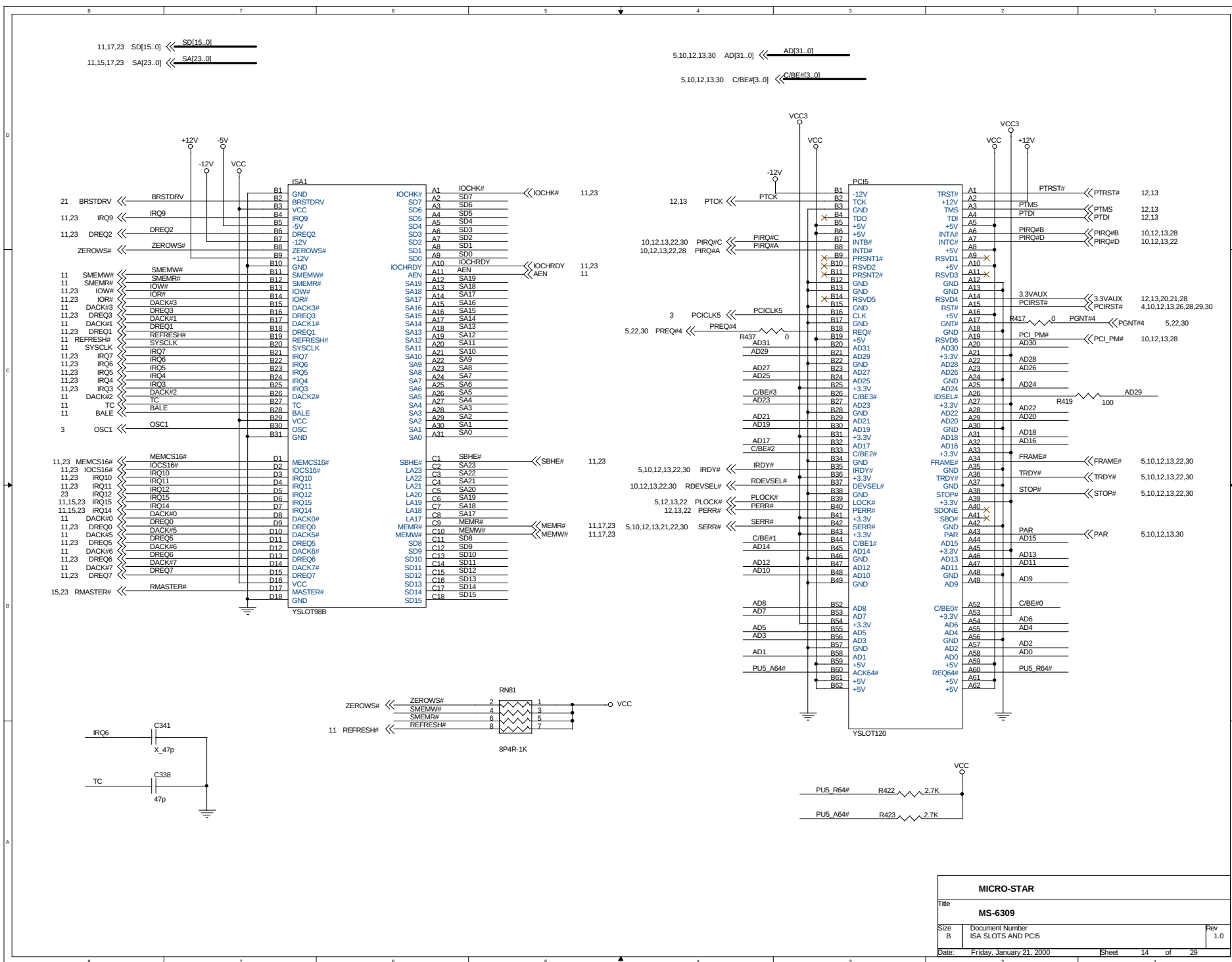


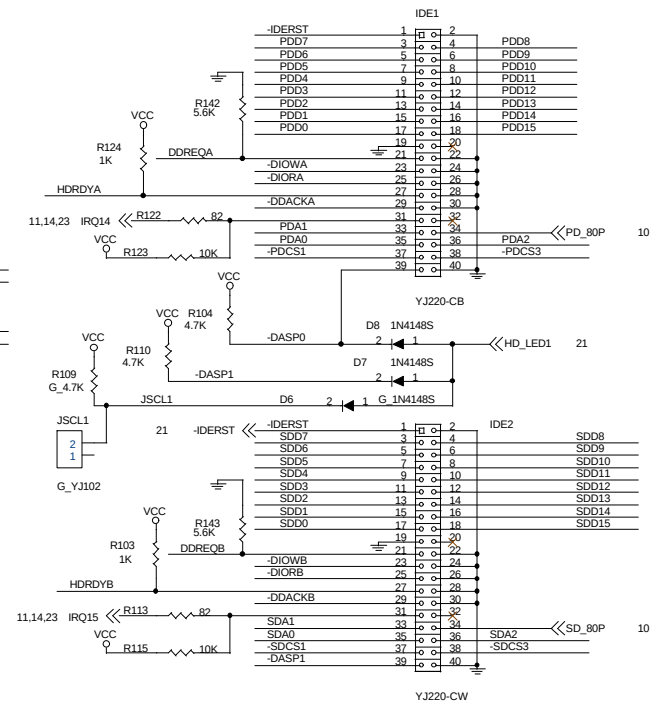
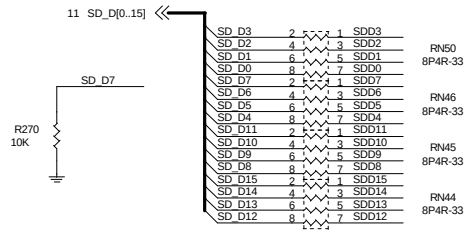
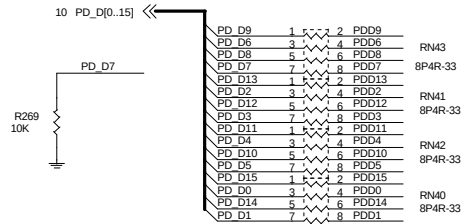
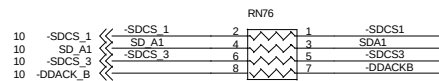
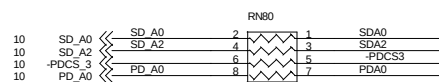
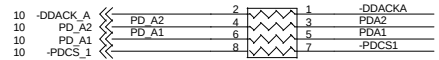
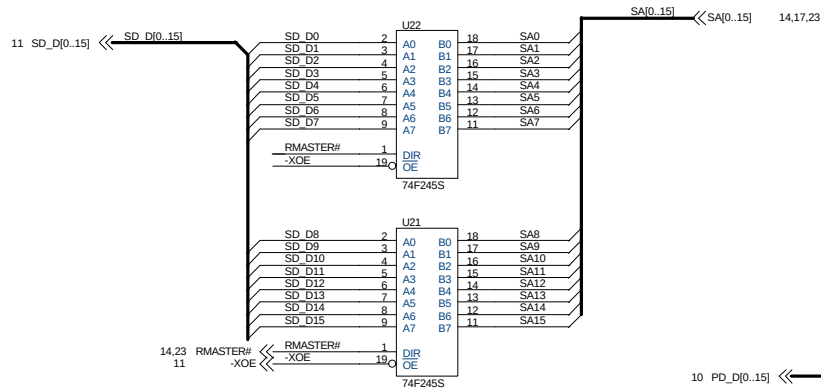
5,10,13,14,30 AD[31..0] << AD[31..0]
5,10,13,14,30 C/BE#[3..0] << C/BE#[3..0]



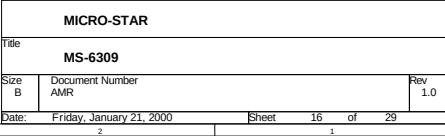
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Title			
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B	PCI CONNECTOR 1 & 2	1.0	
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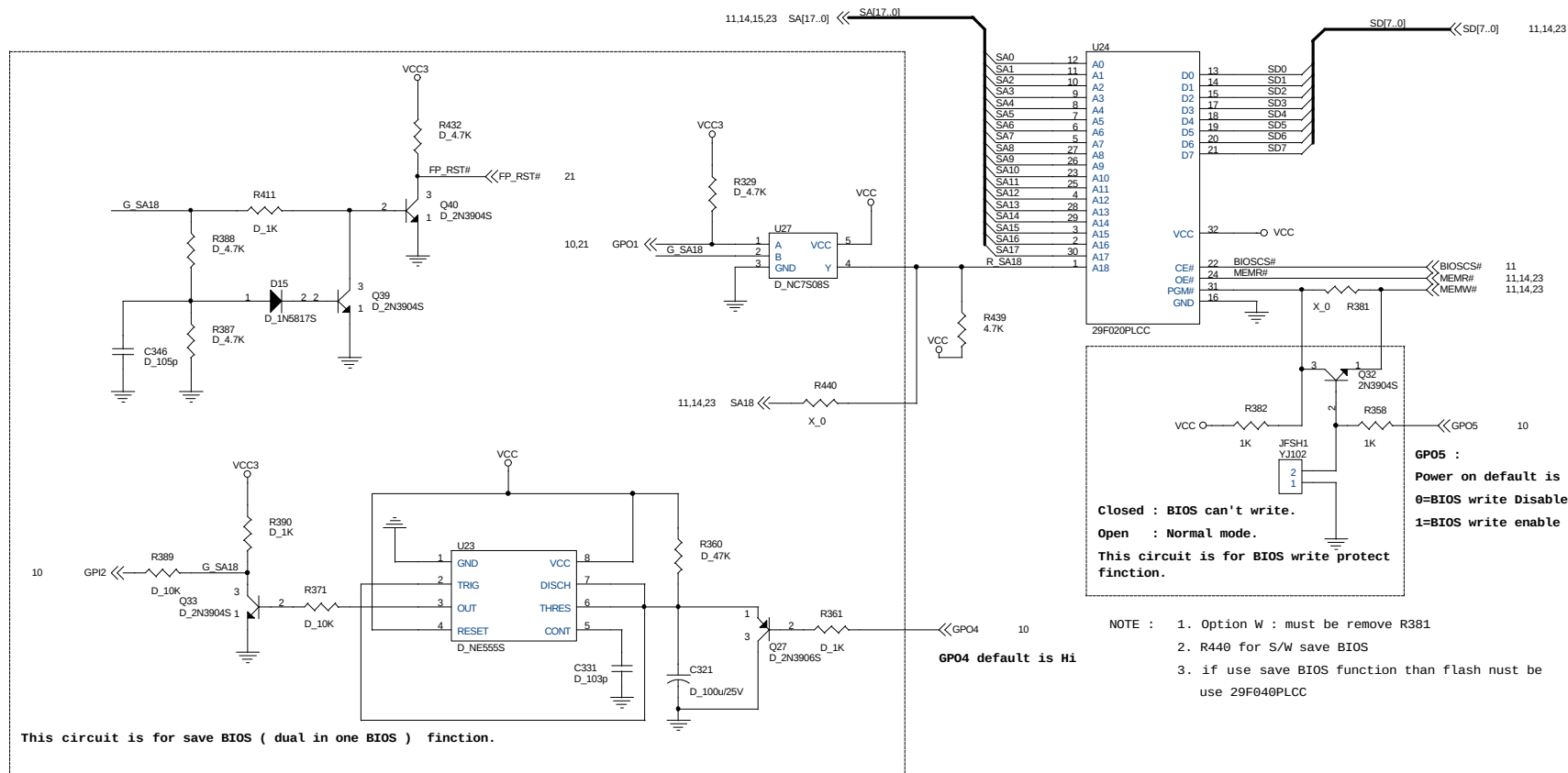




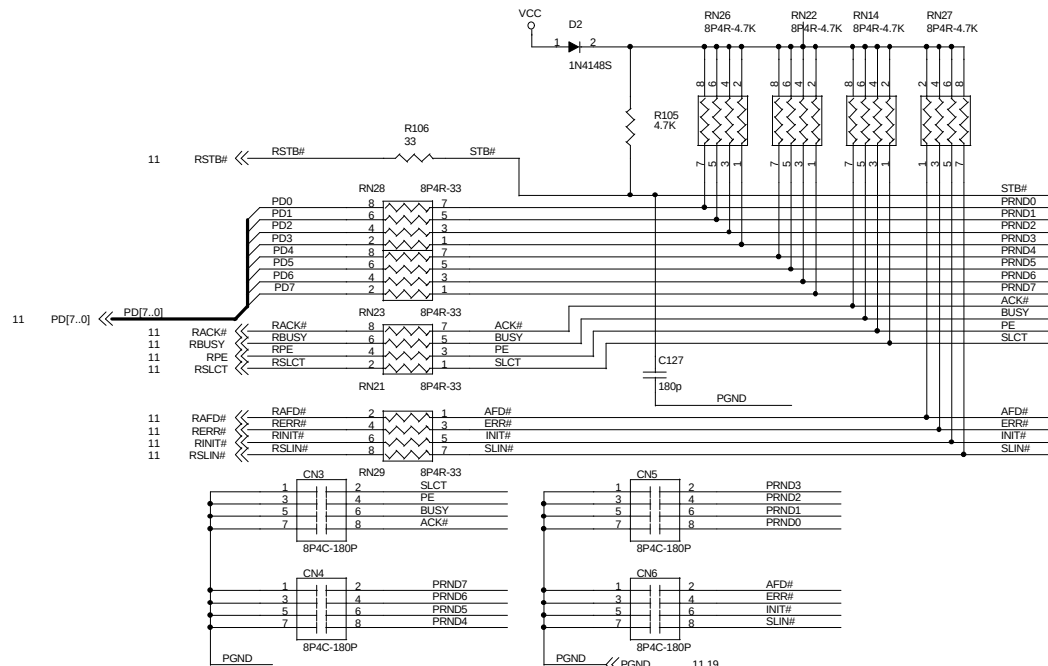
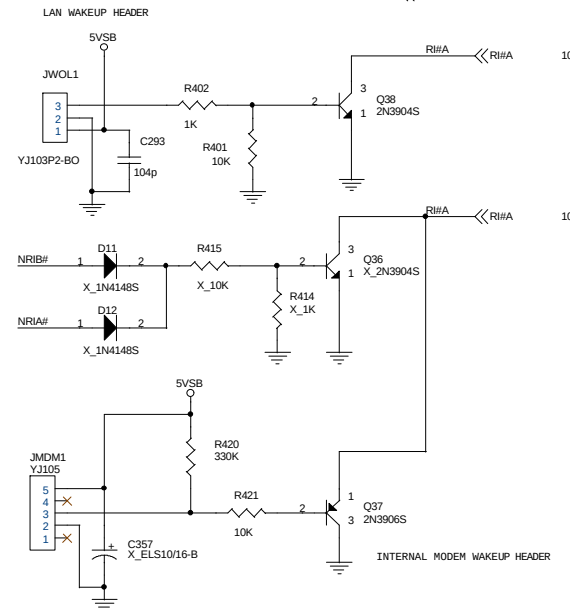
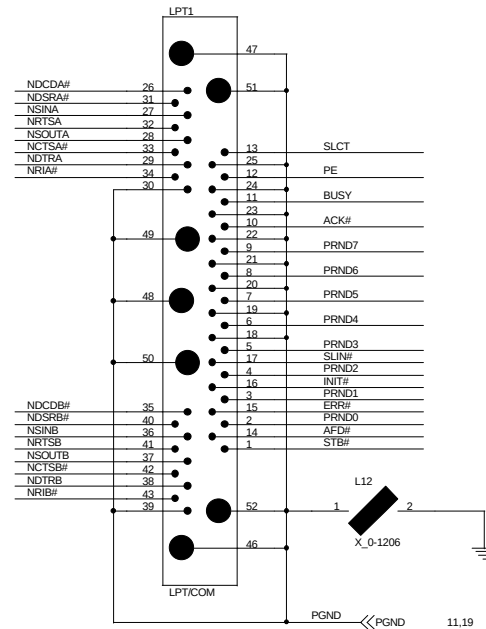
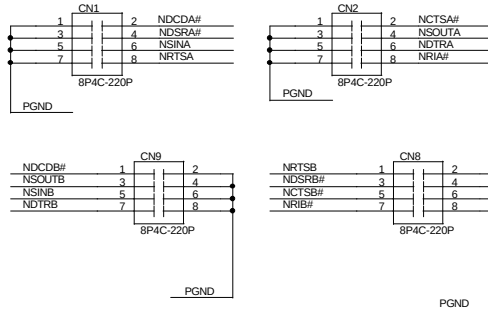
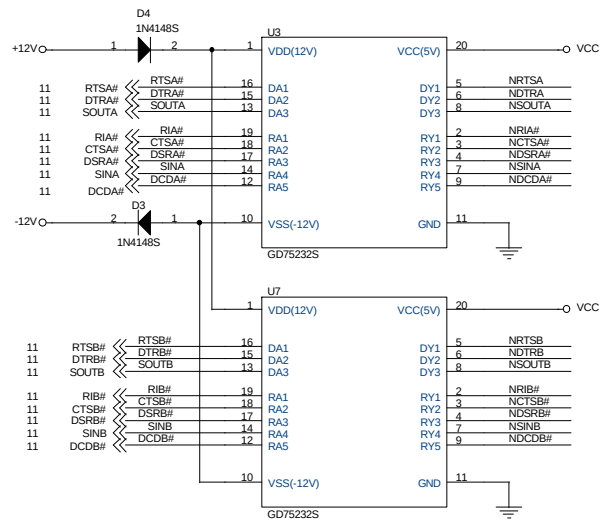


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B	FLASH MEMORY		1.0
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COM1/COM2/LPT1 CONNECTOR		
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If used KB & MS wake up
install JVSBI jumper,
else used jumper wire
short 2-3 pin.

KB password wakeup enable jumper

EN:1-2
DIS:2-3

FUSE USE POLY SWITCH FUSE

1206 SIZE

L1 X_0-1206

KBMSVCC

C24
104p

PGND

JKBMS1

1 7
2 8
3 9
4 10
5 11
6 12

YDM12P-1

C1
104p

PGND

C2
330p

PGND

C6
330p

PGND

C7
330p

PGND

C3
330p

PGND

11,18 PGND

Not support keyboard wakeup.

MICRO-STAR

Title

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Size
B

Document Number
KEYBOARD

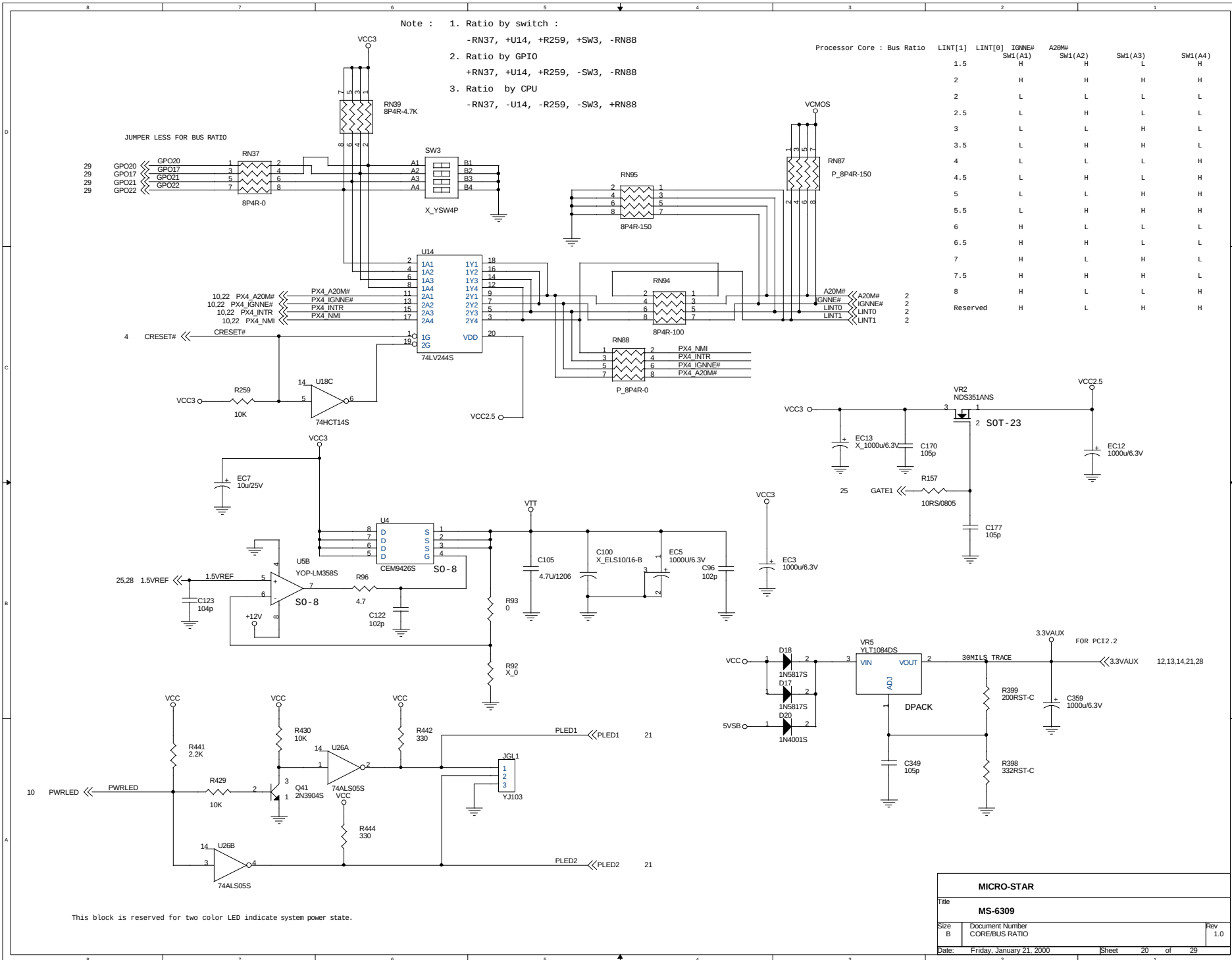
Rev
1.0

Date: Friday, January 21, 2000

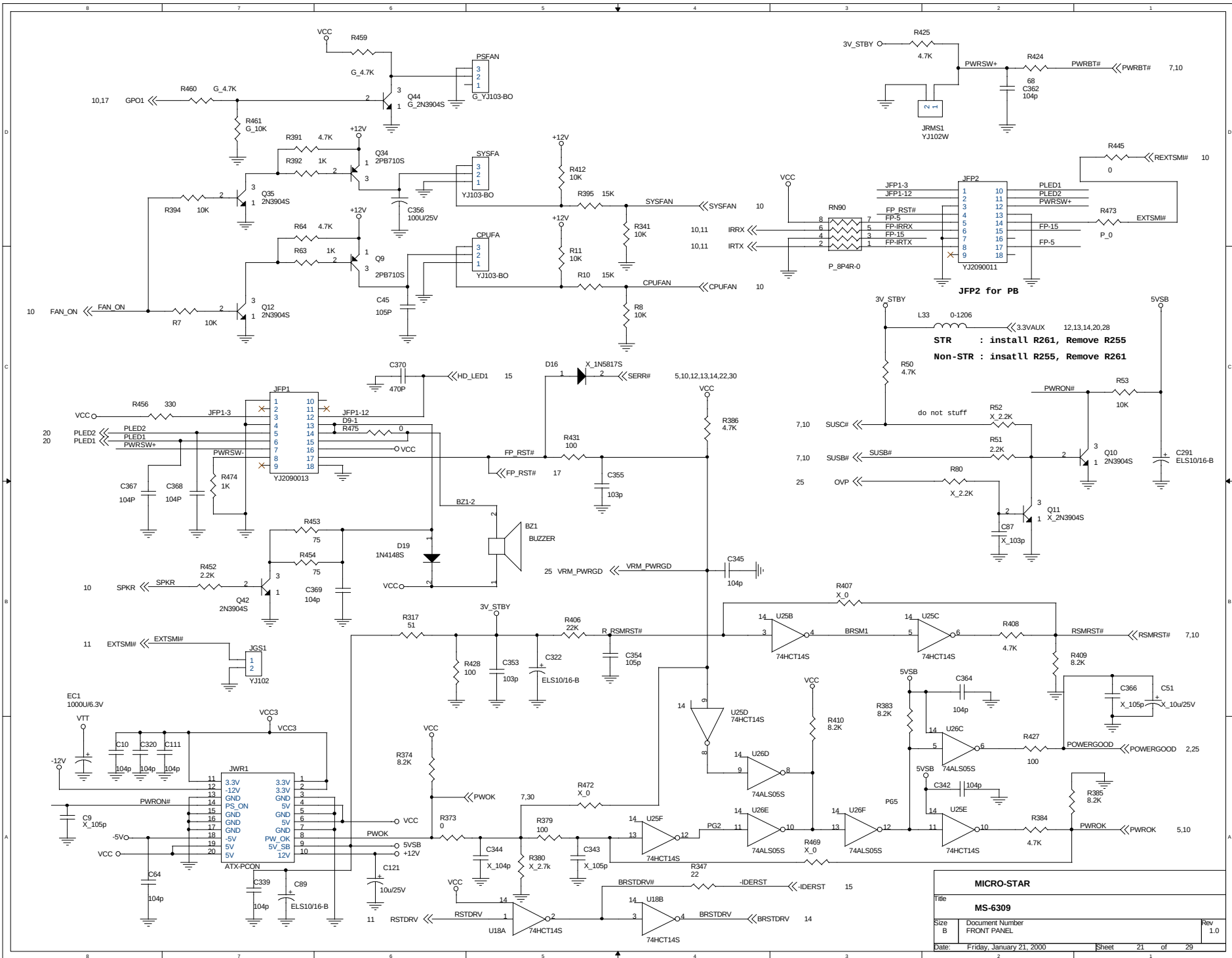
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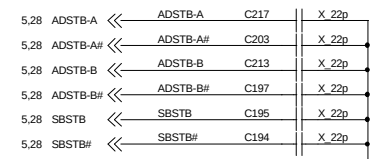
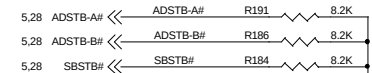
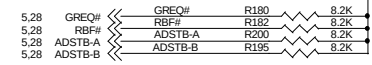
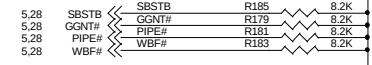
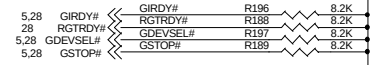
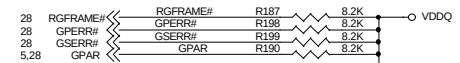
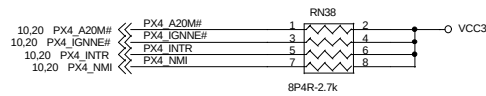
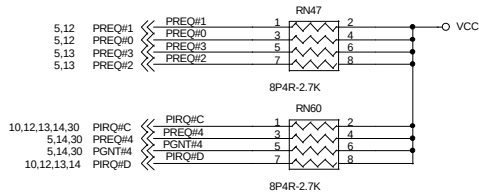
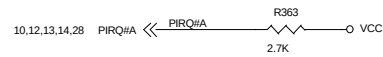
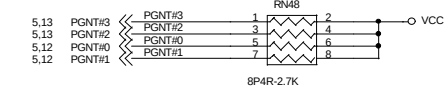
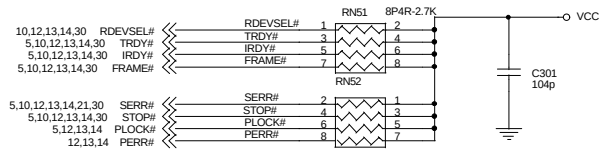
- Note : 1. Ratio by switch :
 -RN37, +U14, +R259, +SW3, -RN88
 2. Ratio by GPIO
 +RN37, +U14, +R259, -SW3, -RN88
 3. Ratio by CPU
 -RN37, -U14, -R259, -SW3, +RN88

Processor Core : Bus Ratio	LINT[1]	LINT[0]	IGNNE#	A20M#	SW1(A1)	SW1(A2)	SW1(A3)	SW1(A4)
1.5			H	H	H	H	H	H
2			H	H	H	H	H	H
2			L	L	L	L	L	L
2.5			L	H	L	L	L	L
3			L	L	H	H	L	L
3.5			L	H	H	H	L	L
4			L	L	L	L	H	H
4.5			L	H	L	H	H	H
5			L	L	H	H	H	H
5.5			L	H	H	H	H	H
6			H	L	L	L	L	L
6.5			H	H	L	L	L	L
7			H	L	H	H	L	L
7.5			H	H	H	H	L	L
8			H	L	L	L	H	H
Reserved			H	L	H	H	H	H

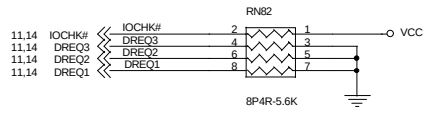
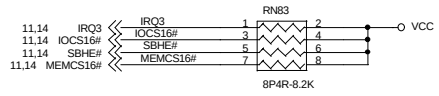
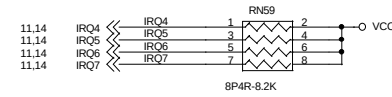
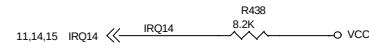
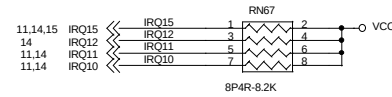
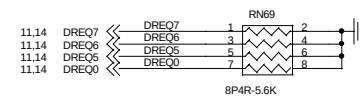
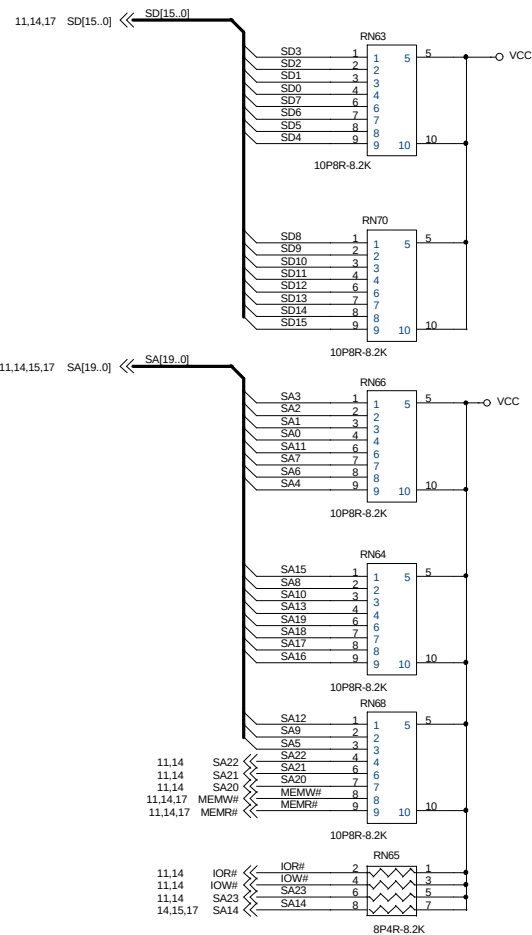


MICRO-STAR		
Title		
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CORE/BUS RATIO		
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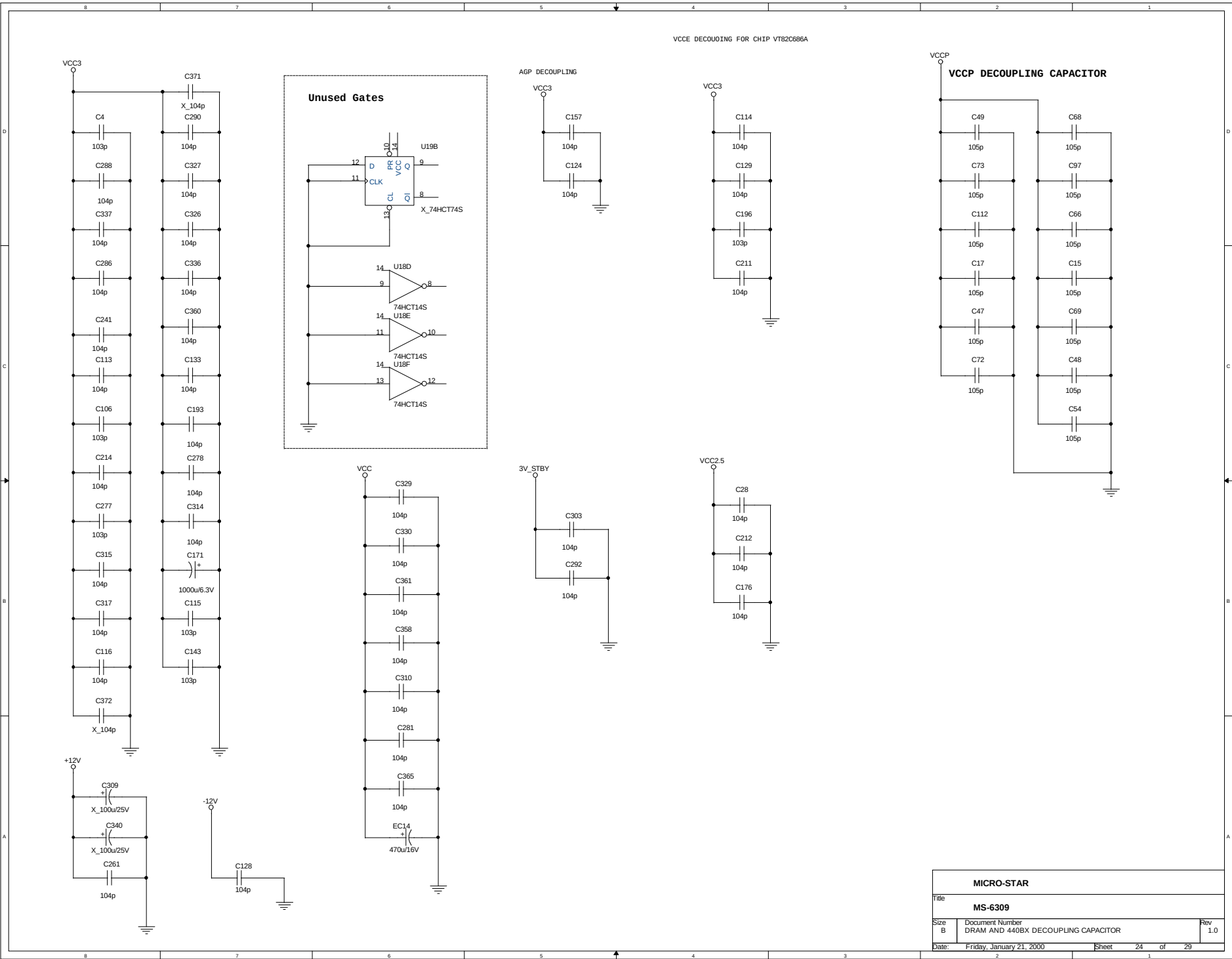


MICRO-STAR			
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Size B	Document Number BUS RESISTOR		Rev 1.0
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2		1	

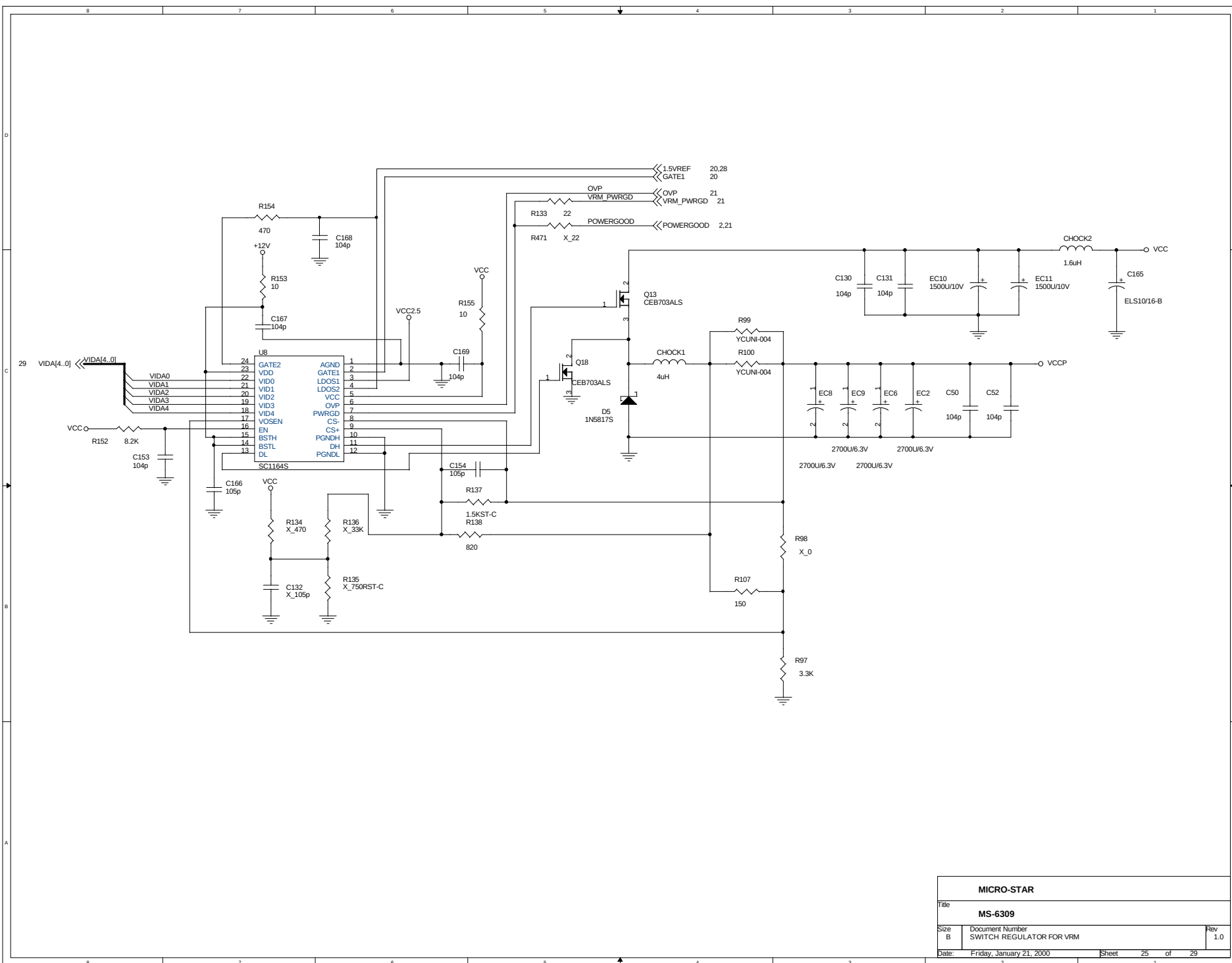


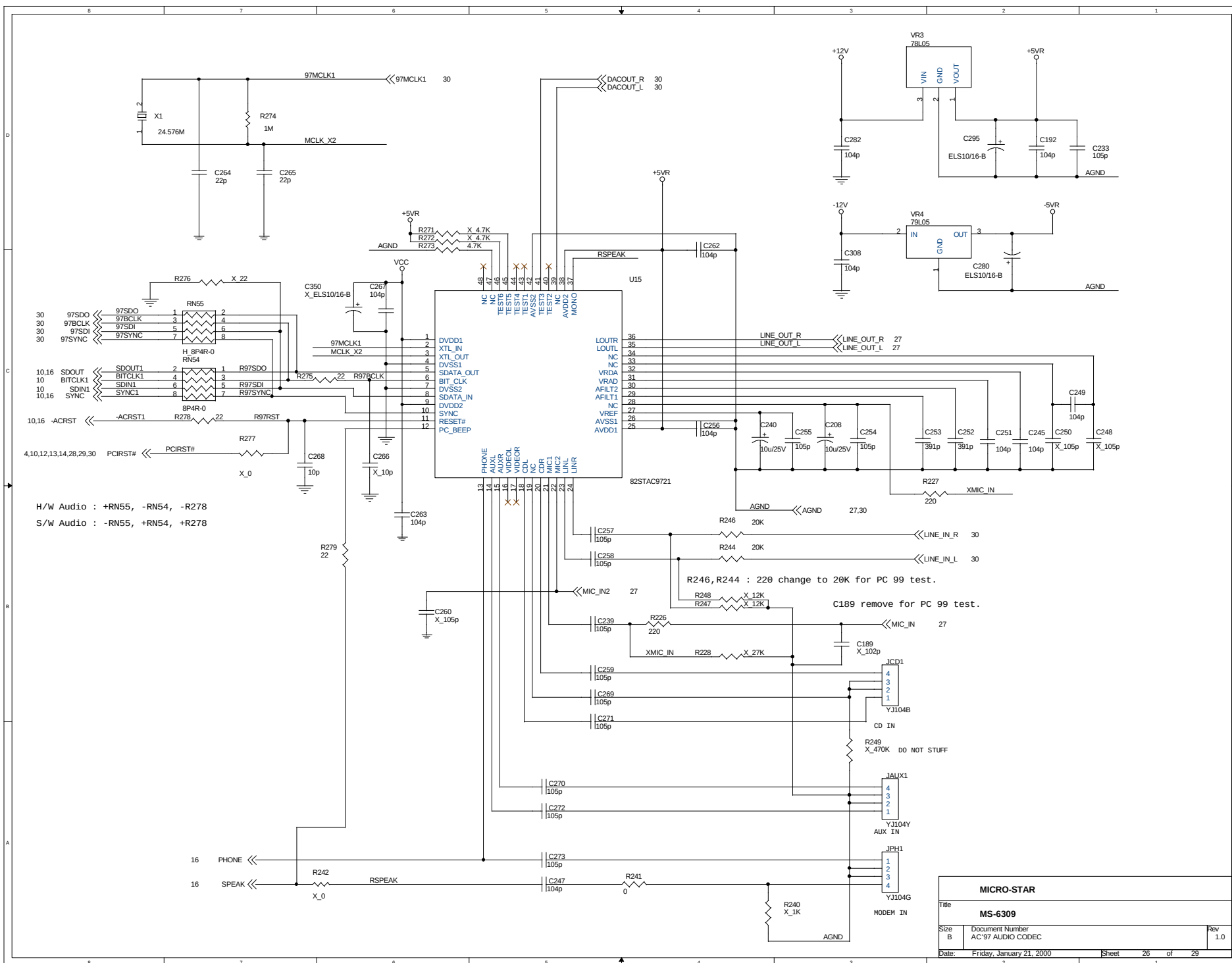
MICRO-STAR			
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Size	Document Number	Rev	
B	ISA BUS RESISTOR	1.0	
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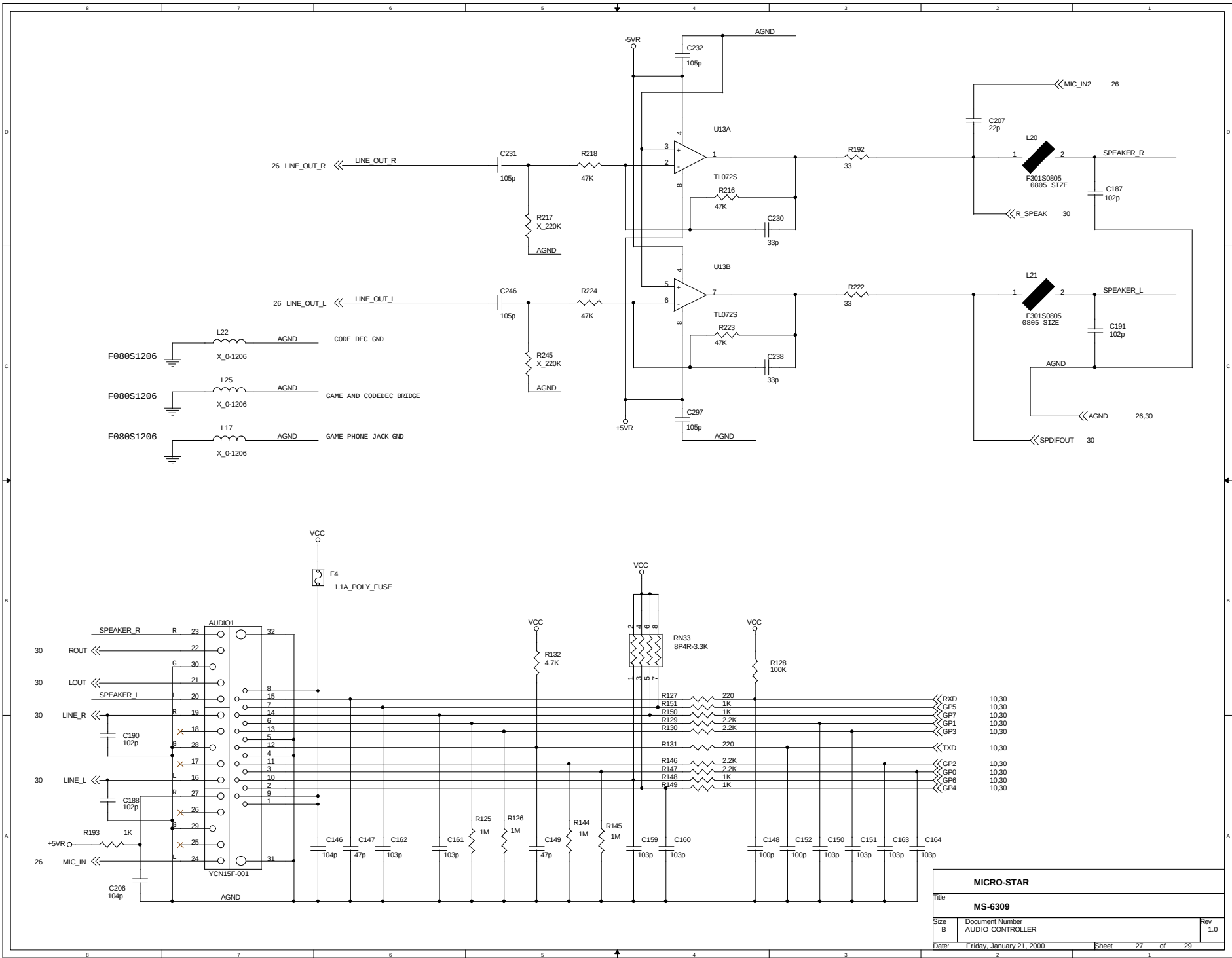
VCCE DECOUPLING FOR CHIP VT82C86A

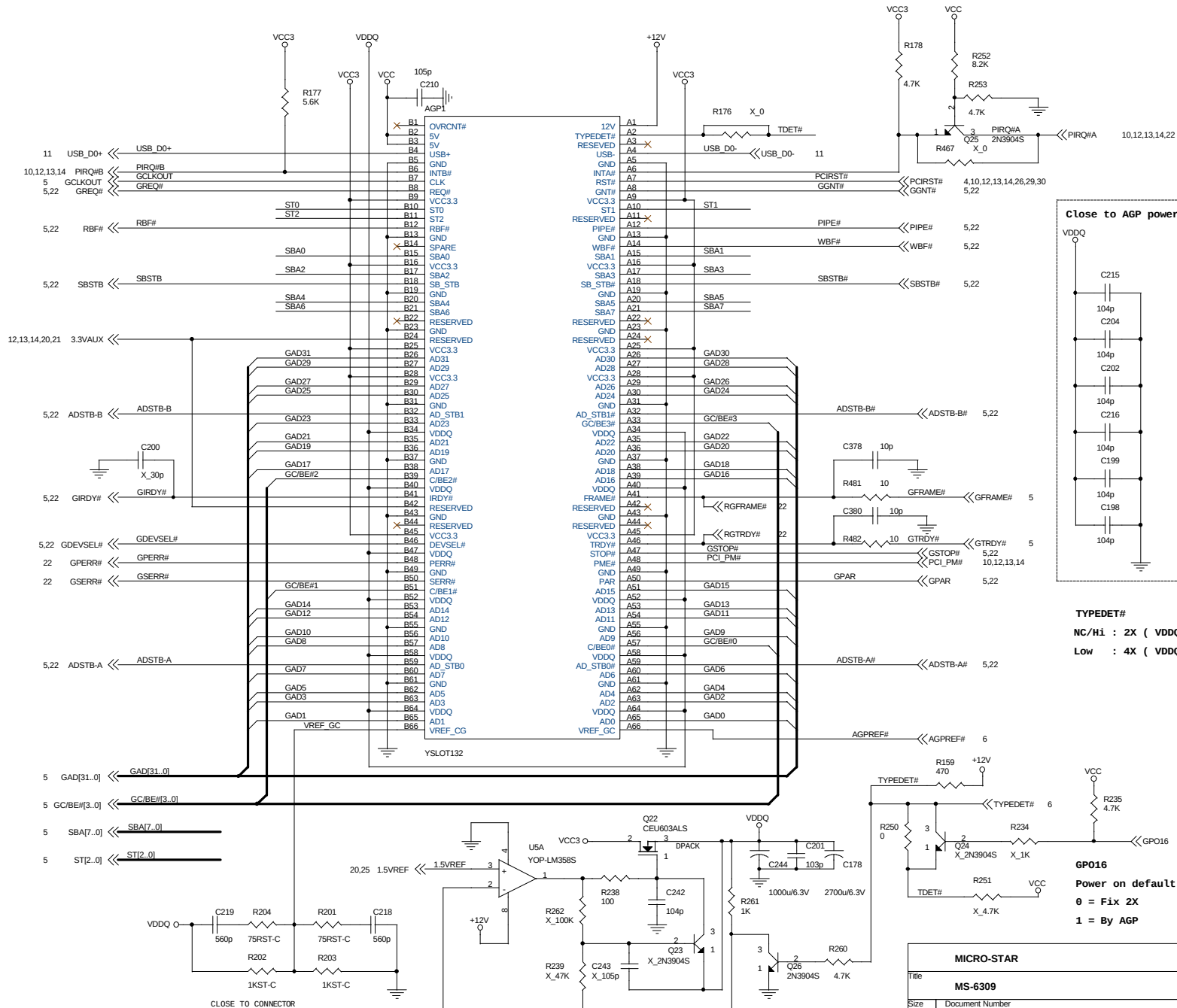


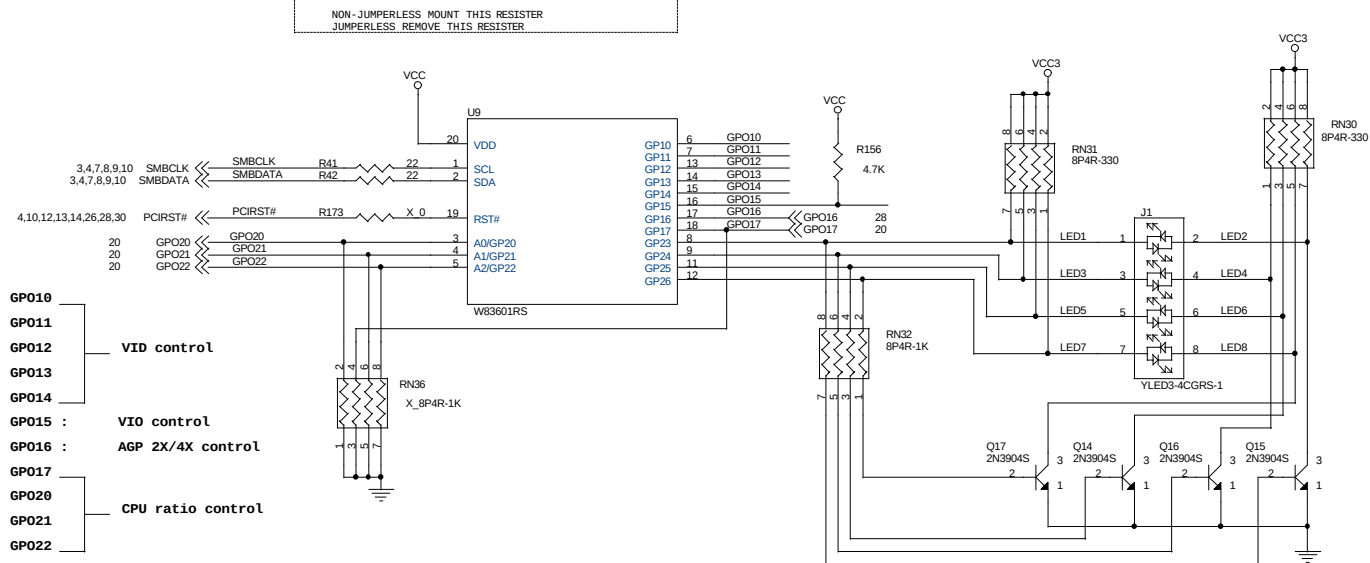
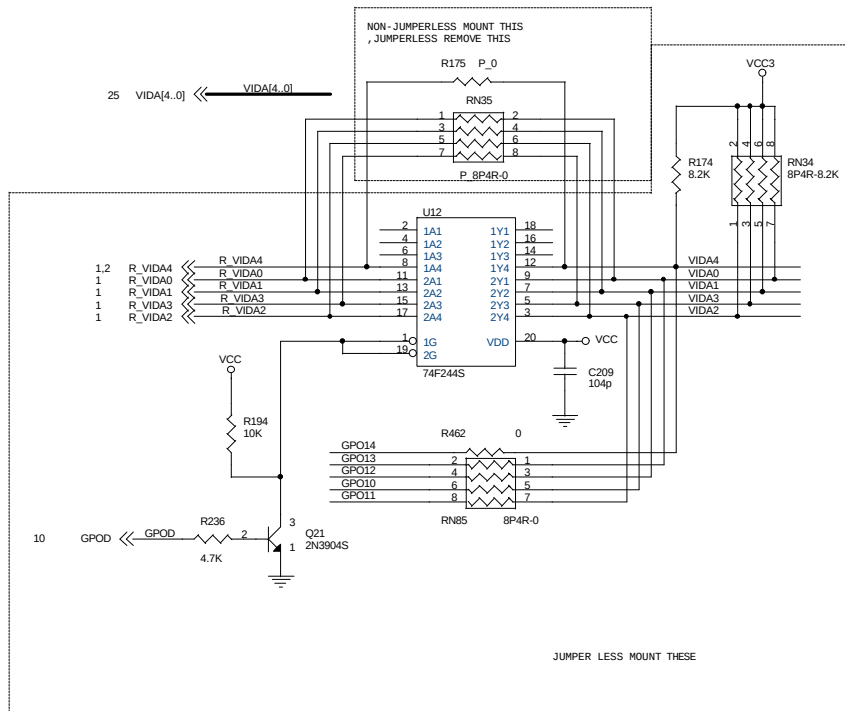
MICRO-STAR			
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B	DRAM AND 440BX DECOUPLING CAPACITOR	1.0	
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B	CPU VOLTAGE MICRO AJUSTMENT	1.0
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