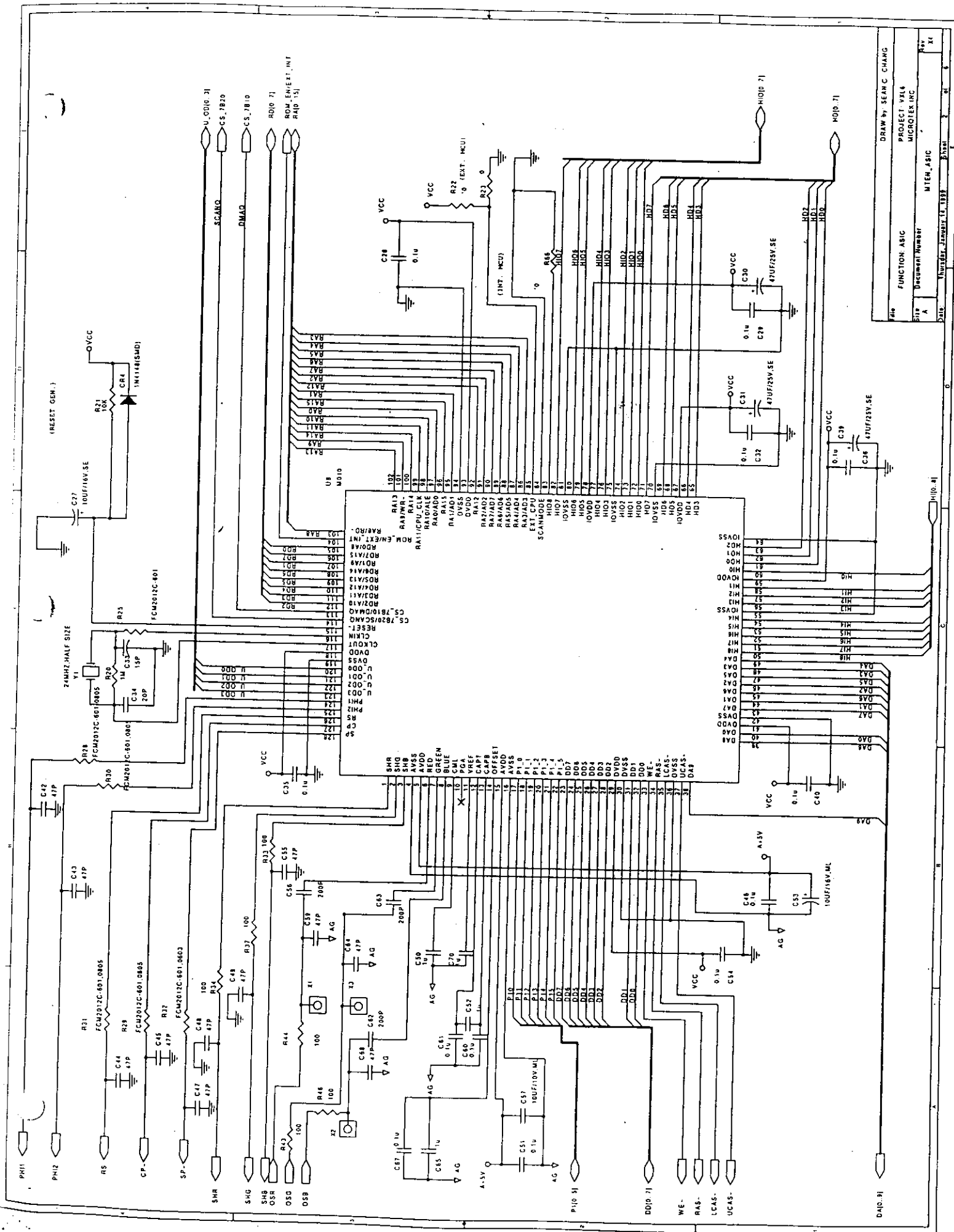
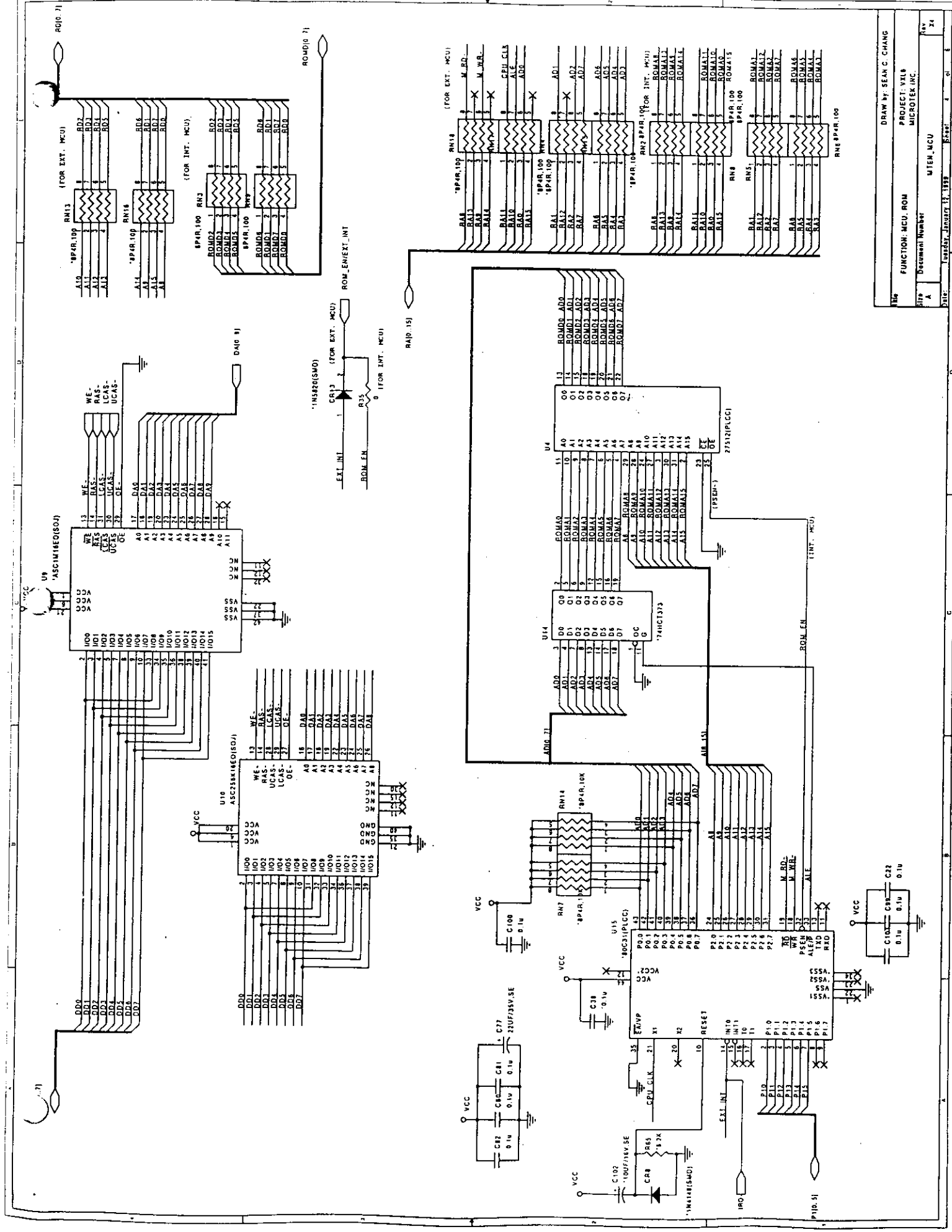
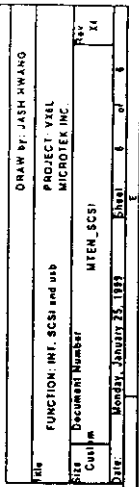
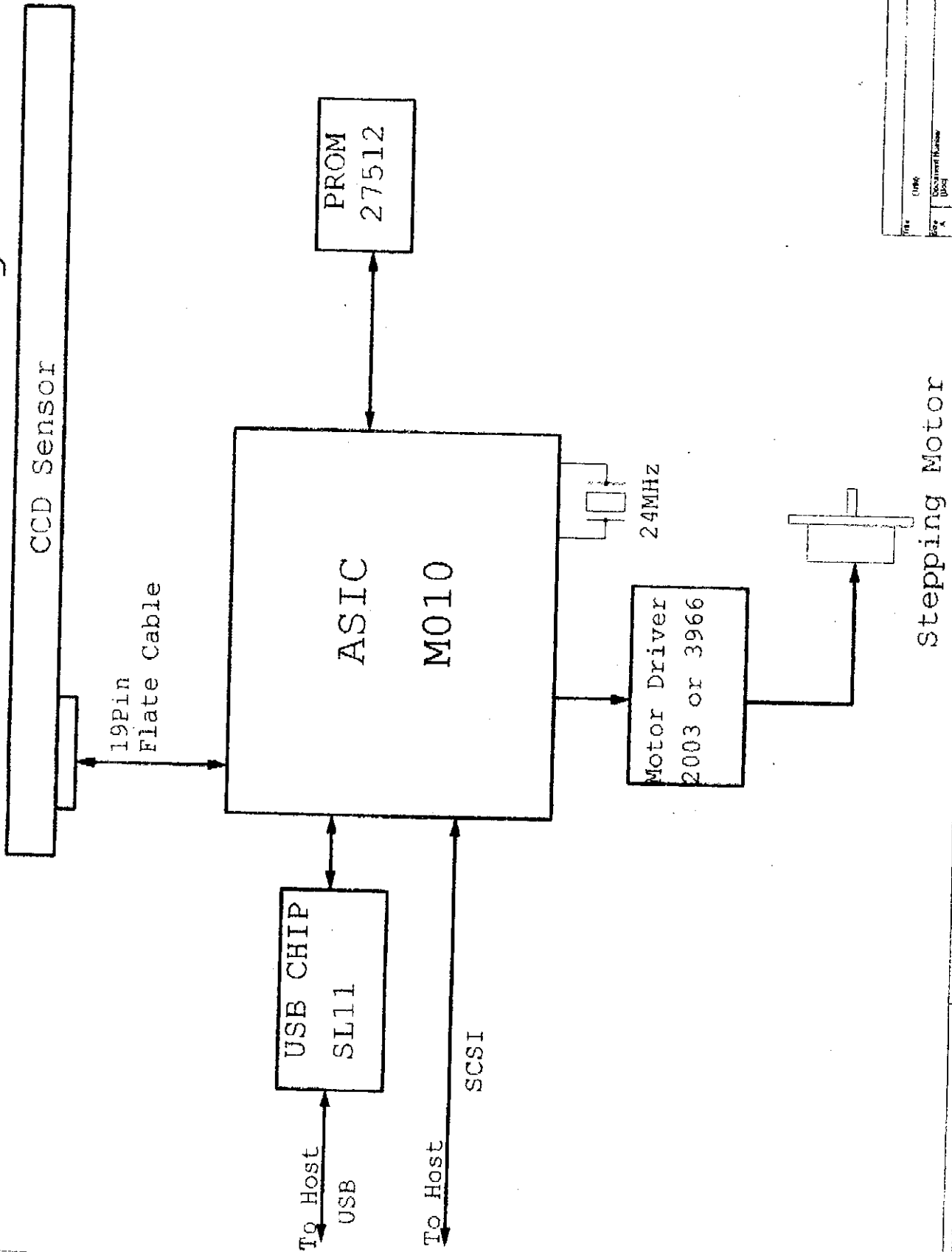








MRS-1200V6US System Block Diagram

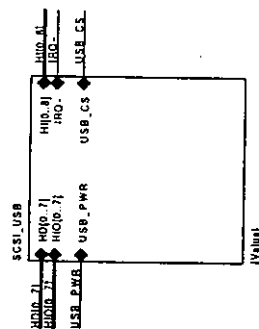
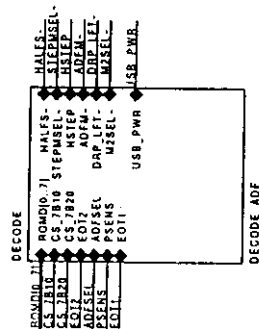
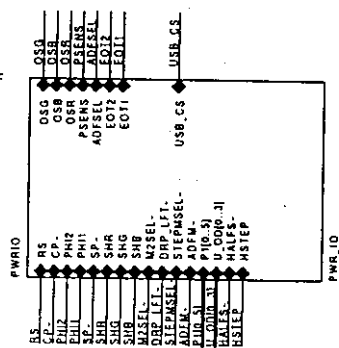
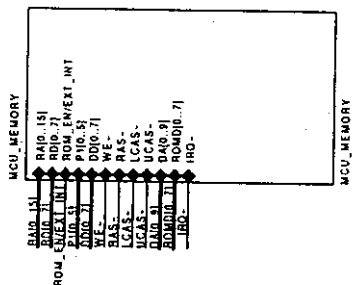


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Doc Engineer	Doc Engineer
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Doc Release	Doc Release
Doc Status	Doc Status
Doc Version	Doc Version

The diagram illustrates the timing of ROM and RAM access operations. The signals shown are:

- ROM Address (DA16-9):** A 16-bit address bus for ROM access.
- ROM Enable (ROM_ENEXT_INT):** A signal that enables ROM access.
- RAM Address (DA16-9):** A 16-bit address bus for RAM access.
- RAM Enable (RAM_ENEXT_INT):** A signal that enables RAM access.
- Data Buses:**
 - RS:** Read/Write Strobe
 - LCAS:** Local Cache Address Strobe
 - WE:** Write Enable
 - BZAS:** Burst Address Strobe
 - PHIL:** Parallel Input/Output Latch Enable
 - PHIZ:** Parallel Input/Output Z-bus
 - CP:** Cache Port
 - SP:** Shared Port
 - SHG:** Shared High
 - SHB:** Shared Low

The diagram shows the sequence of operations for ROM and RAM access, including the timing of address and enable signals relative to the data buses.



P1_0-P1_3	MOTOR
P1_4	SCANNER LAMP
P1_5	HOME SENSOR
P1_4-P1_5	35A LAMP
U_000	READY LED
U_001	SCAM BUTTON
U_002	5V1 3V POWER, I=ON
U_003	USB 3.3V POWER, I=ON
SGS1 ID1	I:SGS1 DISCONNECT
	O:SGS1 CONNECT