PROCEDURE 99-001

ELECTRONIC SYSTEMS TECHNOLOGY 509-735-9092 (O)
415 N. QUAY STREET KENNEWICK, WA 99336 509-783-5475 (FAX)

Date: March 17, 1999

Subject : FCC 15.247(e) Jamming Margin Test on the ESTeem Model 192S

Tools Required : See equipment list in the report.

Parts Required : 2 ea. ESTeem Model 192S

Scope:

This report presents the test procedure, test configuration and test data associated with FCC Part 15.247 (e) Jamming Margin test for indirect measurement of processing gain.

Test Background and Procedure

According to FCC regulations 15.247 (e) , a direct sequence spread spectrum system must have a processing gain, of at least 10 dB. Compliance to this requirement can be shown by demonstrating a bit error ratio (BER) performance improvement between the spread spectrum processes (coding, modulation) are engaged relative to the processes being bypassed. The ESTeem 192S process gain can not be bypassed. The processing gain can be indirectly measured by the Jamming Margin test described in FCC 15.247 (e)2

Test Procedure

Setup the simplex hardware link as shown in Figure 1. Perform all independent instrumentation calibrations prior to starting test. Set operational power levels using fixed and variable attenuators in the system to meet the following objectives:

1. Adjust signal power at receiver to approximately –70 dBm. Use the spectrum analyzer to verify.
2. Ensure that the CW Jammer generator RF output is disabled and measure the Model 192S RF power with the power meter. This measurement will be the relative signal power level.
3. Disable the Model 192S transmitter, and set CW Jammer generator RF output frequency equal to the carrier frequency and enable generator output. Set the CW Jammer reference power level at the power meter to be the same level as Model 192S relative measurement measured in step 2.
4. Disable the CW Jammer and reestablish the communications link between Model 192S unit 1 and 2.
5. Enable CW Jammer at a low power level and gradually increase the CW Jammer output power until the BER test indicates the reference BER level is 10^{-5}.
6. Step the CW Jammer 50 KHz then increase the output power level until the BER is equal to the reference BER. Record the Jammer power level.
7. Repeat step until the all of the receiver passband has been tested. Reference Table 1.

   This technique is used for a fixed signal carrier frequency with uniform frequency increments of 50 KHz across the receiver passband using the CW Jammer. The passband is the calculated from the Data Rate and Chip Rate.

   Passband = Data Rate * Chip Rate

   Passband = 171.875KHz * 16 = 2.75Mhz (+/- 1.375 MHz)

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The processing gain is related to the jamming margin as follows:

$G_p = BER_{REFERENCE} \leftrightarrow (S/N)_{OUTPUT} + (J/S) + L_{system}$

$BER_{reference}$ is the reference bit error ratio with its corresponding theoretical output signal noise ratio per symbol, $(S/N)_{output.}$
(J/S) is the jamming margin (jamming signal power relative to desired signal power)
L_{system} is the system implementation losses.

The ESTeem 192S utilizes the Harris PRISM HFA3824A base band processor. The HFA3824A uses Differential Phase Shift Keying (DPSK) Modulation. There are losses with differential encoding and scrambling that cause loss in performance due to error extension. This means that for every error that occurs, the differential decoding extends that to 2 errors and descrambling further extends that to 6 errors.

Thus, you can expect the theoretical 9.6 dB Eb/No performance for 10^{-5} BER to be degraded to 10.6 dB (plus implementation losses of 2dB) [1].

$Gp = (Eb/No) + (J/S) + L_{system}$

$Gp = 10.6\ dB + (J/S) + 2\ dB$

$Gp = 12.6dB + (J/S)$

The Jammer Margin test procedure allows the worst 20% of the J/S points to be discarded.

The minimum processing gain with 20% worst points removed is **12.6 dB**

The numerical data associated with the above test is tabulated as shown in Table 1. The numerical test data in Table 1 is presented in graphical form in Figure 2.

The test equipment used is listed below.

Equipment	Serial Number	Calibration Date
Fluke PM6680 Frequency Counter	CN944606680011	4/5/98
HP 437B Power Meter w/ Power Sensor HP 8481A	3125U10268 2702A72310	1/21/99
HP 8616A Signal Gen.	54800944	11/23/98
HP8565A Spectrum Analyzer	1937A01424	12/29/98
Mini-Curuits ZSC-2-4 Splitter		
Kay Elemetrics PMAX 3W Step Attenuator		
Mini Circuits CAT-6-75 6dB pad		

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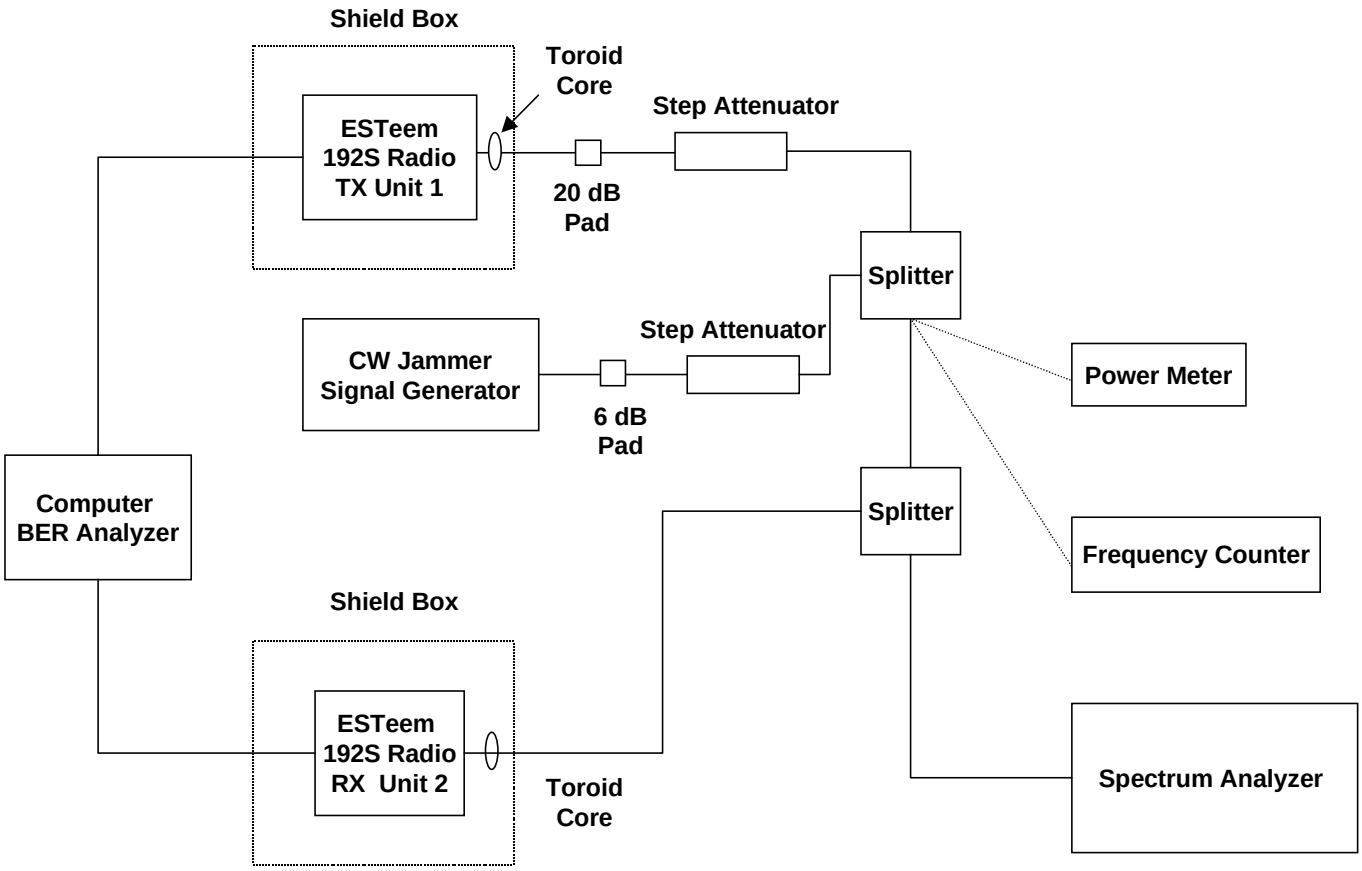
[1]Carl Andren "A Comparison of Frequency Hopping and Direct Sequence Spread Spectrum Modulation for IEEE 802.11



Test Block Diagram
Figure 1

Applications at 2.4 GHz." Harris Semiconductor Palm Bay, Florida

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Jammer Margin Numerical Test Data
Table 1

Frequency (MHz)	Gain (dB)	Frequency (MHz)	Gain (dB)
2435.50	15.6	2437.05	12.6
2435.55	12.6	2437.10	12.6
2435.60	12.6	2437.15	12.6
2435.65	12.6	2437.20	12.6
2435.70	11.6	2437.25	13.6
2435.75	13.6	2437.30	12.6
2435.80	13.6	2437.35	11.6
2435.85	12.6	2437.40	12.6
2435.90	13.6	2437.45	13.6
2435.95	12.6	2437.50	11.6
2436.00	12.6	2437.55	11.6
2436.05	11.6	2437.60	11.6
2436.10	11.6	2437.65	11.6
2436.15	11.6	2437.70	12.6
2436.20	11.6	2437.75	10.6
2436.25	11.6	2437.80	10.6
2436.30	10.6	2437.85	13.6
2436.35	10.6	2437.90	13.6
2436.40	10.6	2437.95	13.6
2436.45	11.6	2438.00	12.6
2436.50	11.6	2438.05	13.6
2436.55	11.6	2438.10	13.6
2436.60	11.6	2438.15	13.6
2436.65	11.6	2438.20	10.6
2436.70	10.6	2438.25	12.6
2436.75	12.6	2438.30	13.6
2436.80	12.6	2438.35	13.6
2436.85	10.6	2438.40	11.6
2436.90	11.6	2438.45	10.6
2436.95	11.6	2438.50	11.6
2437.00	13.6		

Shaded areas show 20% worst test data that has been deleted from analysis

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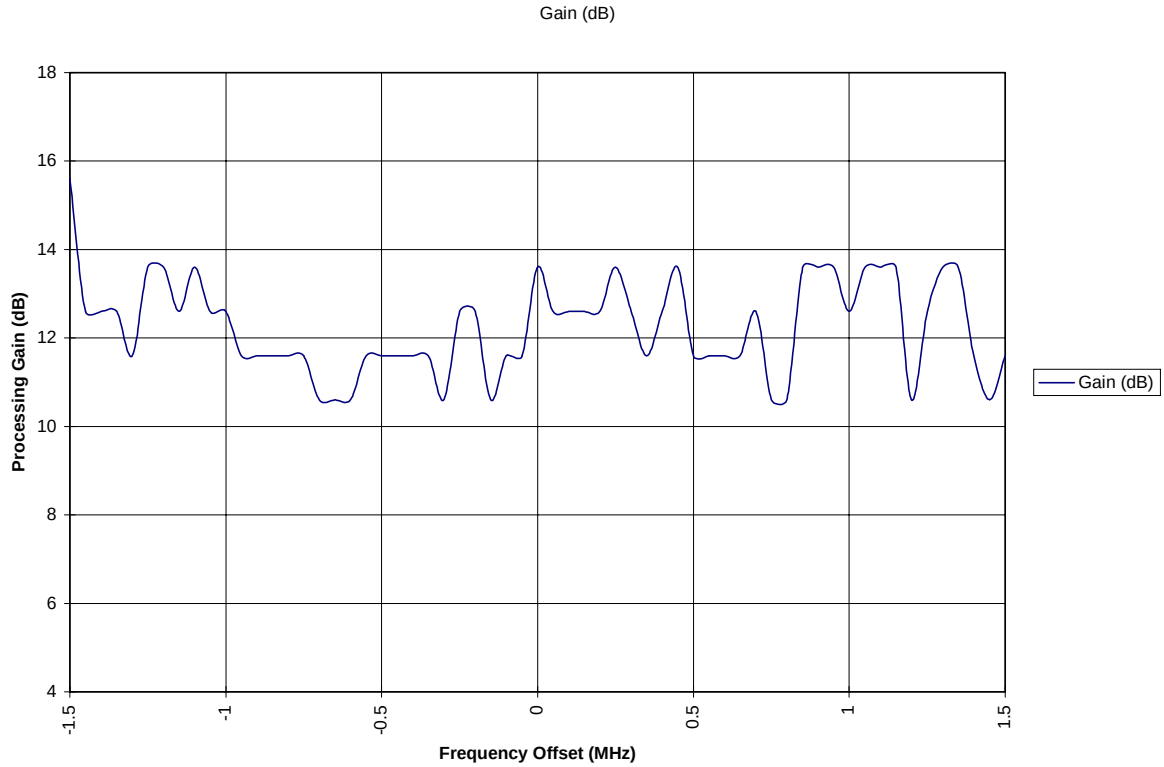

Jamming Margin Numerical Test Data Graph
Figure 2