

二、 Clock Block Diagram for A450

The diagram illustrates the clock distribution for the A450 system. The primary clock source is the **CK100-M IMI-C9714** clock generator, which provides a 2.5V 100MHz signal and a 3.3V 33MHz signal. The 100MHz signal is filtered by a damping resistor and distributed to the CPU (PIII Processor BCLK) via the **HCLKCPU** signal and to the North Bridge (443BX) via the **HCLKIN** signal. The 33MHz signal is distributed to the South Bridge (PIIX4E) via the **PCLKP4** signal and to various peripheral devices via the **PCLKBX** signal. The **PCLKBX** signal is further divided into **PCLKAUDIO** (for the 1946S audio chip), **PCLKML** (for the MINI PCI Modem/LAN), **PCLKCB** (for the PCMCIA O2 6833B), and **PCLKSIO** (for the SUPER/IO FDC37N869). The North Bridge (443BX) also receives a 124MHz signal from the Memory Clock and provides a 66MHz signal to the ATI Mobility M1 graphics chip via the **PCLKAGP** signal. The North Bridge also provides a 100MHz signal to the SODIMM0 and SODIMM1 memory modules via the **HCLKDIM0..3** signal. The South Bridge (PIIX4E) provides a 33MHz signal to the SODIMM0 and SODIMM1 memory modules via the **BUF_IN** and **BUF_OUT** signals. The diagram also shows the distribution of clock signals to the CKBF-M IMI-SC660E clock buffer, which provides a 100MHz signal to the SODIMM0 and SODIMM1 memory modules via the **BUF_IN** and **BUF_OUT** signals.

