



COMPAL

5G RXL-N3n Module

User Manual

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1 Foreword

1.1 Introduction

This document describes the hardware of the COMPAL® 5G LGA Module product. It helps you quickly retrieve interface specifications, electrical and mechanical details, and information on the requirements to be considered for integrating further components. **All relevant LGA HW spec 、figures and design guidelines in this document are common specification for All 5G LGA mode.**

1.2 Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating with 5G LGA module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, we assume no liability for customers' failure to comply with these precautions.



Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.



Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If the device offers an Airplane Mode, then it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on boarding the aircraft.



Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.



Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid SIM card). When emergent help is needed in such conditions, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.



The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric- equipment.



In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.



Safety of Children

Do not allow children to use the wireless device without guidance. Small and sharp components of the wireless device may cause danger to children or cause suffocation if children swallow the components.

Environment Protection

Observe the local regulations regarding the disposal of your packaging materials, used wireless device and accessories, and promote their recycling.

WEEE Approval

The wireless device is in compliance with the essential requirements and other relevant provisions of the Waste Electrical and Electronic Equipment Directive 2012/19/EU (WEEE Directive).

RoHS Approval

The wireless device is in compliance with the restriction of the use of certain hazardous substances in electrical and electronic equipment Directive 2011/65/EU (RoHS Directive).



1.3 Reference Standard

The design of the product complies with the following standards:

Table1-1 3GPP Standards

3GPP TS specification reference	Title	3GPP Release used as the basis for this declaration
23.122	Non-Access-Stratum functions related to Mobile Station (MS) in idle mode	11.4.0
24.008	Mobile radio interface Layer 3 specification; Core network protocols; Stage 3	11.5.0
25.331	Radio Resource Control (RRC); protocol specification	9.0.0
25.133	Requirements for Support of Radio Resource Management (FDD)	13.2.0
25.101	Radio Transmission and Reception (FDD)	14.0.0
24.301	(NAS) protocol for Evolved Packet System (EPS); Stage 3	11.7.0
36.101	(E-UTRA); User Equipment (UE) radio transmission and reception	12.14.1
36.133	(E-UTRA); Requirements for support of radio resource management	14.14.0
36.213	(E-UTRA) Physical layer procedures	12.11.0
36.214	(E-UTRA) Physical layer measurements	12.3.0
36.304	(E-UTRA); User Equipment (UE) procedures in idle mode	12.8.0
36.321	(E-UTRA); Medium Access Control (MAC) protocol specification	12.9.0
36.322	(E-UTRA); Radio Link Control (RLC) protocol specification	12.4.0
36.323	(E-UTRA); Packet Data Convergence Protocol (PDCP) specification	12.6.0
36.331	(E-UTRA); Radio Resource Control (RRC); Protocol specification	15.3.0
24.501	Non-Access-Stratum (NAS) protocol for 5G System (5GS); Stage 3	15.1.0
38.331	NR;Radio Resource Control (RRC) protocol specification	15.3.0
38.133	NR; Requirements for support of radio resource management	15.3.0
38.213	NR; Physical layer procedures for control	15.3.0
38.323	NR; Packet Data Convergence Protocol (PDCP) protocol specification	15.3.0
37.324	Service Data Adaptation Protocol (SDAP) specification	15.1.0
11.11/51.011	Specification of the Subscriber Identity Module - Mobile Equipment (SIM-ME) Interface	4.15.0
31.102	Characteristics of the Universal Subscriber Identity Module (USIM) application	12.11.0
31.103	Characteristics of the IP Multimedia Services Identity Module (ISIM) application	12.2.0
31.101	UICC-terminal interface; Physical and logical characteristics	12.2.0
27.007	AT command set for 3GPP User Equipment (UE)	9.9.0
36.355	(E-UTRA); LTE Positioning Protocol (LPP)	14.2.0
44.031	Location Services (LCS)– MS-SMLC Radio Resource LCS Protocol (RRLP)	14.3.0

Non-3GPP documentation:

Table1-2 ETSI

Document Source	Title	Version
ETSI	TS 102 221: "UICC-Terminal interface; Physical and logical characteristics".	12.1.0
ETSI	TS 102 223: "Smart Cards; Card Application Toolkit".	12.3.0

Table1-3 GSMA

Document Source	Title	Version
GSMA	IR.92 IMS Profile for Voice and SMS	8.0.0
GSMA	IR.94 IMS Profile for Conversational Video Service	7.0.0



Table1-4 OMA

Document Source	Title	Version
OMA	OMA-AD-SUPL-V1	
OMA	OMA-AD-SUPL-V2	

1.4 Related Documents

- 5G_RXL-N3n_CA_And_ENDC_List_S070000047710_Rev.AA



2 Overview

2.1 Introduction

RXL-N3n MODULE is a highly integrated 5G NR wireless communication module that adopts standard PCIe interface and backward supports with LTE/WCDMA system. It is applicable to most broadband communication networks of the mobile operator across the world. **All relevant LGA HW spec 、figures and design guidelines in this document are common specification for All 5G LGA mode.**

2.2 Specification

Table 2-1 LGA module features

Specification		
Platform [3]	QCT SDX72 / SDX75 Quad core Arm Cortex A55 processor at up to 2.2 GHz	
Memory [3]	8GB eMMC Flash, 2GB LPDDR4X	
Operating Band	5G: n2, n5, n7, n12, n13, n14, n25, n26, n30, n38, n41, n48. n66, n70, n71, n77, n78	
	LTE: B2, B4, B5, B7, B12, B13, B14 , B17, B25, B26, B30, b38, B41, B42, B43, B48, B66, B71	
	WCDMA/HSPA+: NA	
	Roaming bands: LTE: B1,B3,B28 (all 2x2) 5G: n1, n3, n28 (all 2x2)	
	GNSS [3]: GPS, GLONASS(GLO), Galileo(GAL) and BeiDou(BDS) L1	
Network option	SA	Option 2
	NSA	Option 3x/3a
Downlink	LTE	LTE CAT20
	5G sub-6	SA 3xCA: TDD Max BW 300MHz(SDX75) SA 3xCA: TDD Max BW 200MHz(SDX72) SA 4xCA:(SDX75): FDD Max BW 100MHz; MIMO 4x4 SA 3xCA:(SDX72),FDD Max BW 100MHz; MIMO 4x4



Uplink	LTE	LTE CAT18
	5G sub-6	SA 2CC;Max BW 100MHz(TDD), 40MHz(FDD); MIMO 2x2
HPUE (Class 2)	- PC2: B41 , n41, n77, n78 , n2*, n7*, n25*, n66*, n70* (*=2x2 UL MIMO)	
HPUE (Class 1.5)	- PC1.5: n41*, n77*, n78* (*=2x2 UL MIMO)	
UL 2x2 MIMO (Option)	n2,n7,n25,n30,n38,n41,n48,n66,n70,n71, n77,n78	
DL 4x4 MIMO	n2,n7,n25,n30,n38,n41,n48,n66,n77,n78. B2,B4,B7,B25,B30,B38,B41,B42,B43,B48,B66	
SRS	MHB/UHB : 1T4R(NSA) + 2T4R(SA)	
Carrier aggregation	ULCA, DLCA and NRDC	
Power Supply	DC 3.4V~4.4V(Typical value is 3.8V)	
Temperature	Operating temperature[1]:-30°C ~+75°C	
	Extended temperature[2] : -40°C ~+85°C	
	Storage temperature: -40°C ~+85°C	
Physical characteristics	Dimension:49x50mm, Thickness=2.75mm(typ.)	
	Weight: 17.5±0.2g (TBD)	
Interface		
Antenna Port	Sub-6: Antenna x 4, GPS: 1xAntenna (Optional)	
	Support 4x4 MIMO	
	USIM	
	I2S/PCM for Audio x 1	
	USB 2.0 HS or USB 3.1 Gen2 SS	
	BLSP2 4-wire UART for Bluetooth command BLSP3 2-wire UART for Debug	



Function Interface	GPIO (General-Purpose I/O) x 140(Overall CPU GPIO Pin)
	Power on/off switch key pin Support Auto Power On
	Hardware reset pin
	SPI interface x 2
	EBI2/LCD(9 bit)
	LED/PWM control pin (up to 10 mA) x 2
	I2C Interface reserve x2
	Tunable antenna(2xMIPI)
	PCIe Gen3 × 3 (Two lane *2 + one lane *1)
Software (Windows 19H1 and later, Linux kernel v4.4)	
Driver	IPV4/IPV6
Protocol Stack	3GPP TS 27.007 and 27.005
AT commands	FOTA
Firmware update	Windows MBIM support
Others feature	Windows update
	Support 5G NR NSA and SA
	Multiple carrier aggregation
	AGNSS



NOTE:

[1] To meet this operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module can meet 3GPP.

[2] To meet this extended temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. When the LGA module works at this temperature, the module remains the ability to establish and maintain functions such as voice, SMS, emergency call, etc.

Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may undergo a reduction in value, exceeding the specified tolerances of 3GPP.

[3] Please contact Compal sales and TAM for SKU option.

2.3 CA combinations and EN-DC combinations with in 5G FR1

CA combinations to be supported in 5G LGA MODULE. For more details, please refer to others file “5G_RXL-N3n_CA_And_ENDC_List_S070000047710”



2.4 Application Block Diagram

The peripheral applications for LGA Module are shown in Figure 2-4

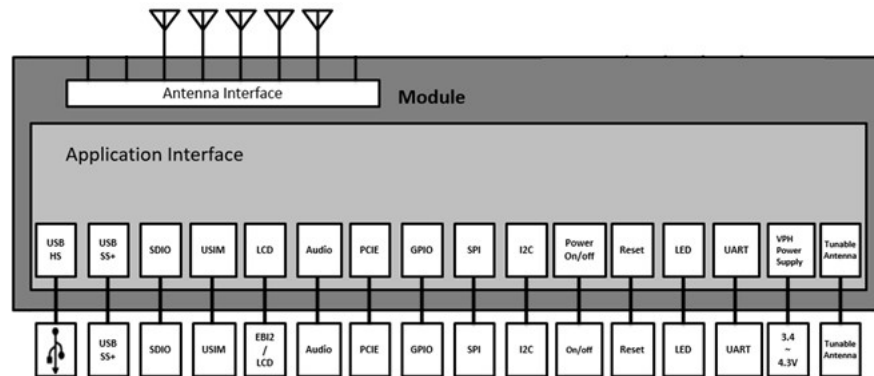


Figure 2-4 Application Block diagram for Peripherals IF

Peripherals Interface Description:

USB Interface:

The USB interface supports USB 2.0 high speed standard and USB 3.1 SuperSpeed (need external MUX Switch IC for type-c connector)

SDIO Interface:

Reserved for internal eMMC memory.

USIM Interface:

The USIM interface.

LCM:

The module supports one EBI2 (9 bit) interface.

Audio Interface:

The module supports I2S/PCM interface (can be configured as either I2S or PCM interface)

PCIE:

Reserved for intelligent module in future.

SPI Interface:

Reserved for intelligent module in future.

I2C Interface:

Reserved for intelligent module in future.



UART Interface:

The module supports 2 UART interfaces. One is 4-wire UARTs. One is 2-wire UART, which is only for debugging.

External Power Supply:

Output Power Supply from LGA module:

A. Dual Voltage Support LV 1.8V/HV 2.95V IF for SIM Card Power.

- Pin SIM1_VCC & VREG_L13_UIM2_NU_1P8
- B. Reserve power supply for ANT tuner (1.2V)
- Pin VREG_L12_1P2
- C. 1.8V/1.2V/0.974V/1.9V Support for WIFI IC Power.
- Pin VREG_1P8_SYS , VREG_1P2_SYS , VREG_L6_1P8, VREG_S7_0P974_1, VREG_S7_0P974_2, VREG_S2_1P224, VREG_S4_1P904_1, VREG_S4_1P904_2, VREG_L15_1P2

Extra Power Supply Require for LGA module:

A. DC 3.8 V is recommended for module VPH_PWR

Don't connect with any module internal power source.

RF Pad:

RF antenna interface.

Tunable ANT CTRL:

Since LTE bands cover wide frequency, tunable ANT CTRL helps customers for tunable antenna design. The firmware with this feature is in plan.

3 Application Interface

3.1 LGA Interface

The RXL-N3n module uses a 412-pin LGA as its external interface. For details about the module and dimensions, see 5.4 Dimensions and Interfaces.



3.2 Pin Map

➤ Module Pin Map ()

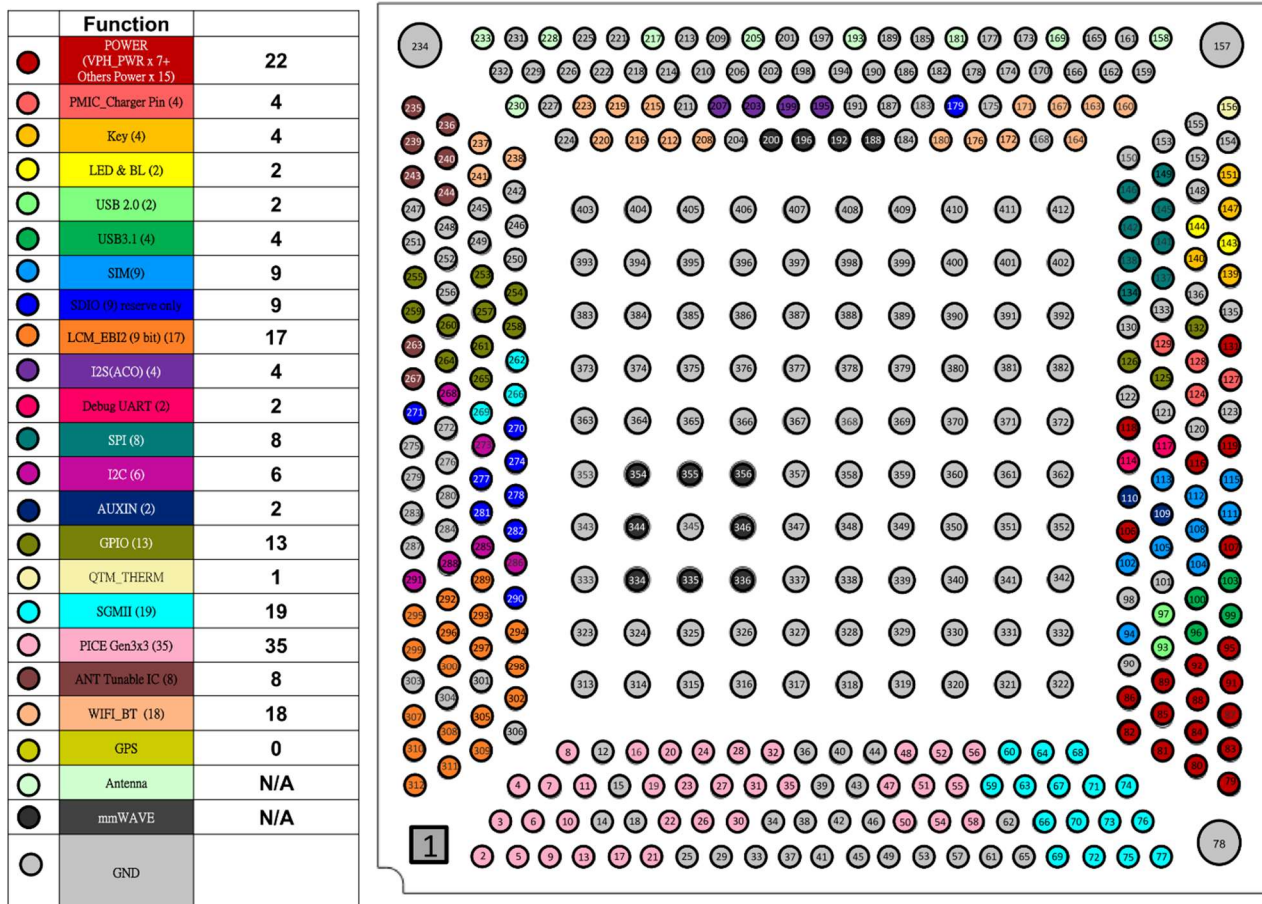


Figure 3-1 PAD Sequence of LGA module (Perspective View from TOP Side)



3.2.1 Pin Definition

The pin definition is as follows Table 3-1:

Table 3-1 Pin definition

Pin NO.	Pin Name	I/O	Pin Description	Type(V)
81	VPH_PWR_1	PI	1. For LGA Module power	3.4~4.3
88	VPH_PWR_2	PI	1. For LGA Module power	3.4~4.3
84	VPH_PWR_3	PI	1. For LGA Module power	3.4~4.3
85	VPH_PWR_4	PI	1. For LGA Module power	3.4~4.3
83	VPH_PWR_5	PI	1. For LGA Module power	3.4~4.3
79	VPH_PWR_6	PI	1. For LGA Module power	3.4~4.3
80	VPH_PWR_7	PI	1. For LGA Module power	3.4~4.3
82	SIM1_VCC	PO	For SIM1 Power only	1.8/2.95
86	VREG_L13_UIM2_NU_1P8	PO	For SIM2 Power only, do not use for other power source.	1.8/2.95
118	VREGV_L12_1P2	PO	Reserve power supply for ANT tuner (1.2V)	1.2
131	USB_VBUS	PI	For USB detection	4.5~5.5
107	VREG_1P8_SYS	PO	Power supply output for WIFI	1.8
116	VREG_1P2_SYS	PO	Power supply output for WIFI	1.2
119	VREG_L6_1P8	PO	Power supply output for WIFI	1.8
91	VREG_S7_0P974_1	PO	Power supply output for WIFI	0.974
87	VREG_S7_0P974_2	PO	Power supply output for WIFI	0.974
89	VREG_S2_1P224	PO	Power supply output for WIFI	1.2
92	VREG_S4_1P904_1	PO	Power supply output for WIFI	1.9
95		PO	Power supply output for WIFI	1.9



	VREG_S4_1P904_2			
106	VREG_L15_1P2	PO	Power supply output for WIFI	1.2
128	PMX_FAULT_N	DIO	PMIC fault communication signal (bidirectional)	1.8
129	SLEEP_CLK	AO	32.7645 kHz sleep clock output to WLAN	1.2
124	SPMI_CLK	DI	Slave and PBUS interface for PMICs – clock	1.2/1.8
127	SPMI_DATA	DIO	Slave and PBUS interface for PMICs – data	1.2/1.8
139	KPD_PWR_N	DI	Power-on key ground switch,(Act_lo)	1.2/1.8
147	FORCED_USB_BOOT	DI	For Forces boot DL from HS USB	1.8V as triggered
151	PMK_RESIN_N	DI	Reset input to PMK75.	1.2/1.8
140	AUTO_ON_N	DI	GPIO_03.(PMX75)	1.8
144	PMX75_ISINK1	DI	Current sink.(up to 10mA)	
143	PMX75_ISINK2	DI	Current sink.(up to 10mA)	
93	USB_HS_DP	AIO	USB high-speed data – positive	1.8
97	USB_HS_DM	AIO	USB high-speed data – negative	1.8
96	USB_SS_TX_P	AIO	USB super-speed transmit – plus	1.8
100	USB_SS_TX_M	AIO	USB super-speed transmit – minus	1.8
99	USB_SS_RX_P	AIO	USB super-speed receive – plus	1.8
103	USB_SS_RX_M	AIO	USB super-speed receive – minus	1.8
113	CARD_UIM1_CLK	DO	For UIM1 clock.	1.8/2.95
112	CARD_UIM1_DATA	DIO	For UIM1 data	1.8/2.95
105	SDX_UIM1_PRESENT	B	For UIM presence detection	1.8
115	CARD_UIM1_RESET_N	DO	For UIM1 reset	1.8/2.95
108	UIM2_CLK	DO	For UIM2 clock	1.8/1.2
104	UIM2_DATA	DIO	For UIM data	1.8/1.2



94	UIM2_PRESENT	B	For UIM2 presence detection	1.8
102	UIM2_RESET	DO	For UIM2 reset	1.8/1.2
111	UIM2_LS_EN	DI	Enable PIN for ESIM level shift.(1.8 to 1.2)	1.2
278	MSDC1_CLK	DO	SDC clock (Reserved only)	1.8/2.95
277	MSDC1_DAT0	DO	SDC data bit 0 (Reserved only)	1.8/2.95
282	MSDC1_DAT1	DIO	SDC data bit 1 (Reserved only)	1.8/2.95
270	MSDC1_DAT2	DIO	SDC data bit 2 (Reserved only)	1.8/2.95
271	MSDC1_DAT3	DIO	SDC data bit 3 (Reserved only)	1.8/2.95
281	MSDC1_CMD	DIO	SDC command (Reserved only)	1.8/2.95
274	SDC1_PWR_EN	B	1. SDC Power Enable (Reserved only) 2. 1.8V GPIO Reserved	1.8
290	SDC1_DET_N	B	1. SDC detect (Reserved only) 2. 1.8V GPIO Reserved	1.8
179	SDC1_VSEL	B	1. SDC VSEL (Reserved only) 2. 1.8V GPIO Reserved	1.8
297	EBI2_A_D0	DO	EBI2 multiplexed address and data - bit 0	1.8
293	EBI2_A_D1	DO	EBI2 multiplexed address and data - bit 1	1.8
296	EBI2_A_D2	DO	EBI2 multiplexed address and data - bit 2	1.8
295	EBI2_A_D3	DO	EBI2 multiplexed address and data - bit 3	1.8
289	EBI2_A_D4	DO	EBI2 multiplexed address and data - bit 4	1.8
292	EBI2_A_D5	DO	EBI2 multiplexed address and data - bit 5	1.8
299	EBI2_A_D6	DO	EBI2 multiplexed address and data - bit 6	1.8
300	EBI2_A_D7	DO	EBI2 multiplexed address and data - bit 7	1.8
294	EBI2_A_D_8	DO	EBI2 multiplexed address and data - bit 8	1.8
298	EBI2_OE_N	DO	EBI2 output enable	1.8
309	EBI2_CLE_UB_N	DO	EBI2 command latch enable	1.8
308	EBI2_NAND_CS_N	DO	EBI2 NAND chip select	1.8
311	EBI2_BUSY_N	DO	EBI2 busy signal	1.8
312	EBI2_ALE_N	DO	EBI2 address latch enable	1.8



307	EBI2_WE_N	DP	EBI2 write enable	1.8
310	EBI2_LCD_TE	DO	EBI2 LCD tearing effect	1.8
302	EBI2_LCD_RESET_N	DO	EBI2 LCD reset	1.8
305	EBI2_LCD_CS_N	DO	EBI2 LCD chip select	1.8
117	DBG_UART_TX	DO	UART transmit data – (used for debug)	1.8
114	DBG_UART_RX	DI	UART receive data (used for debug)	1.8
142	SPI_MISO	DI	SPI master in, slave out	1.8
138	SPI_MOSI	DO	SPI master out, slave in	1.8
146	SPI_SCLK	B	SPI clock	1.8
134	SPI_CS_0	B	SPI chip select	1.8
141	SENSOR_MOSI	DO	Sensor master in, slave out	1.8
145	SENSOR_CLK	DO	Sensor clock	1.8
149	SENSOR_CS_N	DO	Sensor chip select	1.8
137	SENSOR_MISO	DI	SPI master in, slave out6	1.8
286	SENSOR_I2C_SCL	B	I2C clock for sensor	1.8
291	SENSOR_I2C_SDA	B	I2C data for sensor	1.8
285	I2C_SCL	B	I2C clock	1.8
288	I2C_SDA	B	I2C data	1.8
268	MU_INT	DI	Interrupt pin for I2C	1.8
273	ALSP_INT	DI	Interrupt pin for I2C	1.8
109	PMX75_AMUX1	AI	AUXIN(PMX75 GPIO_05)	0~1.875
110	PMX75_AMUX2	AI	AUXIN(PMX75 GPIO_12)	0~1.875
261	SDX_GPIO_18	DIO	General purpose input or output	1.8
264	SDX_GPIO_19	DIO	General purpose input or output	1.8
253	SDX_GPIO_69	DIO	General purpose input or output	1.8
255	SDX_GPIO_74	DIO	General purpose input or output	1.8
258	SDX_GPIO_75	DIO	General purpose input or output	1.8
254	SDX_GPIO_77	DIO	General purpose input or output	1.8
259	SDX_GPIO_78	DIO	General purpose input or output	1.8
260	SDX_GPIO_79	DIO	General purpose input or output	1.8
257	SDX_GPIO_64	DIO	General purpose input or output	1.8



265	SDX_GPIO_65	DIO	General purpose input or output	1.8
125	PMX75_GPIO_2	DIO	Configurable; default digital input with 10 μ A pull-down	1.2/1.8
126	PMX75_GPIO_15	DIO	Configurable; default digital input with 10 μ A pull-down	1.2/1.8
132	PMX75_GPIO_16	DIO	Configurable; default digital input with 10 μ A pull-down	1.2/1.8
156	QTM_THERM	AI	Analog multiplexer (AMUX) input 5 for QTM565_THERM detection	0~1.875
72	SDX_USXGMII_TX_M	AO	USXGMII interface 0 serial data Tx - minus	
70	SDX_USXGMII_TX_P	AO	USXGMII interface 0 serial data Tx - plus	
69	AQR_USXGMII_TX_M	AI	USXGMII interface 0 serial data Rx - minus	
66	AQR_USXGMII_TX_P	AI	USXGMII interface 0 serial data Rx - plus	
76	SDX_USXGMII_1_TX_M	AO	USXGMII interface 1 serial data Tx - minus	
77	SDX_USXGMII_1_TX_P	AO	USXGMII interface 1 serial data Tx - plus	
73	RTL_USXGMII_TX_M	AI	USXGMII interface 1 serial data Rx - minus	
75	RTL_USXGMII_TX_P	AI	USXGMII interface 1 serial data Rx - plus	
67	USXGMII_0_MD_CLK	B	MDIO interface clock signal(USXGMII)	1.8
64	USXGMII_0_MD_DATA	B	MDIO interface data signal(USXGMII)	1.8
63	USXGMII_0_RES ET_N	DO	Reset signal for Ethernet PHY(USXGMII)	1.8
59	USXGMII_0_INT_N	DO	SGMII 0 PHY interrupt(USXGMII)	1.8
74	USXGMII_1_MD_CLK	B	MDIO interface clock signal(USXGMII_1)	1.8
71	USXGMII_1_MD_DATA	B	MDIO interface data signal(USXGMII_1)	1.8
60	USXGMII_1_RES ET_N	DO	Reset signal for ethernet PHY(USXGMII_1)	1.8
68	USXGMII_1_INT_N	DO	SGMII 1 PHY interrupt(USXGMII_1)	1.8
266	ETH0_AQR_PWR_EN	DO	Power enable signal for ethernet PHY(USXGMII)	1.8
269	ETH1_RTL_PWR_EN	DO	Power enable signal for ethernet PHY(USXGMII_1)	1.8
262	SDX_SYNC_1558	DIO	General purpose input or output	1.8
28	SDX_PCIE0_RX0_P	AI	PCIe 0 Gen 3 receive 0 - plus	
31	SDX_PCIE0_RX0_M	AI	PCIe 0 Gen 3 receive 0 - minus	
27	WK_5G_PCIE0_RX0_P	AO	PCIe 0 Gen 3 transmit 0 - plus	



24	WK_5G_PCIE0_RX0_M	AO	PCIe 0 Gen 3 transmit 0 - minus	
20	SDX_PCIE0_RX1_P	AI	PCIe 0 Gen 3 receive 1 - plus	
23	SDX_PCIE0_RX1_M	AI	PCIe 0 Gen 3 receive 1 - minus	
19	WK_5G_PCIE0_RX1_P	AO	PCIe 0 Gen 3 transmit 1 - plus	
16	WK_5G_PCIE0_RX1_M	AO	PCIe 0 Gen 3 transmit 1 - minus	
32	SDX_PCIE0_REFC_LK_P	AO	PCIe 0 Gen 3 reference clock - plus	
35	SDX_PCIE0_REFC_LK_M	AO	PCIe 0 Gen 3 reference clock - minus	
22	SDX_PCIE0_WAKE_N	B	PCIe0 wake up signal	1.8
26	SDX_PCIE0_CLKREQ_N	DO	PCIe0 clock request	1.8
30	SDX_PCIE0_RESET_N	DO	PCIe0 reset signal	1.8
11	SDX_PCIE1_RX0_P	AI	WLAN PCIe transmit output differential signals lane 0 - plus	0.88
8	SDX_PCIE1_RX0_M	AI	WLAN PCIe transmit output differential signals lane 0 - minus	0.88
9	WK_6G_PCIE1_RX0_P	AO	WLAN PCIe receive input differential signals lane 0 - plus	0.88
10	WK_6G_PCIE1_RX0_M	AO	WLAN PCIe receive input differential signals lane 0 - minus	0.88
3	SDX_PCIE1_RX1_P	AI	WLAN PCIe transmit output differential signals lane 1 - plus	0.88
2	SDX_PCIE1_RX1_M	AI	WLAN PCIe transmit output differential signals lane 1 - minus	0.88
6	WK_6G_PCIE1_RX1_P	AO	WLAN PCIe receive input differential signals lane 1 - plus	0.88
5	WK_6G_PCIE1_RX1_M	AO	WLAN PCIe receive input differential signals lane 1 - minus	0.88
7	SDX_PCIE1_REFC_LK_P	AO	WLAN PCIe reference clock input differential signals - plus	0.88
4	SDX_PCIE1_REFC_LK_M	AO	WLAN PCIe reference clock input differential signals - minus	0.88
21	SDX_PCIE1_WAKE_N	DI	WLAN PCIe wake-up signal. It is an open-drain signal that requires an external pull-up resistor. (4.7K PU)	1.8
13	SDX_PCIE1_CLKREQ_N	B	WLAN PCIe clock request signal. It is an open-drain signal that requires an external pull-up resistor. (4.7K PU)	1.8



17	SDX_PCIE1_RESET_N	DO	WLAN PCIe reset	1.8
55	SDX_PCIE2_RX0_P	AI	PCIe 2 Gen 3 receive - plus	
58	SDX_PCIE2_RX0_M	AI	PCIe 2 Gen 3 receive - minus	
47	WK_2G_PCIE2_RX0_P	AO	PCIe 2 Gen 3 transmit - plus	
50	WK_2G_PCIE2_RX0_M	AO	PCIe 2 Gen 3 transmit - minus	
51	SDX_PCIE2_REFCLK_P	AO	PCIe 2 Gen 3 reference clock - plus	
54	SDX_PCIE2_REFCLK_M	AO	PCIe 2 Gen 3 reference clock - minus	
56	SDX_PCIE2_WAKE_N	B	PCIe2 wake up signal	1.8
52	SDX_PCIE2_CLKREQ_N	DO	PCIe2 clock request	1.8
48	SDX_PCIE2_RESET_N	DO	PCIe2 reset signal	1.8
235	SDR_RFFE1_CLK	DO	ANT tuner MIPI_1_CLK (52HMz) form SDR	-
236	SDR_RFFE1_DATA	DO	ANT tuner MIPI_1_DATA form SDR	-
243	SDR_RFFE3_CLK	DO	ANT tuner MIPI_3_CLK (52HMz) form SDR	-
244	SDR_RFFE3_DATA	DO	ANT tuner MIPI_3_DATA form SDR	-
239	SDR_RFFE7_CLK	DO	ANT tuner MIPI_7_CLK (52HMz) form SDR	-
240	SDR_RFFE7_DATA	DO	ANT tuner MIPI_7_DATA form SDR	-
263	SDX_GPIO_29	DIO	1. ANT tuner MIPI_0_DATA form SDX 2. 1.8V SDX GPIO_29 reserved	- 1.8V
267	SDX_GPIO_30	DIO	1. ANT tuner MIPI_0_CLK (38.4HMz) form SDX 2. 1.8V SDX GPIO_30 reserved	- 1.8V
220	DEV_SOL	DIO	Device sign of life (WCN or QFW to HOST sign of life indicator)	1.8
216	WCN_HOST_SOL	DIO	Host sign of life (HOST to WCN or QFW sign of life indicator)	1.8
212	WLAN_LTE_COXM_TXD	DO	WSI interface for WLAN/LTE Co-ex algorithms	1.8
208	WLAN_LTE_COXM_RXD	DI	WSI interface for WLAN/LTE Co-ex algorithms	1.8



160	BT_UART_TXD	DO	BT_UART_RXD	1.8
171	BT_UART_RXD	DI	BT_UART_TXD	1.8
167	BT_UART_CTS_N	DI	BT_UART_RTS	1.8
163	BT_UART_RFR_N	DO	BT_UART_CTS	1.8
207	BT_SEC_I2S_WS	B	BT_I2S_Word Select	1.8
195	BT_SEC_I2S_SCK	B	BT_I2S_SCK	1.8
199	BT_SEC_I2S_D1	B	BT_I2S_SDI	1.8
203	BT_SEC_I2S_D0	B	BT_I2S_SDO	1.8
164	RF_CLK1_WLAN	AO	76.8 MHz RF clock to WLAN	-
172	BT_EN	DO	Bluetooth enable signal. It is an active high to enable Bluetooth operation.	1.2 or 1.8
176	N79_TX_EN_TO_WLAN	DO	WL_XFEM_CTRL_N79_TXEN form SDR GRFC_14	1.2 or 1.8
180	NC		Reserve for n79 LNA control	1.8
219	WK_2G_WLAN_D IS	DO	WLAN enable signal. It is an active high to enable WLAN operation	1.8
215	WK_2G_PWR_EN	DI	Switch request to external PMU between active and sleep mode for WLAN.	1.8
223	WK_6G_WLAN_D IS	DI	Switch request to external PMU between active and sleep mode	1.8
237	WK_5G_PWR_EN	DI/DO	Reserve SDX GPIO_82 for QFW	1.8
241	WK_6G_PWR_EN	DI/DO	Reserve SDX GPIO_17 for QFW	1.8
238	WK_5G_WLAN_D IS	DI/DO	Reserve SDX GPIO_16 for QFW	1.8
1,12,14,15,18,25,29, 33,34,36,37,38,39, 40,41,42,43,44,45,4 6,49,53,57,61,62,65 ,78,90,98,101,120,1 21,122,123,130,133 ,135,136,148,150,1 52,153,155,157,159 ,161,162,204,165,1	GND_1~GND_60			



66,168,170,224,173 ,174,175,177,178,1 82,183				
185,186,187,189,19 0,191,184,194,227, 197,198,201,202,20 6,209	GND_61~75			
210,213,214,211,21 8,221,222,225,226, 229,231,232,234,24 7,248,301,303,304, 306,313,314,315,31 6,317,318,319,320, 321,322,323,324,32 5,326,327,328,329, 330,331,332,333,28 3,287,284,337,338, 339,340,341,342,34 3,279,336,280,347, 348,349,350,351,35 2,353	GND76~135			
275,272,276,357~3 63,356,346,366~36 8,250,246,242,249, 252,245,251,256,15 4	GND136~150 GND195~GND203			
369,370~412	GND151~194			

AI : Analog input

AO : Analog output

B : Bidirectional digital with CMOS input

PD: Pull-Down

PU: Pull-Up

T: Tristate

OD: Open Drain

PP: Push-Pull

PI: Power Input

PO: Power Output

Z: High-impedance (Hi-Z) output



NOTE:

The unused pins can be left floating.

- **P** indicates power pins; **I** indicate pins for digital signal input; **O** indicates pins for digital signal output; **PO** indicates power output pins; **PI** indicates power input pins.
- **VIL** indicates Low-level Input voltage; **VIH** indicates High-level Input voltage; **VOL** indicates Low-level Output voltage; **VOH** indicates High-level Output voltage.
- The **NC** pins are not connected, therefore, before you deal with these pins; please refer to the corresponding hardware guide.
- The **Reserved** pins are internally connected to the module. Therefore, these pins should not be used, otherwise they may cause problems. Please contact with us for more details about this information.
- SIM2 supply two different voltage 1.2V/1.8V. Please contact Compal sales and TAM for SKU option.

3.3 Power Interface

The power interface of 5G LGA Module as shown in the following table 3-2 :

Table 3-2 Power Interface

Pin	Pin Name	Pin Description	DC Parameter (V)		
			Min	Typ	Max
79,80,81,83,84,85,88	VPH_PWR	Power supply input range from Battery type (it still depend on real battery ability and profile to adjust for avoid any safety, swell & thermal issues.)	3.4	3.8	4.4
		Power supply min input from Constant Voltage Mode	3.23	3.4	3.57
		Power supply input Recommended voltage from Constant Voltage Mode	3.8	4	4.2
82	SIM1_VCC	UIM1 dual-voltage 1.8 V or 2.95 V IF	1.7	1.8	1.94
			2.71	2.95	3.04
86	VREG_L13_UIM2_NU_1P8	UIM2 support voltage 1.2/1.8V IF VREG_L13_UIM2_NU_1P8 support 1.8V eSIM only. If eSIM2 use 1.2V, need add external LDO 1.2V. or use Pin106 (VREG L15 1P2)		1.8	
107	VREG_1P8_SYS	Power supply output for WIFI (for Qualcomm WCN chip power only. Do not use for other purpose.)	1.7	1.8	1.9
116	VREG_1P2_SYS		1.14	1.2	1.26
119	VREG_L6_1P8		1.7	1.8	1.9



91,87	VREG_S7_0P974_1, VREG_S7_0P974_2		0.925	0.974	1.022
89	VREG_S2_1P224		1.14	1.2	1.26
92,95	VREG_S4_1P904_1, VREG_S4_1P904_2		1.8	1.9	2.0
106	VREG_L15_1P2			1.2	
118	VREG_L12_1P2	Reserve power supply for ANT tuner (1.2V)	1.14	1.2	1.26

Table 3-2-1 Power interface output capacitance requirement

Pin	Power Name	Output capacitance		
		Nominal max (no derating) Just for reference	Derated Min (after temperature, aging, bias, and tolerance)	Derated Max (after temperature, aging, bias, and tolerance)
119	VREG_L6_1P8	2.2uF	0	6 μF at 1.8 V
106	VREG_L15_1P2	4.7uF	0	18 μF at 1.2 V
118	VREG_L12_1P2	4.7uF	0	17 μF at 1.2 V

Table 3-2-2 Power interface output voltage (V) and Current (A) summary

	Voltage(V)	Irated(A)	Comment
VREG_1P8_SYS	1.8	0.02	For Qualcomm WCN chip power only. Do not use for other purpose.
VREG_1P2_SYS	1.2	N/A	
VREG_L6_1P8	1.8	0.6	
VREG_S7_0P974_1, VREG_S7_0P974_2	0.974	5	
VREG_S2_1P224	1.2	5	
VREG_S4_1P904_1, VREG_S4_1P904_2	1.9	5	
VREG_L15_1P2	1.2	1.2	
VREG_L12_1P2	1.2	1.2	



NOTE:

The Nominal max (no derating) capacitance value is just for your reference. The final capacitance value placement still needs to follow Derated Min/Max spec to setup.

5G LGA Module can use any power source which is followed “Table 3-2 power supply input” as an Input power. Then, it has 5 output powers for each function such as Wi-Fi, USIM and antenna tuner . Due to the limited power trace, all of them should use efficiently when design the layout.



When the 5G LGA module is used for different external applications, pay special attention to the design for the power supply. When the 5G LGA module works at 4G/5G MIMO mode and transmits signals at the maximum power, the transient current may reach the transient peak value of about 4A due to the differences in actual network environments. In this case, the VBAT voltage drops. If you want wireless good performance, please make sure that the voltage does not decrease below 3.4 V in any case. Otherwise, exceptions such as restart of the 5G LGA module may occur.

A low-dropout (LDO) regulator or switch power with current output of more than 4A is recommended for external power supply. Furthermore, five 220 μ F or above energy storage capacitors are connected in parallel at the power interface of the 5G LGA module. In addition, to reduce the impact of channel impedance on voltage drop, you are recommended to try to shorten the power supply circuit of the VBAT interface.

It is recommended that customers add the EMI ferrite bead (FBMJ1608HS280NT manufactured by TAIYO YUDEN or MPZ1608S300ATAH0 manufactured by TDK is recommended) to directly isolate DTE from DCE in the power circuit. Figure 3-3 shows the recommended power circuit of 5G LGA module.

3.4 PCIe Interface

LGA Module supports two PCIe Gen3 2-lane interface which connected to Qualcomm QFW7114/QFW7124(5G, 6G) as WLAN data interface. And one PCIe Gen3 1-lane is connected to QFW7114/QFW7124(2.4G) as WLAN data interface. And need add Ethernet Bridge Controller IC Solution if want to support 10Gbps Ethernet by USXGMII/SGMII interface, the additional components QEP8121, QEP8111 or a third-party PHY is required on the circuit.

3.4.1 Overview

LGA Module supports PCIe Gen3, one lane for data transmission channel. it is also compatible with PCIe Gen1. After LGA Module is inserted into PC, PCIe interface can work with the driver, then map a MBIM port and a GNSS port in Win10 system. While MBIM interface is used for initiating data service in Win10 system and GNSS interface for receiving GNSS data.

3.5 Audio Interface

LGA module provided one I2S/PCM digital audio interface. Table 3-20 lists the signals on the digital audio interface.

Table 3-20 Audio Interface (I2S/PCM)

Pin	Pin Name	Pin Description	DC Parameter (V)		
			Min	Typ	Max
207	BT_SEC_I2S_WS	BT_I2S_Word Select		1.8	
195	BT_SEC_I2S_SCK	BT_I2S_SCK		1.8	
199	BT_SEC_I2S_D1	BT_I2S_SDO (Output pin, connect to DRX (PCM MOSI))		1.8	
203	BT_SEC_I2S_D0	BT_I2S_SDI (Input pin, connect to DTX (PCM MISO))		1.8	

The LGA module I2S interface enables communication with an external codec to support linear format.



NOTE:

- The I2S function of LGA module is only supported in master mode.
- It is recommended that a TVS be used on the related interface, to prevent electrostatic discharge and protect integrated circuit (IC) components.
- The signal level of CODEC must match that of the LGA module.

3.6 General Purpose I/O Interface (Reserved GPIO)

The LGA module provides GPIO pins for customers to use for controlling signals which are worked at 1.8 V CMOS logic levels, it can be release as a GPIO pin when charging function is no use. Customers can use AT command to control the state of logic levels of GPIO output signal. About the details of GPIO command see the Compal LGA LTE Module AT Command Interface Specification.

It is recommended that a TVS be used on the related interface such as interrupt/reset pin, to prevent electrostatic discharge and protect integrated circuit (IC) components.

Table 3-21 LGA and other GPIO signal

Pin	Pin Name	Pin Description	DC Parameter (V)		
			Min	Typ	Max
261	SDX_GPIO_18	General purpose input or output		1.8	



264	SDX_GPIO_19	General purpose input or output		1.8	
253	SDX_GPIO_69	General purpose input or output		1.8	
255	SDX_GPIO_74	General purpose input or output		1.8	
258	SDX_GPIO_75	General purpose input or output		1.8	
254	SDX_GPIO_77	General purpose input or output		1.8	
259	SDX_GPIO_78	General purpose input or output		1.8	
260	SDX_GPIO_79	General purpose input or output		1.8	
257	SDX_GPIO_64	General purpose input or output		1.8	
265	SDX_GPIO_65	General purpose input or output		1.8	
125	PMX75_GPIO_2	Configurable; default digital input with 10 μ A pull-down			
126	PMX75_GPIO_15	Configurable; default digital input with 10 μ A pull-down			
132	PMX75_GPIO_16	Configurable; default digital input with 10 μ A pull-down			
109	PMX75_AMUX1	AUXIN(PMX75_GPIO_05)			
110	PMX75_AMUX2	AUXIN(PMX75_GPIO_12)			

Figure 3-21 Example diagram of GPIO interface



Table 3-23 EBI2 interface (Reserve EBI2 (9 bit) interface for LCM function)

Pin	Pin Name	Pin Description	DC Parameter (V)		
			Min	Typ	Max
297	EBI2_A_D0	EBI2 multiplexed address and data - bit 0		1.8	
293	EBI2_A_D1	EBI2 multiplexed address and data - bit 1		1.8	
296	EBI2_A_D2	EBI2 multiplexed address and data - bit 2		1.8	
295	EBI2_A_D3	EBI2 multiplexed address and data - bit 3		1.8	
289	EBI2_A_D4	EBI2 multiplexed address and data - bit 4		1.8	
292	EBI2_A_D5	EBI2 multiplexed address and data - bit 5		1.8	
299	EBI2_A_D6	EBI2 multiplexed address and data - bit 6		1.8	
300	EBI2_A_D7	EBI2 multiplexed address and data - bit 7		1.8	
294	EBI2_A_D_8	EBI2 multiplexed address and data - bit 8		1.8	
298	EBI2_OE_N	EBI2 output enable		1.8	
309	EBI2_CLE_UB_N	EBI2 command latch enable		1.8	
311	EBI2_BUSY_N	EBI2 busy signal		1.8	
312	EBI2_ALE_N	EBI2 address latch enable		1.8	
307	EBI2_WE_N	EBI2 write enable		1.8	
310	EBI2_LCD_TE	EBI2 LCD tearing effect		1.8	
302	EBI2_LCD_RESET_N	EBI2 LCD reset		1.8	
305	EBI2_LCD_CS_N	EBI2 LCD chip select		1.8	

- LCD controller features include: Data interface width: 8 bits or 9 bits, muxed with NAND flash
- Resolution: HVGA, 320 (V) ×480 (H) pixels at up to 30 fps
- Color depth: up to 18 bits/pixel (RGB 6-6-6) or 16-bit/pixel (RGB 5-6-5)
- LCD interfaces:
 - ◆ DBI type B only
 - ◆ 8-bit or 9-bit parallel data interface



3.7 JTAG Interface

Only Test Point Reserve inside of LGA modules

3.8 RF Antenna Interface

The LGA module provides five antenna pads (four:ANT0~ANT3 and one GNSS) for connecting the external antennas.

The RF pad difference is the most important difference between LGA modules; please refer to 49 mm x 50 mm LGA Module Hardware Migration Guide.

Route the antenna pad as close as possible to antenna connector. In addition, the impedance of RF signal traces must be 50 Ω .

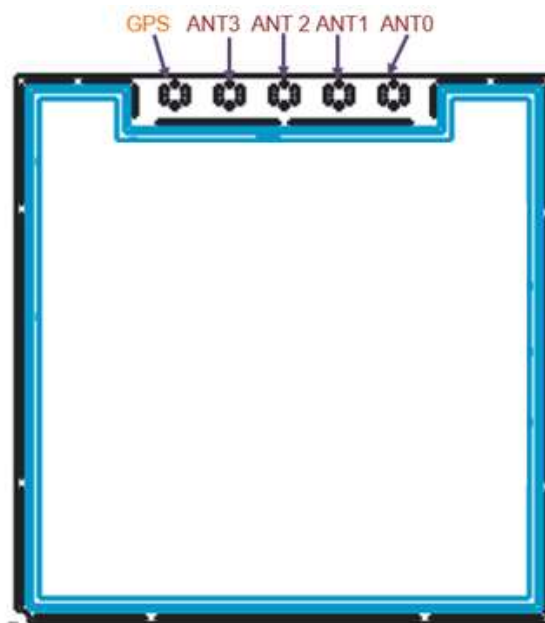


Figure 3-22 Definition of the antenna pinout location (Perspective View from TOP Side)



Table 3-24 Definition of the antenna port mapping

Frequency		Ant_0	Ant_1	Ant_2	Ant_3	Ant_4
LB	600-960 MHz	Tx0/PRx	DRx	DRx2	Tx0/PRx2	
MB	1710-2200 MHz	Tx0/PRx	PRx2	DRx2	Tx1/DRx	
HB	2300-2700 MHz	Tx1/DRx	DRx2	PRx2	Tx0/PRx	
N77/78	3300-4200 MHz	Tx0/PRx	PRx2	DRx2	Tx1/DRx	
GPS L1	1575-1610 MHz					Rx

For NA notice:

LB ANT_0 : TX0 support B5/12/13/14/n5/n12/n13/n14

LB ANT_3 : TX0 support B71/n71

For EU notice:

LB ANT_0 : TX0 support B5/B8/B18/B19/B20/B26/B28/n5/n8/n20/n26/n28

LB ANT_3 : TX0 support B8/n8 , B28/n28 -> for CA & ENDC "20+28/18+28/19+28/28+5"

Supported air Interfaces for each of band groups are listed in the following table 3-24-1.

Table 3-24-1

Band Group	Fmin (MHz)	Fmax (MHz)	Air Interface
LB	600	960	LTE FDD: B5/12/13/14/17/26/29/71 5G NR FR1 FDD: n5/12/13/14/26/29/71
MB	1427.9	2170	LTE FDD: B2/4/25/66 5G NR FR1 FDD: n2/25/66/70
HB	2300	2690	LTE FDD: B7/30 LTE TDD: B38/41 5G NR FR1 FDD: n7/30 5G NR FR1 TDD: n38/41
UHB	3000	6000	LTE TDD: B42/43/48 5G NR FR1 TDD: n48/77/78





3.8.1 RF Connector Characteristic

Table 3-25

Rated Condition		Environment Condition
Frequency Range	DC to 6GHz	Temperature Range
Characteristic Impedance	50Ω	−40°C to +85°C

3.9 Reserved Interface

The LGA module provides some reserved pins in the section 3.13. All reserved pins cannot be used by the customer. All of them must be leave unconnected.

3.10 NC Interface

The LGA module has some NC pins. All NC pins should not be connected.
Please keep these pins open.

Table3-26 lists NC pins signal

Pin	Pin Name	I/O	Pin Description	DC Parameter (V)		
				Minimum Value	Typical Value	Maximum Value



3.11 Tunable Antenna Control

The module provides tunable antenna control pins. The firmware with this feature is in plan.
The mapping of each band to ANT_TUNE outputs is configurable

Table 3-27 tunable antenna control pin

Pin	Pin Name	Type	Pin Description
235	SDR_RFFE1_CLK	DO	ANT tuner MIPI_1_CLK (52HMz) form SDR
236	SDR_RFFE1_DATA	DO	ANT tuner MIPI_1_DATA form SDR
243	SDR_RFFE3_CLK	DO	ANT tuner MIPI_3_CLK (52HMz) form SDR
244	SDR_RFFE3_DATA	DO	ANT tuner MIPI_3_DATA form SDR
239	SDR_RFFE7_CLK	DO	ANT tuner MIPI_7_CLK (52HMz) form SDR
240	SDR_RFFE7_DATA	DO	ANT tuner MIPI_7_DATA form SDR

3.12 SGMII/USXGMII Interface

LGA Module support 2 port SGMII/USXGMII is the interface between 10/11/1000/2500/10000 Mbps PHY and Ethernet MAC. The spec is raised by Cisco in 1999, aiming for pin reduction compared the GMII.

It used two differential data pairs for TX and RX with clock embedded bit stream to convey frame rata and port ability information, SMGII supports up to 10Gbps data rate of MAC by overclocking,



3.12.1 SGMII/USXGMII Interface Pin Definition

Table 3-28 Lists the SGMII/USXGMII interface signals.

Pin NO.	Pin Name	I/O	Pin Description	Type(V)
72	SDX_USXGMII_TX_M	AO	USXGMII interface 0 serial data Tx - minus	
70	SDX_USXGMII_TX_P	AO	USXGMII interface 0 serial data Tx - plus	
69	AQR_USXGMII_TX_M	AI	USXGMII interface 0 serial data Rx - minus	
66	AQR_USXGMII_TX_P	AI	USXGMII interface 0 serial data Rx - plus	
76	SDX_USXGMII_1_TX_M	AO	USXGMII interface 1 serial data Tx - minus	
77	SDX_USXGMII_1_TX_P	AO	USXGMII interface 1 serial data Tx - plus	
73	RTL_USXGMII_TX_M	AI	USXGMII interface 1 serial data Rx - minus	
75	RTL_USXGMII_TX_P	AI	USXGMII interface 1 serial data Rx - plus	
67	USXGMII_0_MD_CLK	B	MDIO interface clock signal(USXGMII)	1.8
64	USXGMII_0_MD_DATA	B	MDIO interface data signal(USXGMII)	1.8
63	USXGMII_0_RESET_N	DO	Reset signal for Ethernet PHY(USXGMII)	1.8
59	USXGMII_0_INT_N	DO	SGMII 0 PHY interrupt(USXGMII)	1.8
74	USXGMII_1_MD_CLK	B	MDIO interface clock signal(USXGMII_1)	1.8
71	USXGMII_1_MD_DATA	B	MDIO interface data signal(USXGMII_1)	1.8
60	USXGMII_1_RESET_N	DO	Reset signal for ethernet PHY(USXGMII_1)	1.8
68	USXGMII_1_INT_N	DO	SGMII 1 PHY interrupt(USXGMII_1)	1.8

3.12.2 SGMII/USXGMII Interface Application

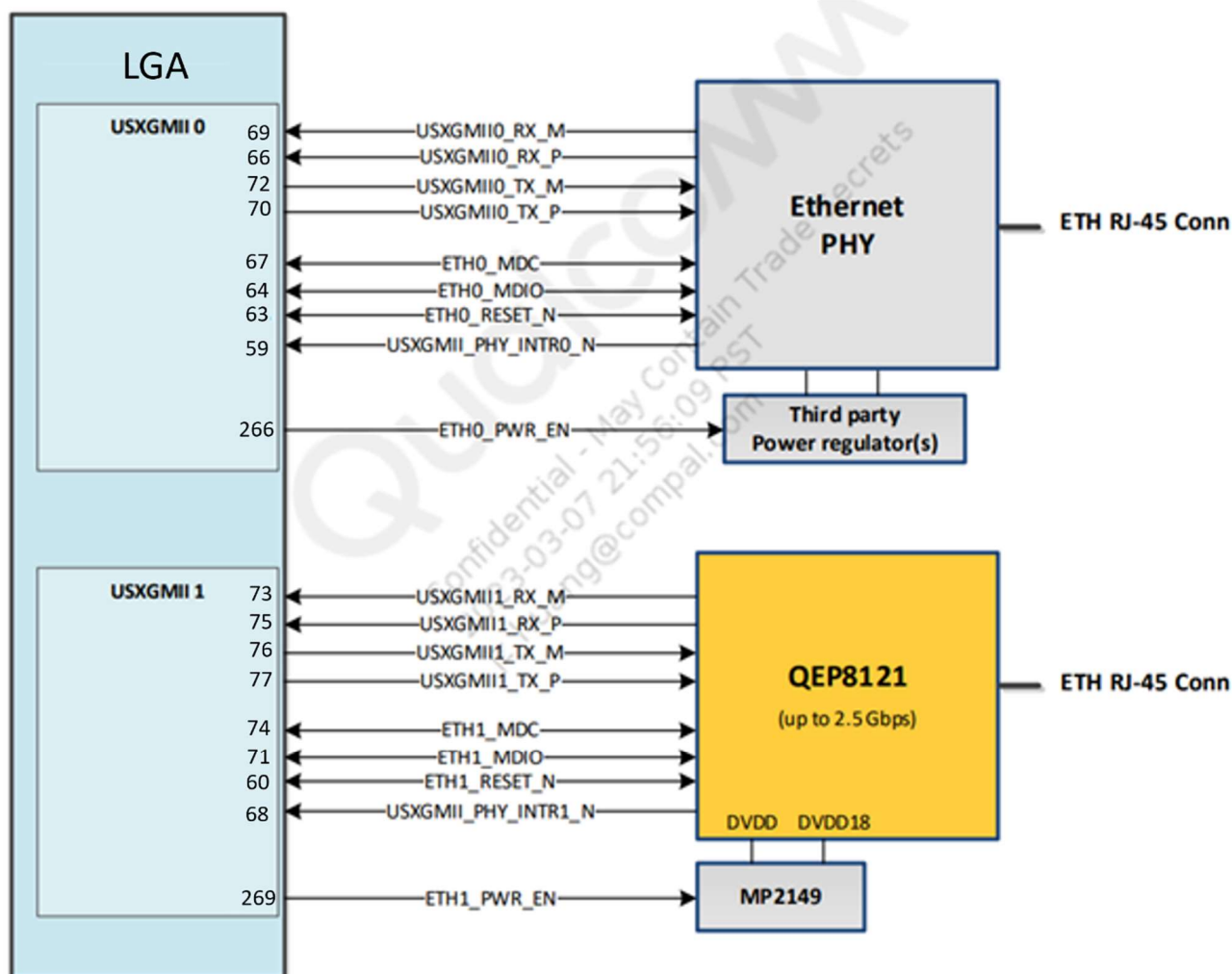


Figure 3-23 shows the circuit of the SGMII/USXGMII card interface

Table 3-29 Reference parts of Supported Ethernet Controllers

Manufacturer	Model	Speeds
Marvell	AQR113C	10 Gbps/5 Gbps/2.5 Gbps/1 Gbps/100 Mbps/10 Mbps
Marvell	AQC113	10 Gbps/5 Gbps/2.5 Gbps/1 Gbps/100 Mbps/10 Mbps
Marvell	AQR114C	5 Gbps/2.5 Gbps/1 Gbps/100 Mbps/10 Mbps
Realtek	RTL8261N	10 Gbps/5 Gbps/2.5 Gbps/1 Gbps/100 Mbps/10 Mbps
Realtek	RTL8125	2.5 Gbps/1 Gbps/100 Mbps/10 Mbps
Qualcomm	QEP8121	2.5 Gbps/1 Gbps/100 Mbps/10 Mbps
Qualcomm	QEP8111	1 Gbps/100 Mbps/10 Mbps



3.12.3 SGMII Routing Constraints

Table3-30 USXGMII layout constraint

Metrics			Guidance
Data rate			10.3125 Gbps
Channel differential insertion loss at 5.5 GHz (dB)			-6 dB (Equalization)
Bus length			216 mm
Impedance *	Differential	Field route	90–110 Ω (nominal 100 Ω)
Length match	Intralane length match		5 ps (0.7 mm)
Isolation	Tx to Rx at <5.15 GHz		> -50 dB
Spacing	To all other signals	Field route	4 × line width
	Rx-to-Tx		4 × line width
Component	DC Blocking Capacitor		0.1 μ F (100 nF)



NOTE :

- Consider the USXGMII bus length include LGA internal routing, the bus length is 185mm
- Both SGMII0:AQR_USXGMII_TX_M and AQR_USXGMII_TX_P (Pin69/66), SGMII1:RTL_USXGMII_TX_M and RTL_USXGMII_TX_P(Pin73/75) should be connected to 0.1uF AC coupling capacitance. (close TX pin of DTE side.)
- The Module IO power domain is 1.8V, so it Must connect to 3.3V level shift on your board if external PHY is 3.3V power domain.
- For MDIO interface, recommend insert GND between MDC and MDIO to prevent crosstalk.
- When SGMII feature is un-used, please keep TX/RX floating.
- Max routing Vias-hole/layer change in the differential pair should be less than 2.
- Keep a safety distance of SGMII trace routing between high EMI parts in order to minimize the side effect of interference
- Routing differential pair straight and symmetrically on the same layer.
- Differential pairs are well-shielding by GND and GND via. (adjacent and up/down layers)
- Resistor on SGMII TX, RX traces in series connection is unnecessary. Use 0-ohm if series resistor have to be reserved.



4 Radio Frequency

4.1 Overview

This chapter describes the RF specifications of the LGA module, including:

- Operating Frequencies
- Conducted Rx Sensitivity and Tx Power
- Antenna Design Requirements

4.2 Operating Band

The 5G LGA Module operating bands of the antennas are as follows table 4-1:

Table 4-1

Band name	Tx (MHz)	Rx (MHz)	LTE	UMTS	5G NR
IMT (2100)	1920 - 1980	2110 - 2170	B1		n1
PCS (1900)	1850 - 1910	1930 - 1990	B2		n2
DCS (1800)	1710 - 1785	1805 - 1880	B3		n3
AWS	1710 - 1755	2110 - 2155	B4		
Cell (850)	824 - 849	869 - 894	B5		n5
IMT-E (2600)	2500 - 2570	2620 - 2690	B7		n7
700 lower A-C	699 - 716	729 - 746	B12		n12
700 upper C	777 - 787	746 - 756	B13		n13
700 D	788 - 798	758 - 768	B14		n14
B17	704 - 716	734 - 746	B17		
PCS + G	1850 - 1915	1930 - 1995	B25		n25
B26	814 - 849	859 - 894	B26		n26
700 APAC	703 - 748	758 - 803	B28		n28
WCS	2305 - 2315	2350 - 2360	B30		n30
B38	2570 - 2620		B38		n38
B41/B41-XGP	2496 - 2690		B41		n41
B42	3400 - 3600		B42		
B43	3600 - 3800		B43		
B48	3550 - 3700		B48		n48



B66	1710 - 1780	2110 - 2200	B66		n66
B70	1695 - 1710	1995 - 2020			n70
B71	663 - 698	617 - 652	B71		n71
n77	3300 - 4200				n77
n78	3300 - 3800				n78

4.3 Transmitting Power

The transmitting power for each band of the LGA module as shown in the following table:

Table 4-3 LTE FDD

Mode	Band	Typical Value (dBm)	Note
LTE FDD	Band 2	24	+0.5/-2
	Band 4	24	+0.5/-2
	Band 5	24	+0.5/-2
	Band 7	24	+0.5/-2
	Band 12	24	+0.5/-2
	Band 13	24.5	+0.5/-2
	Band 14	24.5	+0.5/-2
	Band 17	24	+0.5/-2
	Band 25	24	+0.5/-2
	Band 26	24	+0.5/-2
	Band 30	23.5	+0.5/-2
	Band 66	24.5	+0.5/-2
	Band 71	23.5	+0.5/-2

Table 4-4 LTE TDD

Mode	Band	Typical Value (dBm)	Note
LTE TDD	Band 38	23.5	+0.5/-2



	Band 41	23.5	+0.5/-2
	Band 41 HPUE	26.5	+0.5/-2
	Band 42	23.5	+0.5/-2
	Band 43	23.5	+0.5/-2
	Band 48	23.5	+0.5/-2



Table 4-5 NR-FR1 FDD-SISO

Mode	Band	Typical Value (dBm)	Note
	n2	24	+0.5/-2
	n5	24	+0.5/-2
	n7	24	+0.5/-2
	n12	24	+0.5/-2
	n13	24	+0.5/-2
	n14	24	+0.5/-2
	n25	24	+0.5/-2
	n26	24	+0.5/-2
	n30	23.5	+0.5/-2
	n66	24	+0.5/-2
	n70	24	+0.5/-2
	n71	24	+0.5/-2

Table 4-6 NR-FR1 TDD-SISO

Mode	Band	Typical Value (dBm)	Note
NR-FR1 TDD	n38	23.5	+0.5/-2
	n41 PC2	27	+0.5/-2
	n41 PC3	23.5	+0.5/-2
	n48	23.5	+0.5/-2
	n77 PC2	27	+0.5/-2
	n77 PC3	24	+0.5/-2
	n78 PC2	27	+0.5/-2
	n78 PC3	24	+0.5/-2



Table 4-7 NR-FR1 FDD-MIMO

Mode	Band	Typical Value (dBm)	Note
	n2 PC2	27	+0.5/-2
	n7 PC2	26.5	+0.5/-2
	n25 PC2	27	+0.5/-2
	n30	23.5	+0.5/-2
	n66 PC2	27	+0.5/-2
	n70 PC2	27	+0.5/-2

Table 4-8 NR-FR1 TDD-MIMO

Mode	Band	Typical Value (dBm)	Note
NR-FR1 TDD	n38	24	+0.5/-2
	n41 PC1.5	30	+0.5/-2
	n41 PC2	27	+0.5/-2
	n48	23.5	+0.5/-2
	n77 PC1.5	30	+0.5/-2
	n78 PC1.5	30	+0.5/-2



NOTE:

If device is operated in EN-DC mode, total TX power would be “LTE + NR $\cong 23 \pm 2$ ” due to power sharing algorithm.



4.4 Receiver Sensitivity

The receiver sensitivity for each band of the 5G LGA Module as shown in the following table:

Table 4-7 LTE band

Mode (10MHz)	Band	Single Port(Typical)				Combined Port (Typical)
		PRx	DRx	PRx MIMO	DRx MIMO	3GPP spec
LTE	B1	-96	-96	-96	-96	-99.7
	B2	-96	-96	-96	-96	-97.7
	B3	-96	-96	-96	-96	-96.7
	B4	-96	-96	-96	-96	-99.7
	B5	-97	-97			-95
	B7	-96	-96	-96	-96	-97.7
	B12	-98	-98			-94
	B13	-97	-97			-94
	B14	-97	-97			-94
	B17	-97	-97			-94
	B25	-96	-96	-96	-96	-96.2
	B26	-97	-97			-94.5
	B28	-97	-97			-95.5
	B30	-96	-96	-96	-96	98.7
	B38	-96	-96	-96	-96	-99.7
	B41	-96	-96	-96	-96	-97.7
	B42	-97	-97	-97	-97	-98.2
	B43	-97	-97	-97	-97	-98.2
	B48	-97	-97	-97	-97	-98.2
	B66	-96	-96	-96	-96	-99.2
	B71	-97	-97			-94.2



Table 4-8 NR band

Mode (10MHZ,15K)	Band	Single Port(Typical)				Combined Port (Typical)	
		PRx_0	DRx_0	PRx_1	DRx_1	RX	3GPP spec
NR	n1	-96	-96	-96	-96	-102	-99.5
	n2	-96	-96	-96	-96	-102	-97.5
	n3	-96	-96	-96	-96	-102	-96.5
	n5	-97	-97			-100	-94.8
	n7	-96	-96	-96	-96	-102	-97.1
	n12	-97	-97			-100	-93.8
	n13	-97	-97			-100	-93.8
	n14	-97	-97			-100	-93.8
	n25	-96	-96	-96	-96	-102	-96
	n26	-97	-97			-100	-94.5
	n28	-97	-97			-100	-95.5
	n30	-96	-96	-96	-96	-102	-98.5
	n38	-96	-96	-96	-96	-101.5	-99.7
	n48	-97	-97	-97	-97	-102.5	-98.7
	n66	-96	-96	-96	-96	-102	-99
	n70	-96	-96	-96	-96	-102	-99.5
	n71	-97	-97			-100	-96.7

Mode (100MHZ,30K)	Band	Single Port(Typical)				Combined Port(Typical)	
		PRx_0	DRx_0	PRx_1	DRx_1	4-RX	3GPP spec
NR	n41	-83	-83	-83	-83	-88	-84.7
	n77	-85	-85	-85	-85	-90	-85.1
	n78	-85	-85	-85	-85	-90	-85.6



NOTE:

The above values are measured in one antenna situation.

4.5 GNSS

5G LGA Module supports GNSS/BeiDou and AGNSS functions, and adopts RF Divesity and GNSS/Beidou integrated antenna.

Table 4-9

	Condition		Test Result
GPS	TTFF	Cold start	50s@-130dBm
		Hot Start	2s@-130dBm
	Receive Sensitivity	Tracking	-160 dBm
		Acquisition	-155 dBm



NOTE:

Please note that GPS current is tested with RF disabled.

4.6 Antenna Design

4.6.1 Antenna Design Indicators

Antenna Efficiency

Antenna efficiency is the ratio of the input power to the radiated or received power of an antenna. The radiated power of an antenna is always lower than the input power due to the following antenna losses: return loss, material loss, and coupling loss. The efficiency of an antenna relates to its electrical dimensions. To be specific, the antenna efficiency increases with the electrical dimensions.

In addition, the transmission line from the antenna port of LGA module to the antenna is also part of the antenna. The line loss increases with the line length and the frequency. It is recommended that the line loss is as low as possible.



The following antenna efficiency (free space) is recommended for LGA module to ensure high radio performance of the module:

- Efficiency of the primary antenna: $\geq 40\%$ (below 960 MHz); $\geq 50\%$ (over 1420 MHz)
- Efficiency of the secondary antenna: $\geq$ half of the efficiency of the primary antenna in receiving band.
- Efficiency of the GPS antenna: $\geq 50\%$

In addition, the efficiency should be tested with the transmission line.

S11 (VSWR) and S21

S11 indicates the degree to which the input impedance of an antenna matches the reference impedance

(50 Ω). S11 shows the resonance feature and impedance bandwidth of an antenna. Voltage standing wave ratio (VSWR) is another expression of S11. S11 relates to the antenna efficiency. S11 can be measured with a vector analyzer.

The following S11 values are recommended for the antenna of LGA module:

- S11 of the primary antenna ≤ -6 dB
- S11 of the secondary antenna ≤ -6 dB
- S11 of the GPS antenna ≤ -10 dB

In addition, S11 is less important than the efficiency, and S11 has not strong correlation to wireless performance.

S21 indicates the isolation between two antennas.

Isolation

For a wireless device with multiple antennas, the power of different antennas is coupled with each other. Antenna isolation is used to measure the power coupling. The power radiated by an antenna might be received by an adjacent antenna, which decreases the antenna radiation efficiency and affects the running of other devices. To avoid this problem, evaluate the antenna isolation as sufficiently as possible at the early stage of antenna design.

Antenna isolation depends on the following factors:

- Distance between antennas
- Antenna type



- Antenna direction

The primary antenna must be placed as near as possible to the LGA module to minimize the line length. The secondary antenna needs to be installed perpendicularly to the primary antenna. The secondary antenna can be placed farther away from the LGA module. Antenna isolation can be measured with a two-port vector network analyzer.

The following S21 values are recommended for the antenna:

- Isolation between the primary and secondary antennas ≤ -12 dB
- Isolation between the primary antenna and the GPS antenna ≤ -15 dB
- Isolation between the primary (secondary) antenna and the Wi-Fi antenna ≤ -15 dB

Polarization

The polarization of an antenna is the orientation of the electric field vector that rotates with time in the direction of maximum radiation.

The linear polarization is recommended for the primary/secondary antenna of LGA module. The RHCP (Right-Hand Circular Polarization) is recommended for GPS antenna.

Radiation Pattern

The radiation pattern of an antenna reflects the radiation features of the antenna in the remote field region. The radiation pattern of an antenna commonly describes the power or field strength of the radiated electromagnetic waves in various directions from the antenna. The power or field strength varies with the angular coordinates (θ and φ), but is independent of the radial coordinates.

The radiation pattern of half wave dipole antennas is omnidirectional in the horizontal plane, and the incident waves of base stations are often in the horizontal plane. For this reason, the receiving Performance is optimal. We must notice that GPS signal is coming from the satellite in the outer space; it means that the incident waves are over our head.

The following radiation patterns are recommended for the antenna of LGA module.

- Primary/Secondary antenna: omnidirectional.
- GPS antenna: directional, point to the space.

In addition, the secondary antenna's pattern should be complementary with the primary antenna's pattern.

Gain and Directivity

The radiation pattern of an antenna represents the field strength of the radiated electromagnetic waves in all directions, but not the power density that the antenna radiates in the specific direction. The directivity of an antenna, however, measures the power density that the antenna radiates.



Gain, as another important parameter of antennas, correlates closely to the directivity. The gain of an antenna takes both the directivity and the efficiency of the antenna into account. The appropriate antenna gain prolongs the service life of relevant batteries.

The antenna gain is considered from customer product certification to meet its SAR or RSE limit. Additional, if customer product to meet Japan TELEC, below is TELEC requirement:

Normal condition:

- Gain of the TX antenna ≤ 3.0 dBi

High Power User Equipment (HPUE) condition:

- Gain of the TX antenna ≤ 1.0 dBi

ECC of the antenna

ECC is short for Envelope Correlation Coefficient. It is the cross-correlation value of the complex patterns of the master and diversity antenna. It indicates how similar the magnitude and the phase patterns of the two antennas are. If two antennas have no similarity, the ECC should be zero.

Actually, the less ECC, the better diversity performance.

The following ECC is recommended for LGA module.

- $ECC \leq 0.5$ (working frequency below 0.96 GHz)
- $ECC \leq 0.3$ (working frequency above 1.4 GHz)



NOTE:

- The antenna consists of the antenna body and the relevant RF transmission cable. Take the RF transmission cable into account when measuring any of the preceding antenna indicators.
- Compal cooperates with various famous antenna suppliers who are able to make suggestions on antenna design, for example, Amphenol, Skycross, etc.



4.6.2 Interference

Besides the antenna performance, the interference on the user board also affects the radio performance (especially the TIS) of the module. To guarantee high performance of the module, the interference sources on the user board must be properly controlled.

On the user board, there are various interference sources, such as the LCD, CPU, audio circuits, and power supply. All the interference sources emit interference signals that affect the normal operation of the module. For example, the module sensitivity can be decreased due to interference signals. Therefore, during the design, you need to consider how to reduce the effects of interference sources on the module.

You can take the following measures: Use an LCD with optimized performance; shield the LCD interference signals; shield the signal cable of the board; or design filter circuits.

Compal is able to make technical suggestions on radio performance improvement of the module.

4.6.3 Antenna Requirements

The antenna for LGA module must fulfill the following requirements:

Table 4-10 Antenna Requirements

Antenna Requirements	
Frequency range	Depending on frequency band(s) provided by the network operator, the customer must use the most suitable antenna for that/those band(s)
Bandwidth of primary antenna	70 MHz in GSM 850 80 MHz in GSM 900 170 MHz in GSM 1800 140 MHz in GSM 1900 250 MHz in WCDMA /LTE Band 1 140 MHz in WCDMA/LTE Band 2 70 MHz in WCDMA/LTE Band 5 80 MHz in WCDMA/LTE Band 8 170 MHz in LTE Band 3 190 MHz in LTE Band 7 71 MHz in LTE Band 20



Antenna Requirements	
Bandwidth of secondary antenna	60 MHz in WCDMA/LTE Band 1 60 MHz in WCDMA/LTE Band 2 25 MHz in WCDMA/LTE Band 5 35 MHz in WCDMA/LTE Band 8 75 MHz in LTE Band 3 70 MHz in LTE Band 7 30 MHz in LTE Band 20
Bandwidth of GPS antenna	35 MHz in GNSS
Gain	≤ 2.5 dBi (≥ 3 dBi for GPS antenna)
Impedance	50 Ω
VSWR absolute max	$\leq 3:1$ ($\leq 2:1$ for GPS antenna)
VSWR recommended	$\leq 2:1$ ($\leq 1.5:1$ for GPS antenna)



4.7 RF a with sub-6G Design Guide

4.7.1 Purpose

LGA module supports LTE sub-6G and each of that band can generate the 2nd or 3rd harmonic with the frequency about 5 GHz, so that will deteriorate 5 GHz WIFI receiver performance. That is why Co-existence design needed.

4.7.2 Co-existence Design Main Point

DC Power for LGA and WIFI Circuit

The suggest DC power tree is shown as below, use LC filter circuit for each branch.

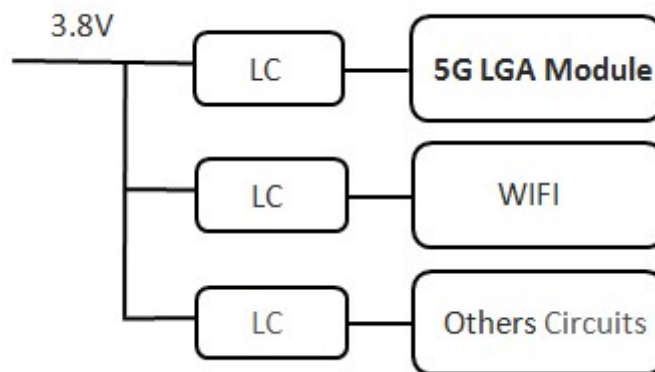


Figure 4-1 The recommend RF front end circuit



PCB Placement Suggestion

For PCB placement, we recommend to keep 5 GHz WIFI antenna away from LGA module and its main antenna as far as possible.

- The recommend isolation between LGA module and WIFI antenna is above 30 dB.
- The recommend isolation between LGA antenna and WIFI antenna is above 30 dB.

5 Mechanical Specifications

5.1 Overview

This chapter describes the process design and mechanical specifications:

- Storage Requirement
- Moisture Sensitivity
- Dimensions and Interfaces
- Packaging
- Label
- Customer PCB Design
- Thermal Design Solution
- Assembly Processes
- Specification of Rework

5.2 Storage Requirement

The module must be stored and sealed properly in vacuum package under a temperature below 40°C and the relative humidity less than 90% in order to ensure the weldability within 12 months.

5.3 Moisture Sensitivity

- The moisture sensitivity is level 3.
- After unpacking, the module must be assembled within 168 hours under the environmental conditions that the temperature is lower than 30°C and the relative humidity is less than 60%. If the preceding conditions cannot be met, the module needs to be baked according to the parameters specified in Table 5-1.

Table 5-1 Baking Parameters

Baking Temperature	Baking Condition	Baking Duration	Remarks
125±5°C	Relative humidity≤60%	48 hours	



NOTE:

Moving, storing, and processing the product must comply with IPC/JEDEC J-STD-033.

Technical drawing of a building section showing a staircase and structural details. The drawing includes dimensions for the staircase width (41.10 to 22.50), riser height (28.80 to 22.50), and tread depth (4.20 to 4.05). It also shows structural details for the staircase and the building frame, including dimensions for the staircase width (41.10 to 22.50), riser height (28.80 to 22.50), and tread depth (4.20 to 4.05). The drawing is labeled with 'CEN-Y' and 'CEN-X' and includes references to 'SEE DETAIL B', 'SEE DETAIL D', 'SEE DETAIL C', and 'SEE DETAIL A'.

2025/03/20

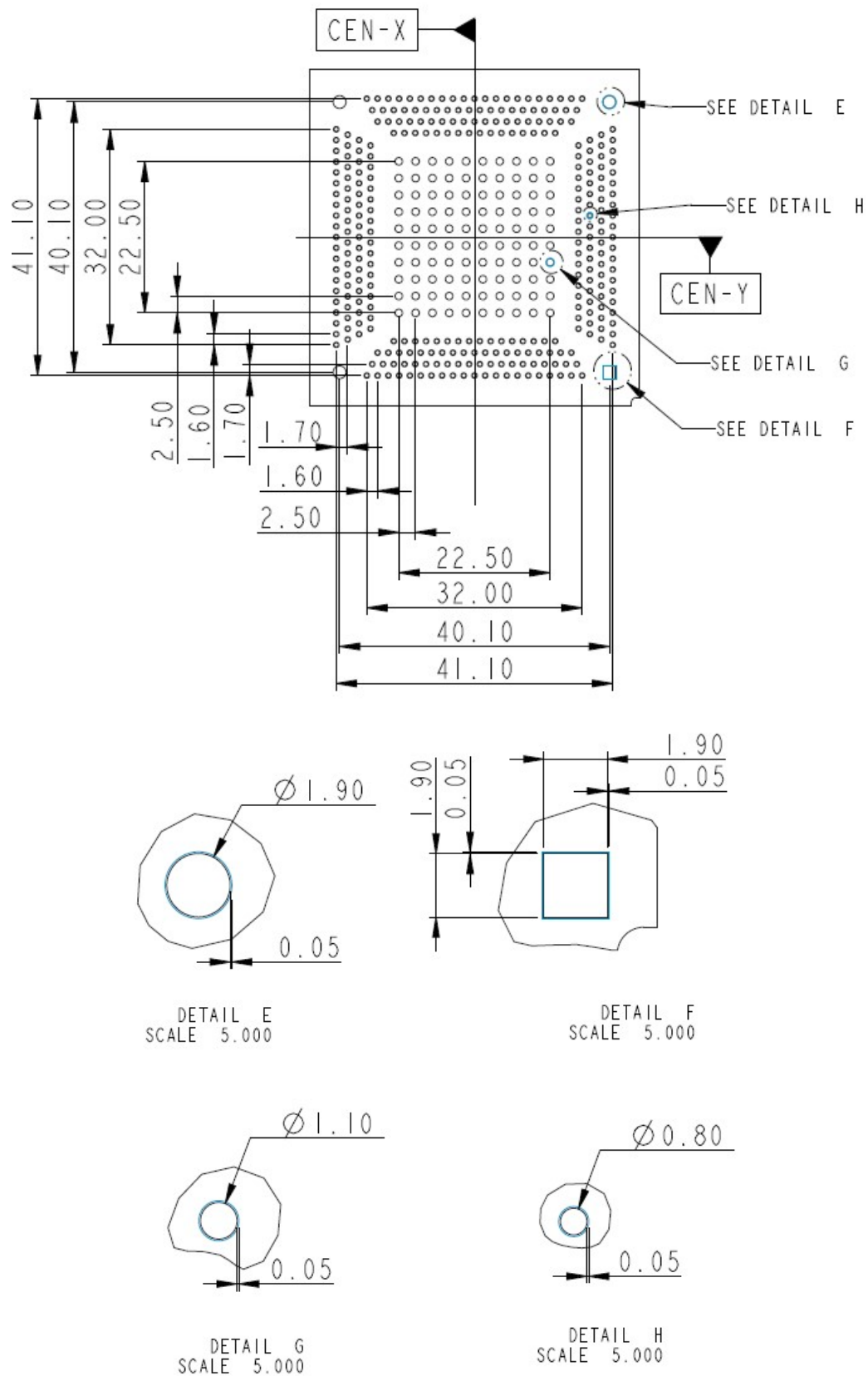


Figure 5-3 The LGA Module Device detail information (Unit: mm) (Intuitive view from BOT side)



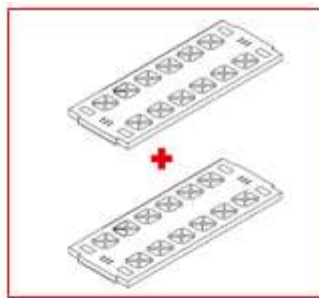
5.5 Packaging

Compal RXL-N3n module uses ESD tray and vacuum bag into boxes. The example process shows in below picture: (Pictures of materials are only for reference.)



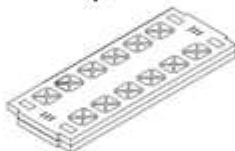
Tray for LGA
12pcs/tray

Outer dimension: (L) 323 *(W)* 135 (H) 8 mm

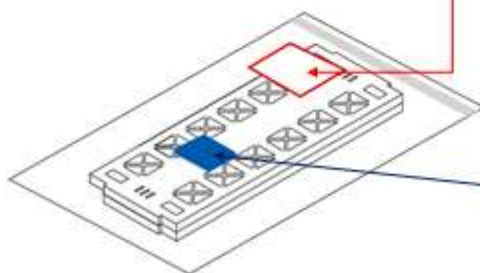


An empty tray as a cover

A tray for loading product.



2 trays should totally match together while stacking



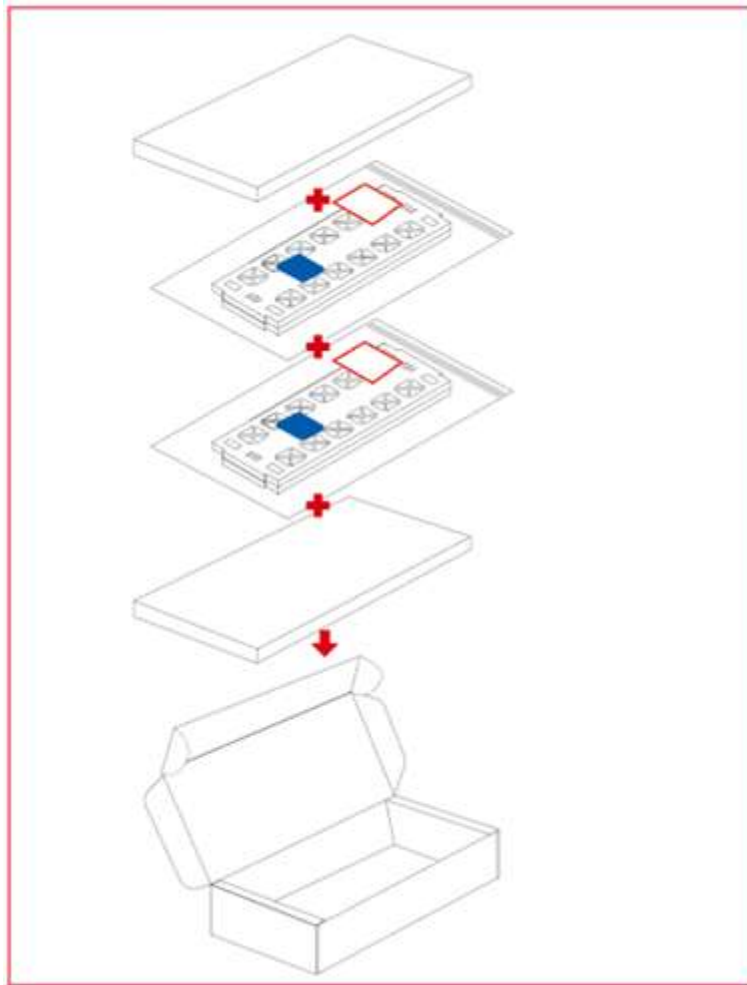
Put trays into a vacuum bag



*Paste the moisture sensitive caution label on the vacuum bag.



*Put the trays with 1pc desiccant in the vacuum bag



A piece of EPE as a upper cover

1 set vacuum bag

1 set vacuum bag

A piece of EPE as a lower cover

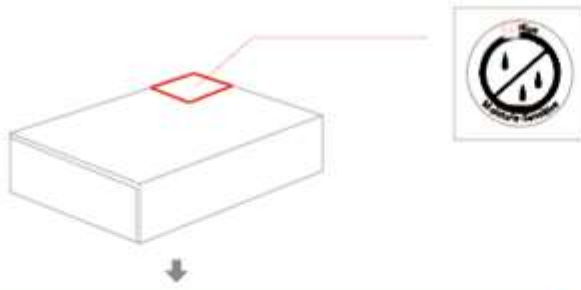
*Put above materials in a pizza box

Pizza box Outer dimension: (L) 360 * (W)* 152 (H) 71 mm

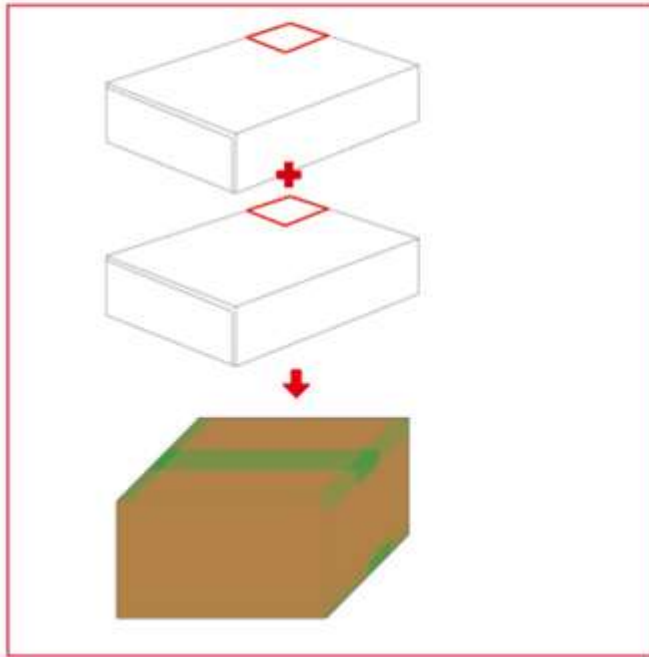


NOTE:

For not fully loaded pizza box, still have to put two pieces of EPE



*Paste the moisture sensitive caution label on the vacuum bag.



*Put 2 boxes in one carton.

Carton Outer dimension: (L) 373 * (W)* 164 (H) 155mm



NOTE:

For not fully loaded carton, please use empty pizza box to full fill the space (Empty pizza box need to be placed on top), and mark these empty boxes with "EMPTY" print or label.



5.5.1 PCB Pad Design

To achieve assembly yields and solder joints of high reliability, it is recommended that the PCB pad size be designed as follows:

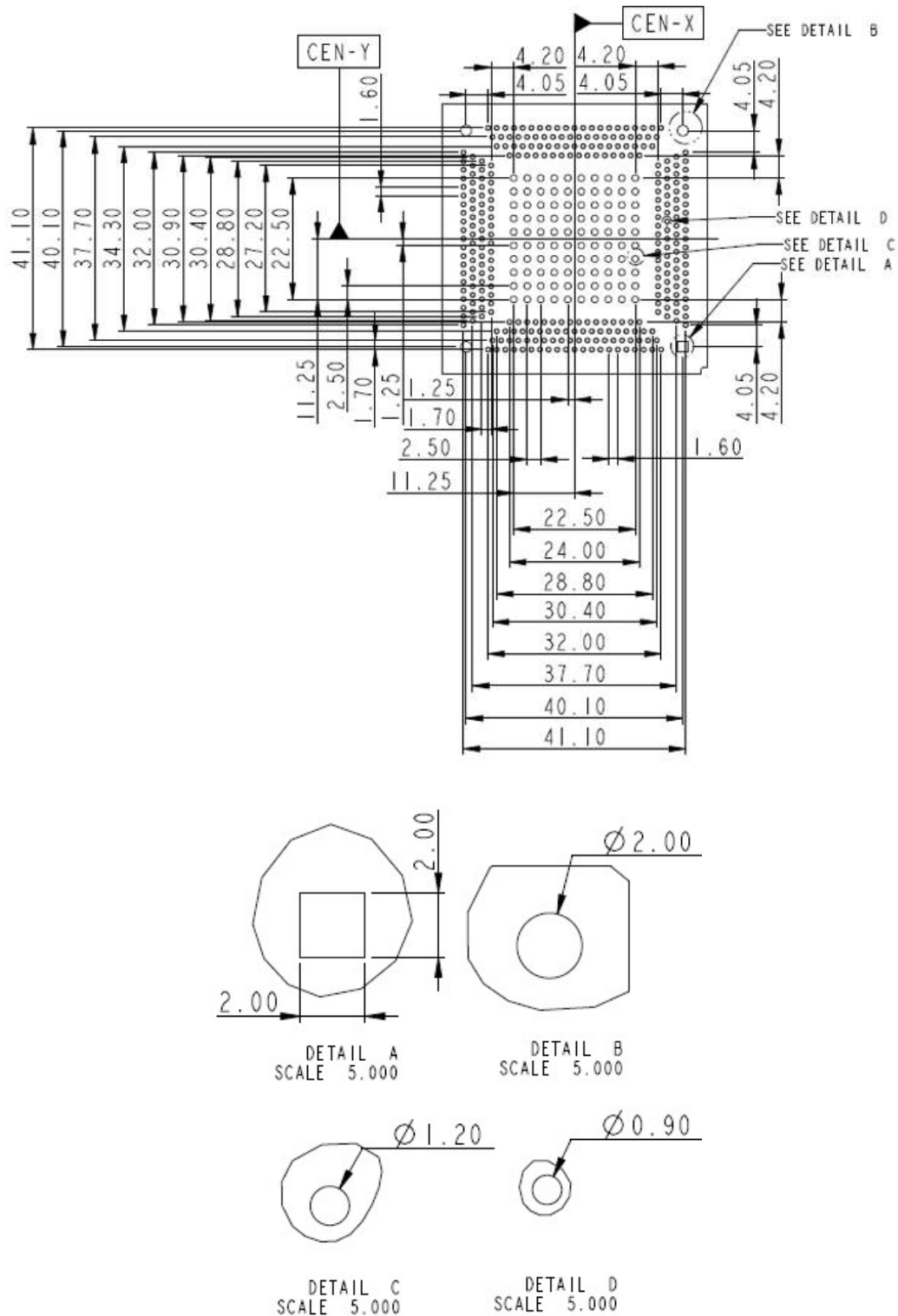


Figure 5-5 PAD Footprint design of customer's PCB (Unit: mm) (Intuitive view from BOT side)



5.5.2 Solder Mask

SMD is recommended. In addition, the solder mask of the SMD (Solder Mask Defined) pad design is larger than the pad so the reliability of the solder joint can be improved.

The solder mask must be 50~100 μm larger than the pad, that is, the single side of the solder mask must be 25~50 μm larger than the pad. The specific size depends on the processing capability of the PCB manufacturer.

Regarding the footprint mask size must be 80 μm ~110 μm larger than the pad, that is, the single side must be 40 μm ~55 μm larger than the pad. Please refer to Figure 5-3 & 5-5 for Module PAD detailed size information.

5.5.3 Requirements on PCB Layout

- To reduce deformation, a thickness of at least 1.2 mm is recommended.
- Other devices must be located more than 3 mm (5 mm recommended) away from the two parallel sides of the LGA module (rework requirement), and other sides with 0.6 mm. The minimum distance between the LGA module and the PCB edge is 0.3 mm.
- When the PCB layout is double sided, the module must be placed on the second side for assembly; so as to avoid module dropped from PCB or component (located in module) re-melting defects caused by uneven weight.
- The thickness of the Stencil is recommended to be 0.15mm~0.18mm, which needs to be determined according to the flatness of the customer's Carrier Board itself.
- It is recommended to use nitrogen(N₂) to assist solder wetting.
- The reflow profile for soldering provided is used as a reference. If the customer uses different solder paste or other temperature measurement software, it can be adjusted according to the actual yield rate.

5.6 Thermal Design Solution

When the module works in the maximum power condition, the module has high power consumption (for details, see Power Consumption). To improve the module reliability and stability, focus on the thermal design of the device to speed up heat dissipation.

For thermal characteristics of the LGA module, you can refer to Operating and Storage Temperatures.



The LGA module has built in thermal interface material, thermal grease, which thermal conductivity is 2.1W/mK.

Below are some thermal recommendation,

The PCB design for thermal heat spreading

- Follow the IC thermal pad placement to put thermal via
- All copper ground layers of the PCB must be connected to each other through via-holes
- Increase the coverage of the PCB ground planes as possible
- The ground planes should be as continuous as possible

Example for thermal heat spreader on LGA module,

- add heat sink on module shielding cover,
- add heat-pipe and copper plate on module shielding cover,
- for extreme condition, use fan(s) and heat sink on module,
- place thermal pad/grease between module cover and heat spreader.

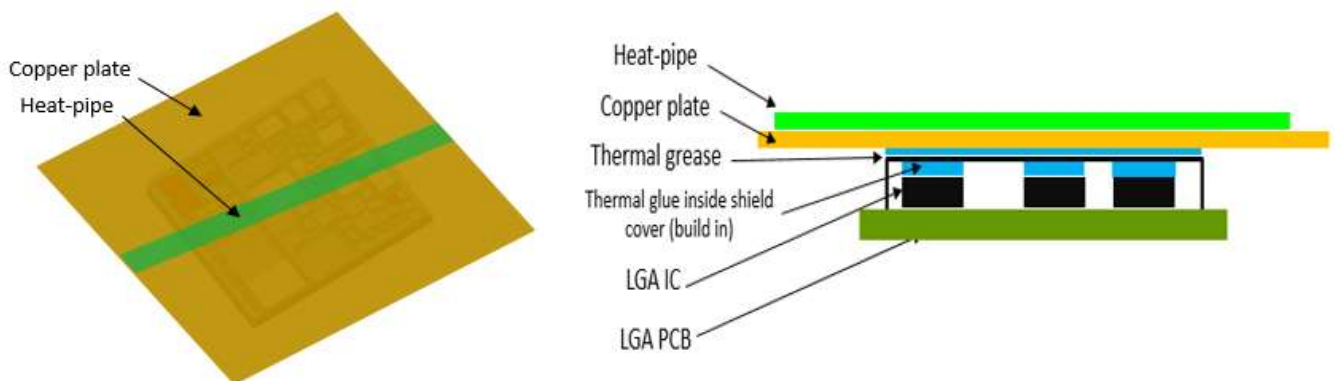


Figure 5-7 Diagrammatic Sketch of Thermal Solutions



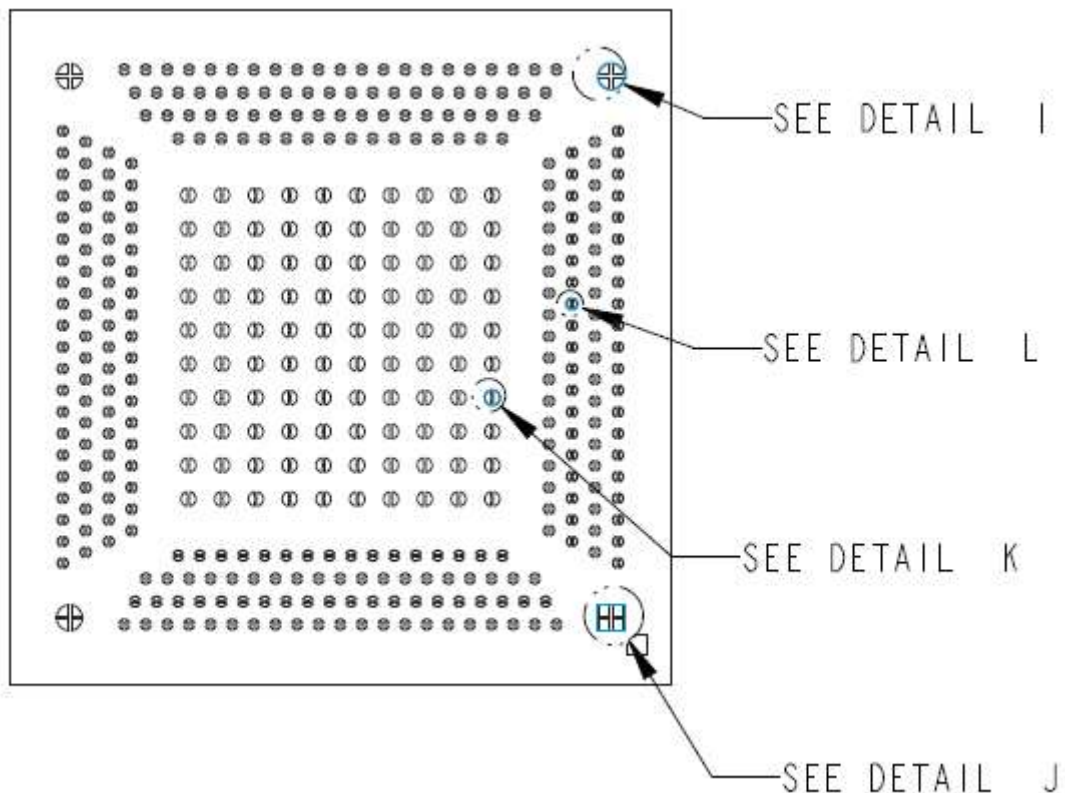
5.7 Assembly Processes

5.7.1 General Description of Assembly Processes

- Tray modules are required at SMT lines, because LGA modules are placed on ESD pallets.
- Reflow ovens with at least seven temperature zones are recommended.
- Use reflow ovens or rework stations for soldering, because LGA modules have large solder pads and cannot be soldered manually.

5.7.2 Stencil Design

It is recommended that the stencil for the LGA module be **0.15-0.18** mm in thickness. For the stencil design, See the following figure:



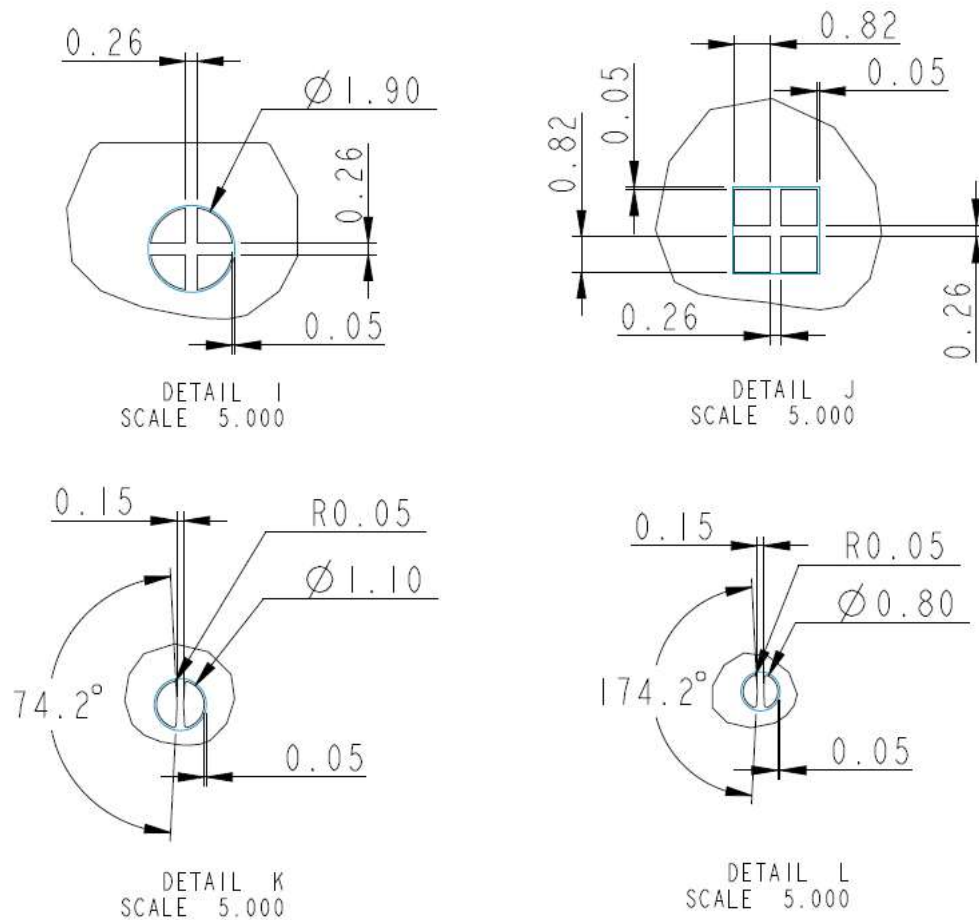


Figure 5-8 Recommended stencil design of LGA module (Unit: mm) (Intuitive view from BOT side)



NOTE:

The stencil design has been qualified for Compal motherboard assembly, customers can adjust the parameters by their motherboard design and process situation to assure LGA module soldering quality and no defect.

It is recommended to refer to the footprint diagram of Module (Figure 5-5) first before stencil design. The dimensions and directionality are marked in the footprint.



5.7.3 Reflow Profile

For the soldering temperature of the LGA module, see the following figure.

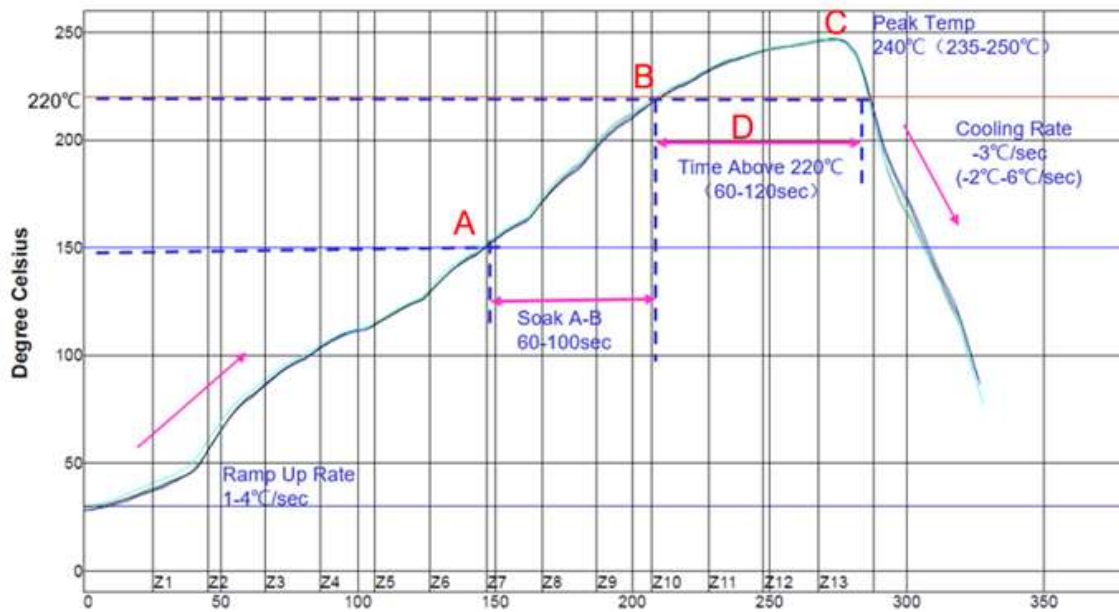


Figure 5-9 Reflow profile

Table 5-2 Reflow parameters

Category		Lower Limit	Recommend	Upper Limit
20°C - A	Ramp Up Rate	1°C/sec	2°C/sec	4°C/sec
A	Soak Zone start temp	140°C	150°C	160°C
B	Soak Zone End temp	210°C	220°C	230°C
A-B	A-B Section Time	60sec	80sec	100sec
C	Peak Temp	230°C	240°C	250°C
D	Time above 220°C	60sec	80sec	120sec
	Cooling Rate	-2°C/ sec	-3°C/ sec	-6°C/ sec

5.9 Ordering information

All relevant LGA HW spec、figures and design guidelines in this document are common specification for All 5G LGA mode

5.9.1 Specification-compliant devices

This device can be ordered using the identification code shown in Table5-4.

Table 5-4 Device ordering information

Character	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	11th	12th
Module		Module Solution	Module Type	SKU Region	Version-1	Version-2			Sample Type	SW Application	SW Version	CPU Version
Code	R	X	L (LGA Module)	N = US J=Japan E=EU	3=3GPP release 17	n=with roaming band			0— SIM2=1.2V,8G 1— SIM2=1.8V,8G QFW(1.8V) 2— SIM2=1.8V,8G WCN(1.2V)			



NOTE:

Example: RXL-N3, RXL-E3, RXL-E3n, RXL-N3n

Sample Type note:

1. "0" define support 8GB eMMC with 2GB LPDDR4X.---SIM2 voltage=1.2V*¹ WiFi solution:WKK(QFW) I/O 1.8V
2. "1" define support 8GB eMMC with 2GB LPDDR4X.---SIM2 voltage=1.8V . WiFi solution:WKK(QFW) I/O 1.8V
3. "2" define support 8GB eMMC with 2GB LPDDR4X.---SIM2 voltage=1.8V . WiFi solution:WCN I/O 1.2V



6 Reliability test

This chapter is definition reliability test item. Table 6-1 lists the test conditions of the reliability of the LGA module.

Table 6-1 lists the test conditions of the reliability of the LGA module.

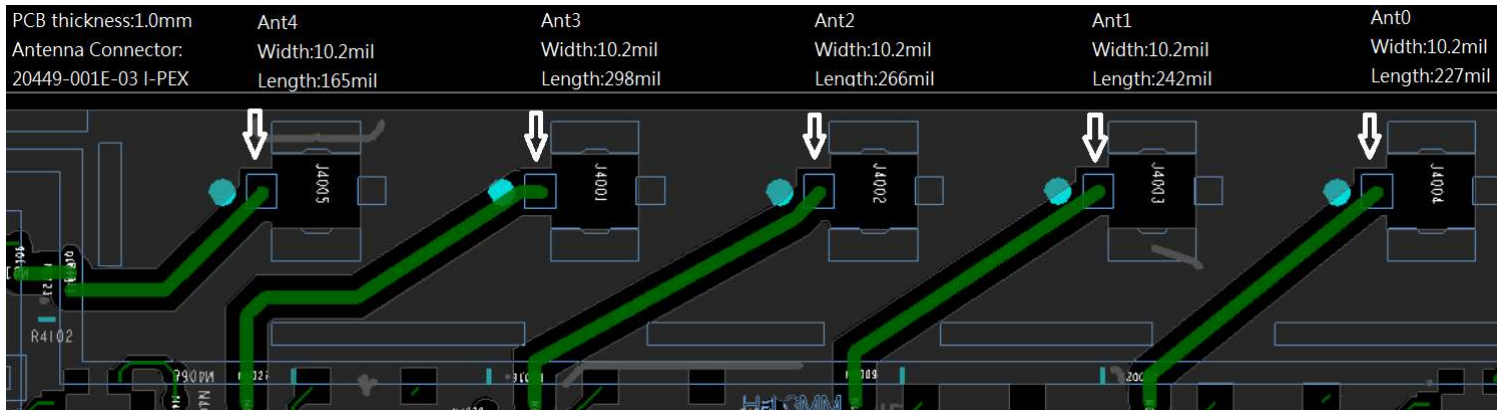
Item		Test Condition	Standard	Sample Size	Result
ESD	HBM (Human Body Model)	1 kV (Class 1 B) Operation mode: no power	JESD22-A114-D	3 pcs/group	Visual inspection : ok Function test: ok RF specification : ok
	ESD with EVB (or embedded in the host)	1. Contact Voltage: ± 2 kV, ± 4 kV 2. Air Voltage : ± 2 kV, ± 4 kV, ± 8 kV 3. Operation mode: working with service connected	IEC61000-4-2	3 pcs/group	Visual inspection : ok Function test: ok RF specification : ok
Stress	Shock Test (Reference test)	Method 2002.5, Condition B 30 Half-sine/1,000G/0.5ms	MIL-STD-883	3 pcs/group	Visual inspection : ok Function test: ok RF specification : ok
	High temperature operation	1. Temperature: 55°C 2. Humidity: 50%RH 3. During time: 48hrs	IEC60068	3 pcs/group	Visual inspection : ok Function test: ok RF specification : ok
	Low temperature operation	1. Temperature: -20°C 2. During time: 48hrs	IEC60068	3 pcs/group	Visual inspection : ok Function test: ok RF specification : ok
	Thermal shock	1. Temperature: 75°C/ -40°C 2. During time: 30mins 3. Test cycles: 168	IEC60068	3 pcs/group	Visual inspection : ok Function test: ok RF specification : ok



	High temperature storage	1. Temperature: 85°C 2. During time: 168hrs	IEC60068	3 pcs/group	Visual inspection : ok Function test: ok RF specification : ok
	High temperature storage	1. Temperature: -40°C 2. During time: 168hrs	IEC60068	3 pcs/group	Visual inspection : ok Function test: ok RF specification : ok
Life	High temperature High humidity	1. Temperature: 55°C 2. Humidity: 90%RH 3. During time: 48hrs	IEC60068	3 pcs/group	Visual inspection : ok Function test: ok RF specification : ok
Package test	Temperature storage	1. Temperature: 70°C During time: 12 hrs, 2. Temperature: -20°C During time: 12 hrs	ISTA 2A	3 pcs/group	Visual inspection : ok Function test: ok RF specification : ok
	High temperature High humidity	1. Temperature: 65°C 2. Humidity: 90%RH 3. During time: 24 hrs			
	Drop test	I. 0 - 10kg: 97cm II. 10 - 19kg: 81cm III. 19 - 28kg: 66cm			
	Vibration test	I. Frequency 5~50 Hz II. Acceleration 1.44 m/s ²			



7 Antenna Trace Design



Trace design

The trace from module transmitter to antenna connector must be maintained identical as the above specification with i-pex connector. Only trace designs approved by the module original grantee or through permissive change can be used by an host manufacturer. Any changes are deemed as antenna type change and should be reviewed to ensure compliance with the FCC regulation rules.

Verification must be conducted and the results shall not exceed below ranges to ensure identical antenna design is applied to subsequent integration and end product production.

Test procedures of Verification

1. Set Transmission in the supported modulation mode, band and Channel.
2. Verify RF tuned-up power through conducted measurement with appropriate cable loss. The KDB guidance 971168 D01 can be followed to obtain the measurement results.
3. Verify the RF output power results obtained if it's accordance with the datasheet and test reports.



FCC Notice

Model: RXL_N3n

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).

Antenna Installation

- (1) The antenna must be installed such that 20 cm is maintained between the antenna and users.
- (2) The transmitter module may not be co-located with any other transmitter or antenna.
- (3) To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, the maximum antenna gain including cable loss in a mobile exposure condition must not exceed:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.



Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Module Warning statements

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) This device may not cause harmful interference
- (2) This device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

RF Exposure

This device has been tested and meets applicable limits for Radio Frequency (RF) exposure. The antenna(s) used for this transmitter should be installed and operated with minimum distance 20 cm between the radiator & your body.



Label requirements

Any device incorporating this module must include an external, visible, permanent marking or label which states:

“Contains FCC ID: GKRRXLN3N”

Industry Canada Statement

This device contains licence-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada’s licence-exempt RSS(s). Operation is subject to the following two conditions:

- (1) This device may not cause interference.
- (2) This device must accept any interference, including interference that may cause undesired operation of the device.

L’émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d’Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L’exploitation est autorisée aux deux conditions suivantes :

- (1) L’appareil ne doit pas produire de brouillage;
- (2) L’appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d’en compromettre le fonctionnement.

CAN ICES-3(B)/ NMB-3(B)

Radiation Exposure Statement

This equipment complies with FCC/IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Cet équipement est conforme aux limites d'exposition aux rayonnements FCC/IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec une distance minimale de 20 cm entre le radiateur et votre corps.

To ensure RF exposure compliance under portable exposure conditions, the antenna(s) used with this module must be



installed in host platforms to provide a **20 cm** minimum separation distance from all persons, in all operating modes and orientations of the host platform. The antenna separation distance applies to both horizontal and vertical orientation of the antenna when installed in the host system. Any separation distances less than **20 cm** will require additional evaluation and ISED authorization.

OEM integrators must identify all possible combinations of simultaneous transmission configuration for all transmitters and antennas installed in the host platform. When there are multiple transmitting devices installed in a host platform, an RF exposure evaluation for the simultaneous transmission condition must be performed.

End Product Labeling

When the module is installed in the host device, the IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text:

"Contains IC: 2533B-RXLN3N"