```
*********************************************************
*       MODEL :  LYNX 3D                                *
*       DATE  :  sep.29.1998                            *
*       FILE NAME  : LY3DSPEC.MAT                       *
*********************************************************
```

**** SPECIFICATION OF TRANSMITTER ****

1. FREQUENCY : 75MHz BAND
2. NO.CHANNELS : 3CH
4. OUTPUT IMPEDANCE : TELESCOPE WHIP ANTENNA
5. SPURIOUS : -50dB
6. RF OUTPUT POWER (AT 9.6V) : 400 +/-50 mW
7. CURRENT DRAIN (AT 9.6V) : 170 +/-20 mA
8. MODULATION : FM MODE 2.8KHz
9. PULSE SPACING AT CONTROL NEUTRAL : 1500 usec
10. FRAME TIME : 21 +/-2 msec
11. RF BAND WIDTH : +/-10KHz AT -50dB
12. OPERATING VOLTAGE : 9.6V
13. OPERATING TEMPRETURE : -20'C ---- 50'C
14. CONTROL RANGE SPEC. SHEET

UNIT : u/sec

FUNCTION		STEERING	THROTTLE
STICK	UPPER	+110-- +127	+110-- +127
	NORMAL	+/-5	+/-5
	LOWER	-110-- -127	-50 -- -65
TRIM	HI - LOW	30 %	30 %

SANYO No.4411

2SC4910

NPN Epitaxial Planar Silicon Transistor

VHF-Band Power Amp Applications

Features

- On-chip emitter ballast resistors.

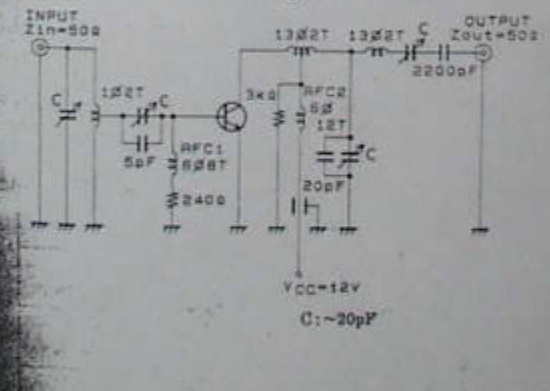
Absolute Maximum Ratings at Ta = 25°C

			unit
Collector to Base Voltage	V_{CBO}	38	V
Collector to Emitter Voltage	V_{CEO}	18	V
Emitter to Base Voltage	V_{EBO}	3	V
Collector Current	I_C	0.75	A
Collector Current (Pulse)	I_{CP}	1.2	A
Base Current	I_B	150	mA
Collector Dissipation	P_C	1.5	W
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	−55 to +150	°C

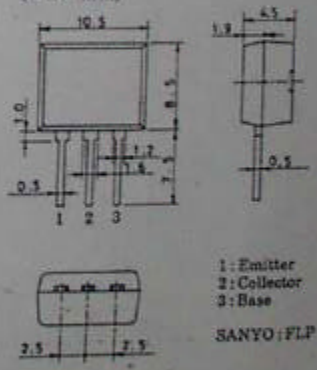
Electrical Characteristics at Ta = 25°C

			min	typ	max	unit
Collector Cutoff Current	I_{CBO}	V_{CB} = 30V, I_E = 0			50	μA
Emitter Cutoff Current	I_{EBO}	V_{EB} = 2V, I_C = 0			50	μA
DC Current Gain	h_{FE}	V_{CE} = 10V, I_C = 200mA	20		200	
C-B Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0	38			V
C-E Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, R_{BE} = ∞	18			V
E-B Breakdown Voltage	$V_{(BR)EBO}$	I_E = 100μA, I_C = 0	3			V
Output Capacitance	Cob	V_{CB} = 10V, f = 1MHz		6	10	pF
Output Power	P_O	V_{CC} = 12V, f = 175MHz, P_{IN} = 50mW	0.7	0.9		W
Collector Efficiency	ηc	See specified Test Circuit.	55	70		%

Collector Efficiency Test Circuit



Case Outline 2084A
(unit : mm)



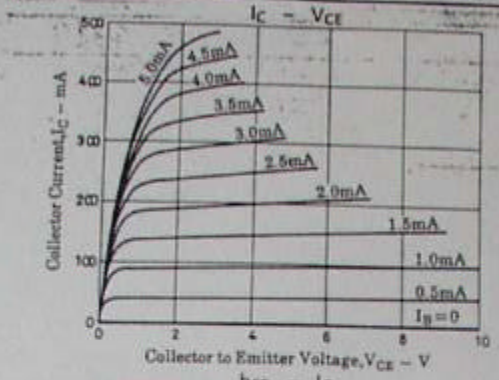
1 : Emitter
2 : Collector
3 : Base

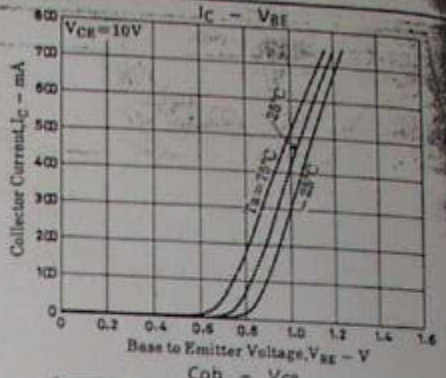
SANYO : FLP

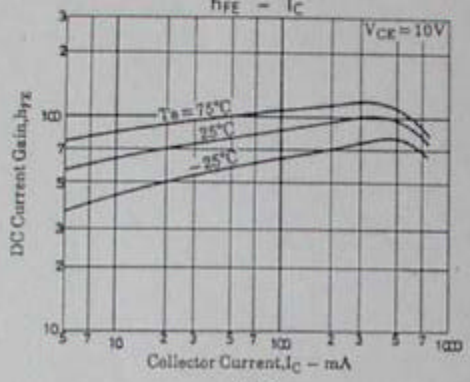
Specifications and information herein are subject to change without notice.

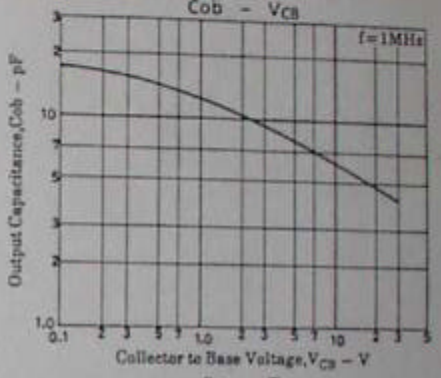
SANYO Electric Co.,Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

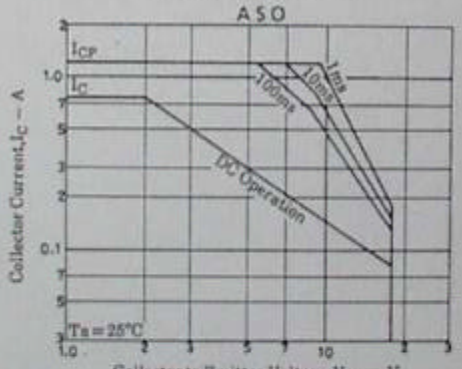
2SC4910

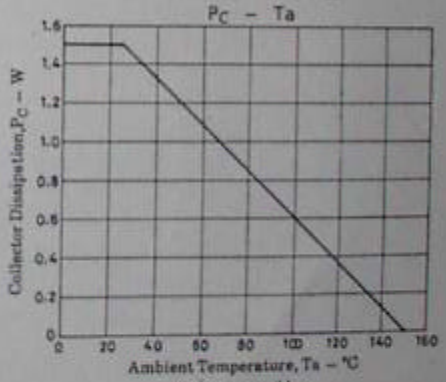

I_C – V_{CE}
Collector Current, I_C – mA
Collector to Emitter Voltage, V_{CE} – V
5.0mA
4.5mA
4.0mA
3.5mA
3.0mA
2.5mA
2.0mA
1.5mA
1.0mA
0.5mA
I_B = 0

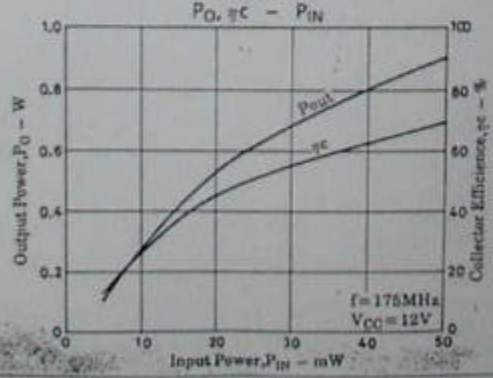

I_C – V_{BE}
V_{CE} = 10V
Collector Current, I_C – mA
Base to Emitter Voltage, V_{BE} – V
Ta = 75°C
25°C
–25°C

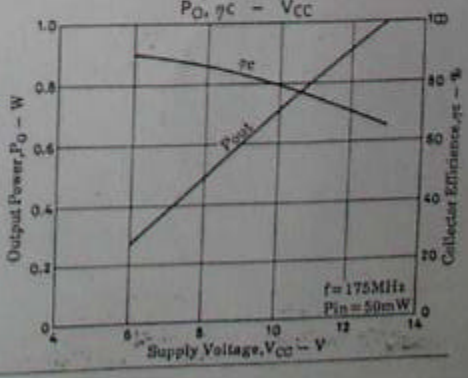

h_{FE} – I_C
V_{CE} = 10V
DC Current Gain, h_{FE}
Collector Current, I_C – mA
Ta = 75°C
25°C
–25°C


Cob – V_{CB}
f = 1MHz
Output Capacitance, Cob – pF
Collector to Base Voltage, V_{CB} – V


ASO
I_{CP}
I_C
1ms
10ms
100ms
DC Operation
Ta = 25°C
Collector Current, I_C – A
Collector to Emitter Voltage, V_{CE} – V


P_C – Ta
Collector Dissipation, P_C – W
Ambient Temperature, Ta – °C


P_O, η_C – P_{IN}
Pout
η_C
f = 175MHz
V_{CC} = 12V
Output Power, P_O – W
Collector Efficiency, η_C – %
Input Power, P_{IN} – mW


P_O, η_C – V_{CC}
η_C
Pout
f = 175MHz
Pin = 50mW
Output Power, P_O – W
Collector Efficiency, η_C – %
Supply Voltage, V_{CC} – V

KSA812 PNP EPITAXIAL SILICON TRANSISTOR

LOW FREQUENCY AMPLIFIER

- Complement to KSC1623
- Collector-Base Voltage $V_{CBO} = -60V$

SOT-23

1. Base 2. Emitter 3. Collector

ABSOLUTE MAXIMUM RATINGS ($T_a = 25°C$)

Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	−60	V
Collector-Emitter Voltage	V_{CEO}	−50	V
Emitter-Base Voltage	V_{EBO}	−5	V
Collector Current	I_C	−100	mA
Collector Dissipation	P_C	150	mW
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	−55 ~ 150	°C

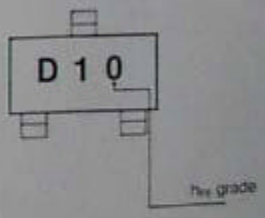
ELECTRICAL CHARACTERISTICS ($T_a = 25°C$)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Collector Cutoff Current	I_{CBO}	$V_{CB} = -60V$, $I_E = 0$			−0.1	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = -5V$, $I_C = 0$			−0.1	μA
DC Current Gain	h_{FE}	$V_{CE} = -6V$, $I_C = -1mA$	90	200	600	
Collector-Emitter Saturation Voltage	$V_{CE}(sat)$	$I_C = -100mA$, $I_B = -10mA$		−0.18	−0.3	V
Base-Emitter On Voltage	$V_{BE}(on)$	$I_C = -1mA$, $V_{CE} = -6V$	−0.55	−0.62	−0.65	V
Current Gain-Bandwidth Product	f_T	$I_C = -10mA$, $V_{CE} = -6V$		180		MHz
Output Capacitance	Cob	$V_{CB} = -10V$, $I_E = 0$ f = 1MHz		4.5		pF

h_{FE} CLASSIFICATION

Classification	O	Y	G	L
h_{FE}	90-180	135-270	200-400	300-600

Marking



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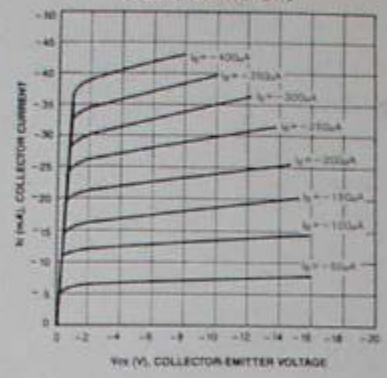
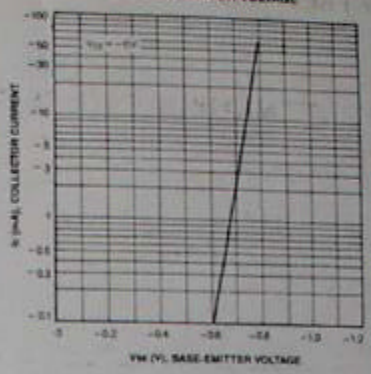
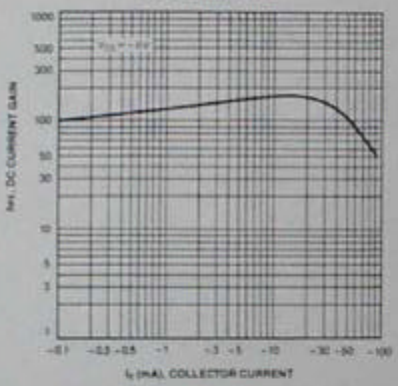
STATIC CHARACTERISTIC



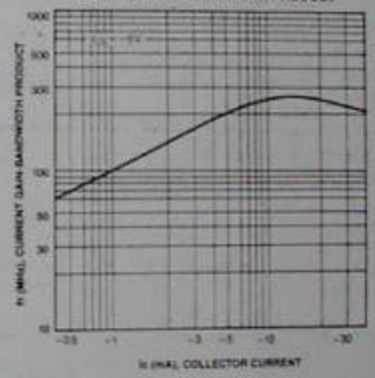
BASE-EMITTER ON VOLTAGE



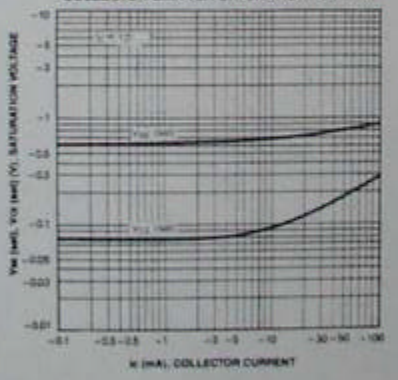
DC CURRENT GAIN



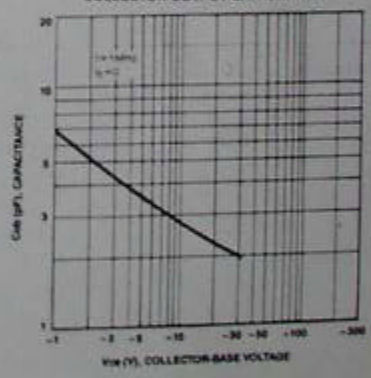
CURRENT GAIN-BANDWIDTH PRODUCT



BASE-EMITTER SATURATION VOLTAGE
COLLECTOR-EMITTER SATURATION VOLTAGE



COLLECTOR OUTPUT CAPACITANCE



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KSR1102 NPN EPITAXIAL SILICON TRANSISTOR

SWITCHING APPLICATION (Bias Resistor Built In)

- Switching Circuit, Inverter, Interface circuit Driver circuit
- Built in bias Resistor (R_1=10KΩ, R_2=10KΩ)
- Complement to KSR2102

SOT-23

1. Base 2. Emitter 3. Collector

ABSOLUTE MAXIMUM RATINGS (T_a=25°C)

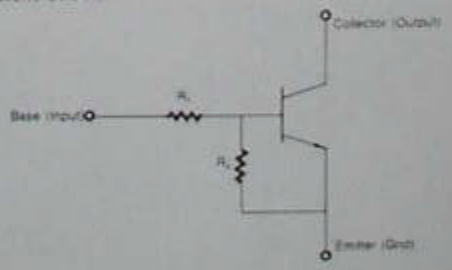
Characteristic	Symbol	Rating	Unit
Collector-Base Voltage	V_{CBO}	50	V
Collector-Emitter Voltage	V_{CEO}	50	V
Emitter-Base Voltage	V_{EBO}	10	V
Collector Current	I_C	100	mA
Collector Dissipation	P_C	200	mW
Junction Temperature	Tj	150	°C
Storage Temperature	Tstg	−55 ~ 150	°C

3

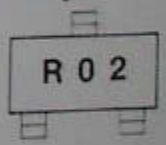
ELECTRICAL CHARACTERISTICS (T_a=25°C)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
Collector-Base Breakdown Voltage	BV_{CBO}	I_C=10μA, I_E=0	50			V
Collector-Emitter Breakdown Voltage	BV_{CEO}	I_C=100μA, I_B=0	50			V
Collector Cutoff Current	I_{CBO}	V_{CB}=40V, I_E=0			0.1	μA
DC Current Gain	h_{FE}	V_{CE}=5V, I_C=5mA	30			
Collector-Emitter Saturation Voltage	V_{CE}(sat)	I_C=10mA, I_B=0.5mA			0.3	V
Current Gain-Bandwidth Product	f_T	V_{CE}=5mA, I_C=10V		250		MHz
Output Capacitance	Cob	V_{CB}=10V, I_E=0 f=1.0MHz		3.7		pF
Input Off Voltage	Vi(off)	V_{CE}=5V, I_C=100μA	0.5			V
Input On Voltage	Vi(on)	V_{CE}=0.3V, I_C=10mA			3	V
Input Resistor	R_1		7	10	13	KΩ
Resistor Ratio	R_1/R_2		0.9	1	1.1	

Equivalent Circuit



Marking



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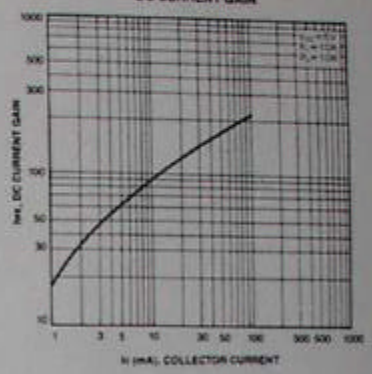
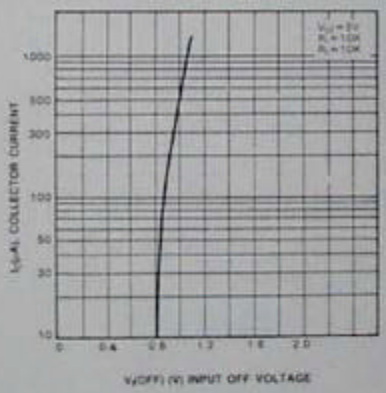
INPUT ON VOLTAGE

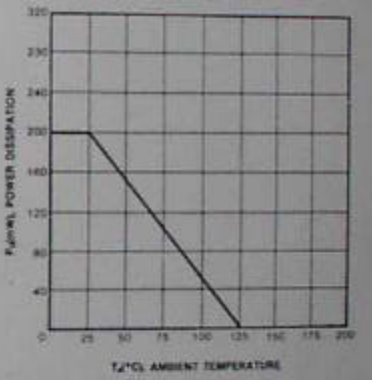
DC CURRENT GAIN



INPUT OFF VOLTAGE



POWER DERATING



SAMSUNG Electronics

GD4051B

8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

DESCRIPTION – The 4051B is an 8-Channel Analog Multiplexer/Demultiplexer with three Address Inputs (A_0–A_2), an active LOW Enable Input ($\overline{E}$), eight Independent Inputs/Outputs (Y_0–Y_7) and a Common Input/Output (Z).

The 4051B contains eight bidirectional analog switches, each with one side connected to an Independent Input/Output (Y_0–Y_7) and the other side connected to a Common Input/Output (Z). With the Enable Input ($\overline{E}$) LOW, one of the eight switches is selected (low impedance, ON state) by the three Address Inputs (A_0–A_2). With the Enable Input ($\overline{E}$) HIGH, all switches are in the high impedance OFF state, independent of the Address Inputs.

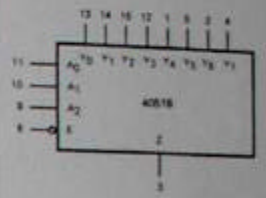
V_{DD} and V_{SS} are the two supply voltage connections for the digital control inputs (A_0–A_2, $\overline{E}$). Their voltage limits are the same as for all other digital CMOS. The analog Inputs/outputs (Y_0–Y_7, Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. V_{DD}–V_{EE} may not exceed 15 V. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).

- ANALOG OR DIGITAL MULTIPLEXER/DEMULTIPLEXER
- COMMON ENABLE INPUT (ACTIVE LOW)

PIN NAMES

Y_0–Y_7	Independent Inputs/Outputs
A_0–A_2	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
Z	Common Input/Output

LOGIC SYMBOL



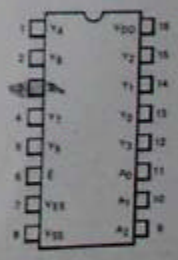
V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7

TRUTH TABLE

INPUTS				CHANNELS							
$\overline{E}$	A_2	A_1	A_0	Y_0–Z	Y_1–Z	Y_2–Z	Y_3–Z	Y_4–Z	Y_5–Z	Y_6–Z	Y_7–Z
L	L	L	L	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
L	L	L	H	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
L	L	H	L	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
L	L	H	H	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF
L	H	L	L	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF
L	H	L	H	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
L	H	H	L	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
L	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
H	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

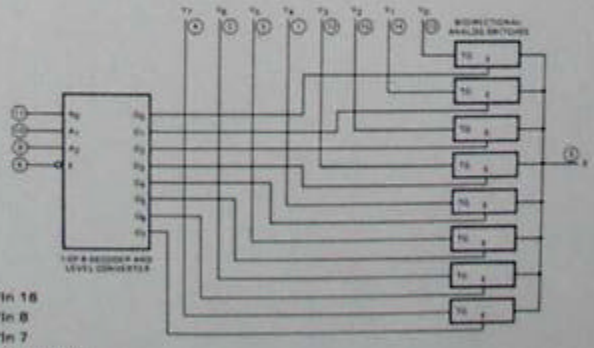
L = LOW Level
H = HIGH Level
X = Don't Care

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The SO Package has the same pinouts (Connection Diagram as the Dual In-line Package.

4051B FUNCTIONAL LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
V_{EE} = Pin 7
○ = Pin Numbers

DC CHARACTERISTICS: V_{DD} as shown, V_{EE} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
R_{ON}	ON Resistance	XC		95	900		55	380		35	210	Ω	MIN	V_{is} = V_{DD} to V_{EE} Note 2
				100	1000		65	500		40	280		25°C	
				125	1100		100	600		65	340		MAX	
		XM		90	850		50	340		30	190	Ω	MIN	
				100	1000		65	500		40	280		25°C	
				150	1150		110	660		70	370		MAX	
ΔR_{ON}	"Δ" ON Resistance Between Any Two Channels			25			10			5		Ω	25°C	Note 2
I_Z	OFF State Leakage Current, All Channels OFF	XC						800				nA	25°C	E = V_{DD} V_{SS} = V_{DD}/2 V_{is} = V_{DD} or V_{EE} V_{os} = V_{EE} or V_{DD}
		XM						80						
	Any Channel OFF	XC						100						E = V_{SS} = V_{DD}/2 V_{is} = V_{DD} or V_{EE} V_{os} = V_{EE} or V_{DD}
		XM						10						
I_{DD}	Quiescent Power Supply Dissipation	XC			20			40			80	μA	MIN, 25°C	V_{SS} = V_{EE} All inputs at V_{DD} or V_{EE}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

Notes on following page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{EE} = 0 V, T_A = 25°C (See Note 3)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay,		25			10			6		ns	C_L = 50 pF, R_L = 200 kΩ
t_{PHL}	Input to Output		10			6			4			$\overline{E}$ = V_{SS} = V_{EE},
t_{PLH}	Propagation Delay,		170			95			80		ns	A_n or V_{is} = V_{DD} or V_{EE}
t_{PHL}	Address to Output		210			125			95			Note 5
t_{PZL}	Output Enable Time		185			95			75		ns	C_L = 50 pF, R_L = 1 kΩ
t_{PZH}			205			105			85			E or A_n = V_{SS} = V_{EE}
t_{PLZ}	Output Disable Time		1250			1130			1080		ns	V_{is} = V_{DD} or V_{EE}
t_{PHZ}			1240			1120			1070			Note 5
	Distortion, Sine Wave Response		0.2			0.2			0.2		%	R_L = 10 kΩ V_{SS} = V_{DD}/2, $\overline{E}$ = V_{EE}, V_{is} = V_{DD}/2 (sine wave) p-p f_{is} = 1 kHz
	Crosstalk Between Any Two Channels					1					MHz	R_L = 1 kΩ $\overline{E}$ = V_{EE} V_{is} = V_{DD}/2 (sine wave) p-p at -40 dB V_{SS} = V_{DD}/2, 20 Log_{10} (V_{os}/V_{is}) = -40 dB
	OFF State Feedthrough					1					MHz	R_L = 1 kΩ, V_{SS} = V_{DD}/2 $\overline{E}$ = V_{DD} V_{is} = V_{DD}/2 (sine wave) p-p 20 Log_{10} (V_{os}/V_{is}) = -40 dB
f_{MAX}	ON State Frequency Response		13			40			70		MHz	R_L = 1 kΩ, $\overline{E}$ = V_{SS} V_{is} = V_{DD}/2 (sine wave) p-p V_{SS} = V_{DD}/2 20 Log_{10} (V_{os}/V_{os} @ 1 kHz) = -3 dB

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. $\overline{E}$ = V_{SS} R_L = 10 kΩ, any channel selected and V_{SS} = V_{EE} or V_{DD}/2.
3. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
4. V_{is}/V_{os} is the voltage signal at an Input/Output terminal (Y_n/Z_n).
5. V_{IN} = V_{DD} (Square Wave), Input transition times ≤ 20 ns, R_L = 10 kΩ.
6. In certain applications, the current through the external load resistor (R_L) may include both V_{DD} and signal line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 2, 4, 5, 12, 13, 14, or 15 the voltage drop across the bidirectional switch must not exceed 0.5 V at T_A ≤ 25°C, or 0.3 V at T_A > 25°C. No V_{DD} current will flow through R_L if the switch current flows into terminal 3.

OKI Semiconductor

MSM65512/65P512

OKI ORIGINAL HIGH PERFORMANCE CMOS 8 BIT SINGLE CHIP MICROCONTROLLER

GENERAL DESCRIPTION

MSM65512 is a high-performance 8-bit single-chip controller that employs Oki's original nX-8/50 CPU core. With a minimum instruction execution time of 400 ns (10MHz clock), the MSM65512 is capable of high-speed processing, and includes 8 Kbytes of program memory, 256 bytes of data memory, timers and serial ports on chip. Also available is the MSM65P512, which replaces the on-chip program memory with one-time PROM.

OPERATING RANGE

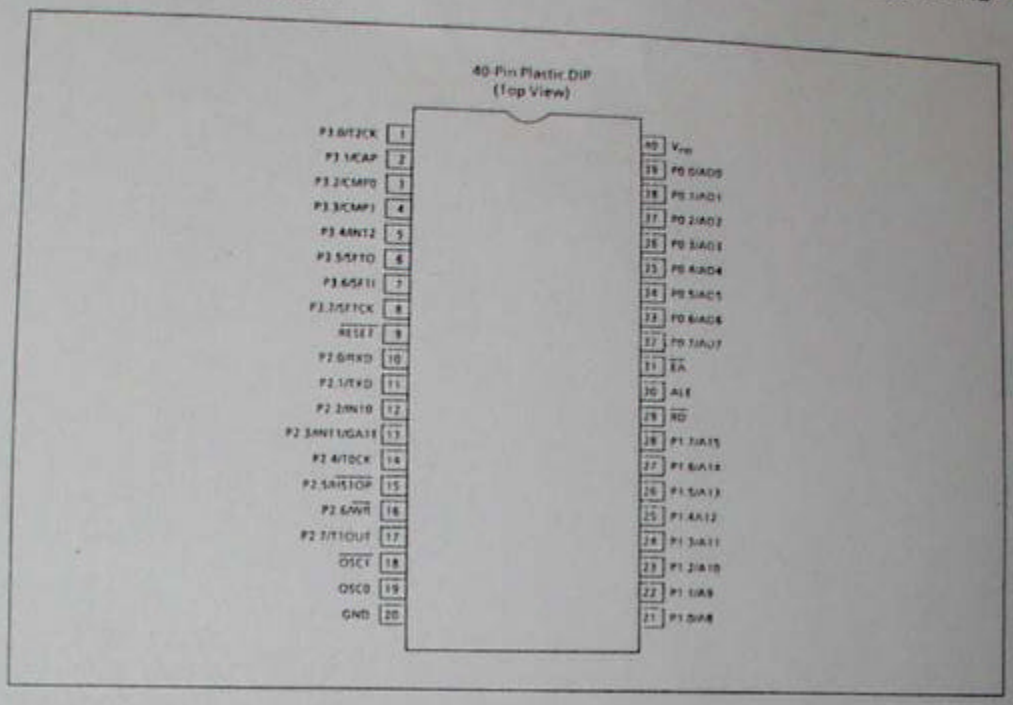
- Operating Frequency : DC ~ 10 MHz
- Operating Voltage : 4.5 ~ 5.5 V
- Operating Temperature : -40 ~ 85°C

FEATURES

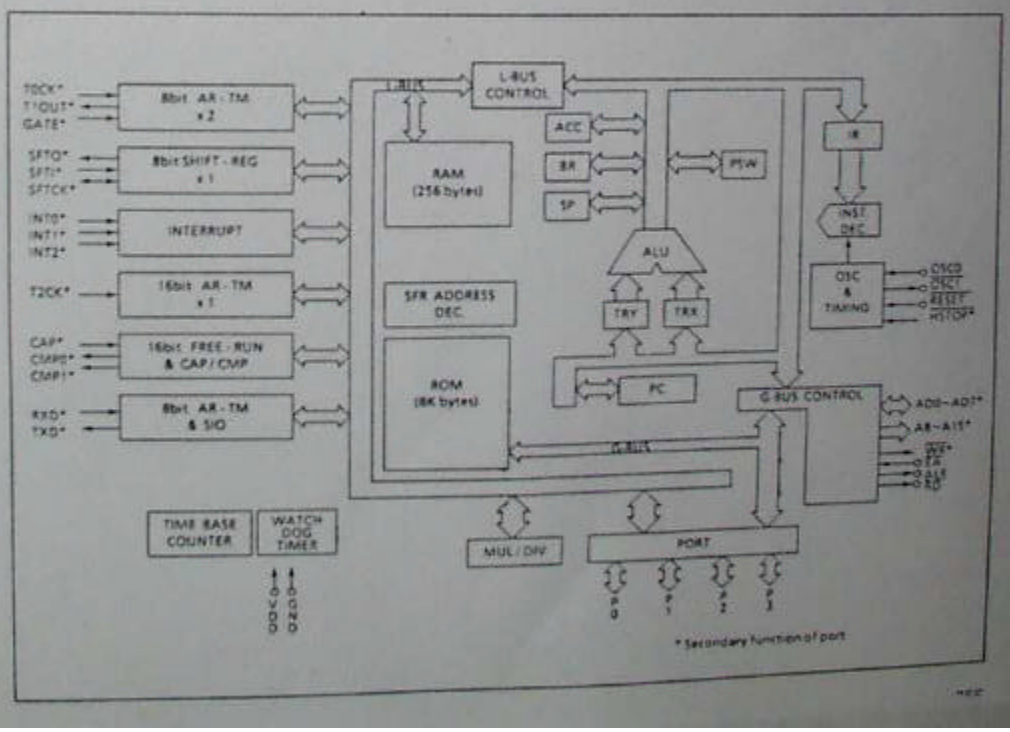
- Memory Space : 64 Kbytes
  - On-Chip Program Memory : 8 Kbytes
  - On-Chip Data Memory : 256 bytes
- Minimum Instruction Execution Cycle:
  400nS @ 10 MHz
- Powerful instruction set:
  - 83 basic instructions
  - 8/16-bit operation instructions
  - Bit manipulation instructions
  - Compound function instructions
- Abundant addressing modes
- Multiplication/division operation functions
  - 16 ← 8 x 8
  - 16 ← 16/8, 8 ← 16 mod 8
- I/O ports: 8-bit x 4
- Timers
  - 8-bit auto-reload timer x 2
  - 16-bit auto-reload timer x 1
  - Watchdog timer x 1
- Counters
  - Time base counter x 1
  - 16-bit free-running counter x 1
- Capture input: 1 channel
- Compare output: 2 channels
- Serial ports
  - Shift register x 1
  - Serial port with baud rate generator (UART/synchronous) x 1
- External interrupts: 3
- Interrupt factors: 15
- Package:
  - 40 pin plastic DIP (DIP40-P-600)
  - 44 pin plastic QFP (T.B.D)
  - 44 pin PLCC (QFJ44-P-S650)
  - 64 pin plastic QFP (T.B.D)

* Specifications are subject to change without notice.

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



3-Wire Serial CMOS E^2PROMs

1K (128 x 8 or 64 x 16)

2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

Features

- Low Voltage and Standard Voltage Operation
  - 5.0 V (V_{CC} = 4.5 V to 5.5 V)
  - 3.0 V (V_{CC} = 2.7 V to 5.5 V)
  - 2.5 V (V_{CC} = 2.5 V to 5.5 V)
  - 2.0 V (V_{CC} = 1.8 V to 5.5 V)
- User Selectable Internal Organization
  - 1K: 128 x 8 or 64 x 16
  - 2K: 256 x 8 or 128 x 16
  - 4K: 512 x 8 or 256 x 16
- Three-Wire Serial Interface
- Self-Timed Write Cycle (10 ms Max)
- High Reliability
  - Endurance: 100,000 Cycles
  - Data Retention: 100 Years
- Eight-Pin PDIP, JEDEC SOIC, and EIAJ SOIC Packages

Description

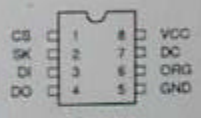
The AT93C46/56/57/66 provides 1024/2048/4096 bits of serial E^2PROM (Electrically Erasable Programmable Read Only Memory) organized as 64/128/256 words of 16 bits each, when the ORG Pin is connected to V_{CC} and 128/256/512 words of eight bits each when it is tied to ground. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT93C46/56/57/66 is available in space saving eight-pin PDIP and eight-pin JEDEC and EIAJ SOIC packages.

The AT93C46/56/57/66 is enabled through the Chip Select pin (CS), and accessed via a three-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. When CS is brought "high" following the initiation of a WRITE cycle, the DO pin outputs the READY/BUSY status of the part.

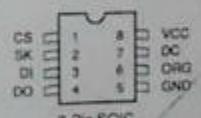
Atmel's E^2PROMs are designed and tested for applications requiring extended endurance. Devices in this family are guaranteed for 100,000 ERASE/WRITE cycles and 100-year data retention. The AT93C46/56/57/66 is available in 5.0 V ± 10%, 2.7 V to 5.5 V, 2.5 V to 5.5 V, and 1.8 V to 5.5 V versions.

Pin Configurations

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Internal Organization
DC	Don't Connect

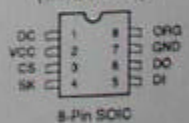


8-Pin PDIP



8-Pin SOIC

Rotated (R)
(1K JEDEC Only)



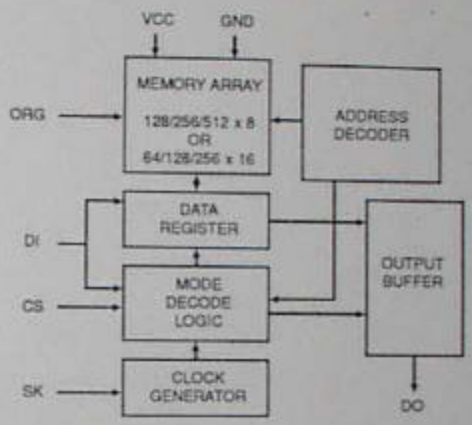
8-Pin SOIC

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.25 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram (1)



Note:
1. When the ORG pin is connected to V_{CC}, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x 16 organization.

Pin Capacitance (1)

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0 V (unless otherwise noted)

	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0 V
C_{IN}	Input Capacitance (CS, SK, DI)	5	pF	V_{IN} = 0 V

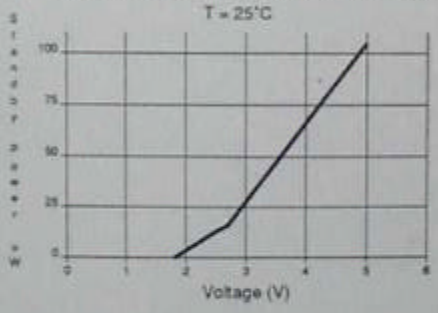
Note: 1. This parameter is characterized and is not 100% tested.

D.C. Characteristics

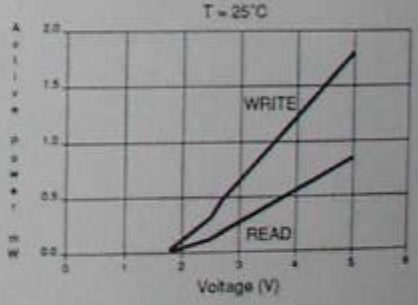
Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +1.8 V to +5.5 V, T_{AC} = 0°C to + 70°C, V_{CC} = +1.8 V to +5.5 V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1} [1]	Supply Voltage			1.8	5.0	5.5	V
V_{CC2}	Supply Voltage			2.5	5.0	5.5	V
V_{CC3}	Supply Voltage			2.7	5.0	5.5	V
V_{CC4}	Supply Voltage			4.5	5.0	5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0 V	READ at 1.0 MHz		0.2	0.5	mA
			WRITE at 1.0 MHz		0.4	1.0	mA
I_{SB1} [1]	Standby Current	V_{CC} = 1.8 V	CS = 0 V		0.0	0.1	µA
I_{SB2}	Standby Current	V_{CC} = 2.5 V	CS = 0 V		5.0	7.0	µA
I_{SB3}	Standby Current	V_{CC} = 2.7 V	CS = 0 V		6.0	10.0	µA
I_{SB4}	Standby Current	V_{CC} = 5.0 V	CS = 0 V		21.0	30.0	µA
I_{IL}	Input Leakage	V_{IN} = 0 V to V_{CC}			0.1	1.0	µA
I_{OL}	Output Leakage	V_{IN} = 0 V to V_{CC}			0.1	1.0	µA
V_{IL1} [2] V_{IH1} [2]	Input Low Voltage Input High Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V		-0.1 2.0		0.8 V_{CC}+1	V
V_{IL2} [2] V_{IH2} [2]	Input Low Voltage Input High Voltage	1.8 V ≤ V_{CC} ≤ 5.5 V		0.0 1.4		0.4 V_{CC}+1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V				0.4 2.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	1.8 V ≤ V_{CC} ≤ 5.5 V				0.2 V_{CC}-0.2	V

Typical Standby Power vs. Voltage[3]



Typical Active Power vs. Voltage[3]



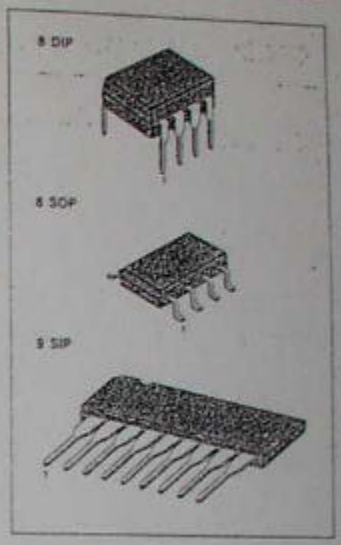
Notes: 1. This parameter is preliminary and Atmel may change the specifications upon further characterization.
2. V_{IL} min and V_{IH} max are reference only and are not tested.
3. These graphs are for reference only and are not guaranteed by test.

DUAL OPERATIONAL AMPLIFIERS

The LM258 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltage.

Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

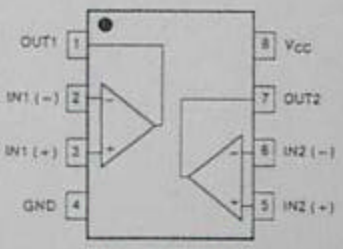
Application areas include transducer amplifier, DC gain blocks and all the conventional OP amp circuits which now can be easily implemented in single power supply systems.

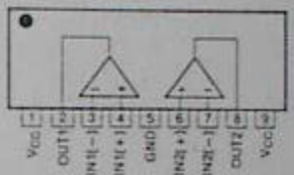


FEATURES

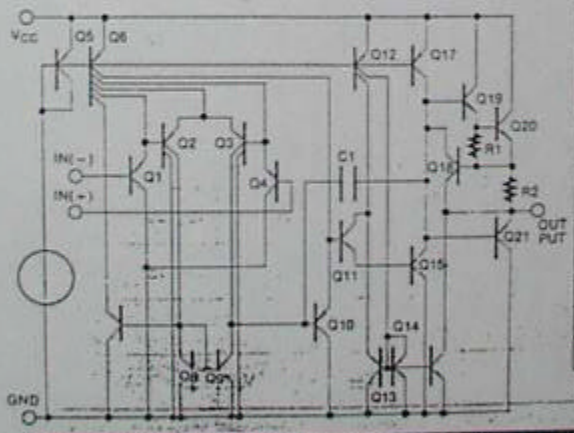
- Internally frequency compensated for unity gain
- Large DC voltage gain: 100dB
- Wide power supply range: LM258/A, LM358/A: 3V – 32V (or ±1.5V – ±16V)
  LM2904: 3V – 26V (or ±1.5V – ±13V)
- Input common-mode voltage range includes ground
- Large output voltage swing: 0V DC to V_{CC} – 1.5V DC
- Power drain suitable for battery operation.

BLOCK DIAGRAM





SCHEMATIC DIAGRAM (One section only)



ORDERING INFORMATION

Device	Package	Operation Temperature
LM358N LM358AN	8 DIP	0 ~ +70°C
LM358S LM358AS	9 SIP	
LM358D LM358AD	8 SOP	
LM258N LM258AN	8 DIP	–25 ~ +85°C
LM258S LM258AS	9 SIP	
LM258D LM258AD	8 SOP	
LM2904N	8 DIP	–40 ~ +85°C
LM2904S	9 SIP	
LM2904D	8 DIP	

** Under development

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	LM258/LM258A	LM358/LM358A	LM2904	Unit
Power Supply Voltage	V_S	± 16 or 32	± 16 or 32	± 13 or 26	V
Differential Input Voltage	V_{ID}	± 32	± 32	± 26	V
Input Voltage	V_I	− 0.3 to + 32	− 0.3 to + 32	− 0.3 to + 26	V
Output Short Circuit to GND $V_{CC} \leq 15V$ Ta = 25°C (One Amp)		Continuous	Continuous	Continuous	
Operating Temperature Range	T_{opr}	− 25 ~ + 85	0 ~ + 70	− 40 ~ + 85	°C
Storage Temperature Range	T_{stg}	− 65 ~ + 150	− 65 ~ + 150	− 65 ~ + 150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, Ta = 25°C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		LM258			LM358			LM2904			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} − 1.5V V_o = 1.4V, R_S = 0Ω			2.9	5.0		2.9	7.0		2.9	7.0	mV
Input Offset Current	I_{IO}				3	30		5	50		5	50	nA
Input Bias Current	I_{IB}				45	150		45	250		45	250	nA
Input Common-Mode Voltage Range	V_{ICM}	V_{CC} = 30V (LM2904, V_{CC} = 26V)		0		V_{CC} -1.5	0		V_{CC} -1.5	0		V_{CC} -1.5	V
Supply Current	I_{CC}	R_L = ∞, V_{CC} = 30V (LM2902, V_{CC} = 26V)			0.8	2.0		0.8	2.0		0.8	2.0	mA
		R_L = ∞, over full temperature range			0.5	1.2		0.5	1.2		0.5	1.2	mA
Large Signal Voltage Gain	A_V	V_{CC} = 15V, $R_L \geq 2K\Omega$ V_O = 1V to 11V		50	100		25	100		25	100		V/mV
Output Voltage Swing	V_{OH}	V_{CC} = 30V	R_L = 2KΩ	26			26			22			V
	V_{OH}	V_{CC} = 26V for 2904	R_L = 10KΩ	27	28		27	28		23	24		V
	V_{OL}	V_{CC} = 5V $R_L \geq 10K\Omega$			5	20		5	20		5	100	mV
Common-Mode Rejection Ratio	CMRR			70	85		65	80		50	80		dB
Power Supply Rejection Ratio	PSRR			65	100		65	100		50	100		dB
Channel Separation	CS	f = 1KHz to 20KHz			120			120			120		dB
Short Circuit to GND	I_{OS}				40	60		40	60		40	60	mA
Output Current	I_{source}	V_{in+} = 1V, V_{in-} = 0V V_{CC} = 15V, V_o = 2V		10	30		10	30		10	30		mA
	I_{sink}	V_{in+} = 0V, V_{in-} = 1V V_{CC} = 15V, V_o = 2V		10	15		10	15		10	15		mA
		V_{in+} = 0V, V_{in-} = 1V V_{CC} = 15V, V_o = 200mV		12	100		12	100					μA
Differential Input Voltage	V_{ID}					V_{CC}			V_{CC}			V_{CC}	V

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{EE} = GND, unless otherwise specified)
The following specification apply over the range of $-25°C \leq Ta \leq +85°C$ for the LM258; and the $0°C \leq Ta \leq +70°C$ for the LM358; and the $-40°C \leq Ta \leq +85°C$ for the LM2904

Characteristic	Symbol	Test Conditions		LM258			LM358			LM2904			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC}-1.5V V_O = 1.4V, R_S = 0Ω				7.0			9.0			10.0	mV
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	R_S = 0Ω			7.0			7.0			7.0		μV/°C
Input Offset Current	I_{IO}					100			150		45	200	nA
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$				10			10			10		pA/°C
Input Bias Current	I_{IB}				40	300		40	500		40	500	nA
Input Common-Mode Voltage Range	V_{ICR}	V_{CC} = 30V (LM2904, V_{CC} = 26V)		0		V_{CC} -2.0	0		V_{CC} -2.0	0		V_{CC} -2.0	V
Large Signal Voltage Gain	A_V	V_{CC} = 15V, $R_L \geq 2.0K\Omega$ V_O = 1V to 11V		25			15			15			V/mV
Output Voltage Swing	V_{OH}	V_{CC} = 30V V_{CC} = 26V for 2904	R_L = 2KΩ	26			26			26			V
			R_L = 10KΩ	27	28		27	28		27	28		V
	V_{OL}	V_{CC} = 5V, $R_L \geq 10K\Omega$			5	20		5	20		5	100	mV
Output Current	I_{source}	V_{in+} = 1V, V_{in-} = 0V V_{CC} = 15V, V_O = 2V		10	30		10	30		10	30		mA
	I_{sink}	V_{in+} = 0V, V_{in-} = 1V V_{CC} = 15V, V_O = 2V		5	8		5	9		5	9		mA
Differential Input Voltage	V_{ID}					V_{CC}			V_{CC}			V_{CC}	V