

ATTACHMENT 5**EUT TECHNICAL DESCRIPTION****HomeRF version 2.0 PC Card Technical Description**

Document # 610.00xx

PRODUCT:

The product is a FHSS WLAN adapter operating in the 2.4-2.4835 GHz band with a nominal TX output power of 100mW. It is an enclosed circuit board assembly with a 68-pin data / power connector and a coaxial antenna connector.

USER CONNECTIONS:

Data and power are provided through the 68-pin connector. A unique antenna connector is provided for attaching the antenna to the adapter.

INTERNAL CLOCK AND RF OSCILLATOR FREQUENCIES:

Processor ASIC	40 MHz, 32.768 kHz
RF synthesizer	reference 8MHz
	TX frequency 1201-1240MHz, 500kHz steps
	RX frequency 1146-1185MHz, 500kHz steps
transmit LO, transmit and receive range	2402-2480MHz in low rate TX
	2405-2475MHz in high rate TX
receive LO	2292-2370MHz
receive IF	110MHz, 1MHz or 5MHz BW

SIGNAL FLOW:

Data is transferred through the 68-pin connector to the processor. The processor ASIC also contains the baseband radio functions, A/D and D/A converters, transceiver control functions and memory interface.

In low rate transmit, the synthesizer tunes from 1201 to 1240MHz in 500kHz steps. In high rate, transmit, the synthesizer tunes from 1202.5 to 1237.5MHz in 2.5MHz steps. It is part of an integrated 2.4GHz transceiver IC, using an external VCO and buffer, loop, and modulation filters. The reference for the synthesizer is an 8 MHz processor ASIC output derived from the 40 MHz oscillator. The VCO is directly FM modulated with -20dB BW of less than 1MHz in low rate and less than 5MHz in high rate. The transceiver IC doubles the modulated external VCO and sends the signal to a bandpass filter, power amplifier, transmit / receive switch, lowpass filter, and antenna connector.

In receive, the synthesizer tunes from 1146 to 1185MHz in 500kHz steps. The receive signal path is from the antenna connector, through the lowpass filter and transmit / receive switch shared with the transmitter, an LNA, an image reject filter, and to the integrated transceiver IC. It is mixed down to IF by the receive LO which is generated inside the transceiver IC by doubling the VCO output. The IF output of the mixer goes off chip for bandpass filtering, back on for additional amplification, off again for more filtering and then back on chip for limiting. The limiter output signal is filtered at baseband before being converted to a bit stream in the processor ASIC.

There are two shielded areas. The VCO and buffer are under one shield, and the balance of the RF is under the other shield. RF filtering is distributed at each stage with final TX filtering between the transmit/receive switch and the antenna.