

EXHIBIT # 10

FCC Requirements CRF 47 Part 2.1033,c (10)

Frequency, Spurious and Power Control

JXBLMDSXP4-8T

EXHIBIT 10 Frequency Control for 28 to 31 GHZ LMDS Radio

The transmit frequency is controlled by a DDS modulator device (AD7008) made by Analog devices. The AD7008 direct digital synthesis (DDS) chip is a numerically controlled oscillator employing a 32-bit phase accumulator.

$$\text{DDS(frequency)} = \frac{\text{TX}_{\text{FREQUENCY}}(\text{Hz})}{4096} \times 214.7483648$$

To arrive at a program value for the DDS the ODU microprocessor takes the desired Transmit frequency in Hertz and divides by 4096 then multiplies by $2^{32} / 20,000,000$

AD7008 Theory of operation

The internal circuit of the AD7008 consists of four main sections. These are:

- Numerical Controlled Oscillator (NCO) + Phase Modulator
- SIN and Cosine LOOK UP tables
- In Phase and Quadrature modulators
- Digital to Analog Converter

The first section consists of two frequency select registers, a phase accumulator and a phase offset register. The main component of the NCO is a 32 bit phase accumulator which accumulates a phase step on every clock cycle. The value of the phase step determines how many clocks cycles are required for the phase accumulator to count 2π radians (i.e., one cycle of the output frequency). the output frequency, f_{OUT} , is given by:

$$f_{\text{OUT}} = \frac{\text{Phase_Step}}{2\pi} f_{\text{CLOCK}} = \frac{\Delta\text{Phase}}{2^{32}} f_{\text{CLOCK}}$$

$$0 \leq \Delta \text{Phase} \leq 2^{32} - 1$$

The input to the phase accumulator (i.e., the phase step) can be selected either from the **FREQ0** Register or **FREQ1** Register and this is controlled by the **FSELECT** pin. The XP-4 design uses the **FREQ0** Register only and the serial assembly mode. The transfer control pins are hardwired (see table).

This allows binary frequency shift keying to be easily implemented. The two FSK frequencies can be loaded into **FREQ0** and **FREQ1** and selected using the **FSELECT** pin. NCOs inherently generate continuous phase signals, thus avoiding any output discontinuity when switching between frequencies. More complex frequency modulation schemes, such as GMSK, can be implemented by updating the contents of these registers.

Following the NCO, a phase offset can be added to perform phase modulation using the 12 bit PHASE Register. The content of this register are added to the most significant bits of the NCO.

	TC1	TC0	Destination Register
XP4 hardwired register selection	0	0	FREQ0 Register
	0	1	FREQ1 Register
	1	0	PHASE Register
	1	1	IQMOD Register

Table 1 - AD7008 Destination Register selection

	TC3	TC2	Destination Register
XP4 hardwired register selection	0	0	Parallel Assembly Register
	0	1	Not used
	1	0	Parallel Assembly Register
	1	1	Serial Assembly Register

Table 2 - AD7008 Source Register selection

The output of the phase accumulator is converted to an amplitude signal by means of an Sine/Cosine ROM look up table. Although the NCO contains a 32 bit accumulator, the output of the NCO is truncated to 12 bits. Using the full resolution of the phase accumulator is both impractical and unnecessary as this would require a look up table of 2^{32} entries. It is necessary only to have sufficient phase resolution in the look up tables such that the dc error of the output waveform is dominated by the quantization error in the DAC. this requires the look up tables to have two or more bits of phase resolution than the 0 bit DAC.

Because no amplitude modulation is required, the IQ multipliers are bypassed. The sine output is directly sent to the 10 bits DAC. This device includes a high impedance source 10 bit DAC, capable of driving wide range of loads at different speeds. Full scale output current can be adjusted, for optimum power and external load requirements, through the use of a single external resistor.

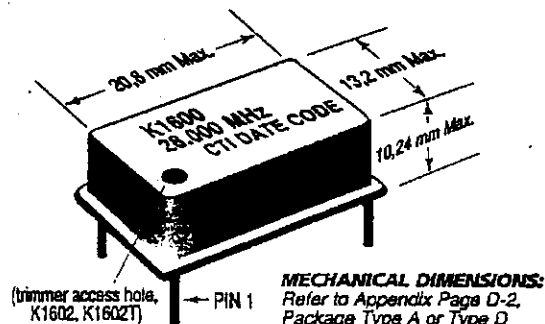
The DAC can be configured for single or differential ended operation. A single ended mode is used in the XP-4 radio. The negative output is tied directly to ground. In the XP-4 radio the frequency is programmed from the following equation.

$$f_{OUT} = \frac{\text{Phase_Step}}{2\pi} f_{CLOCK} = \frac{\text{PROGRAM_value}}{2^{32}} * 20\text{Mhz}$$

One AD7008 DDS is used for the transmitter and another for the receiver. They are controlled through the QSM in the MC68332 microprocessor.

CHAMPION K1600 SERIES

- ▲ **APPLICATIONS** Reference Clock;
Phase-Locked Loops (PLL's); Signal Tracking;
Clocking "Sync" to NTSC Video Standards
- ▲ 2.0 to 30.0 MHz Frequency Range
- ▲ ± 2.0 ppm Frequency Stability
- ▲ ± 1.0 ppm Available (K1601 Series)
- ▲ -40°C to $+85^{\circ}\text{C}$ Operating Temperature
- ▲ $+0.5\text{V}$ to $+4.5\text{V}$ Control Voltage
- ▲ Manual Frequency Adjustment Capability Option
- ▲ Hermetically Sealed Package Options
- ▲ TTL/CMOS and Sinewave Outputs



ELECTRICAL SPECIFICATIONS

MODEL	K1602	K1602TE	K1602T	K1603T
Frequency Range (MHz)	16 to 30	2 to 30	2 to 30	2 to 30
Package Type (Page D)	Type D	Type A (TC)VCXO	Type D	Type A
Frequency Stability (ppm)				
Overall	Inclusive of temperature, voltage, load.			
25° Calibration	±1.5			Inclusive
Aging (10 years)	< ±2ppm			Inclusive
0°C to 55°C	±1.0			
-40°C to +85°C	±2.0			±4.6
Frequency Control Function:				Not Available
Voltage Control	Included		Not Available	
Minimum Deviation (ppm)	±28	±28 (*TEW* = ±40ppm)		
Min. Deviation Sensitivity (ppm/V)	+14			
Nominal Control Voltage (V)	2.5			
Control Voltage Range (V)	0.5 to 4.5			
Linearity	10%			
Manual Adjustment	Included	Not Available	Included	
Minimum Adjustment (ppm)	±5		±5	
Output	1.0V p-p min.	Refer to Page B, Table 2		
	"Clipped" Sinewave			
	10 Kohms/10pF			
Symmetry (%) CMOS/TTL	-	45/55 <14 MHz; 40/60 ≥14 MHz		
Input Current (mA)	<2.0	<20		
Supply Voltage (V)	+5.0 ±5%			
Temperature Range (°C)				
Operable	-40°C to +85°C			
Storage	-40°C to +85°C			
Start Up Time (ms)	<5	<20	<10	
Test Circuit Diagram	Refer to Page B, Figure 3 (K1600T) or Figure 4 (K1600).			

ORDERING INFORMATION

Typical Phase Noise (dBc/Hz)

Offset from Carrier

10 Hz	-70
100 Hz	-95
1 KHz	-120
10 KHz	-140
100 KHz	-150

K160XX- Specify Frequency

- Blank = Sinewave output
- T = TTL/CMOS output
- TE = TTL/CMOS output, hermetic package
- TEW = TE version with ± 40 ppm min. deviation
- 1 = 0°C to 55°C Operating Temp., ± 1 ppm
- 2 = -40°C to 85°C Operating Temp., ± 2 ppm
- 3 = -40°C to 85°C Operating Temp., ± 4.8 ppm, inclusive, hermetic package

innova

3325 S. 116TH ST BLDG 2 SEATTLE, WA 98168
(206) 439-9121 (206) 439-2700 FAX

SIZE

A

DWG NO.

394-000001-000

REV

C

CAD FILE:

39400001.SCD

SHEET:

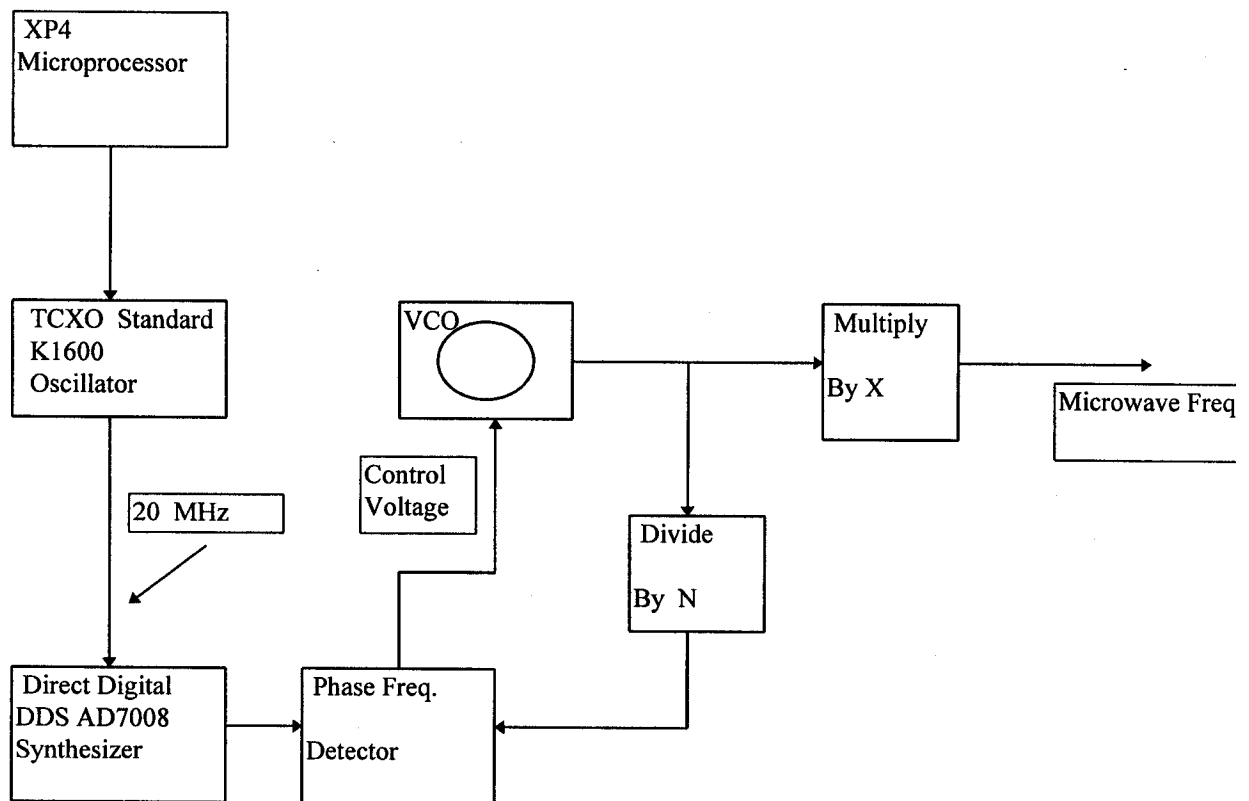
3

CFR 47 part 2.1055 / 101.107 (IO) Frequency setting and stabilization:

Frequency Stability is a function of the Reference clock as shown in the specification sheet by Champion part number K 1 600. The requirement for the LMDS application (CFR 47 part 101.107) is $\pm 0.001\%$. This radio will provide stability of better than $\pm 0.0005\%$. The following drawing shows the arrangement of the various frequency determining elements for the XP4 radio. Additionally, the process which the computer controls the setting for the required frequency is also illustrated in this section.

Transmitter Frequency Control Circuit

Transmitter Frequency Control Circuit



To: Pat MacDonald
 From: Peter Castagna
 Topic: Transmitter Frequency Shaping and Filtering on 4XT1/8XT1 4FSK Baseband Signal Processor
 Date: 6/3/99 9:57:35 AM

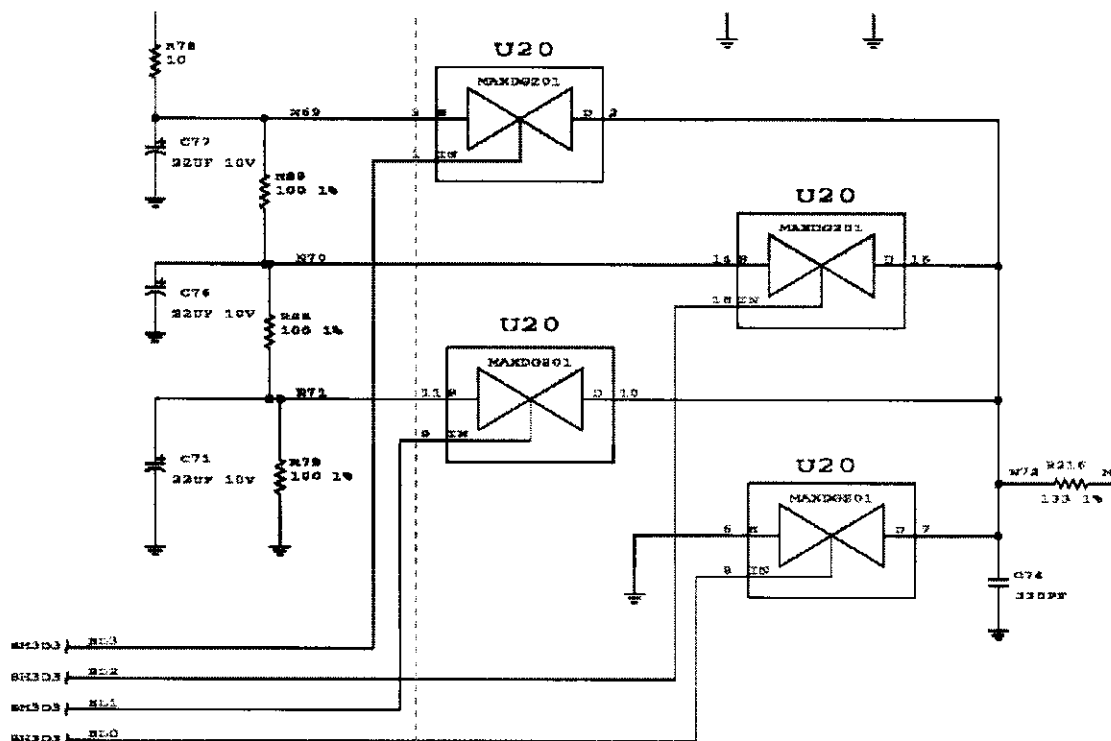


Fig. 1 Transmit 4-Level Data Source for 4XT1/8XT1 Signal Processor

Four levels are created in a resistor ladder and one level is selected by one of four analog switches. The source resistance is set to about 150 ohms by the combination of the switch resistance and the series 133 ohm resistor. The symbol rate is 7.25 Ms/s (Nyquist frequency 3.625MHz) for 8XT1 or 3.625 Ms/s for 4XT1 (Nyquist frequency 1.8125MHz). The source is switched into either a 4XT1 or an 8XT1 filter. The 4XT1 filter input is attenuated so that the filter output level for 4XT1 is half the filter output level for 8XT1.

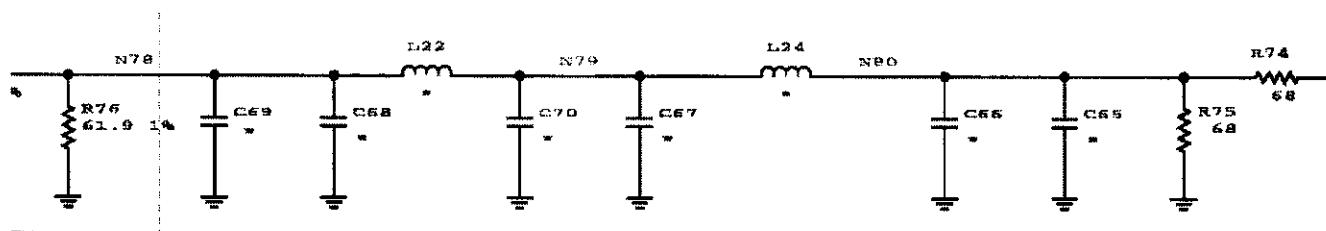


Fig. 2 Transmit Filter for 4XT1 Signal Output of Signal Processor

The 4XT1 filter is shown. Inductors are wound toroids (26 turns of 30AWG enameled wire wound in a single layer on MICROMETALS T25-2 ferrite core, 2.33uH 10% adjusted and set by manufacturer using Q-Dope adhesive, marked with yellow dot on red wire) with design Q exceeding 140 for frequencies between 3.5MHz and 10 MHz. Capacitors are ceramic with values 1290pf (820+470) and 1880pf (1200+680). This is approximately a 50.3 ohm 5th-order .5dB ripple Chebyshev at 4.5MHz 3dB frequency. This filter is compatible with the 4XT1 transmit shaping filter (and the 4XT1 receive baseband raised-cosine filter) used in the earlier 4XT1 product.

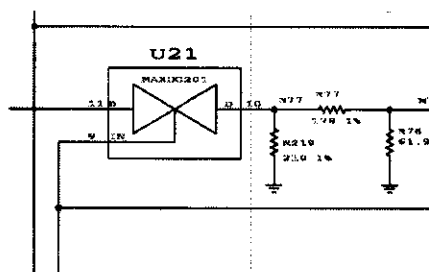


Fig. 3 6dB Pad on 4XT1 Signal Output of Signal Processor

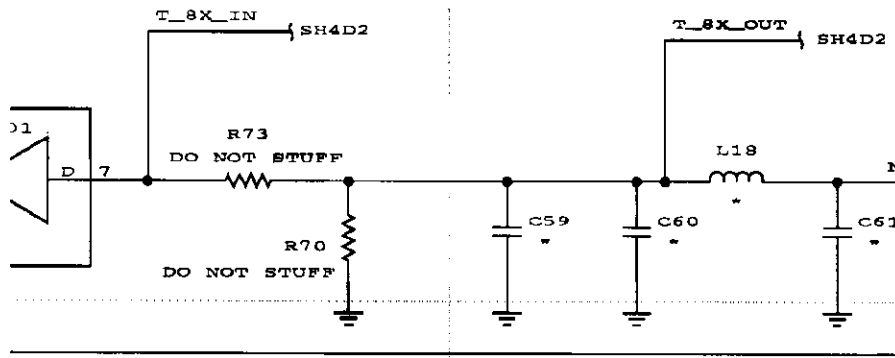


Fig. 4 Equalizer Bypass for 8XT1 Signal Output of Signal Processor, shown with Equalizer connected.

The 8XT1 baseband filter is preceded by an analog tapped delay line equalizer. The actual 8XT1 baseband transmit filter is a scaled version of the 4XT1 baseband transmit filter. Inductors are similar (18 turns on T25-2 MICROMETALS core, 1.16UH 10% adjusted and set by manufacturer using Q-Dope and marked with blue dot on red wire), and capacitors are similar (642 pf 2%, 970pf 2%) with a similar conclusion of a 50 ohm 9MHz 5th order .5dB ripple Chebyshev filter.

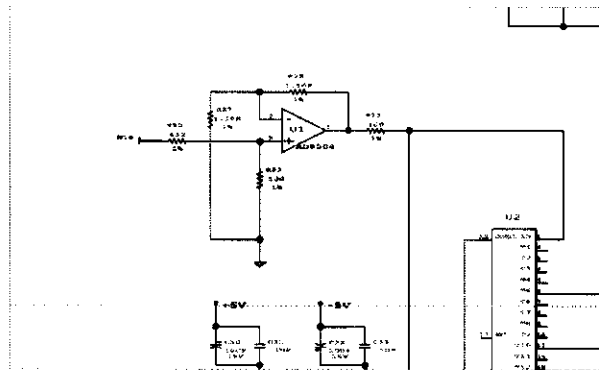


Fig. 5 Equalizer Input Buffer and Delay Line Connection

The analog tapped delay line equalizer input is buffered by a preamplifier. The preamplifier drives a 100-ohm delay line with 4 delay taps spaced at one symbol interval.

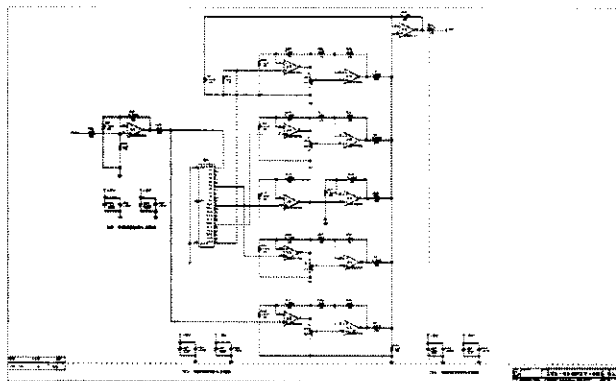


Fig. 6 Equalizer 5-Tap Analog Delay Line Filter with Alignment Potentiometers

This filter is set during module test (PCB setup before insertion into a working system) by adjusting the amplitudes of the four off-center taps using an oscilloscope to fixed values. This filter is adjusted by the system test technician using a specified order of adjustments and with a specific criterion (optimal eye scatter in the remote receiver) for adjustment. The adjustment is verified during the Factory Acceptance Test by examining the RF spectrum mask-fit.

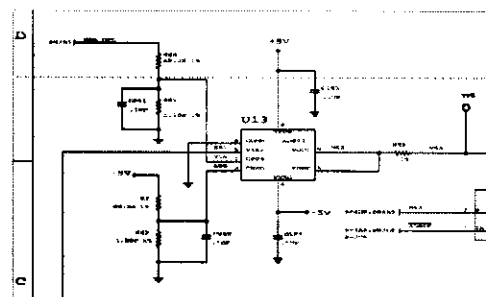


Fig. 7 Gain-Control Amplifier for Electronic Setting of Modulation Index

The purpose of this equalizer is to adjust the system to compensate for small manufacturing variances. A transmitter when adjusted using this equalizer will work well into any corresponding receiver.

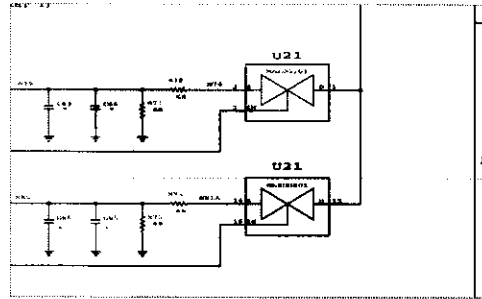


Fig. 8 Filter Output Switch

The two filter outputs are switched separately into an adjustable-gain amplifier with 100 ohms input impedance through matching pads. This amplifier is used during system adjustment test to set the FM modulation index. The adjustment range is ± 6 dB adjustable in .05dB increments.

The eye waveform is examined at TP5 during module test to verify the eye pattern closely matches a pictured eye pattern in terms of eye shape and closure and amplitude. The transmit RF spectrum is verified against a mask during Factory Acceptance Testing, as is the system BER performance versus RF level over temperature.

2 Measured Frequency Response, 4XT1 Transmitter

An HP3577B Network Analyzer (5Hz – 200MHz) is connected to the UUT, which has been mounted in a standard DMC Link Simulator Test Fixture.

R216 133 1% is removed. The switch and resistor are replaced by the B (output) port of the Network Analyzer and a 100 ohm 1% resistor (the switch is modeled as a 20 ohm resistor, and return loss is not measured).

The PWB TX-EYE output is measured at the Link Simulator TX EYE output, which is connected directly to the A (input) Port of the Network Analyzer.

The gain and group delay of the 4X connection are scanned and plotted. The gain and group delay of the 8X connection are scanned and plotted.

P CASTAGNA

5-25-1999

GROUP DELAY PLOT OF 8XT1

TRANSMIT (CH53MHz)

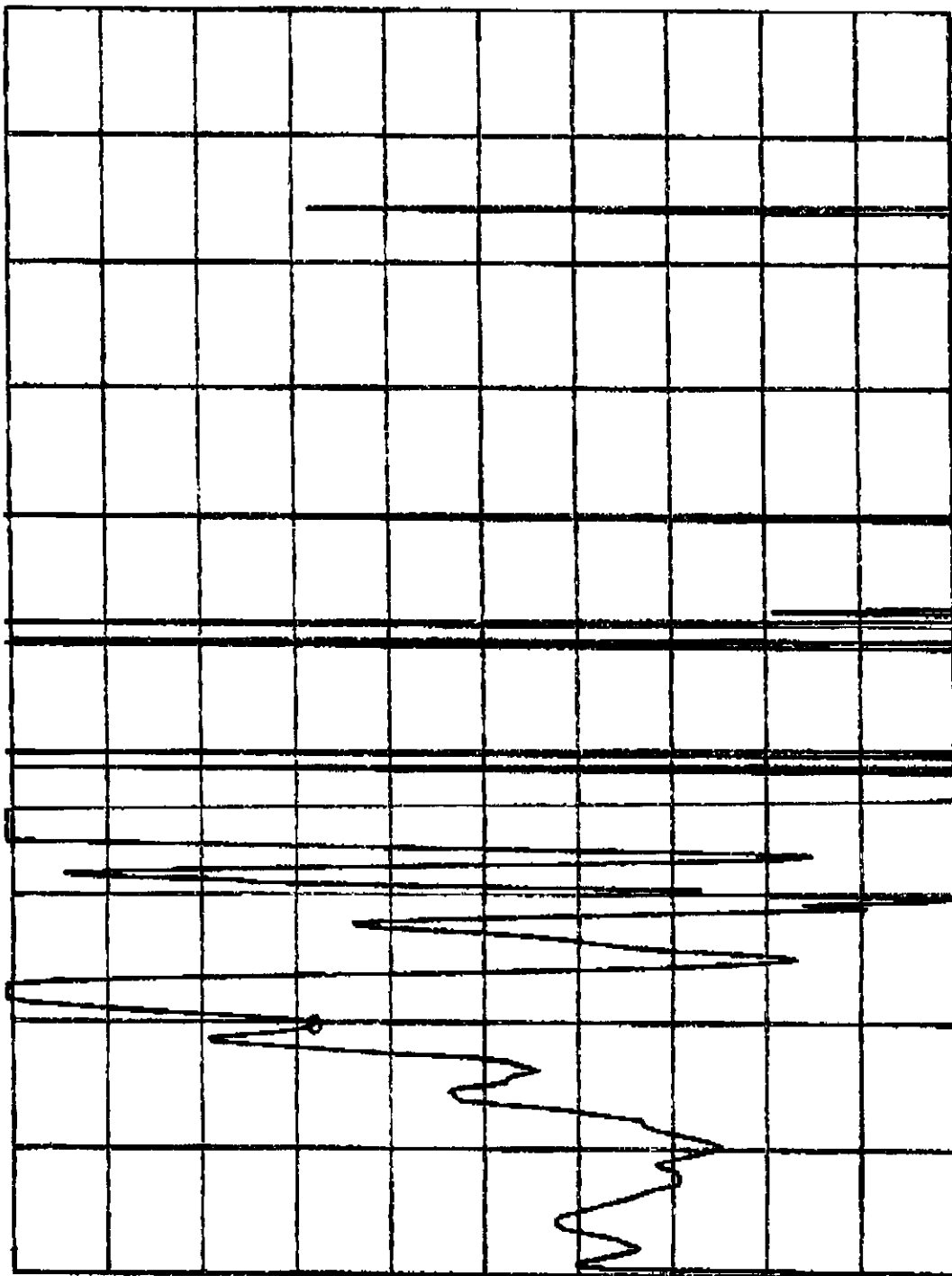
FILTER, 0-40 MHz on

8X/4XT1 Signal

Processor.

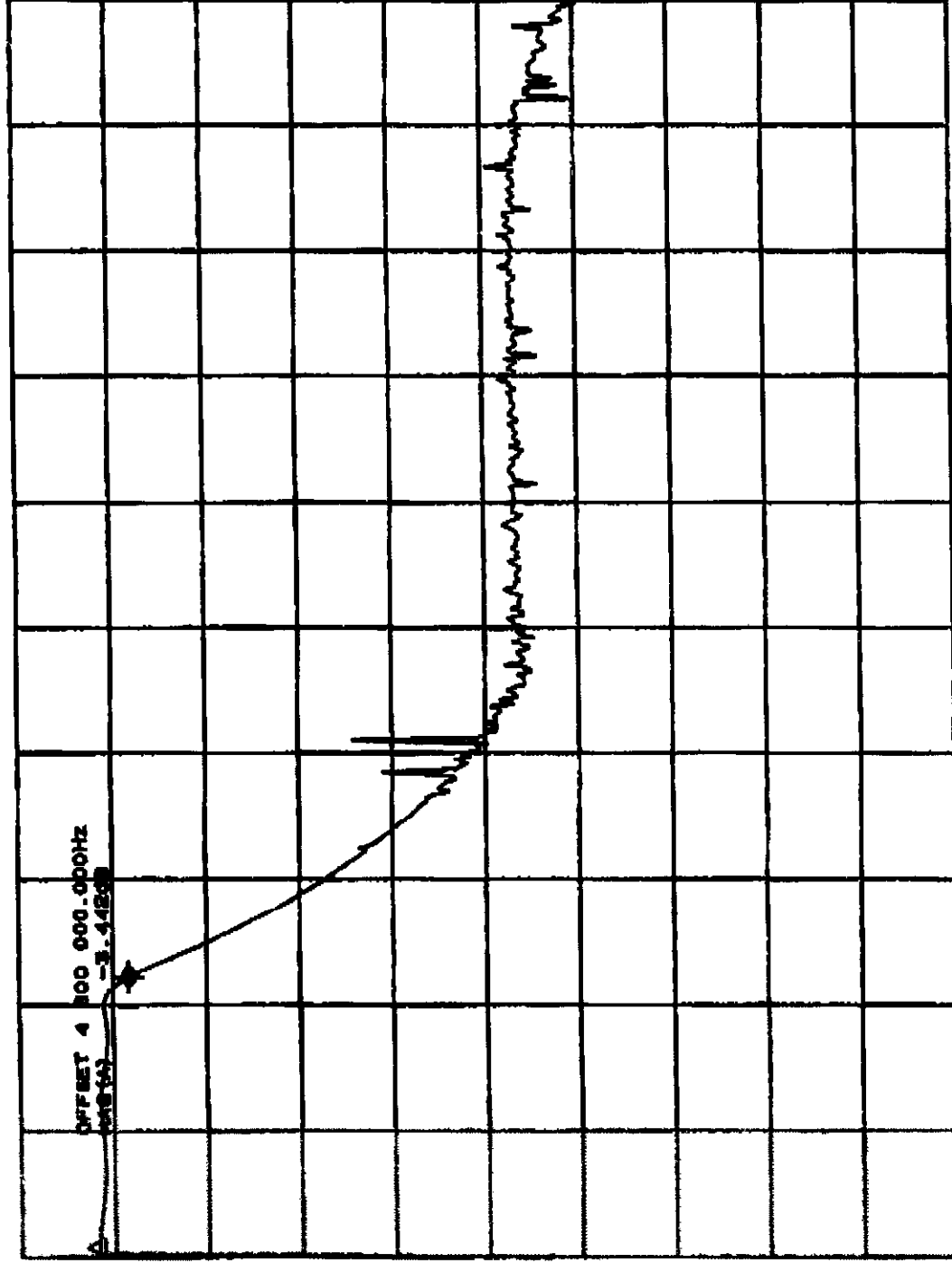
Note: see above

20 ns/div 0-40 MHz



R. CASTAGNA
 5-25-1998
 GAIN PLOT OF 4x71
 TRAUSCHIT (CHEBYKHEV)
 FILTER, 0-20 MHz.
 on 8x4x71 Signal
 Processor.

REF LEVEL /DIV OFFSET 4 300 000.000HZ
 -10.000dBm 10.000dB MAG (A) -3.436dB
 400.00nSEC 20.000nSEC OFFSET 4 350 000.000HZ
 DELAY (X1) 369.11nSEC



START 0.000HZ STOP 20 000 000.000HZ
 AMPTD -10.0dBm

P. CASTAGNA

5-25-1990

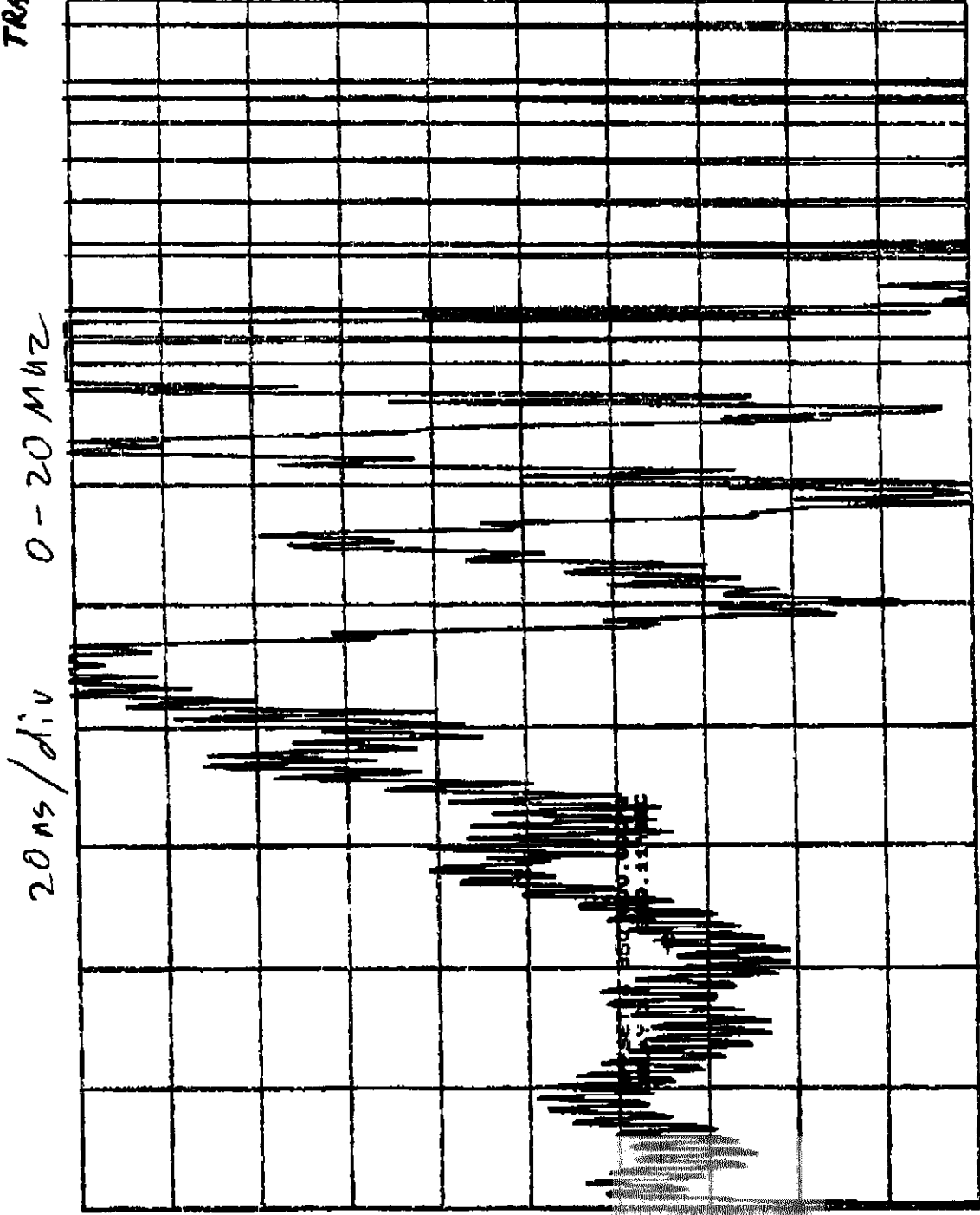
GROUP DELAY PLOT OF 4177

TRANSMIT (CARRIAGE)

FILTER, 0-20 MHz

on 4177 signal

PROCEED



P. CASTAGNA

5-25-1998

GAIN PLOT OF 8X11

TRANSMIT (CHEBYCHEV)

FILTER, 0-20MHZ.

ON 8X/4X11 Signal

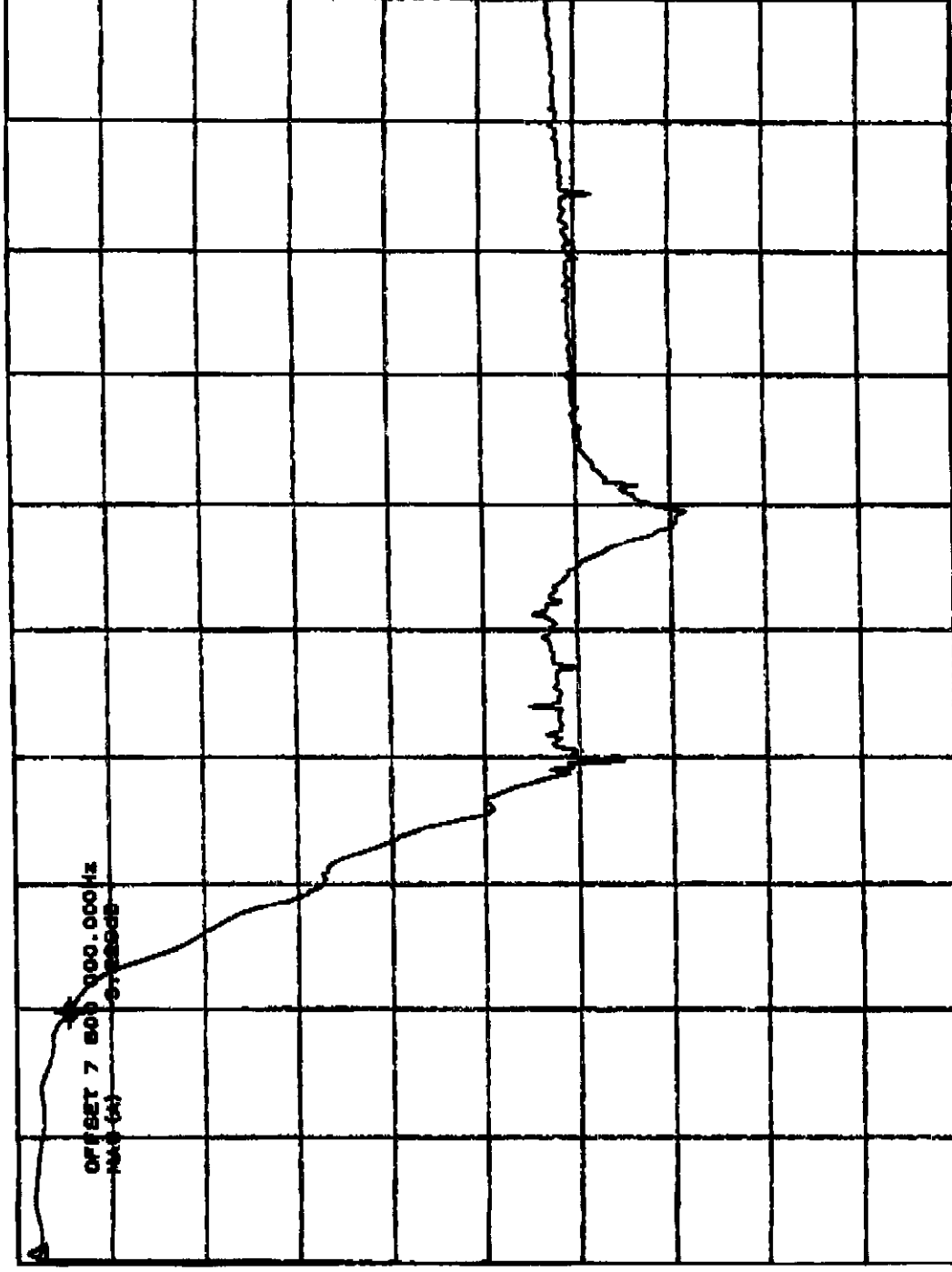
PROCESSOR

NOTE: TX EQ ADJUSTED

TO COMPENSATE

FOR ARX ~~ADJUSTED~~ IN
SYSTEM.

REF LEVEL /DIV OFFSET 7 600 000.000HZ
-10.000dBm 10.000dB MAG (A) -3.231dB
400.00nSEC 20.000nSEC OFFSET 7 800 000.000HZ
 DELAY (A) 434.51nSEC



START 0.000HZ STOP 40 000 000.000HZ
AMPTD -10.0dBm DELAY APER 200.0KHZ