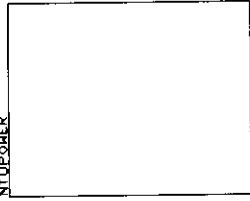


EXHIBIT D

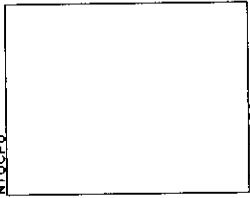
Circuit Diagram

NTUPOMER



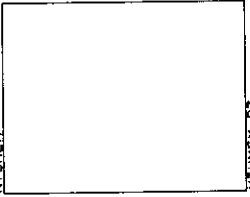
NTUPOMER.P1

NTUCPU



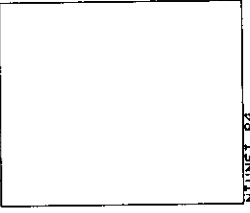
NTUCPU.P2

NTUMEM



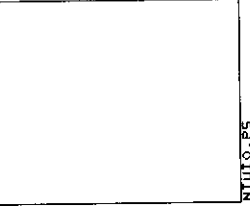
NTUMEM.P3

NTUNET



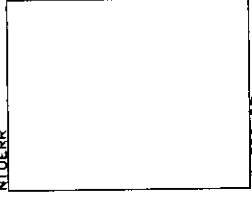
NTUNET.P4

NTUIO



NTUIO.P5

NTUERR



NTUERR.P7

NTURACK

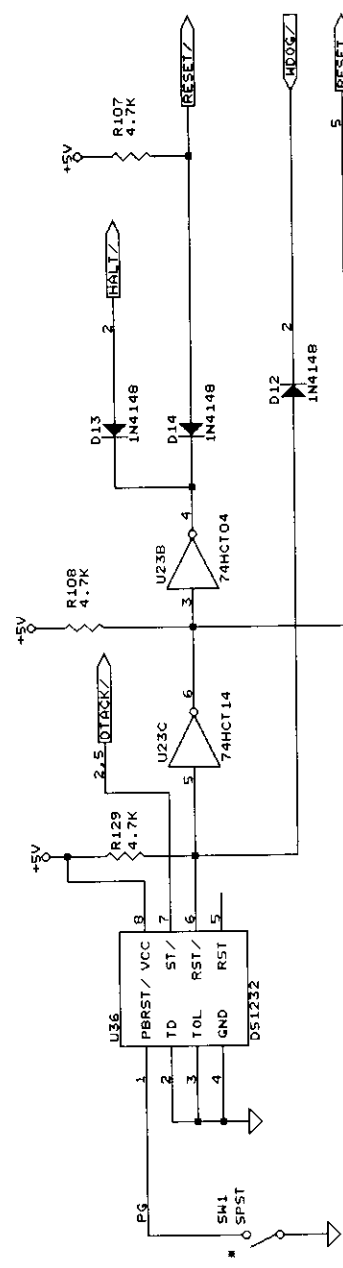
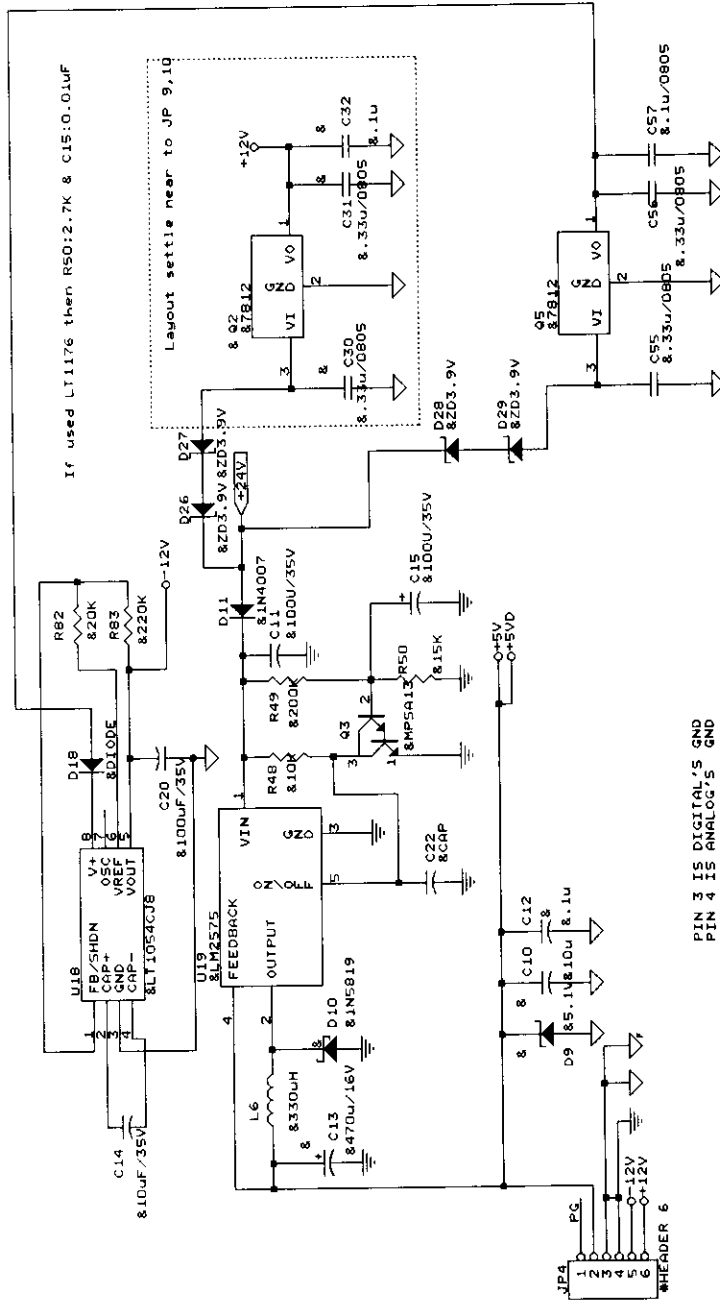


NTURACK.P8

NTUCLK



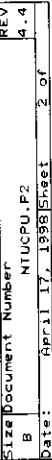
NTUCLK.P9

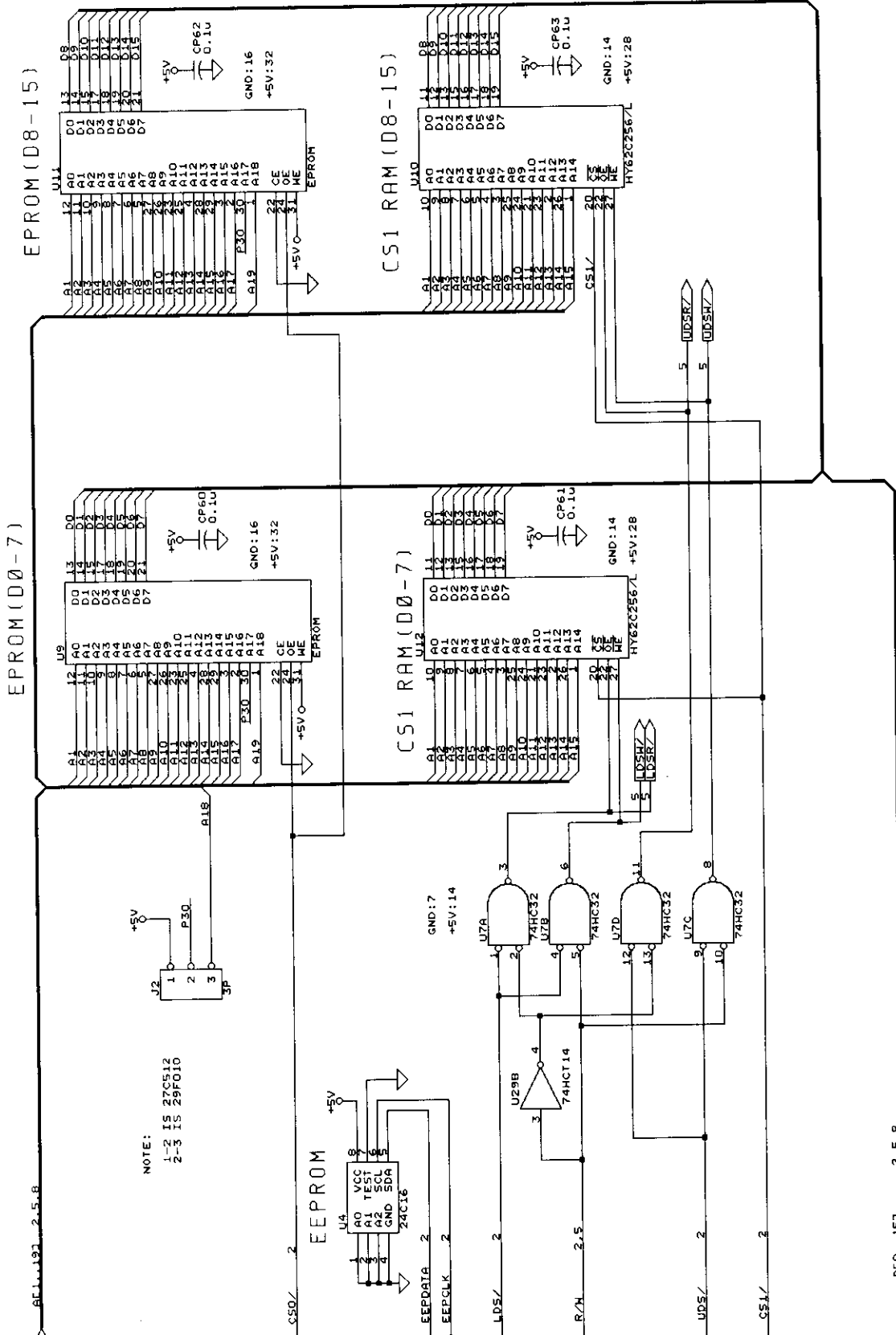


NTUPOWER.SCH

SW1 : POWER RESET
* USED ON TESTING
& USED RACK

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REV	4.4
Date	April 22, 1998
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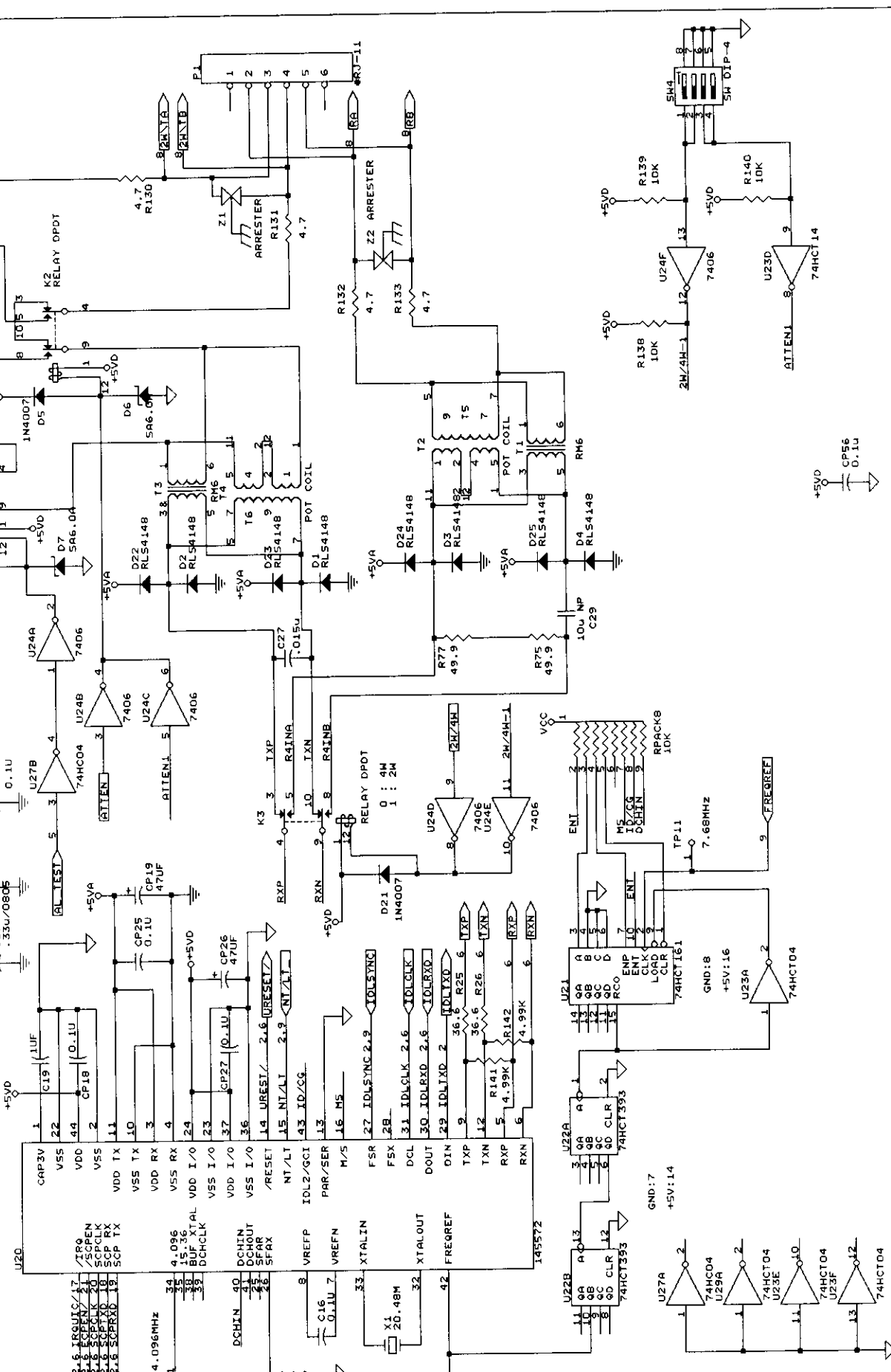




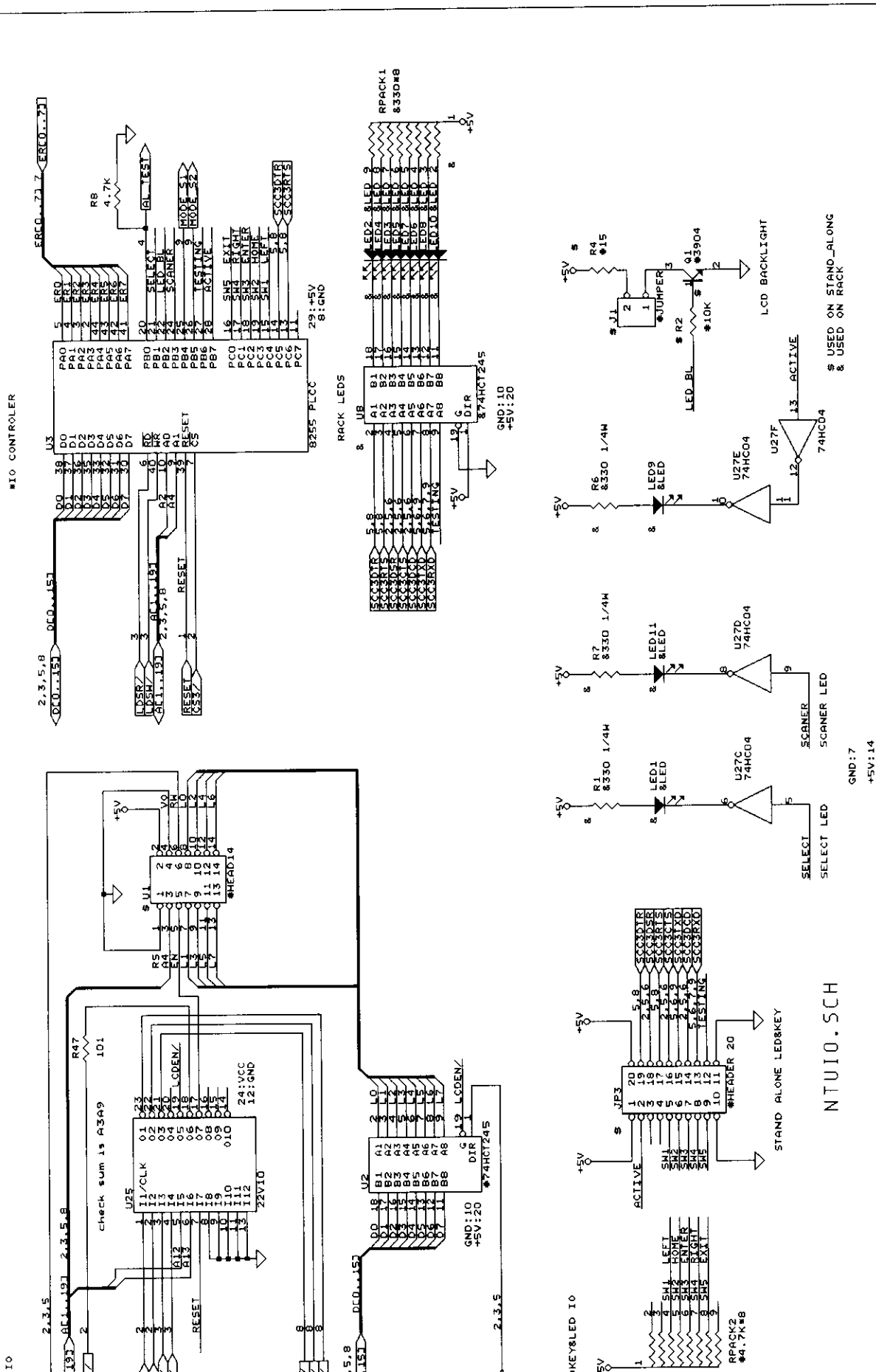
NEAR TO 145572

8 USED ON RACK
5 USED ON STAND ALONG

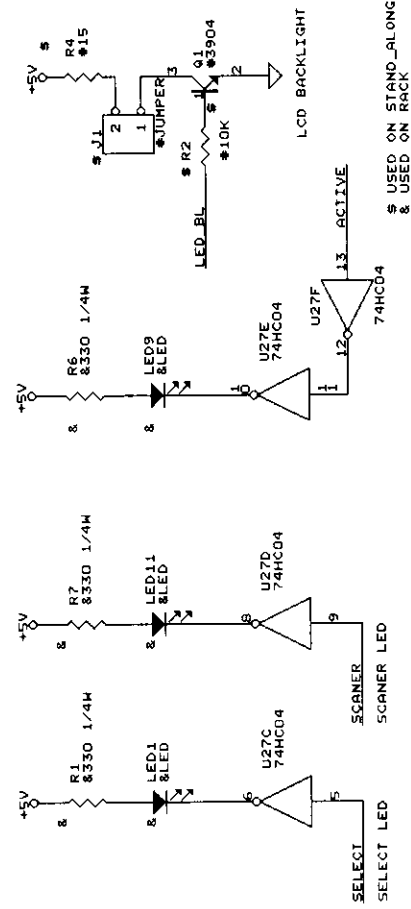
U INTERFACE



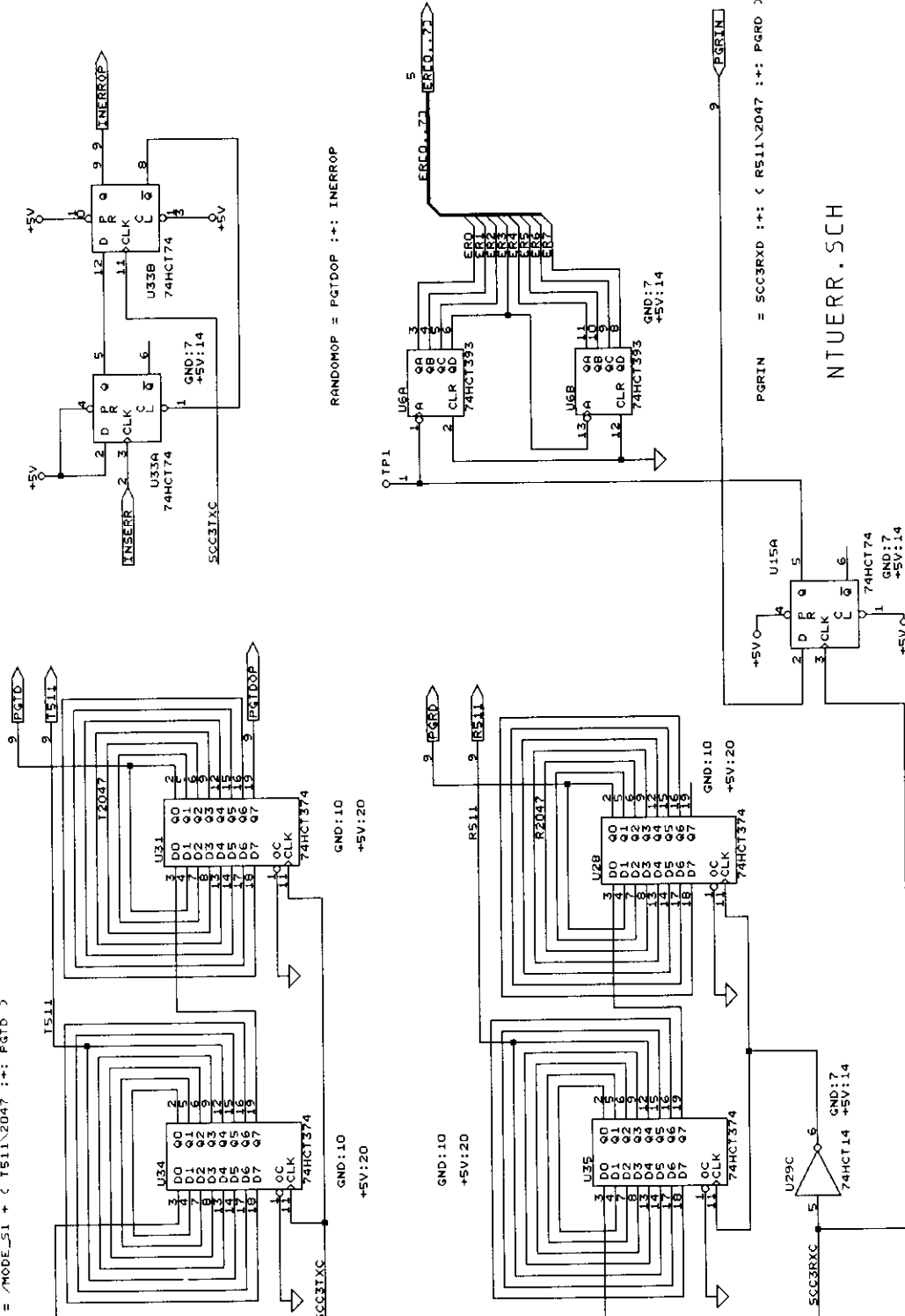
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Size	DT-128
Document Number	NTUNET.P4
REV	4.4
Date	April 17, 1998
Sheet	4 of 9



NTU10.SCH

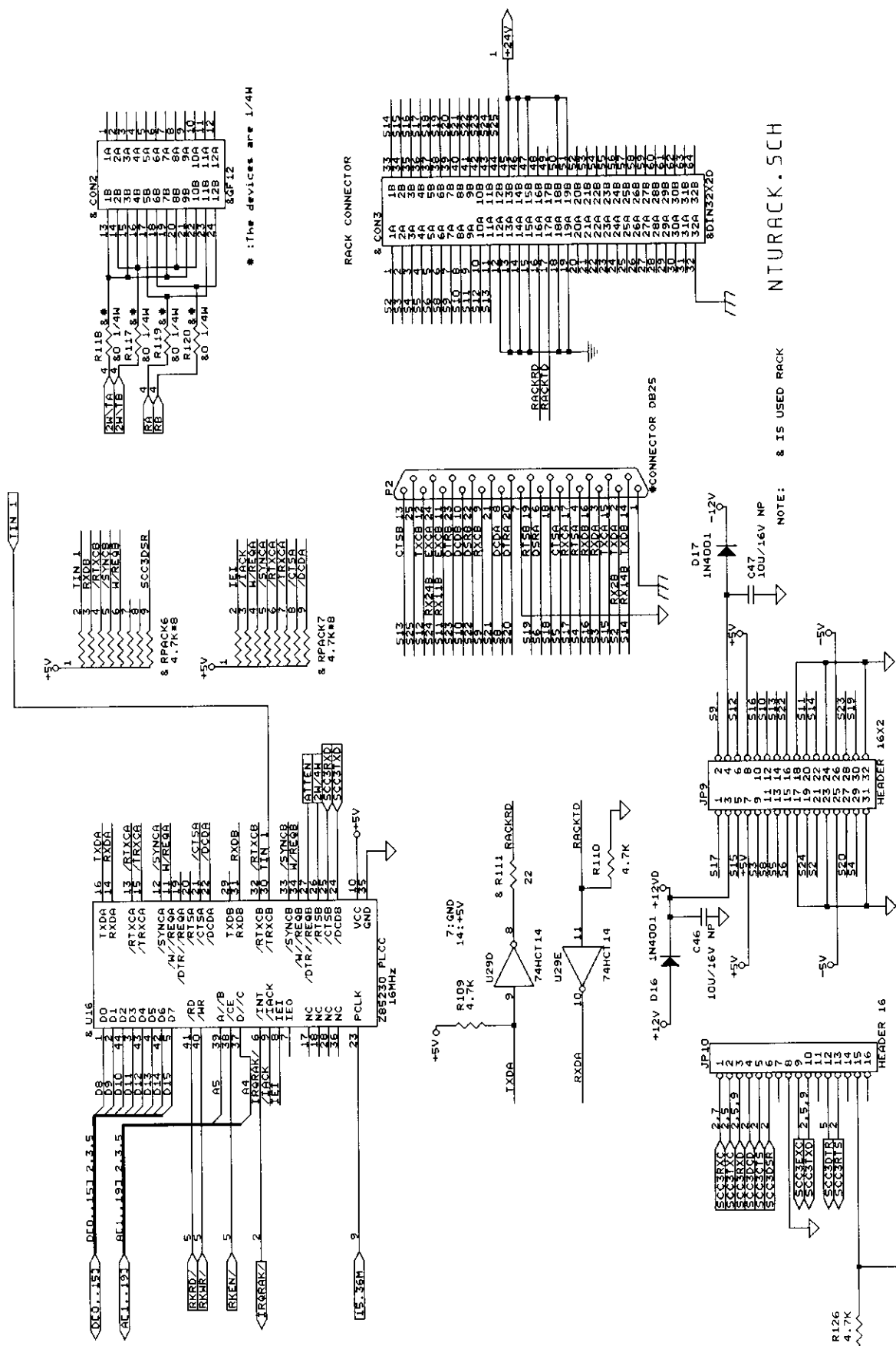


= /MODE_S1 + (T511\2047 :+ : PGTD)



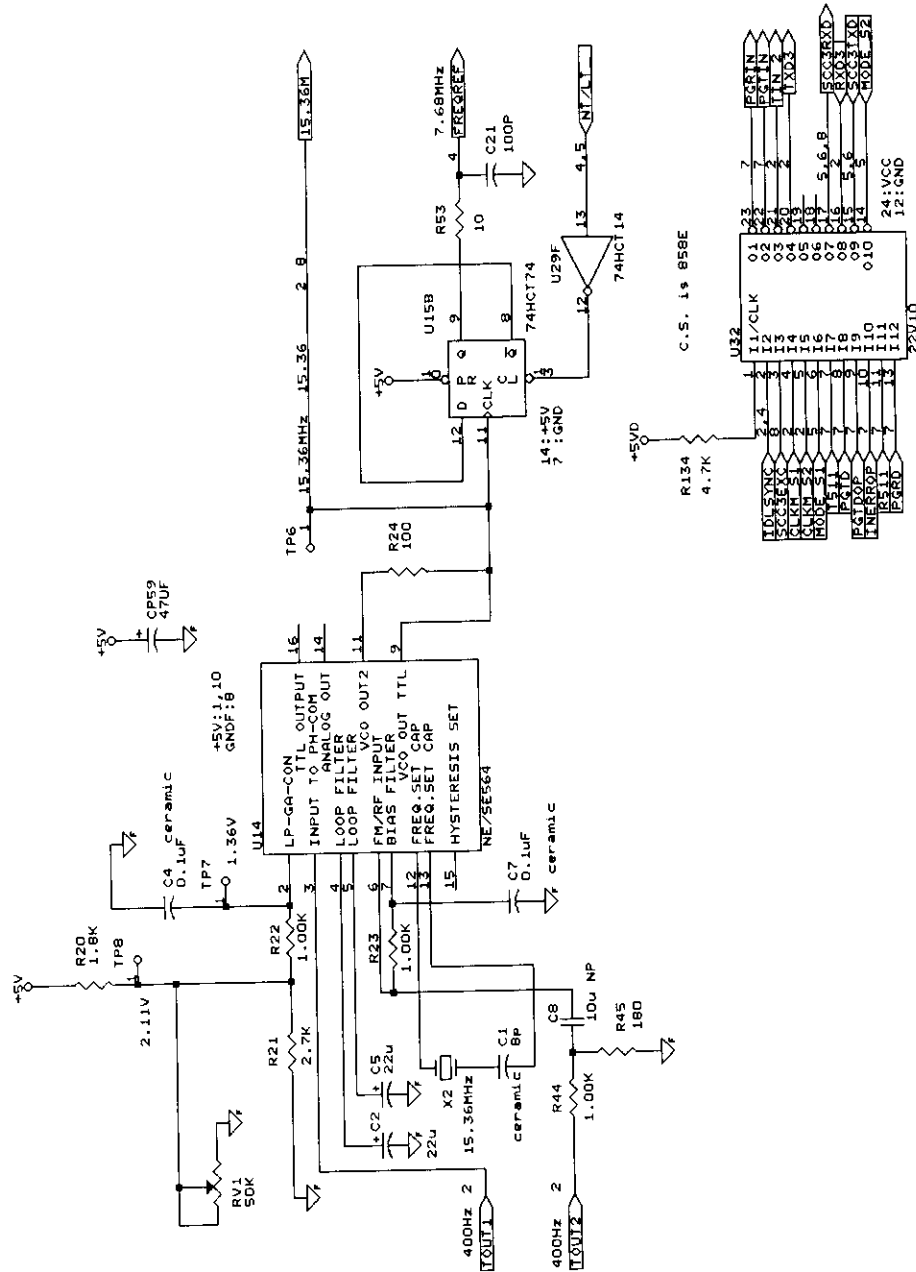
NTUERR.SCH

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NTURACK.5CH

Title	5058-0016
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NOTE:

CLKM_S2	CLKM_S1	CLK	MODE
0	1	INTERNAL	NORMAL
1	0	LOOPBACK	PATTERN
1	1	EXTERNAL	TEST

PS: # is "DON'T CARE"

NTUCLK.SCH