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WL18MODGI 8 Dual-Band Industrial Module – Wi-Fi®, Bluetooth®, and Bluetooth Low Energy (LE)

1 Features

- General
  - Integrates RF, power amplifiers (PAs), clocks, RF switches, filters, passives, and power management
  - Operating temperature: –40°C to +85°C industrial temperature grade
  - Small form factor: 13.3mm × 13.4mm × 2mm
  - 100-pin MOC package
- Wi-Fi®
  - WLAN baseband processor and RF transceiver support of IEEE Std 802.11a, 802.11b, 802.11g, and 802.11n
  - 20MHz and 40MHz SISO and 20MHz 2 × 2 MIMO at 2.4GHz for high throughput: 80Mbps (TCP), 100Mbps (UDP)
  - 2.4GHz MRC support for extended range and 5GHz diversity capable
  - Fully calibrated: Production calibration is not required
  - 4-bit SDIO host interface support
  - Wi-Fi direct concurrent operation (multichannel, multirole)
- Bluetooth® and Bluetooth Low Energy:
  - Bluetooth 5.1 secure connection compliant and CSA2 support; declaration ID: D052427
  - Host controller interface (HCI) transport for Bluetooth over UART
  - Dedicated audio processor support of SBC encoding + A2DP
  - Dual-mode Bluetooth and Bluetooth Low Energy
- Key benefits
  - Reduces design overhead
  - Differentiated use cases by configuring module simultaneously in two roles (STA and AP) to connect directly with other Wi-Fi devices on different RF channel (Wi-Fi networks)
  - Best-in-class Wi-Fi with high-performance audio and video streaming reference applications with up to 1.4× the range versus one antenna
  - Different provisioning methods for in-home devices' connectivity to Wi-Fi in one step
  - Lowest Wi-Fi power consumption in connected idle (< 800µA)
  - Configurable wake on WLAN filters to only wake up the system
  - Wi-Fi and Bluetooth single antenna coexistence

Description

The WL18MODGI module from DCI offers a high throughput and extended range along with Wi-Fi® and *Bluetooth*® coexistence in a power-optimized design. The WL18MODGI is a Wi-Fi, dual- band, 2.4GHz and 5GHz module solution with two antennas supporting industrial temperature grade. The device is FCC, IC, ETSI/CE, and TELEC certified for AP (with DFS support) and client.

Device Information (1)

PART NUMBER	BODY SIZE
WL18MODGI	13.3mm × 13.4mm × 2mm

(1) For more information, see Section 12.

3 Functional Block Diagram

Model WL18MODGI, Test Grade: 07 Functional Block Diagram

Figure 4-1 shows a functional block diagram of the WL18MODGI.

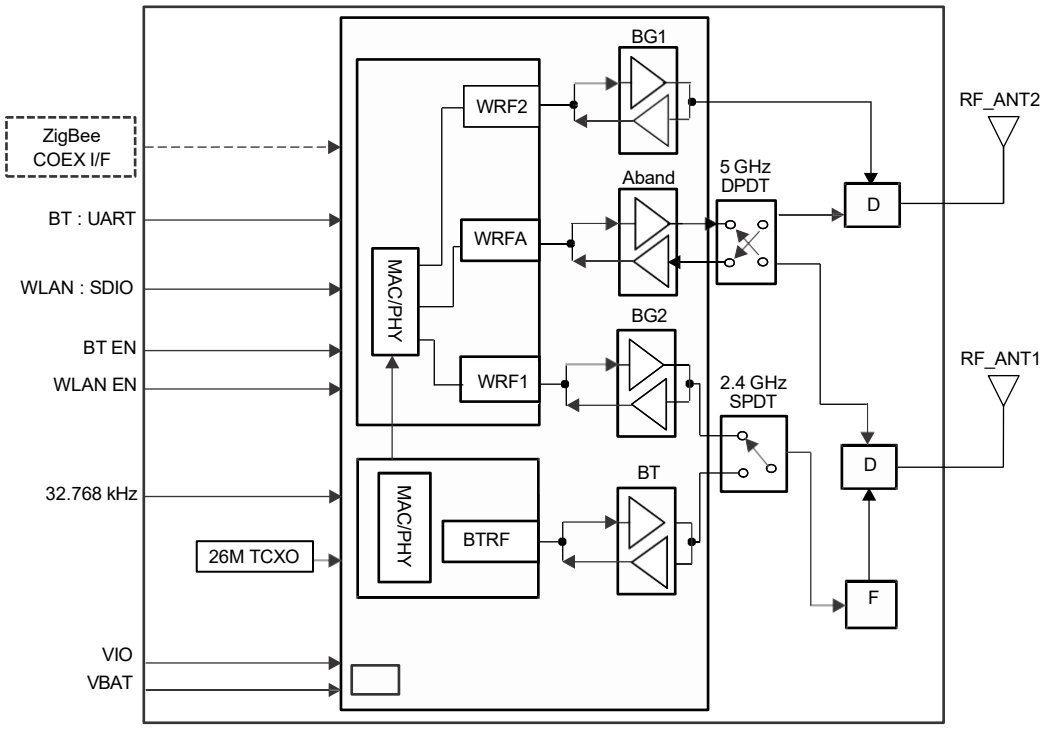


Figure 4-1. WL18MODGI Functional Block Diagram

Note

Dashed lines indicate optional configurations and are not applied by default.

4 Device Comparison

The WL18MODGI module offers two footprint-compatible dual-band 2.4- and 5GHz industrial temperature grade variants providing stand-alone Wi-Fi and Bluetooth combo connectivity

Table 5-1.

DEVICE	FEATURE				
	WLAN 2.4GHz SISO(1)	WLAN 2.4GHz MIMO(1)	WLAN 2.4GHz MRC(2)	Bluetooth	WLAN 5GHz SISO(1)
WL18MODGI	✓	✓	✓	✓	✓

(1) SISO: single input, single output; MIMO: multiple input, multiple output.
(2) MRC: maximum ratio combining; supported at 11 g,n only.

Pin Configuration and Functions

Figure 6-1 shows the pin assignments for the 100-pin MOC package.

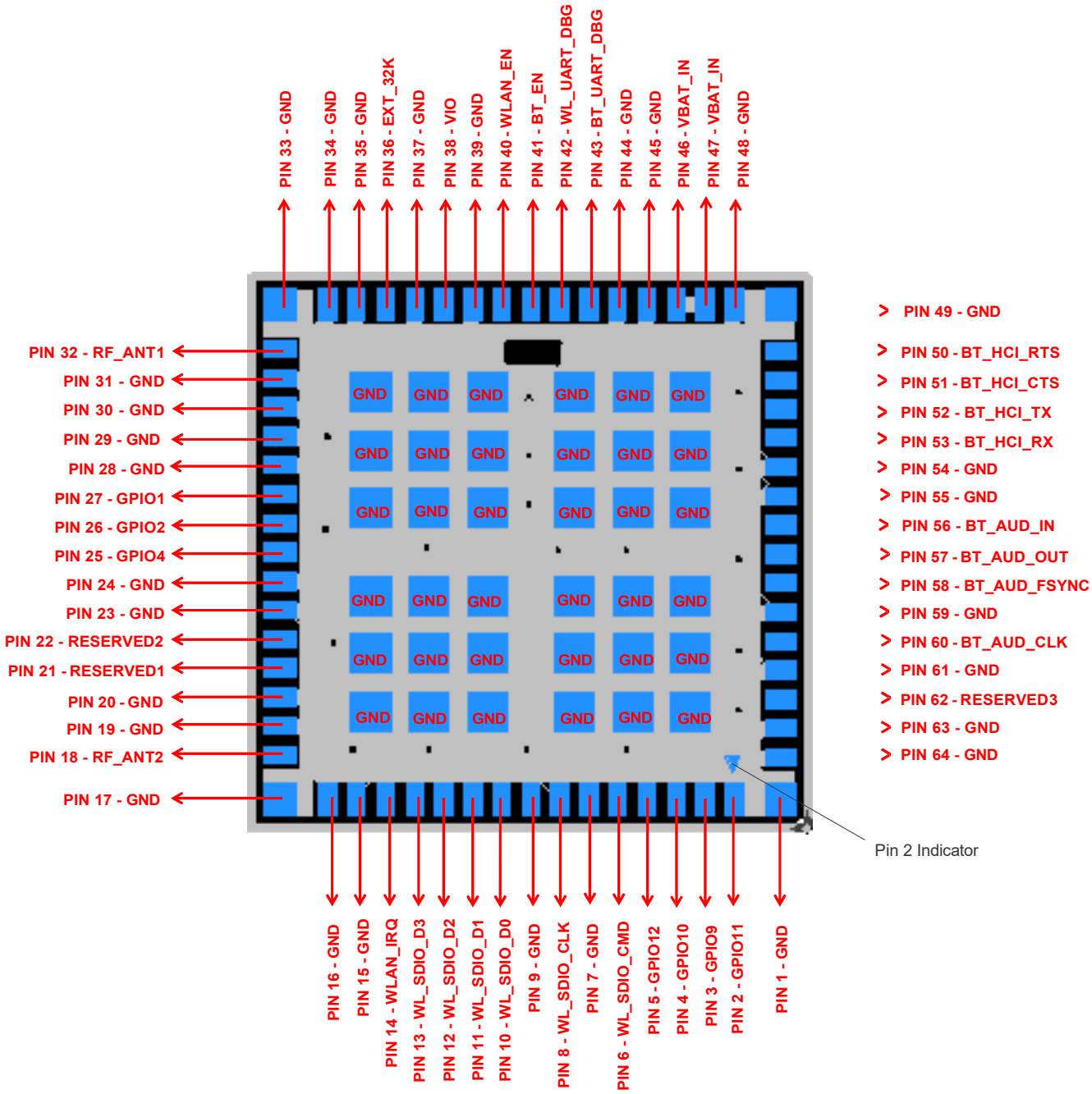


Figure 6-1. 100-Pin MOC Package (Bottom View)

Pin Attributes

Table 6-1 describes the module pins.

Table 6-1. Pin Attributes

PIN NAME	PIN NO.	TYPE/ DIR	SHUTDOWN STATE(1)	AFTER POWER UP(1)	VOLTAGE LEVEL	CONNECTIVITY(2)		DESCRIPTION(3)
						1807	1837	
Clocks and Reset Signals								
WL_SDIO_CLK_1V8	8	I	Hi-Z	Hi-Z	1.8V	v	v	WLAN SDIO clock. Must be driven by the host.
EXT_32K	36	ANA			–	v	v	Input sleep clock: 32.768 kHz
WLAN_EN	40	I	PD	PD	1.8V	v	v	Mode setting: high = enable
BT_EN	41	I	PD	PD	1.8V	x	v	Mode setting: high = enable. If Bluetooth is not used, connect to ground.
Power-Management Signals								
VIO_IN	38	POW	PD	PD	1.8V	v	v	Connect to 1.8V external VIO
VBAT_IN	46	POW			VBAT	v	v	Power supply input, 2.9 to 4.8V
VBAT_IN	47	POW			VBAT	v	v	Power supply input, 2.9 to 4.8V
TI Reserved								
GPIO11	2	I/O	PD	PD	1.8V	v	v	Reserved for future use. NC if not used.
GPIO9	3	I/O	PD	PD	1.8V	v	v	Reserved for future use. NC if not used.
GPIO10	4	I/O	PU	PU	1.8V	v	v	Reserved for future use. NC if not used.
GPIO12	5	I/O	PU	PU	1.8V	v	v	Reserved for future use. NC if not used.
RESERVED1	21	I	PD	PD	1.8V	x	x	Reserved for future use. NC if not used.
RESERVED2	22	I	PD	PD	1.8V	x	x	Reserved for future use. NC if not used.
GPIO4	25	I/O	PD	PD	1.8V	v	v	Reserved for future use. NC if not used.
RESERVED3	62	O	PD	PD	1.8V	x	x	Reserved for future use. NC if not used. Option: External TCXO.

Table 6-1. Pin Attributes (continued)

PIN NAME	PIN NO.	TYPE/ DIR	SHUTDOWN STATE(1)	AFTER POWER UP(1)	VOLTAGE LEVEL	CONNECTIVITY(2)		DESCRIPTION(3)
						1807	1837	
WLAN Functional Block: Int Signals								
WL_SDIO_CMD_1V8	6	I/O	Hi-Z	Hi-Z	1.8V	v	v	WLAN SDIO command
WL_SDIO_D0_1V8	10	I/O	Hi-Z	Hi-Z	1.8V	v	v	WLAN SDIO data bit 0
WL_SDIO_D1_1V8	11	I/O	Hi-Z	Hi-Z	1.8V	v	v	WLAN SDIO data bit 1
WL_SDIO_D2_1V8	12	I/O	Hi-Z	Hi-Z	1.8V	v	v	WLAN SDIO data bit 2
WL_SDIO_D3_1V8	13	I/O	Hi-Z	PU	1.8V	v	v	WLAN SDIO data bit 3. Changes state to PU at WL_EN or BT_EN assertion for card detects. Later disabled by software during initialization.
WL_IRQ_1V8	14	O	PD	0	1.8V	v	v	SDIO available, interrupt out. Active high. (For WL_RS232_TX/RX pullup is at power up.) Set to rising edge (active high) on power up. The Wi-Fi interrupt line can be configured by the driver according to the IRQ configuration (polarity/ level/edge).
RF_ANT2	18	ANA			–	v	v	5G ANT diversity TX/RX , 2.4G Secondary antenna MRC/MIMO only
GPIO2	26	I/O	PD	PD	1.8V	v	v	WL_RS232_RX (when WLAN_IRQ = 1 at power up)
GPIO1	27	I/O	PD	PD	1.8V	v	v	WL_RS232_TX (when WLAN_IRQ = 1 at power up)
RF_ANT1	32	ANA			–	v	v	5G main ANT TX/RX, 2.4G WLAN main antenna SISO, Bluetooth
WL_UART_DBG	42	O	PU	PU	1.8V	v	v	Option: WLAN logger
Bluetooth Functional Block: Int Signals								
BT_UART_DBG	43	O	PU	PU	1.8V	x	v	Option: Bluetooth logger
BT_HCI_RTS_1V8	50	O	PU	PU	1.8V	x	v	UART RTS to host. NC if not used.
BT_HCI_CTS_1V8	51	I	PU	PU	1.8V	x	v	UART CTS from host. NC if not used.
BT_HCI_TX_1V8	52	O	PU	PU	1.8V	x	v	UART TX to host. NC if not used.
BT_HCI_RX_1V8	53	I	PU	PU	1.8V	x	v	UART RX from host. NC if not used.
BT_AUD_IN	56	I	PD	PD	1.8V	x	v	Bluetooth PCM/I2S bus. Data in. NC if not used.
BT_AUD_OUT	57	O	PD	PD	1.8V	x	v	Bluetooth PCM/I2S bus. Data out. NC if not used.
BT_AUD_FSYNC	58	I/O	PD	PD	1.8V	x	v	Bluetooth PCM/I2S bus. Frame sync. NC if not used.
BT_AUD_CLK	60	I/O	PD	PD	1.8V	x	v	Bluetooth PCM/I2S bus. NC if not used.

Table 6-1. Pin Attributes (continued)

PIN NAME	PIN NO.	TYPE/ DIR	SHUTDOWN STATE(1)	AFTER POWER UP(1)	VOLTAGE LEVEL	CONNECTIVITY(2)		DESCRIPTION(3)
						1807	1837	
Ground Pins								
GND	1	GND			–	v	v	v
GND	7	GND			–	v	v	v
GND	9	GND			–	v	v	v
GND	15	GND			–	v	v	v
GND	16	GND			–	v	v	v
GND	17	GND			–	v	v	v
GND	19	GND			–	v	v	v
GND	20	GND			–	v	v	v
GND	23	GND			–	v	v	v
GND	24	GND			–	v	v	v
GND	28	GND			–	v	v	v
GND	29	GND			–	v	v	v
GND	30	GND			–	v	v	v
GND	31	GND			–	v	v	v
GND	33	GND			–	v	v	v
GND	34	GND			–	v	v	v
GND	35	GND			–	v	v	v
GND	37	GND			–	v	v	v
GND	39	GND			–	v	v	v
GND	44	GND			–	v	v	v
GND	45	GND			–	v	v	v
GND	48	GND			–	v	v	v
GND	49	GND			–	v	v	v
GND	54	GND			–	v	v	v
GND	55	GND			–	v	v	v
GND	59	GND			–	v	v	v
GND	61	GND			–	v	v	v
GND	63	GND			–	v	v	v
GND	G1 – G36	GND			–	v	v	v
GND	64	GND			–	v	v	v

(1) PU = pullup; PD = pulldown; Hi-Z = high-impedance
(2) v = connect; x = no connect.
(3) Host must provide PU using a 10kΩ resistor for all non-CLK SDIO signals.

Specifications

All measurements are performed with V_{BAT} = 3.7V, V_{IO} = 1.8V, 25°C for typical values with matched RF antennas, unless otherwise indicated.

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
V_{BAT}		4.8(2)	V
V_{IO}	–0.5	2.1	V
Input voltage to analog pins	–0.5	2.1	V
Input voltage limits (CLK_IN)	–0.5	VDD_IO	V
Input voltage to all other pins	–0.5	(VDD_IO + 0.5 V)	V
Operating ambient temperature	–40	85 (3)	°C
Storage temperature, T_{stg}	–40	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) 4.8V cumulative to 2.33 years, including charging dips and peaks
(3) In the WL18xx system, a control mechanism exists to ensure T_j < 125°C. When T_j approaches this threshold, the control mechanism manages the transmitter patterns.

4.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{BAT} (1)	DC supply range for all modes		2.9	3.7	4.8	V
V_{IO}	1.8-V I/O ring power supply voltage		1.62	1.8	1.95	V
V_{IH}	I/O high-level input voltage		0.65 × VDD_IO		VDD_IO	V
V_{IL}	I/O low-level input voltage		0		0.35 × VDD_IO	V
V_{IH_EN}	Enable inputs high-level input voltage		1.365		VDD_IO	V
V_{IL_EN}	Enable inputs low-level input voltage		0		0.4	V
V_{OH}	High-level output voltage	At 4 mA	VDD_IO –0.45		VDD_IO	V
V_{OL}	Low-level output voltage	At 4 mA	0		0.45	V
T_r,T_f	Input transitions time T_r,T_f from 10% to 90% (digital I/O)(2)		1		10	ns
T_r	Output rise time from 10% to 90% (digital pins)(2)	C_L < 25 pF			5.3	ns
T_f	Output fall time from 10% to 90% (digital pins)(2)	C_L < 25 pF			4.9	ns
	Ambient operating temperature		–40		85	°C

7.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Maximum power dissipation	WLAN operation			2.8	W
	Bluetooth operation			0.2	

(1) 4.8 V is applicable only for 2.33 years (30% of the time). Otherwise, maximum V_{BAT} must not exceed 4.3 V.
(2) Applies to all digital lines except SDIO, UART, I2C, PCM and slow clock lines.

7.4 External Digital Slow Clock Requirements

The supported digital slow clock is 32.768kHz digital (square wave). All core functions share a single input.

		CONDITION	MIN	TYP	MAX	UNIT
	Input slow clock frequency			32768		Hz
	Input slow clock accuracy (initial, temperature, and aging)	WLAN, Bluetooth			±250	ppm
T_r, T_f	Input transition time (10% to 90%)				200	ns
	Frequency input duty cycle		15%	50%	85%	
V_{IH}, V_{IL}	Input voltage limits	Square wave, DC coupled	0.65 × VDD_IO		VDD_IO	V_{peak}
			0		0.35 x VDD_IO	
	Input impedance		1			MΩ
	Input capacitance				5	pF

7.5 Thermal Resistance Characteristics for MOC 100-Pin Package

THERMAL METRICS(1)		(°C/W)(2)
θ_{JA}	Junction to free air(3)	16.6
θ_{JB}	Junction to board	6.06
θ_{JC}	Junction to case(4)	5.13

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics Application Report*.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R_{\theta JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)
- JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
- JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements

Power dissipation of 2W and an ambient temperature of 70°C is assumed.

(3) According to the JEDEC EIA/JESD 51 document
(4) Modeled using the JEDEC 2s2p thermal test board with 36 thermal vias

7.6 WLAN Performance: 2.4GHz Receiver Characteristics

over operating free-air temperature range (unless otherwise noted). All RF and performance numbers are aligned to the module pin.

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
	RF_ANT1 pin 2.4GHz SISO				
Operation frequency range		2412		2484	MHz
Sensitivity: 20-MHz bandwidth. At < 10% PER limit	1 Mbps DSSS		–95.0		dBm
	2 Mbps DSSS		–92.0		
	5.5 Mbps CCK		–89.2		
	11 Mbps CCK		–86.3		
	6 Mbps OFDM		–91.0		
	9 Mbps OFDM		–89.0		
	12 Mbps OFDM		–88.0		
	18 Mbps OFDM		–85.5		
	24 Mbps OFDM		–82.5		
	36 Mbps OFDM		–79.0		
	48 Mbps OFDM		–74.0		
	54 Mbps OFDM		–72.5		
	MCS0 MM 4K		–89.3		
	MCS1 MM 4K		–86.5		
	MCS2 MM 4K		–84.5		
	MCS3 MM 4K		–81.5		
	MCS4 MM 4K		–78.0		
	MCS5 MM 4K		–73.5		
	MCS6 MM 4K		–71.5		
	MCS7 MM 4K		–70.0		
	MCS0 MM 4K 40 MHz		–86.0		
	MCS7 MM 4K 40 MHz		–66.3		
	MCS0 MM 4K MRC		–91.0		
	MCS7 MM 4K MRC		–73.0		
	MCS13 MM 4K		–70.0		
	MCS14 MM 4K		–69.0		
	MCS15 MM 4K		–68.3		
Maximum input level	OFDM	–20.0	–10.0		dBm
	CCK	–10.0	–6.0		
	DSSS	–4.0	–1.0		
Adjacent channel rejection: Sensitivity level +3 dB for OFDM; Sensitivity level +6 dB for 11b	2 Mbps DSSS	42.0			dB
	11 Mbps CCK	38.0			
	54 Mbps OFDM	2.0			
RX leakage			–70		dBm
PER floor			1.0%		
RSSI accuracy				±3	dB

7.7 WLAN Performance: 2.4GHz Transmitter Power

over operating free-air temperature range (unless otherwise noted). All RF and performance numbers are aligned to the module pin.

PARAMETER	CONDITION[1]	MIN	TYP	MAX	UNIT
	RF_ANT1 Pin 2.4GHz SISO				
Output Power: Maximum RMS output power measured at 1 dB from IEEE spectral mask or EVM[2]	1 Mbps DSSS		17.3		dBm
	2 Mbps DSSS		17.3		
	5.5 Mbps CCK		17.3		
	11 Mbps CCK		17.3		
	6 Mbps OFDM		17.1		
	9 Mbps OFDM		17.1		
	12 Mbps OFDM		17.1		
	18 Mbps OFDM		17.1		
	24 Mbps OFDM		16.2		
	36 Mbps OFDM		15.3		
	48 Mbps OFDM		14.6		
	54 Mbps OFDM		13.8		
	MCS0 MM		16.1		
	MCS1 MM		16.1		
	MCS2 MM		16.1		
	MCS3 MM		16.1		
	MCS4 MM		15.3		
	MCS5 MM		14.6		
	MCS6 MM		13.8		
	MCS7 MM[3]		12.6		
	MCS0 MM 40 MHz		14.8		
	MCS7 MM 40 MHz		11.3		
	RF_ANT1 + RF_ANT2 MIMO				
	MCS12 (WL18x5)		18.5		dBm
	MCS13 (WL18x5)		17.4		
	MCS14 (WL18x5)		14.5		
	MCS15 (WL18x5)		13.4		
	RF_ANT1 + RF_ANT2				
Operation frequency range		2412		2484	MHz
Return loss			–10.0		dB
Reference input impedance			50.0		Ω

(1) Maximum transmitter power (TP) degradation of up to 30% is expected, starting from 80°C ambient temperature on MIMO operation

(2) Regulatory constraints limit TI module output power to the following:

- Channel 14 is used only in Japan; to keep the channel spectral shaping requirement, the power is limited: 14.5 dBm.
- Channels 1, 11 at OFDM legacy and HT 20-MHz rates: 12 dBm
- Channels 1, 11 at HT 40-MHz rates: 10 dBm
- Channel 7 at HT 40-MHz lower rates: 10 dBm
- Channel 5 at HT 40-MHz upper rates: 10 dBm
- All 11B rates are limited to 16 dBm to comply with the ETSI PSD 10 dBm/MHz limit.
- All OFDM rates are limited to 16.5 dBm to comply with the ETSI EIRP 20 dBm limit.

(3) To ensure compliance with the EVM conditions specified in the PHY chapter of IEEE Std 802.11™ – 2012:

- MCS7 20 MHz channel 12 output power is 2 dB lower than the typical value.

- MCS7 20 MHz channel 8 output power is 1 dB lower than the typical value.

7.8 WLAN Performance: 5GHz Receiver Characteristics

over operating free-air temperature range (unless otherwise noted). All RF and performance numbers are aligned to the module pin.

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
RF_ANT1 or RF_ANT2					
Operation frequency range		4910.0		5825.0	MHz
Sensitivity: 20-MHz bandwidth. At < 10% PER limit	6 Mbps OFDM 1K		–92.5		dBm
	9 Mbps OFDM 1K		–90.5		
	12 Mbps OFDM 1K		–90.0		
	18 Mbps OFDM 1K		–87.5		
	24 Mbps OFDM 1K		–84.5		
	36 Mbps OFDM 1K		–81.0		
	48 Mbps OFDM 1K		–76.5		
	54 Mbps OFDM 1K		–74.6		
	MCS0 MM 4K		–91.4		
	MCS1 MM 4K		–88.0		
	MCS2 MM 4K		–86.0		
	MCS3 MM 4K		–83.0		
	MCS4 MM 4K		–79.8		
	MCS5 MM 4K		–75.5		
	MCS6 MM 4K		–74.0		
	MCS7 MM 4K		–72.4		
	MCS0 MM 4K 40 MHz		–88.5		
	MCS7 MM 4K 40 MHz		–69.3		
Maximum input level	OFDM	–30.0	–15.0		dBm
Adjacent channel rejection sensitivity +3 dB	OFDM54	2.0			dBm
RX LO leakage			–52.0		dBm
PER floor			1.0%	2.0%	
RSSI accuracy			±3		dB

7.9 WLAN Performance: 5GHz Transmitter Power

over operating free-air temperature range (unless otherwise noted)

PARAMETER[1]	CONDITION[2]	MIN	TYP	MAX	UNIT
RF_ANT1 or RF_ANT2					
Operation frequency range		4920		5825	MHz
RMS output power complies with IEEE mask and EVM requirements[3]	6 Mbps OFDM		18.0		dBm
	9 Mbps OFDM		18.0		
	12 Mbps OFDM		18.0		
	18 Mbps OFDM		18.0		
	24 Mbps OFDM		17.4		
	36 Mbps OFDM		16.5		
	48 Mbps OFDM		15.8		
	54 Mbps OFDM		14.5		
	MCS0 MM		18.0		
	MCS1 MM 4K		18.0		
	MCS2 MM 4K		18.0		
	MCS3 MM 4K		18.0		
	MCS4 MM 4K		16.5		
	MCS5 MM 4K		15.8		
	MCS6 MM 4K		14.5		
	MCS7 MM 4K		13.0		
	MCS0 MM 40 MHz		16.5		
	MCS7 MM 40 MHz		12.0		
Output power resolution			0.125		dB
Return loss			–10.0		dB
Reference input impedance			50.0		Ω

(1) All RF and performance numbers are aligned to the module pin.
(2) Maximum TP degradation of up to 30% is expected, starting from 80°C ambient temperature on 5GHz TX operation.

7.10 WLAN Performance: Currents

over operating free-air temperature range (unless otherwise noted)

PARAMETER[1]	SPECIFICATION	TYP (AVG) –25°C	UNIT
Receiver	Low-power mode (LPM) 2.4GHz RX SISO20 single chain	49	mA
	2.4GHz RX search SISO20	58	
	2.4GHz RX search MIMO20	74	
	2.4GHz RX search SISO40	63	
	2.4GHz RX 20 M SISO 11 CCK	60	
	2.4GHz RX 20 M SISO 6 OFDM	61	
	2.4GHz RX 20 M SISO MCS7	69	
	2.4GHz RX 20 M MRC 1 DSSS	74	
	2.4GHz RX 20 M MRC 6 OFDM	81	
	2.4GHz RX 20 M MRC 54 OFDM	85	
	2.4GHz RX 40-MHz MCS7	81	
	5GHz RX 20-MHz OFDM6	68	
	5GHz RX 20-MHz MCS7	77	
	5GHz RX 40-MHz MCS7	85	
Transmitter[2]	2.4GHz TX 20 M SISO 6 OFDM	285	mA
	2.4GHz TX 20 M SISO 11 CCK	283	
	2.4GHz TX 20 M SISO 54 OFDM	247	
	2.4GHz TX 20 M SISO MCS7	238	
	2.4GHz TX 20 M MIMO MCS15	510	
	2.4GHz TX 40 M SISO MCS7	243	
	5GHz TX 20 M SISO 6 OFDM	366	
	5GHz TX 20 M SISO 54 OFDM	329	
	5GHz TX 20 M SISO MCS7	324	
	5GHz TX 40 M SISO MCS7	332	

(1) All RF and performance numbers are aligned to the module pin.
(2) Numbers reflect the typical current consumption at maximum output power per rate.

7.11 Bluetooth Performance: BR, EDR Receiver Characteristics—In-Band Signals

over operating free-air temperature range (unless otherwise noted)

PARAMETER[1]	CONDITION		MIN	TYP	MAX	UNIT
Bluetooth BR, EDR operation frequency range			2402		2480	MHz
Bluetooth BR, EDR channel spacing				1		MHz
Bluetooth BR, EDR input impedance				50		Ω
Bluetooth BR, EDR sensitivity[2] dirty TX on	BR, BER = 0.1%			–92.2		dBm
	EDR2, BER = 0.01%			–91.7		
	EDR3, BER = 0.01%			–84.7		
Bluetooth EDR BER floor at sensitivity + 10 dB Dirty TX off (for 1,600,000 bits)	EDR2		1e-6			
	EDR3		1e-6			
Bluetooth BR, EDR maximum usable input power	BR, BER = 0.1%		–5.0			dBm
	EDR2, BER = 0.1%		–15.0			
	EDR3, BER = 0.1%		–15.0			
Bluetooth BR intermodulation	Level of interferers for n = 3, 4, and 5		–36.0	–30.0		dBm
Bluetooth BR, EDR C/I performance Numbers show wanted signal-to-interfering-signal ratio. Smaller numbers indicate better C/I performances (Image frequency = –1 MHz)	BR, co-channel				10	dB
	EDR, co-channel	EDR2			12	
		EDR3			20	
	BR, adjacent ±1 MHz				–3.0	
	EDR, adjacent ±1 MHz, (image)	EDR2			–3.0	
		EDR3			2.0	
	BR, adjacent +2 MHz				–33.0	
	EDR, adjacent +2 MHz	EDR2			–33.0	
		EDR3			–28.0	
	BR, adjacent –2 MHz				–20.0	
	EDR, adjacent –2 MHz	EDR2			–20.0	
		EDR3			–13.0	
	BR, adjacent ≥I±3I MHz				–42.0	
	EDR, adjacent ≥I±3I MHz	EDR2			–42.0	
		EDR3			–36.0	
Bluetooth BR, EDR RF return loss				–10.0		dB

(1) All RF and performance numbers are aligned to the module pin.
(2) Sensitivity degradation up to –3dB may occur due to fast clock harmonics with dirty TX on.

7.12 Bluetooth Performance: Transmitter, BR

over operating free-air temperature range (unless otherwise noted)

PARAMETER[1]		MIN	TYP	MAX	UNIT
BR RF output power[2]	$V_{BAT} \geq 3V$[3]		11.7		dBm
	$V_{BAT} < 3V$[3]		7.2		
BR gain control range			30.0		dB
BR power control step			5.0		dB
BR adjacent channel power |M-N| = 2			–43.0		dBm
BR adjacent channel power |M-N| > 2			–48.0		dBm

(1) All RF and performance numbers are aligned to the module pin.
(2) Values reflect maximum power. Reduced power is available using a vendor-specific (VS) command.
(3) VBAT is measured with an on-chip ADC that has an accuracy error of up to 5%.

7.13 Bluetooth Performance: Transmitter, EDR

over operating free-air temperature range (unless otherwise noted)

PARAMETER[1]		MIN	TYP	MAX	UNIT
EDR output power[2]	$V_{BAT} \geq 3V$[3]		7.2		dBm
	$V_{BAT} < 3V$[3]		5.2		
EDR gain control range			30		dB
EDR power control step			5		dB
EDR adjacent channel power |M-N| = 1			–36		dBc
EDR adjacent channel power |M-N| = 2			–30		dBm
EDR adjacent channel power |M-N| > 2			–42		dBm

(1) All RF and performance numbers are aligned to the module pin.
(2) Values reflect default maximum power. Maximum power can be changed using a VS command.
(3) VBAT is measured with an on-chip ADC that has an accuracy error of up to 5%.

7.14 Bluetooth Performance: Modulation, BR

over operating free-air temperature range (unless otherwise noted)

CHARACTERISTICS[1]	CONDITION[2]		MIN	TYP	MAX	UNIT
BR –20-dB bandwidth				925	995	kHz
BR modulation characteristics	Δf1avg	Mod data = 4 1s, 4 0s: 111100001111...	145	160	170	kHz
	Δf2max ≥ limit for at least 99.9% of all Δf2max	Mod data = 1010101...	120	130		kHz
	Δf2avg, Δf1avg		85%	88%		
BR carrier frequency drift	One-slot packet		–25		25	kHz
	Three- and five-slot packet		–35		35	kHz
BR drift rate	lfk+5 – fkl , k = 0 to max				15	kHz/50 µs
BR initial carrier frequency tolerance[3]	f0–fTX		±75		±75	kHz

(1) All RF and performance numbers are aligned to the module pin.
(2) Performance values reflect maximum power.
(3) Numbers include XTAL frequency drift over temperature and aging.

7.15 Bluetooth Performance: Modulation, EDR

over operating free-air temperature range (unless otherwise noted)

PARAMETER[1] [2]	CONDITION	MIN	TYP	MAX	UNIT
EDR carrier frequency stability		–5		5	kHz
EDR initial carrier frequency tolerance[3]		±75		±75	kHz
EDR RMS DEVM	EDR2		4%	15%	
	EDR3		4%	10%	
EDR 99% DEVM	EDR2			30%	
	EDR3			20%	
EDR peak DEVM	EDR2		9%	25%	
	EDR3		9%	18%	

(1) All RF and performance numbers are aligned to the module pin.
(2) Performance values reflect maximum power.
(3) Numbers include XTAL frequency drift over temperature and aging.

7.16 Bluetooth Low Energy Performance: Receiver Characteristics – In-Band Signals

over operating free-air temperature range (unless otherwise noted)

PARAMETER[1]	CONDITION[2]	MIN	TYP	MAX	UNIT
Bluetooth Low Energy operation frequency range		2402		2480	MHz
Bluetooth Low Energy channel spacing			2		MHz
Bluetooth Low Energy input impedance			50		Ω
Bluetooth Low Energy sensitivity[3] Dirty TX on			–92.2		dBm
Bluetooth Low Energy maximum usable input power		–5			dBm
Bluetooth Low Energy intermodulation characteristics	Level of interferers. For n = 3, 4, 5	–36	–30		dBm
Bluetooth Low Energy C/I performance. Note: Numbers show wanted signal-to-interfering-signal ratio. Smaller numbers indicate better C/I performance. Image = –1MHz	Low energy, co-channel			12	dB
	Low energy, adjacent ±1MHz			0	
	Low energy, adjacent +2MHz			–38	
	Low energy, adjacent –2MHz			–15	
	Low energy, adjacent ≥ |±3| MHz			–40	

(1) All RF and performance numbers are aligned to the module pin.
(2) BER of 0.1% corresponds to PER of 30.8% for a minimum of 1500 transmitted packets, according to the Bluetooth Low Energy test specification.
(3) Sensitivity degradation of up to –3dB can occur due to fast clock harmonics.

7.17 Bluetooth Low Energy Performance: Transmitter Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER[1]		MIN	TYP	MAX	UNIT
Bluetooth Low Energy RF output power[2]	V_{BAT} ≥ 3V[3]		7.0		dBm
	V_{BAT} < 3V[3]		7.0		
Bluetooth Low Energy adjacent channel power |M-N| = 2			–51.0		dBm
Bluetooth Low Energy adjacent channel power |M-N| > 2			–54.0		dBm

(1) All RF and performance numbers are aligned to the module pin.
(2) Bluetooth Low Energy power is restricted to comply with the ETSI 10dBm EIRP limit requirement.
(3) VBAT is measured with an on-chip ADC that has an accuracy error of up to 5%.

7.18 Bluetooth Low Energy Performance: Modulation Characteristics

over operating free-air temperature range (unless otherwise noted)

CHARACTERISTICS[1]	CONDITION[2]		MIN	TYP	MAX	UNIT
Bluetooth Low Energy modulation characteristics	Δf1avg	Mod data = 4 1s, 4 0s: 111100001111...	240	250	260	kHz
	Δf2max ≥ limit for at least 99.9% of all Δf2max	Mod data = 1010101...	195	215		
	Δf2avg, Δf1avg		85%	90%		
Bluetooth Low Energy carrier frequency drift	lf0 – fnl , n = 2,3 …. K		–25		25	kHz
Bluetooth Low Energy drift rate	lf1 – f0l and lfn – fn-5l , n = 6,7…. K				15	kHz/50 µs
Bluetooth Low Energy initial carrier frequency tolerance[3]	fn – fTX		±75		±75	kHz

(1) All RF and performance numbers are aligned to the module pin.
(2) Performance values reflect maximum power.
(3) Numbers include XTAL frequency drift over temperature and aging.

7.19 Bluetooth BR and EDR Dynamic Currents

Current is measured at output power as follows: BR at 11.7dBm; EDR at 7.2dBm.

USE CASE[1] [2]	TYP	UNIT
BR voice HV3 + sniff	11.6	mA
EDR voice 2-EV3 no retransmission + sniff	5.9	mA
Sniff 1 attempt 1.28 s	178.0	µA
EDR A2DP EDR2 (master). SBC high quality – 345 kbps	10.4	mA
EDR A2DP EDR2 (master). MP3 high quality – 192 kbps	7.5	mA
Full throughput ACL RX: RX-2DH5[3] [4]	18.0	mA
Full throughput BR ACL TX: TX-DH5[4]	50.0	mA
Full throughput EDR ACL TX: TX-2DH5[4]	33.0	mA
Page scan or inquiry scan (scan interval is 1.28 s or 11.25 ms, respectively)	253.0	µA
Page scan and inquiry scan (scan interval is 1.28 s and 2.56 s, respectively)	332.0	µA

(1) The role of Bluetooth in all scenarios except A2DP is slave.
(2) CL1P5 PA is connected to V_{BAT}, 3.7V.
(3) ACL RX has the same current in all modulations.
(4) Full throughput assumes data transfer in one direction.

7.20 Bluetooth Low Energy Currents

All current measured at output power of 6.5dBm

USE CASE[1]	TYP	UNIT
Advertising, not connectable[2]	131	µA
Advertising, discoverable[2]	143	µA
Scanning[3]	266	µA
Connected, master role, 1.28s connect interval[4]	124	µA
Connected, slave role, 1.28s connect interval [4]	132	µA

(1) CL1p% PA is connected to V_{BAT}, 3.7V.
(2) Advertising in all three channels, 1.28s advertising interval, 15 bytes advertise data
(3) Listening to a single frequency per window, 1.28s scan interval, 11.25ms scan window
(4) Zero slave connection latency, empty TX and RX LL packets

7.21 Timing and Switching Characteristics

7.21.1 Power Management

7.21.1.1 Block Diagram – Internal DC-DCs

The device incorporates three internal DC-DCs (switched-mode power supplies) to provide efficient internal supplies, derived from V_{BAT}.

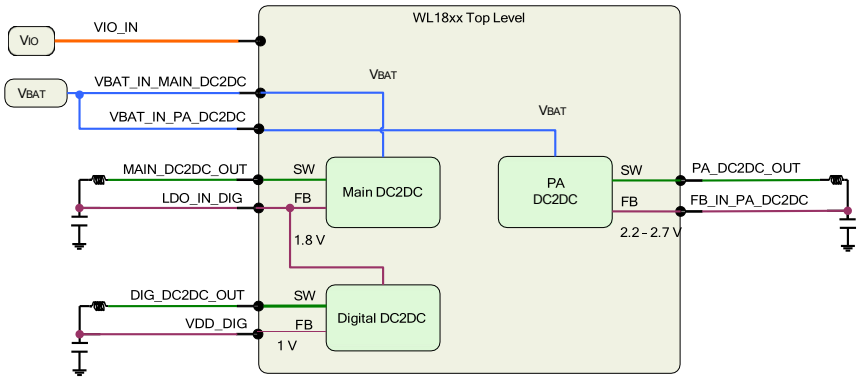


Figure 7-1. Internal DC-DCs

7.21.2 Power-Up and SHUTDOWN States

The correct power-up and shutdown sequences must be followed to avoid damage to the device.

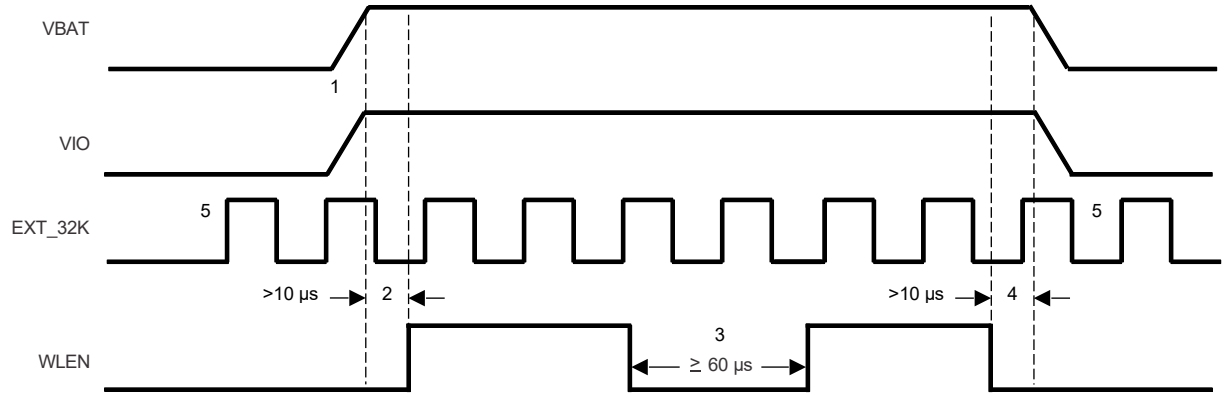
While V_{BAT} or V_{IO} or both are deasserted, no signals should be driven to the device. The only exception is the slow clock that is a failsafe I/O.

While V_{BAT}, V_{IO}, and slow clock are fed to the device, but WL_EN is deasserted (low), the device is in SHUTDOWN state. In SHUTDOWN state all functional blocks, internal DC-DCs, clocks, and LDOs are disabled.

To perform the correct power-up sequence, assert (high) WL_EN. The internal DC-DCs, LDOs, and clock start to ramp and stabilize. Stable slow clock, V_{IO}, and V_{BAT} are prerequisites to the assertion of one of the enable signals.

To perform the correct shut-down sequence, deassert (low) WL_EN while all the supplies to the device (V_{BAT}, V_{IO}, and slow clock) are still stable and available. The supplies to the chip (V_{BAT} and V_{IO}) can be deasserted only after both enable signals are deasserted (low).

Figure 7-2 shows the general power scheme for the module, including the power-down sequence.



NOTE: 1. Either VBAT or VIO can come up first.
2. VBAT and VIO supplies and slow clock (SCLK), must be stable prior to EN being asserted and at all times. When the EN is active.
3. At least 60µs is required between two successive device enables. The device is assumed to be in shutdown state during that period, meaning all enables to the device are LOW for that minimum duration.

4. EN must be deasserted at least 10µs before VBAT or VIO supply can be lowered (order of supply turn off after EN shutdown is immaterial).
5. EXT_32K - Failsafe I/O

Figure 7-2. Power-Up System

7.21.3 Chip Top-level Power-Up Sequence

Figure 7-3 shows the top-level power-up sequence for the chip.

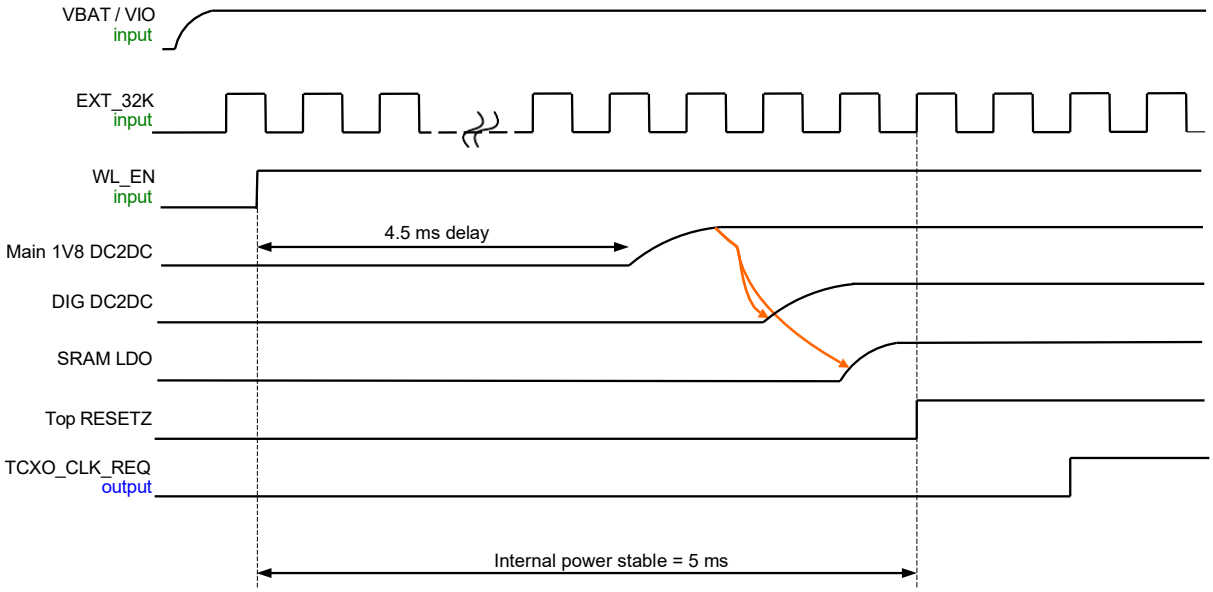


Figure 7-3. Chip Top-Level Power-Up Sequence

7.21.4 WLAN Power-Up Sequence

Figure 7-4 shows the WLAN power-up sequence.

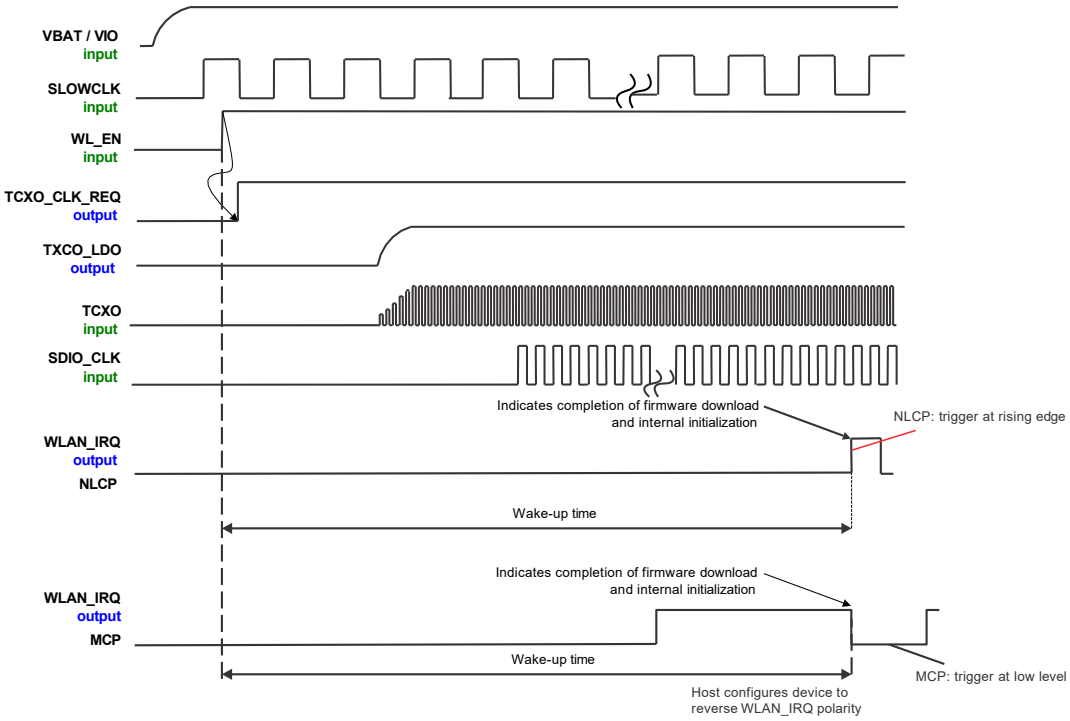


Figure 7-4. WLAN Power-Up Sequence

7.21.5 Bluetooth-Bluetooth Low Energy Power-Up Sequence

Figure 7-5 shows the Bluetooth-Bluetooth Low Energy power-up sequence.

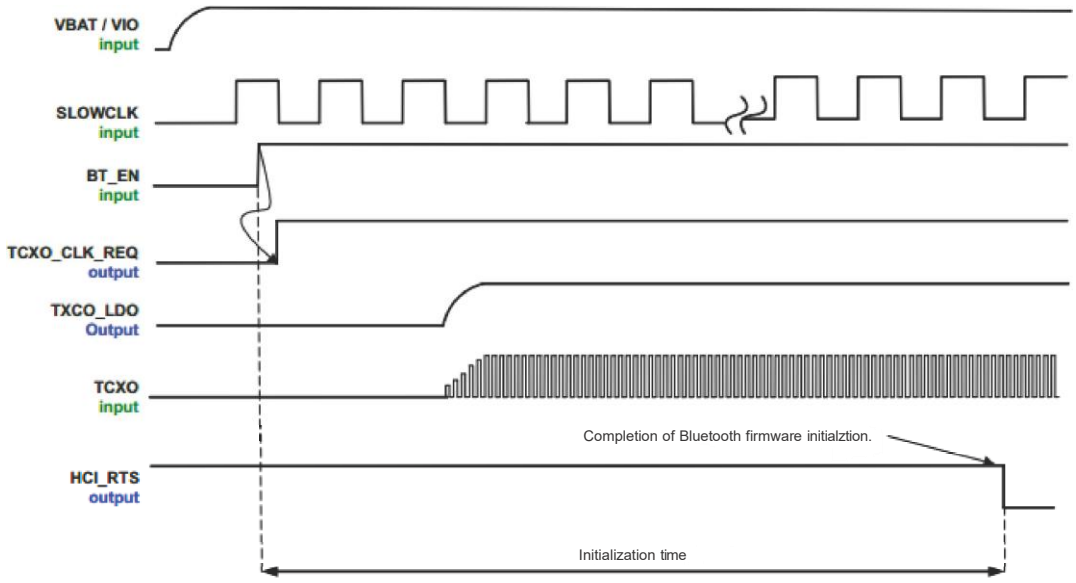


Figure 7-5. Bluetooth-Bluetooth Low Energy Power-Up Sequence

7.21.6 WLAN SDIO Transport Layer

The SDIO is the host interface for WLAN. The interface between the host and the WL18xx module uses an SDIO interface and supports a maximum clock rate of 50 MHz.

The device SDIO also supports the following features of the SDIO V3 specification:

- 4-bit data bus
- Synchronous and asynchronous in-band interrupt
- Default and high-speed (HS, 50 MHz) timing
- Sleep and wake commands

7.21.6.1 SDIO Timing Specifications

Figure 7-6 and Figure 7-7 show the SDIO switching characteristics over recommended operating conditions and with the default rate for input and output.

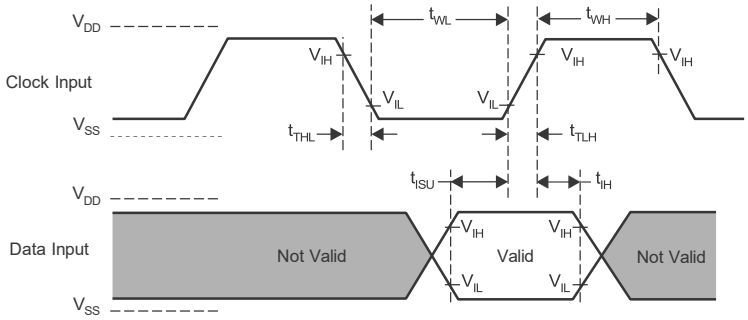


Figure 7-6. SDIO Default Input Timing

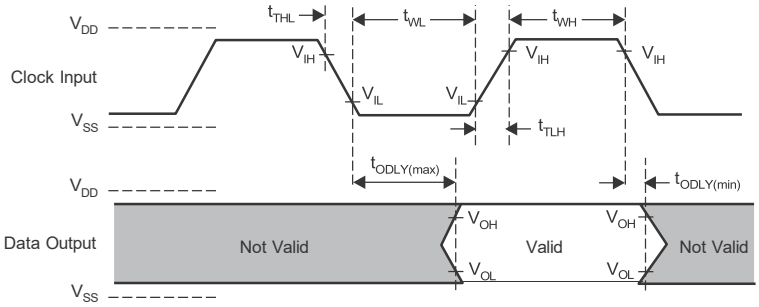


Figure 7-7. SDIO Default Output Timing

Table 7-1 lists the SDIO default timing characteristics.

Table 7-1. SDIO Default Timing Characteristics

(1)		MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK(2)	0.0	26.0	MHz
DC	Low, high duty cycle(2)	40.0%	60.0%	
t_{TLH}	Rise time, CLK(2)		10.0	ns
t_{THL}	Fall time, CLK(2)		10.0	ns
t_{ISU}	Setup time, input valid before CLK ↑(2)	3.0		ns
t_{IH}	Hold time, input valid after CLK ↑(2)	2.0		ns
t_{ODLY}	Delay time, CLK ↓ to output valid(2)	7.0	10.0	ns
C_l	Capacitive load on outputs(2)		15.0	pF

(1) To change the data out clock edge from the falling edge (default) to the rising edge, set the configuration bit.
(2) Parameter values reflect maximum clock frequency.

7.21.6.2 SDIO Switching Characteristics – High Rate

Figure 7-8 and Figure 7-9 show the parameters for maximum clock frequency.

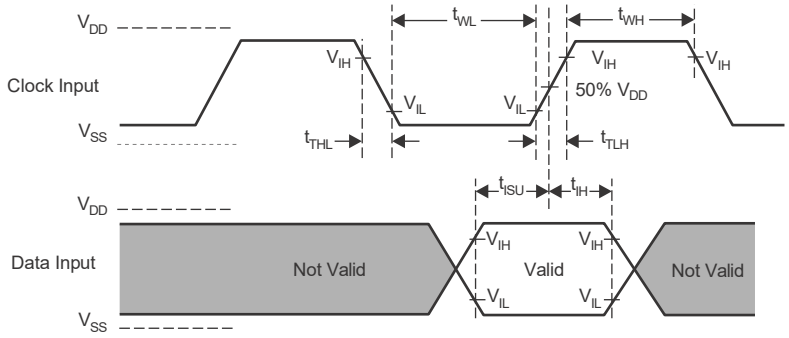


Figure 7-8. SDIO HS Input Timing

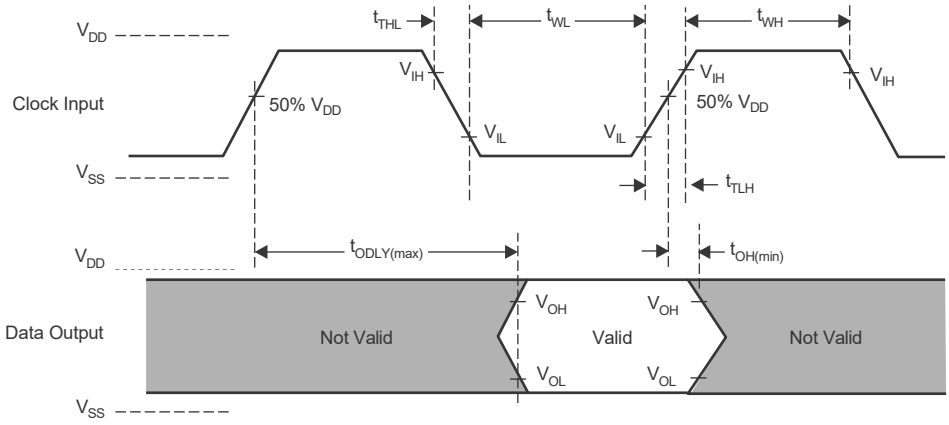


Figure 7-9. SDIO HS Output Timing

Table 7-2 lists the SDIO high-rate timing characteristics.

Table 7-2. SDIO HS Timing Characteristics

		MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK	0.0	52.0	MHz
DC	Low, high duty cycle	40.0%	60.0%	
t_{TLH}	Rise time, CLK		3.0	ns
t_{THL}	Fall time, CLK		3.0	ns
t_{ISU}	Setup time, input valid before CLK ↑	3.0		ns
t_{IH}	Hold time, input valid after CLK ↑	2.0		ns
t_{ODLY}	Delay time, CLK ↑ to output valid	7.0	10.0	ns
C_l	Capacitive load on outputs		10.0	pF

7.21.7 HCI UART Shared-Transport Layers for All Functional Blocks (Except WLAN)

The device includes a UART module dedicated to the Bluetooth shared-transport, host controller interface (HCI) transport layer. The HCI transports commands, events, and ACL between the Bluetooth device and its host using HCI data packets ack as a shared transport for all functional blocks except WLAN. Table 7-3 lists the transport mechanism for WLAN and bluetooth audio.

Table 7-3. Transport Mechanism

WLAN	SHARED HCI FOR ALL FUNCTIONAL BLOCKS EXCEPT WLAN	Bluetooth VOICE-AUDIO
WLAN HS SDIO	Over UART	Bluetooth PCM

The HCI UART supports most baud rates (including all PC rates) for all fast-clock frequencies up to a maximum of 4 Mbps. After power up, the baud rate is set for 115.2 Kbps, regardless of the fast-clock frequency. The baud rate can then be changed using a VS command. The device responds with a Command Complete Event (still at 115.2 Kbps), after which the baud rate change occurs.

HCI hardware includes the following features:

- Receiver detection of break, idle, framing, FIFO overflow, and parity error conditions
- Receiver-transmitter underflow detection
- CTS, RTS hardware flow control
- 4 wire (H4)

Table 7-4 lists the UART default settings.

Table 7-4. UART Default Setting

PARAMETER	VALUE
Bit rate	115.2 Kbps
Data length	8 bits
Stop bit	1
Parity	None

7.21.7.1 UART 4-Wire Interface – H4

The interface includes four signals:

- TXD
- RXD
- CTS
- RTS

Flow control between the host and the device is byte-wise by hardware.

When the UART RX buffer of the device passes the flow-control threshold, the buffer sets the UART_RTS signal high to stop transmission from the host. When the UART_CTS signal is set high, the device stops transmitting on the interface. If HCI_CTS is set high in the middle of transmitting a byte, the device finishes transmitting the byte and stops the transmission.

Figure 7-10 shows the UART timing.

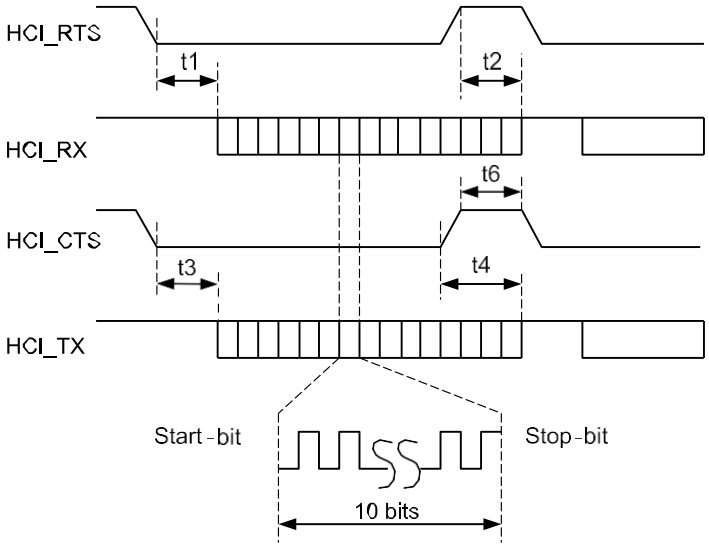


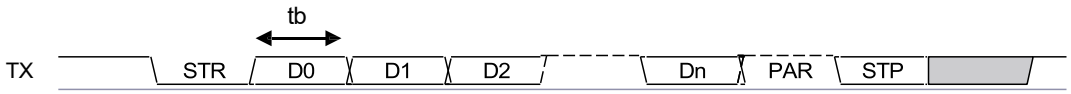
Figure 7-10. UART Timing Diagram

Table 7-5 lists the UART timing characteristics.

Table 7-5. UART Timing Characteristics

PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
	Baud rate		37.5		4364	Kbps
	Baud rate accuracy per byte	Receive-transmit	–2.5%		1.5%	
	Baud rate accuracy per bit	Receive-transmit	–12.5%		12.5%	
t3	CTS low to TX_DATA on		0.0	2.0		µs
t4	CTS high to TX_DATA off	Hardware flow control			1.0	bytes
t6	CTS high pulse duration		1.0			Bit
t1	RTS low to RX_DATA on		0.0	2.0		µs
t2	RTS high to RX_DATA off	Interrupt set to 1/4 FIFO			16.0	bytes

Figure 7-11 shows the UART data frame.



STR-Start-bit; D0..Dn - Data bits (LSB first); PAR - Parity bit (if used); STP - Stop-bit

Figure 7-11. UART Data Frame

7.21.8 Bluetooth Codec-PCM (Audio) Timing Specifications

Figure 7-12 shows the Bluetooth codec-PCM (audio) timing diagram.

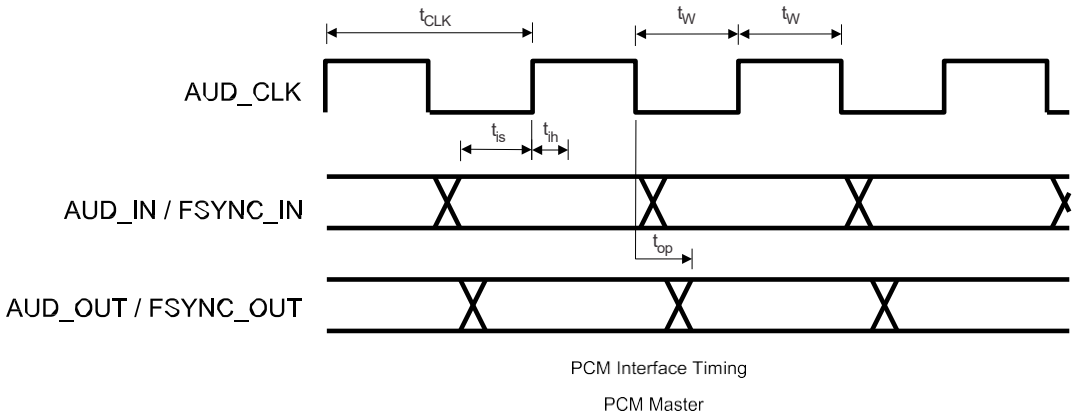


Figure 7-12. Bluetooth Codec-PCM (Audio) Master Timing Diagram

Table 7-6 lists the Bluetooth codec-PCM master timing characteristics.

Table 7-6. Bluetooth Codec-PCM Master Timing Characteristics

PARAMETER		MIN	MAX	UNIT
T_{clk}	Cycle time	162.76 (6.144 MHz)	15625 (64 kHz)	ns
T_w	High or low pulse duration	35% of T_{clk} min		
t_{is}	AUD_IN setup time	10.6		
t_{ih}	AUD_IN hold time	0		
t_{op}	AUD_OUT propagation time	0	15	
t_{op}	FSYNC_OUT propagation time	0	15	
C_l	Capacitive loading on outputs		40	pF

Table 7-7 lists the Bluetooth codec-PCM slave timing characteristics.

Table 7-7. Bluetooth Codec-PCM Slave Timing Characteristics

PARAMETER		MIN	MAX	UNIT
T_{clk}	Cycle time	81.38 (12.288 MHz)		ns
T_w	High or low pulse duration	35% of T_{clk} min		
t_{is}	AUD_IN setup time	5		
t_{ih}	AUD_IN hold time	0		
t_{is}	AUD_FSYNC setup time	5		
t_{ih}	AUD_FSYNC hold time	0		
t_{op}	AUD_OUT propagation time	0	19	
C_l	Capacitive loading on outputs		40	pF

8 Detailed Description

The WL18MODGI module is a self-contained connectivity solution based on WL18MODGIconnectivity. As the eighth- generation connectivity combo chip from TI, the WL18MODGImodule is based on proven technology.

Figure 8-1 shows a high-level view of the WL18MODGI.

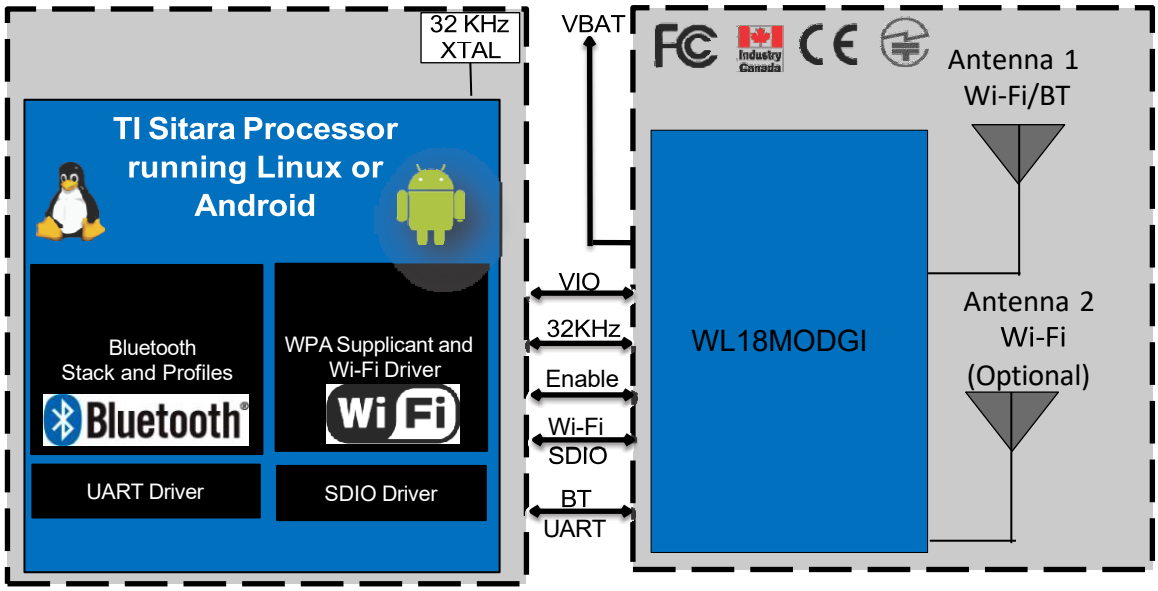


Figure 8-1. WL18MODGI High-Level System Diagram

Table 8-1, Table 8-2, and Table 8-3 list performance parameters along with shutdown and sleep currents.

Table 8-1. WLAN Performance Parameters

WLAN(1)	CONDITIONS	SPECIFICATION (TYP)	UNIT
Maximum TX power, 5GHz (OFDM6)	6Mbps OFDM	18	dBm
Maximum TX power, 2.4GHz (1DSSS)	1Mbps DSSS	16.5	dBm
Minimum sensitivity, 5GHz (OFDM6)	6Mbps OFDM	–92.5	dBm
Minimum sensitivity, 2.4GHz (1DSSS)	1Mbps DSSS	–95	dBm
Sleep current	Leakage, firmware retained	160	µA
Connected IDLE	No traffic IDLE connect	750	µA
RX search	2.4GHz SISO 20	58	mA
RX current (SISO20)	MCS7, 2.4GHz	69	mA
RX current (SISO20)	MCS7, 5GHz	77	mA
TX current (SISO20)	MCS7, 2.4GHz	238	mA
TX current (SISO20)	MCS7, 5GHz	324	mA
Maximum peak current consumption during calibration(2)		850	mA

(1) The system design power scheme must comply with both peak and average TX bursts.
(2) Peak current V_{BAT} can hit 850mA during device calibration.

- At wakeup, the WL18MODGI module performs the entire calibration sequence at the center of the 2.4GHz band.
- After a link is established, calibration is performed periodically (every 5 minutes) on the specific channel tuned.
- The maximum VBAT value is based on peak calibration consumption with a 30% margin.

Table 8-2. Bluetooth Performance Parameters

BLUETOOTH	CONDITIONS	SPECIFICATION (TYP)	UNIT
Maximum TX power	GFSK	11.7	dBm
Minimum sensitivity	GFSK	–92.2	dBm
Sniff	1 attempt, 1.28s (+4dBm)	178	µA
Page or inquiry	1.28s interrupt, 11.25ms scan window (+4dBm)	253	µA
A2DP	MP3 high quality 192kbps (+4dBm)	7.5	mA

Table 8-3. Shutdown and Sleep Currents

PARAMETER	POWER SUPPLY CURRENT	TYP	UNIT
Shutdown mode All functions shut down	VBAT	10	µA
	VIO	2	
WLAN sleep mode	VBAT	160	µA
	VIO	60	
Bluetooth sleep mode	VBAT	110	µA
	VIO	60	

8.1 WLAN Features

The device supports the following WLAN features:

- Integrated 2.4GHz power amplifiers (PAs) for a complete WLAN solution
- Baseband processor: IEEE Std 802.11a, 802.11b/g, and IEEE Std 802.11n data rates with 20MHz or 40MHz SISO and 20MHz MIMO
- Fully calibrated system (production calibration not required)
- Medium access controller (MAC)
  - Embedded Arm® central processing unit (CPU)
  - Hardware-based encryption-decryption using 64-, 128-, and 256-bit WEP, TKIP, or AES keys
  - Requirements for Wi-Fi-protected access (WPA and WPA2.0) and IEEE Std 802.11i (includes hardware-accelerated Advanced Encryption Standard [AES])
- New advanced coexistence scheme with Bluetooth and Bluetooth Low Energy wireless technology
- 2.4GHz and 5GHz radio
  - Internal LNA and PA
  - IEEE Std 802.11a, 802.11b, 802.11g, and 802.11n
- 4-bit SDIO host interface, including high speed (HS) and V3 modes

8.2 Bluetooth Features

The device supports the following Bluetooth features:

- Bluetooth 5.1 secure connection as well as CSA2
- Concurrent operation and built-in coexisting and prioritization handling of Bluetooth and Bluetooth Low Energy wireless technology, audio processing, and WLAN
- Dedicated audio processor supporting on-chip SBC encoding + A2DP
  - Assisted A2DP (A3DP): SBC encoding implemented internally
  - Assisted WB-speech (AWBS): modified SBC codec implemented internally

8.3 Bluetooth Low Energy Features

The device supports the following Bluetooth Low Energy features:

- Bluetooth 5.1 low-energy dual-mode standard
- All roles and role combinations, mandatory as well as optional
- Up to 10 low-energy connections
- Independent low energy buffering allowing multiple connections with no effect on BR-EDR performance

8.4 Device Certification

The WL18MODGI module from DCI is certified for FCC and IC. Customers who build products based on the WL18MODGI device can save on testing costs and time per product family. Table 8-4 shows the certification list for the WL18MODGI module.

Table 8-4. Device Certification

REGULATORY BODY	SPECIFICATION	ID (IF APPLICABLE)
FCC (USA)	Part 15C + MPE FCC RF exposure	KKG-WL18DBMOD
ISED (Canada)	RSS-102 (MPE) and RSS-247 (Wi-Fi, Bluetooth)	2213A-WL18DBMOD

8.4.1 FCC Certification and Statement

The WL18MODGI module is certified for the FCC as a single-modular transmitter. The module is an FCC-certified radio module that carries a modular grant. Users are cautioned that changes or modifications not expressly approved by the party responsible for compliance could void the authority of the user to operate the equipment.

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference.
- This device must accept any interference received, including interference that may cause undesired operation of the device.

CAUTION

FCC RF Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions to satisfy RF exposure limits. This transmitter must not be colocated or operate with any other antenna or transmitter.

8.4.2 Innovation, Science, and Economic Development Canada (ISED)

The WL18MODGI module is certified for IC as a single-modular transmitter. The WL18MODGI module meets IC modular approval and labeling requirements. The IC follows the same testing and rules as the FCC regarding certified modules in authorized equipment. This device complies with Industry Canada licence-exempt RSS standards.

Operation is subject to the following two conditions:

- This device may not cause interference.
- This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence.

L'exploitation est autorisée aux deux conditions suivantes:

- L'appareil ne doit pas produire de brouillage.
- L'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

CAUTION

IC RF Radiation Exposure Statement:

To comply with IC RF exposure requirements, this device and its antenna must not be colocated or operating in conjunction with any other antenna or transmitter.

Pour se conformer aux exigences de conformité RF canadienne l'exposition, cet appareil et son antenne ne doivent pas étre co-localisés ou fonctionnant en conjonction avec une autre antenne or transmitter.

8.5 Module Markings

Figure 8-2 shows the markings for the WL18MODGI module.

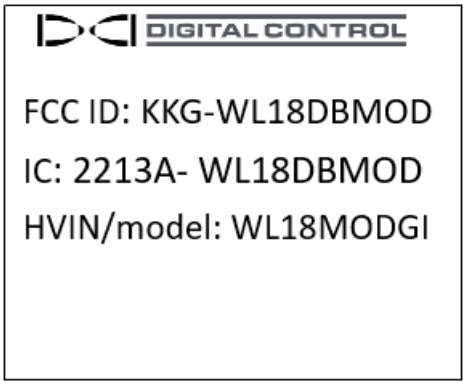


Figure 8-2. WL18MODGIModule Markings

Table 8-5 describes the WL18MODGImodule markings.

Table 8-5. Description of WL18MODGIModule Markings

MARKING	DESCRIPTION
WL18MODGI	Model/HVIN
&7	Test grade (for more information, see Section 8.6)
KKG-WL18DBMOD	FCC ID: single modular FCC grant ID
2213A-WL18DBMOD	IC: single modular IC grant ID

8.1 End Product Labeling

This module is designed to comply with the FCC single modular FCC grant, FCC ID: KKG-WL18DBMOD. The host system using this module must display a visible label indicating the following text:

Contains FCC ID: KKG-WL18DBMOD

These modules are designed to comply with the IC single modular FCC grant, IC: 2213A-WL18DBMOD. The host system using this module must display a visible label indicating the following text:

Contains IC: 2213A-WL18DBMOD

8.2 Manual Information to the End User

The OEM integrator must be aware of not providing information to the end user regarding how to install or remove this RF module in the user's manual of the end product that integrates this module. The end user's manual must include all required regulatory information and warnings as shown in this manual.

9 Applications, Implementation, and Layout

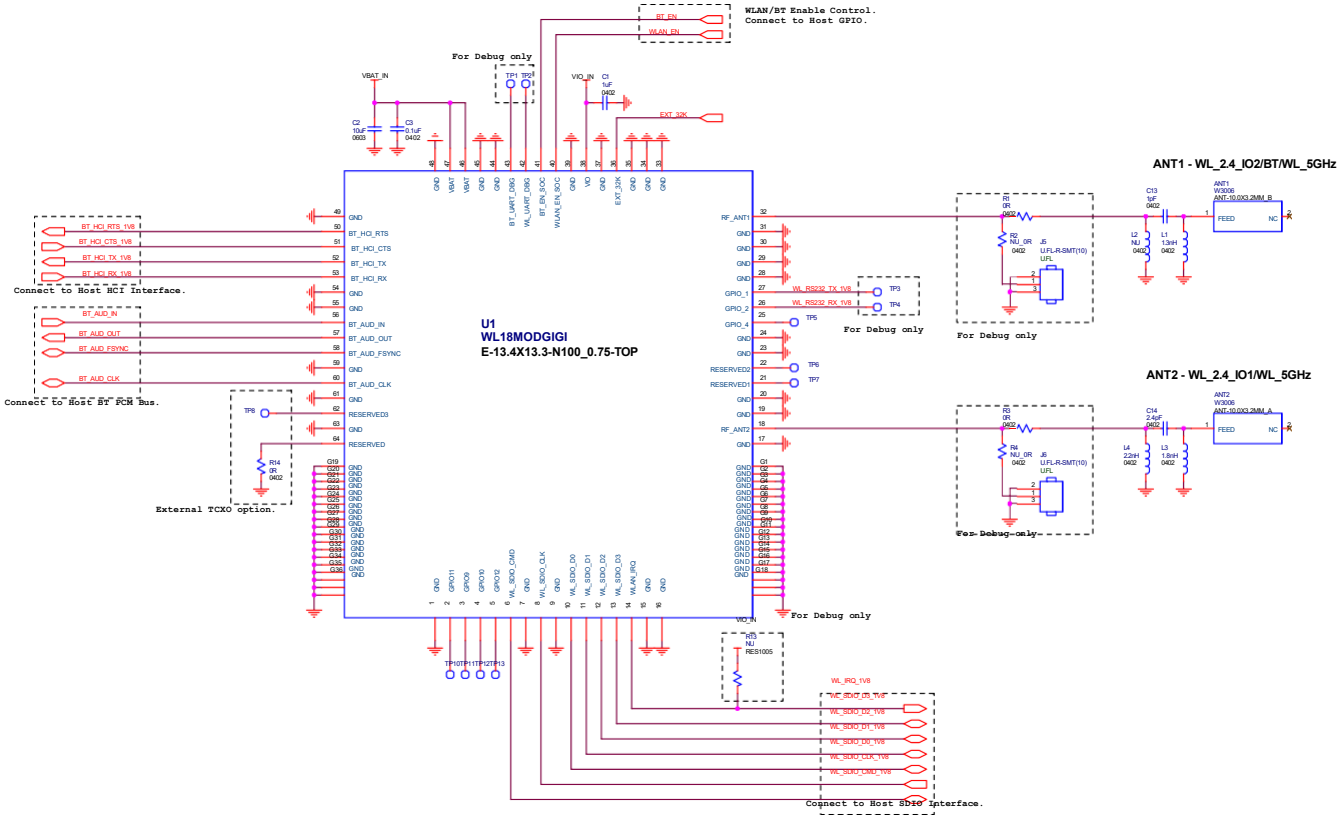
Note

Customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Typical Application – WL18MODGI Reference Design

Figure 9-1 shows the WL18MODGI reference design.



Module Reference Schematics

Table 9-1 lists the bill materials (BOM).

Table 9-1. Bill of Materials

ITEM	DESCRIPTION	PART NO.	PACKAGE	REFERENCE	QTY	MFR
1	WL1837 Wi-Fi / Bluetooth module	WL18MODGI	13.4 × 13.3 × 2.0 mm	U1	1	TI
2	XOSC 3225 / 32.768 kHz / 1.8 V / ±50 ppm	7XZ3200005	3.2 × 2.5 × 1.0 mm	OSC1	1	TXC
3	ANT / Chip / 2.4 GHz and 5 GHz(1)	W3006	10.0 × 3.2 × 1.5 mm	ANT1, ANT2	2	Pulse
4	Mini-RF header receptacle	U.FL-R-SMT-1 (10)	3.0 × 2.6 × 1.25 mm	J5, J6	2	Hirose
5	Inductor 0402 / 1.3 nH / ±0.1 nH / SMD	LQP15MN1N3B02	0402	L1	1	Murata
6	Inductor 0402 / 1.8 nH / ±0.1 nH / SMD	LQP15MN1N8B02	0402	L3	1	Murata
7	Inductor 0402 / 2.2 nH / ±0.1 nH / SMD	LQP15MN2N2B02	0402	L4	1	Murata
8	Capacitor 0402 / 1 pF/ 50 V / C0G / ±0.1 pF	GJM1555C1H1R0BB01	0402	C13	1	Murata
9	Capacitor 0402 / 2.4 pF / 50 V / C0G / ±0.1 pF	GJM1555C1H2R4BB01	0402	C14	1	Murata
10	Capacitor 0402 / 0.1 µF / 10 V / X7R / ±10%	0402B104K100CT	0402	C3	1	Walsin
11	Capacitor 0402 / 1 µF / 6.3 V / X5R / ±10%/HF	GRM155R60J105KE19D	0402	C1	1	Murata
12	Capacitor 0603 / 10 µF / 6.3 V / X5R / ±20%	C1608X5R0J106M	0603	C2	1	TDK
13	Resistor 0402 / 0R / ±5%	WR04X000 PTL	0402	R1, R3	2	Walsin

(1) For more information, see the Pulse Electronics W3006 product page.

9.1.2 Design Recommendations

This section describes the layout recommendations for the WL18MODGI module, RF trace, and antenna.

Table 9-2 summarizes the layout recommendations.

Table 9-2. Layout Recommendations Summary

ITEM	DESCRIPTION
Thermal	
1	The proximity of ground vias must be close to the pad.
2	Signal traces must not be run underneath the module on the layer where the module is mounted.
3	Have a complete ground pour in layer 2 for thermal dissipation.
4	Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.
5	Increase the ground pour in the first layer and have all of the traces from the first layer on the inner layers, if possible.
6	Signal traces can be run on a third layer under the solid ground layer, which is below the module mounting layer.
RF Trace and Antenna Routing	
7	The RF trace antenna feed must be as short as possible beyond the ground reference. At this point, the trace starts to radiate.
8	The RF trace bends must be gradual with an approximate maximum bend of 45° with trace mitered. RF traces must not have sharp corners.
9	RF traces must have via stitching on the ground plane beside the RF trace on both sides.
10	RF traces must have constant impedance (microstrip transmission line).
11	For best results, the RF trace ground layer must be the ground layer immediately below the RF trace. The ground layer must be solid.
12	There must be no traces or ground under the antenna section.
13	RF traces must be as short as possible. The antenna, RF traces, and modules must be on the edge of the PCB product. The proximity of the antenna to the enclosure and the enclosure material must also be considered.

Table 9-2. Layout Recommendations Summary (continued)

ITEM	DESCRIPTION
Supply and Interface	
14	The power trace for V_{BAT} must be at least 40-mil wide.
15	The 1.8-V trace must be at least 18-mil wide.
16	Make VBAT traces as wide as possible to ensure reduced inductance and trace resistance.
17	If possible, shield V_{BAT} traces with ground above, below, and beside the traces.
18	SDIO signals traces (CLK, CMD, D0, D1, D2, and D3) must be routed in parallel to each other and as short as possible (less than 12 cm). In addition, every trace length must be the same as the others. There should be enough space between traces – greater than 1.5 times the trace width or ground – to ensure signal quality, especially for the SDIO_CLK trace. Remember to keep these traces away from the other digital or analog signal traces. TI recommends adding ground shielding around these buses.
19	SDIO and digital clock signals are a source of noise. Keep the traces of these signals as short as possible. If possible, maintain a clearance around them.

9.1.3 RF Trace and Antenna Layout Recommendations

Follow these RF trace routing recommendations:

- RF traces must have 50Ω impedance.
- RF traces must not have sharp corners.
- RF traces must have via stitching on the ground plane beside the RF trace on both sides.
- RF traces must be as short as possible. The antenna, RF traces, and module must be on the edge of the PCB product in considering the product enclosure material and proximity.

9.1.4 Module Layout Recommendations

Figure 9-3 and Figure 9-4 show layer 1 and layer 2 of the module layout.

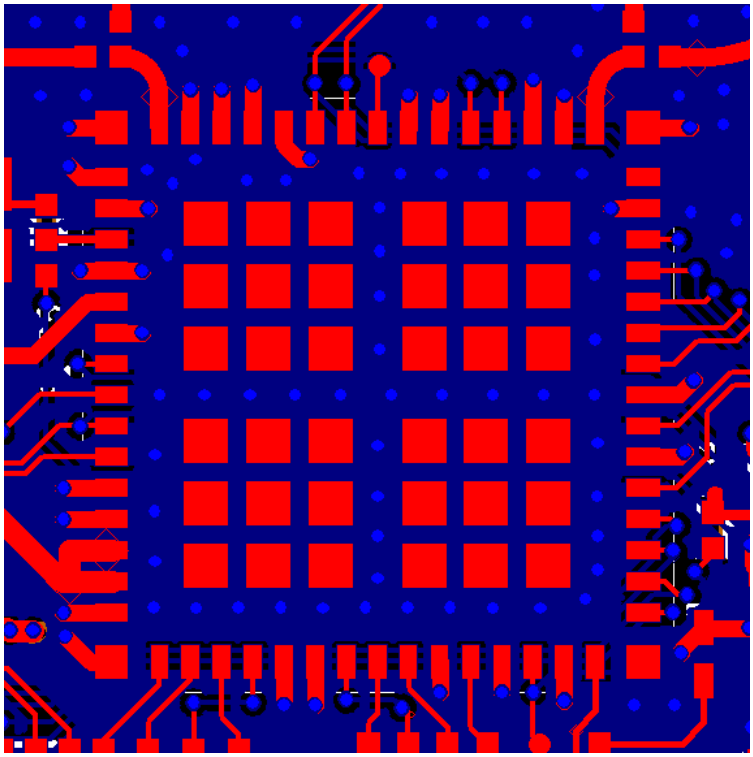


Figure 9-3. Module Layout: Layer 1

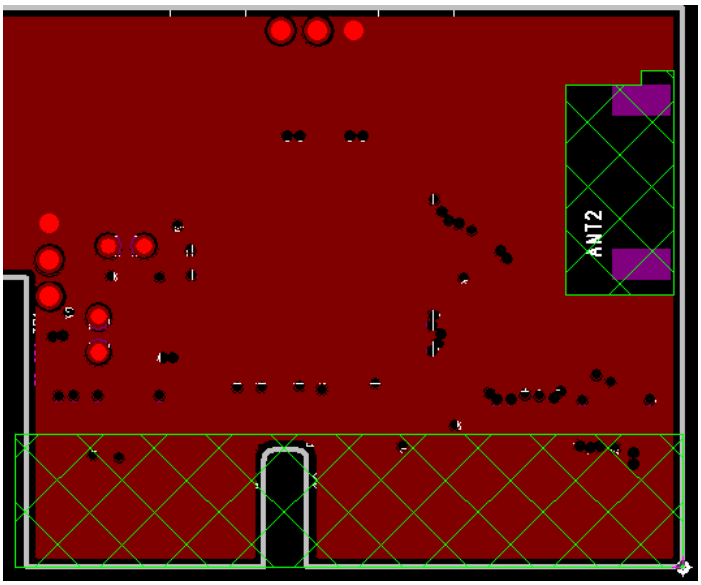


Figure 9-4. Module Layout: Layer 2 (Solid GND)

Follow these module layout recommendations:

- Ensure a solid ground plane and ground vias under the module for a stable system and thermal dissipation.
- Do not run signal traces under the module on a layer where the module is mounted.
- Signal traces can be run on a third layer under the solid ground layer and beneath the module mounting.
- Run the host interfaces with ground on the adjacent layer to improve the return path.
- TI recommends routing the signals as short as possible to the host.

9.1.5 Thermal Board Recommendations

The module uses µvias for layers 1 through 6 with full copper filling, providing heat flow all the way to the module ground pads.

DCI recommends using one big ground pad under the module with vias all the way to connect the pad to all ground layers (see Figure 9-5).

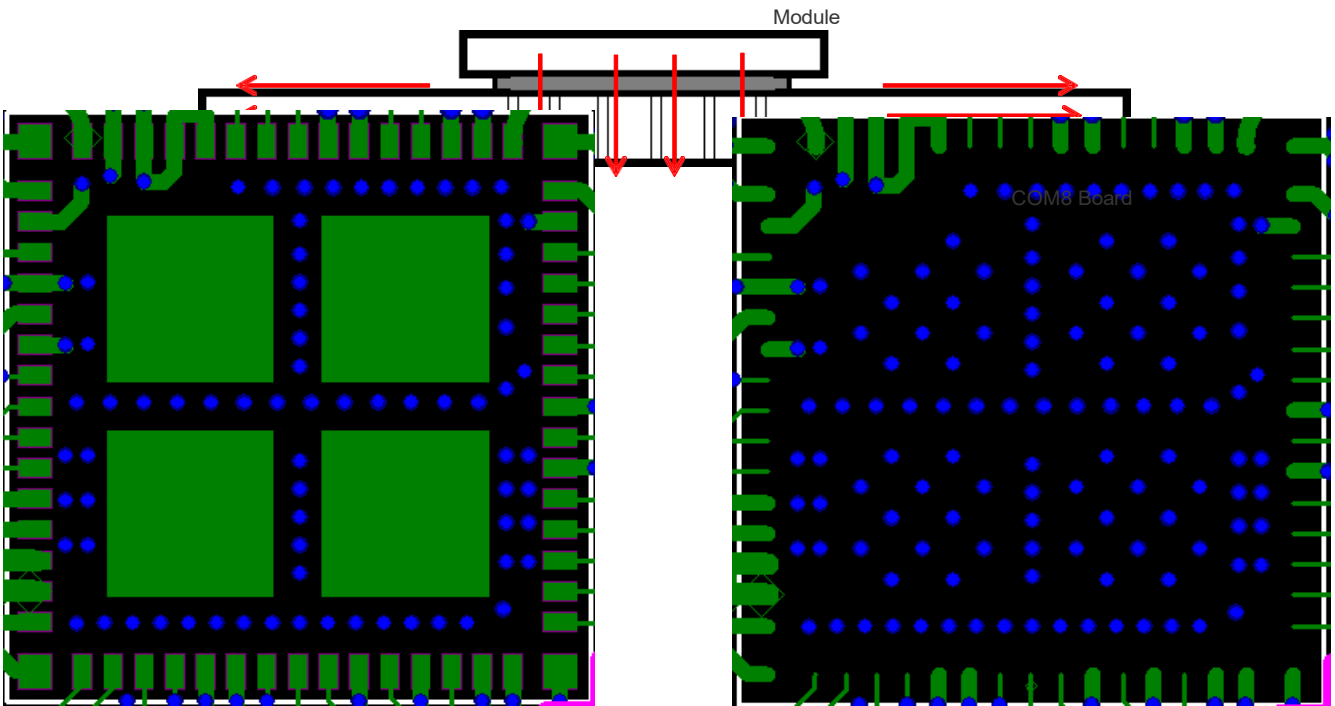


Figure 9-5. Block of Ground Pads on Bottom Side of Package

Figure 9-6 shows via array patterns, which are applied wherever possible to connect all of the layers to the module central or main ground pads.

Figure 9-6. Via Array Patterns

9.1.6 Baking and SMT Recommendations

9.1.6.1 Baking Recommendations

Follow these baking guidelines for the WL18MODGI module:

- Follow MSL level 3 to perform the baking process.
- After the bag is open, devices subjected to reflow solder or other high-temperature processes must be mounted within 168 hours of factory conditions (< 30°C/60% RH) or stored at <10% RH.
- If the humidity indicator card reads >10%, devices require baking before they are mounted.
- If baking is required, bake devices for 8 hours at 125°C.

9.1.6.2 SMT Recommendations

Figure 9-7 shows the recommended reflow profile for the WL18MODGI module.

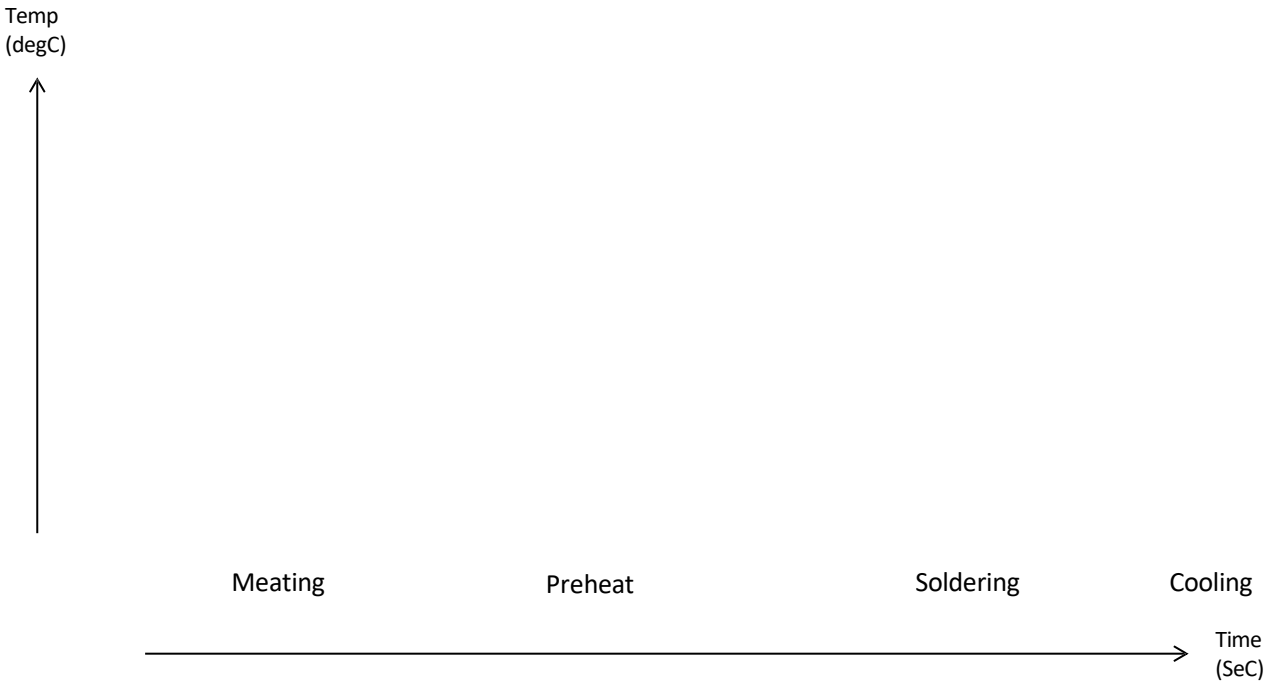


Figure 9-7. Reflow Profile for the WL18MODGI Module

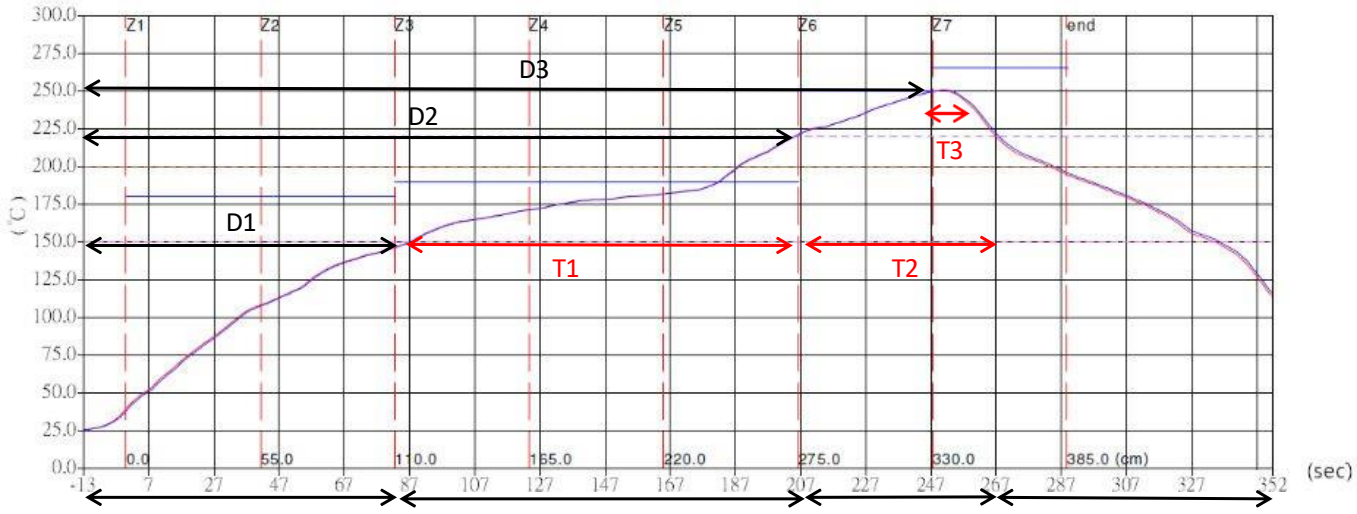
Table 9-3 lists the temperature values for the profile shown in Figure 9-7.

Table 9-3. Temperature Values for Reflow Profile

ITEM	TEMPERATURE (°C)	TIME (s)
Preheat	D1 to approximately D2: 140 to 200	T1: 80 to approximately 120
Soldering	D2: 220	T2: 60 ±10
Peak temperature	D3: 250 maximum	T3: 10

Note

DCI does not recommend the use of conformal coating or similar material on the WL18MODGI module. This coating can lead to localized stress on the WCSP solder connections inside the module and impact the device reliability. Care should be taken during module assembly process to the final PCB to avoid the presence of foreign material inside the module.



10 Mechanical, Packaging, and Orderable Information

10.1 Module Mechanical Outline

Figure 12-1 shows the mechanical outline for the device.

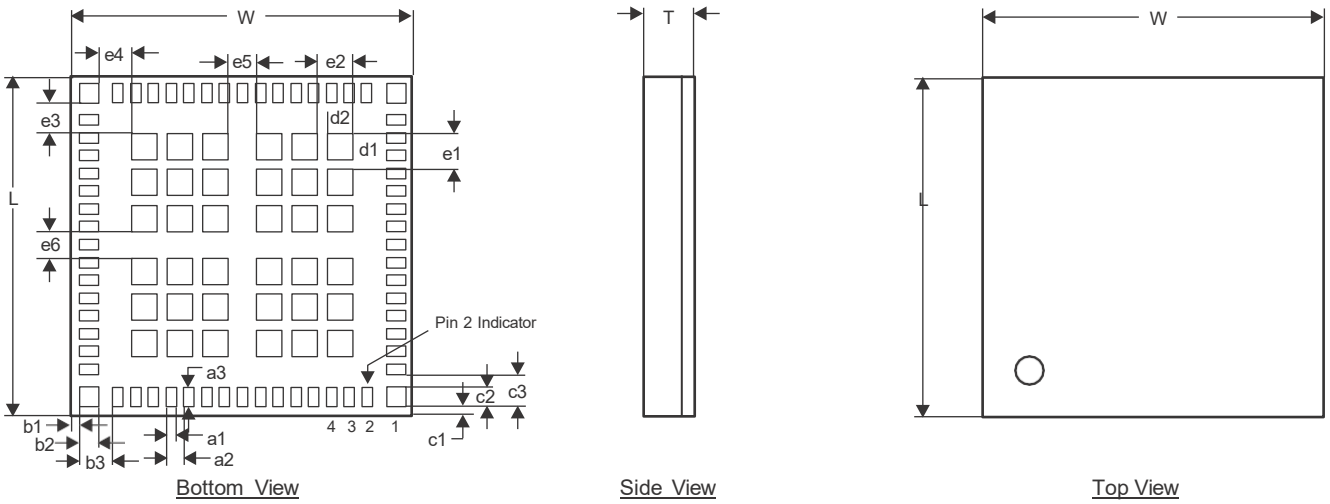


Figure 12-1. Module Mechanical Outline

Table 12-1 lists the dimensions for the mechanical outline of the device.

Note

The module weighs 0.684 g typical.

Table 12-1. Dimensions for Module Mechanical Outline

MARKING	MIN (mm)	NOM (mm)	MAX (mm)	MARKING	MIN (mm)	NOM (mm)	MAX (mm)
L (body size)	13.20	13.30	13.40	c2	0.65	0.75	0.85
W (body size)	13.30	13.40	13.50	c3	1.15	1.25	1.35
T (thickness)	1.80	1.90	2.00	d1	0.90	1.00	1.10
a1	0.30	0.40	0.50	d2	0.90	1.00	1.10
a2	0.60	0.70	0.80	e1	1.30	1.40	1.50
a3	0.65	0.75	0.85	e2	1.30	1.40	1.50
b1	0.20	0.30	0.40	e3	1.15	1.25	1.35
b2	0.65	0.75	0.85	e4	1.20	1.30	1.40
b3	1.20	1.30	1.40	e5	1.00	1.10	1.20
c1	0.20	0.30	0.40	e6	1.00	1.10	1.20

10.2 Tape and Reel Information

Emboss taping specification for MOC 100 pin.

10.2.1 Tape and Reel Specification

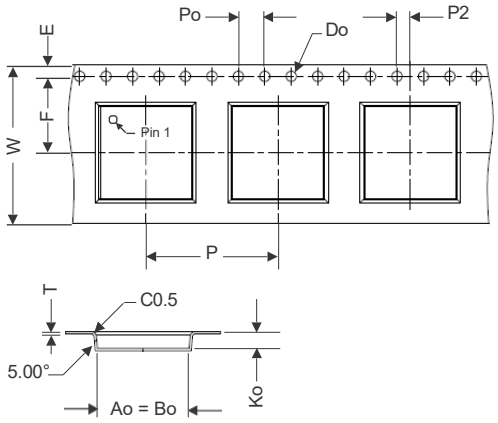


Figure 12-2. Tape Specification

Table 12-2. Dimensions for Tape Specification

ITEM	W	E	F	P	Po	P2	Do	T	Ao	Bo	Ko
DIMENSION (mm)	24.00 (±0.30)	1.75 (±0.10)	11.50 (±0.10)	20.00 (±0.10)	4.00 (±0.10)	2.00 (±0.10)	2.00 (±0.10)	0.35 (±0.05)	13.80 (±0.10)	13.80 (±0.10)	2.50 (±0.10)

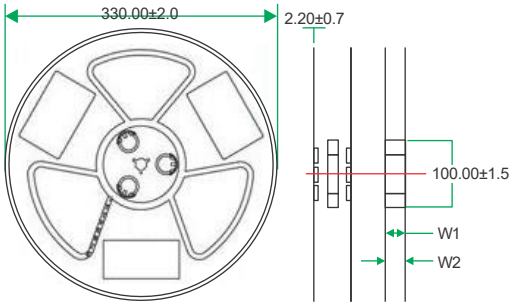


Figure 12-3. Reel Specification

Table 12-3. Dimensions for Reel Specification

ITEM	W1	W2
DIMENSION (mm)	24.4 (+1.5, –0.5)	30.4 (maximum)

10.2.2 Packing Specification

10.2.2.1 Reel Box

The reel is packed in a moisture barrier bag fastened by heat-sealing. Each moisture-barrier bag is packed into a reel box, as shown in Figure 12-4.

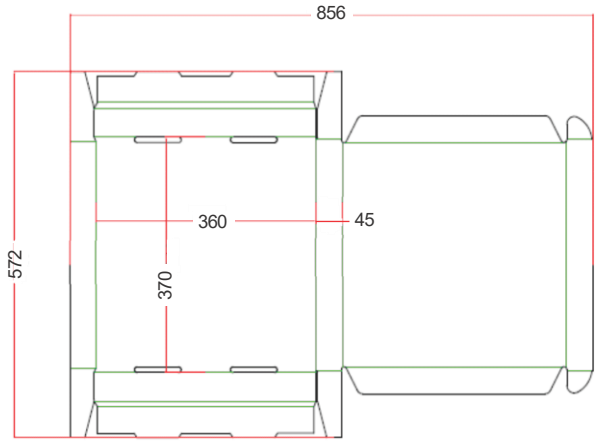


Figure 12-4. Reel Box

The reel box is made of corrugated fiberboard.

10.2.2.2 Shipping Box

Figure 12-5 shows a typical shipping box. If the shipping box has excess space, filler (such as cushion) is added.

Note

The size of the shipping box may vary depending on the number of reel boxes packed.

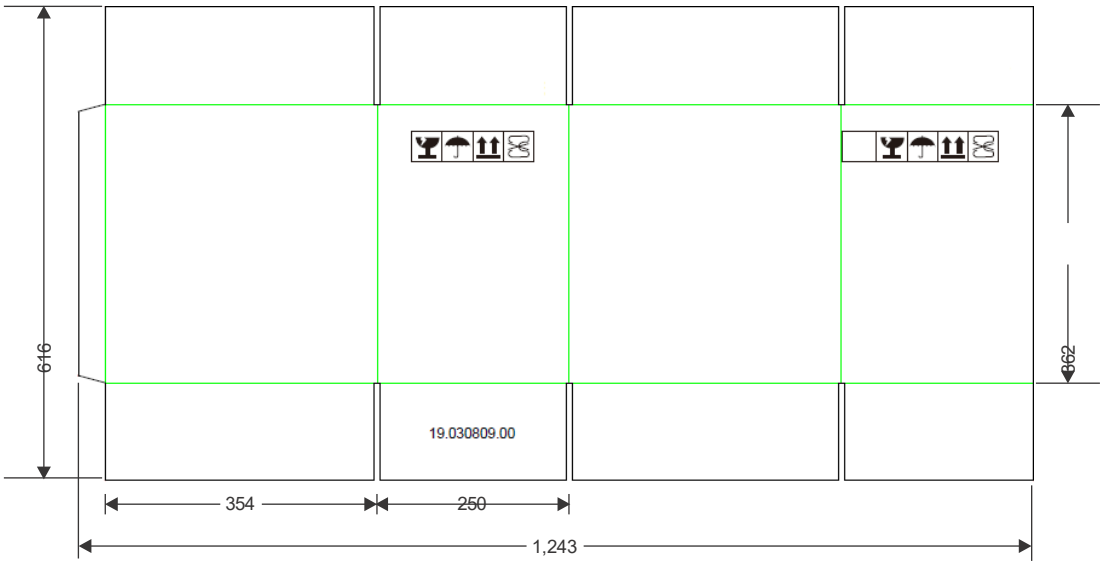
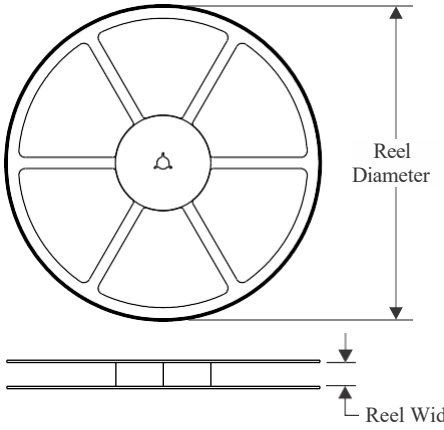


Figure 12-5. Shipping Box

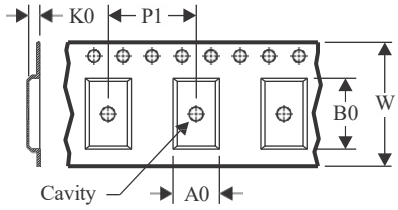
The shipping box is made of corrugated fiberboard.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

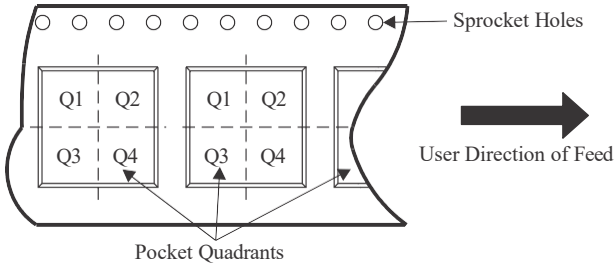


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

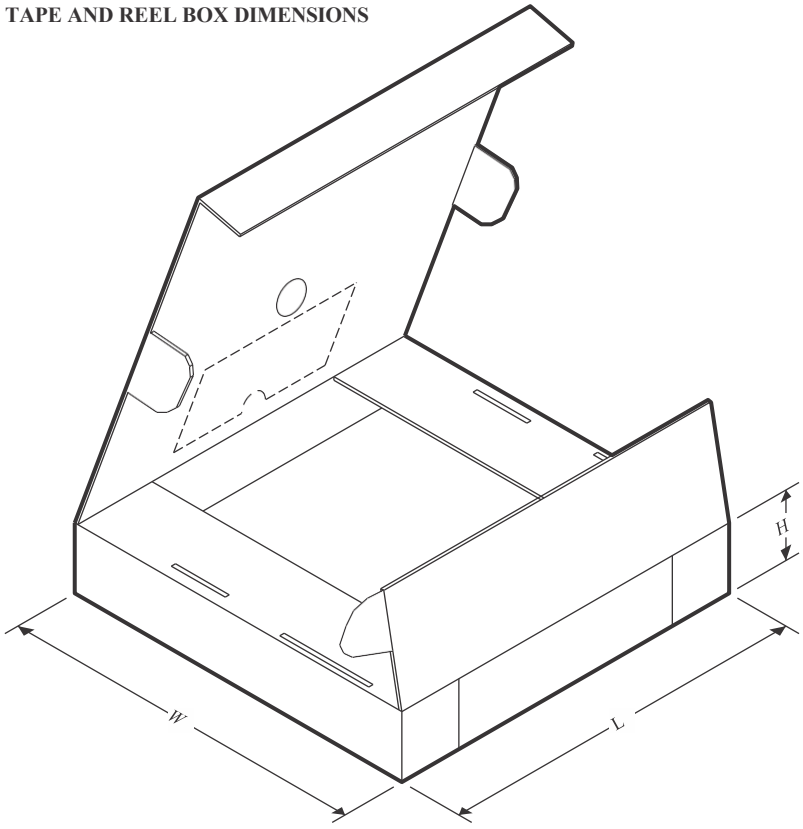
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
WL1807MODGIMOCR	QFM	MOC	100	1200	330.0	24.4	13.8	13.8	2.5	20.0	24.0	Q1
WL1807MODGIMOCT	QFM	MOC	100	250	330.0	24.4	13.8	13.8	2.5	20.0	24.0	Q1
WL18MODGIGIMOCR	QFM	MOC	100	1200	330.0	24.4	13.8	13.8	2.5	20.0	24.0	Q1
WL18MODGIGIMOCT	QFM	MOC	100	250	330.0	24.4	13.8	13.8	2.5	20.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



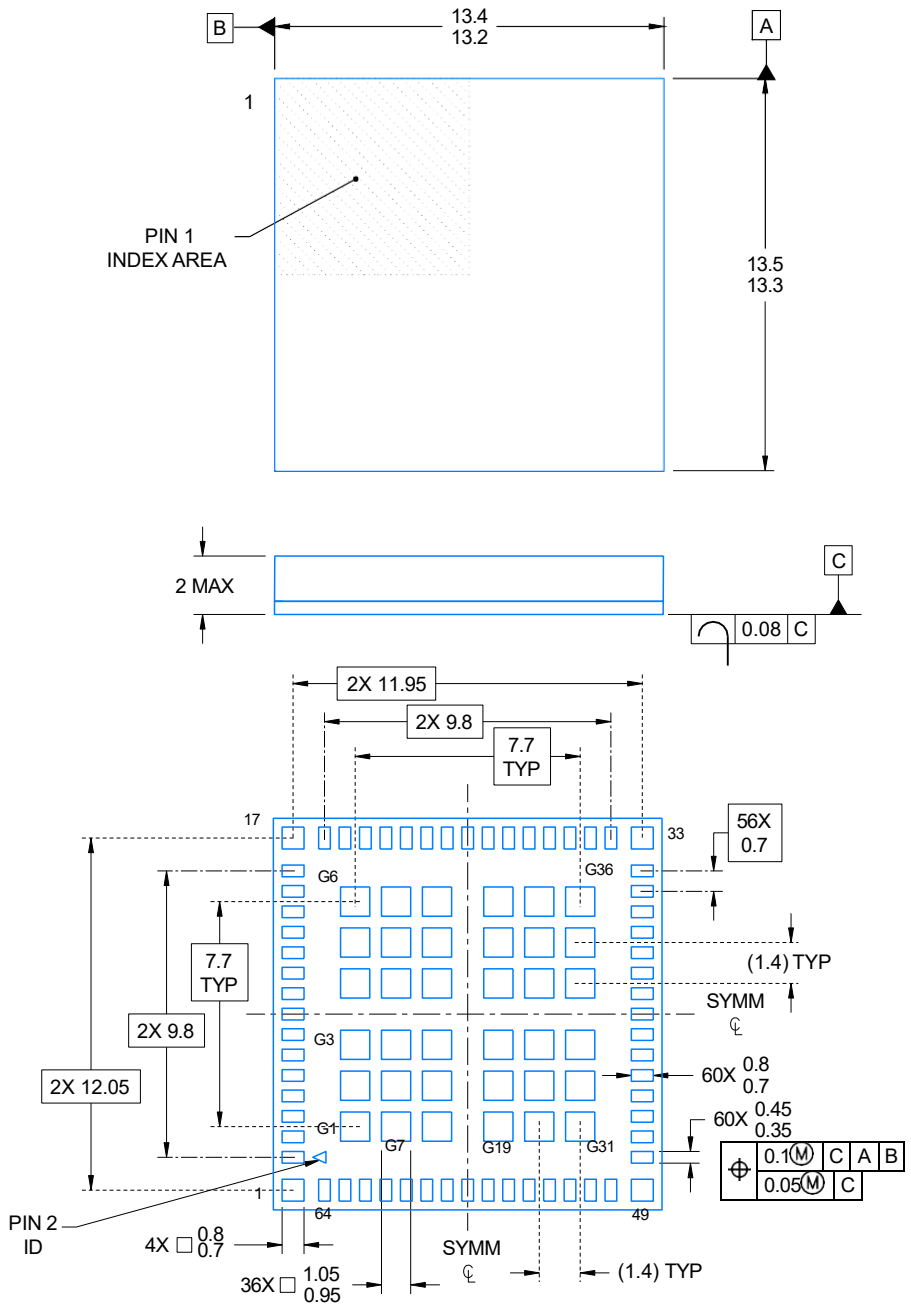
*All dimensions are nominal

PACKAGE OUTLINE

MOC0100A

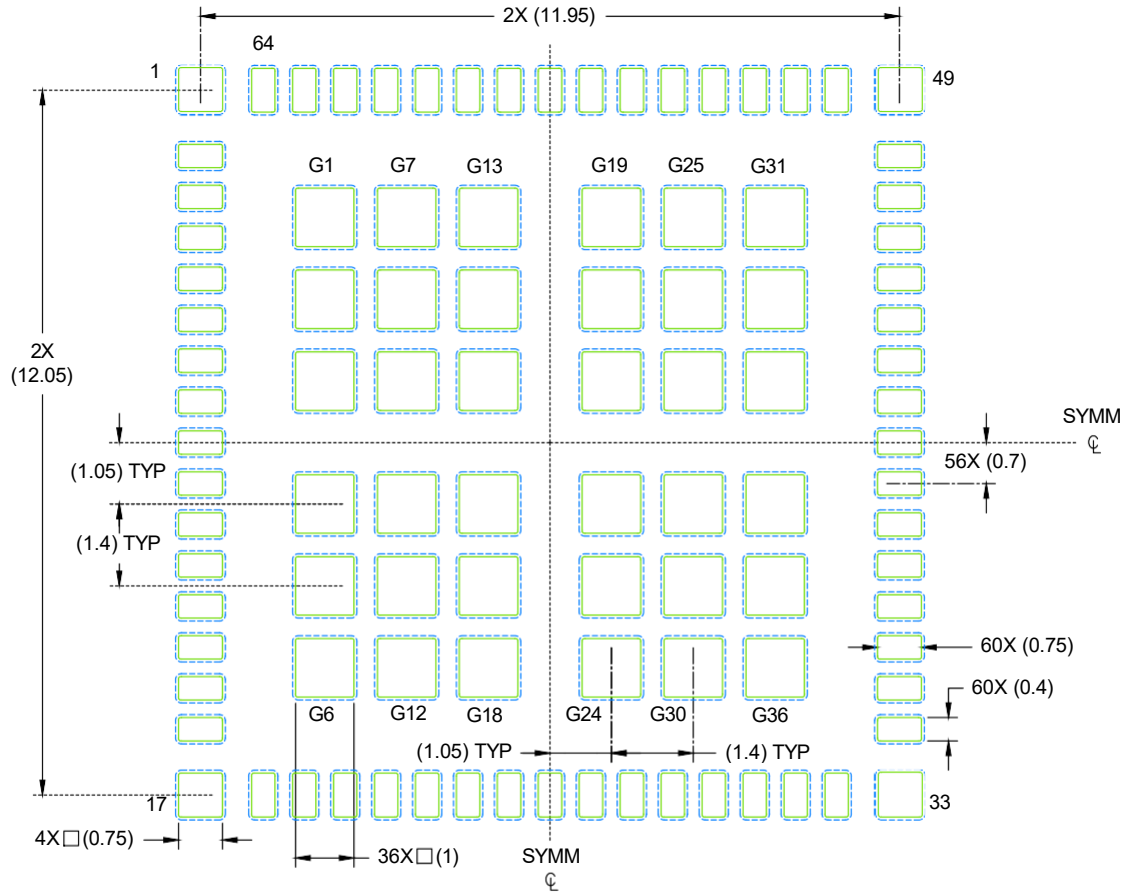
QFM - 2.0 mm max height

QUAD FLAT MODULE



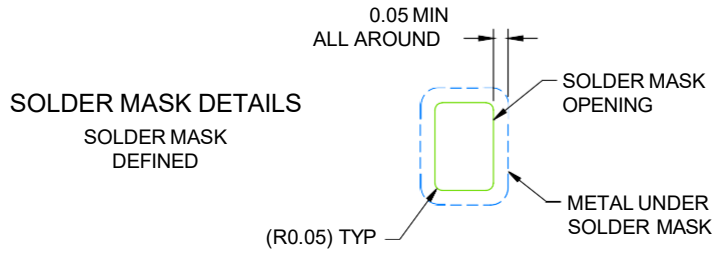
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 8X



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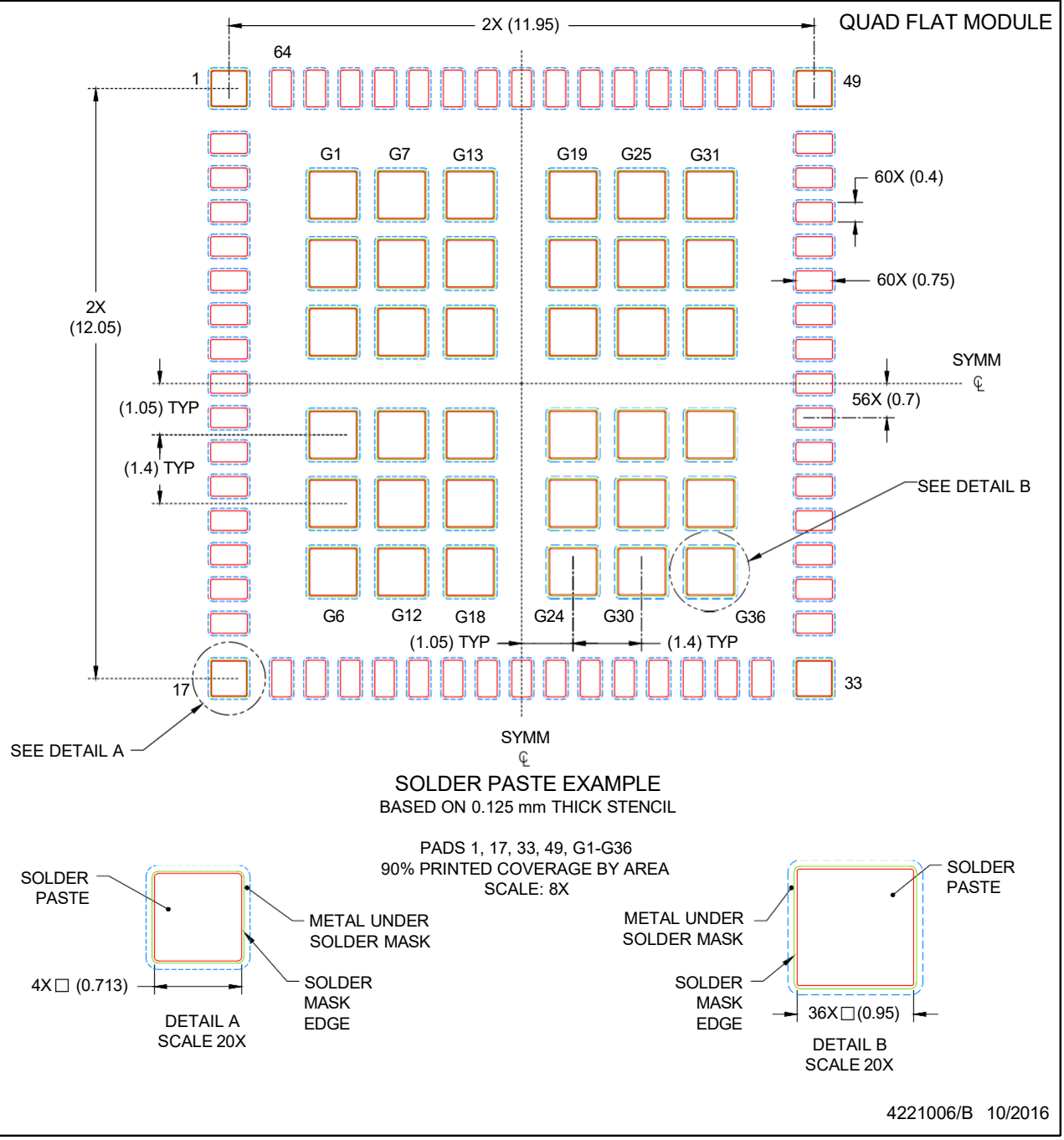
NOTES: (continued)

4. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..