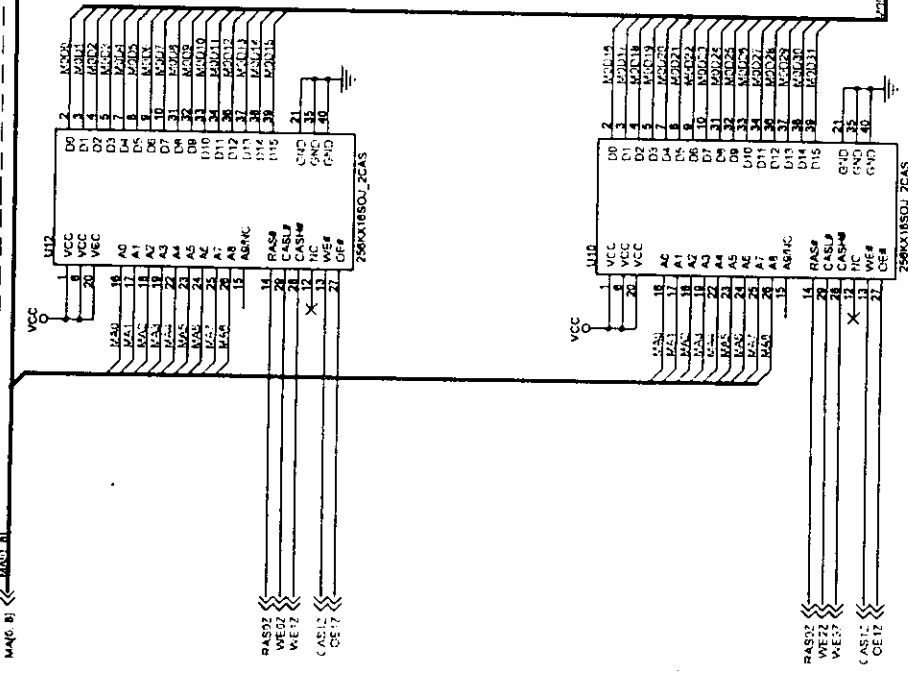
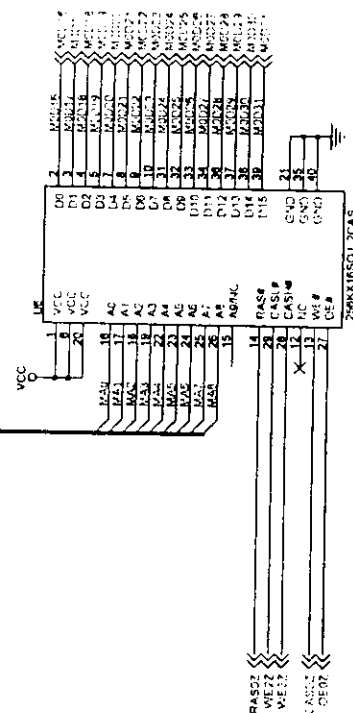
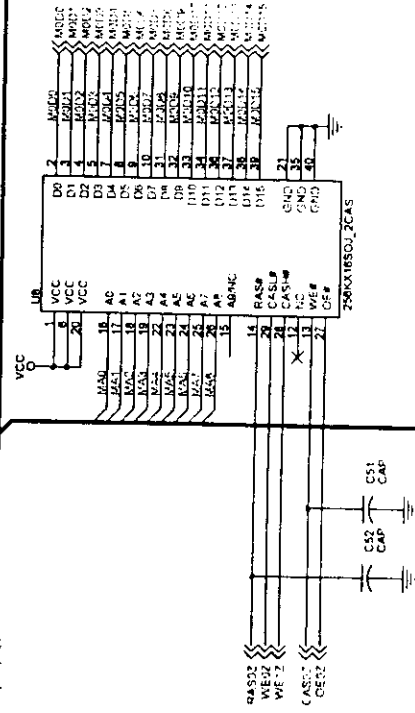


3rd MB DRAM (Dual CAS)



1st MB DRAM (Dual CAS)

2nd MB DRAM (Dual CAS)



COMPONENT SIDE

CIRCUIT SIDE

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PCIBUS_C

PCIBUS_D

PCIBUS_E

PCIBUS_F

PCIBUS_G

PCIBUS_H

PCIBUS_I

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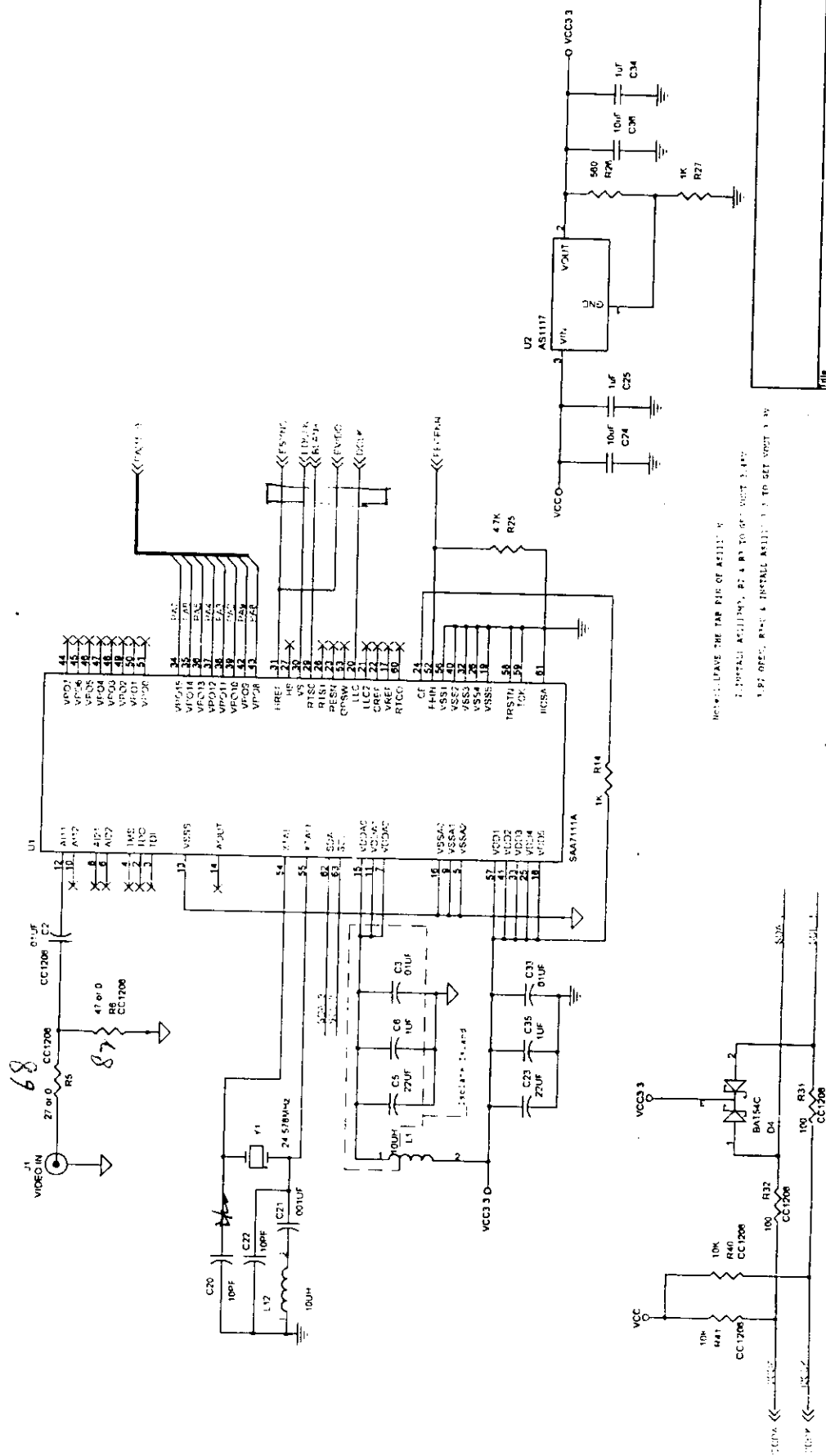
PCIBUS

Figure 1 is a block diagram of the 2716 EPROM. It shows a 16x8 array of memory cells. The vertical axis is labeled with addresses 00 to 0F. The horizontal axis is labeled with data bits D7 to D0. The array is divided into four 4x4 quadrants. The top-left quadrant is labeled 'M1020' through 'M1027'. The top-right quadrant is labeled 'M1028' through 'M1035'. The bottom-left quadrant is labeled 'M1036' through 'M1043'. The bottom-right quadrant is labeled 'M1044' through 'M1051'. The array is connected to a VCC pin and a GND pin. The array is also connected to a 2716 EPROM chip.

NOTE: PLEASE DO NOT CONFUSE

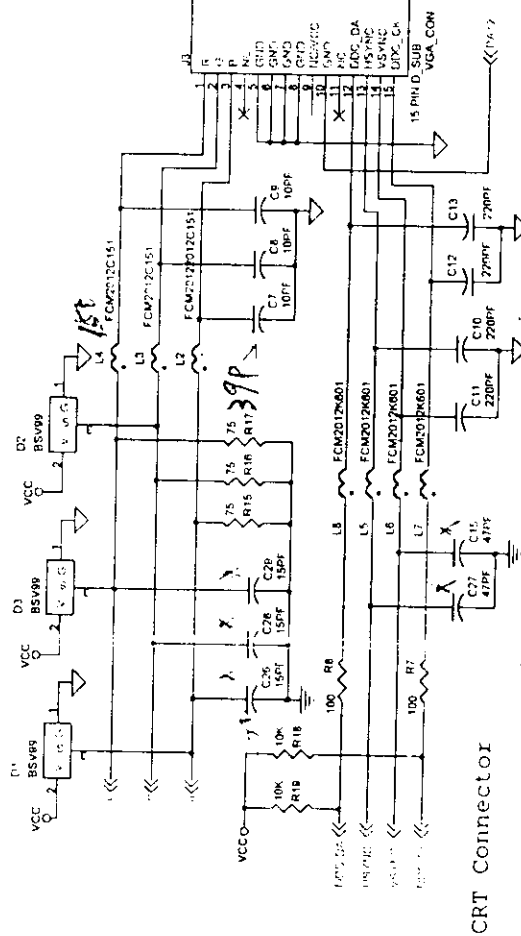
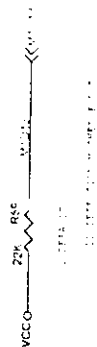
Title DTCT-9705, PCI BUS & RIOs

File B	Document Number 9705-7 SCH	Rev 1.0
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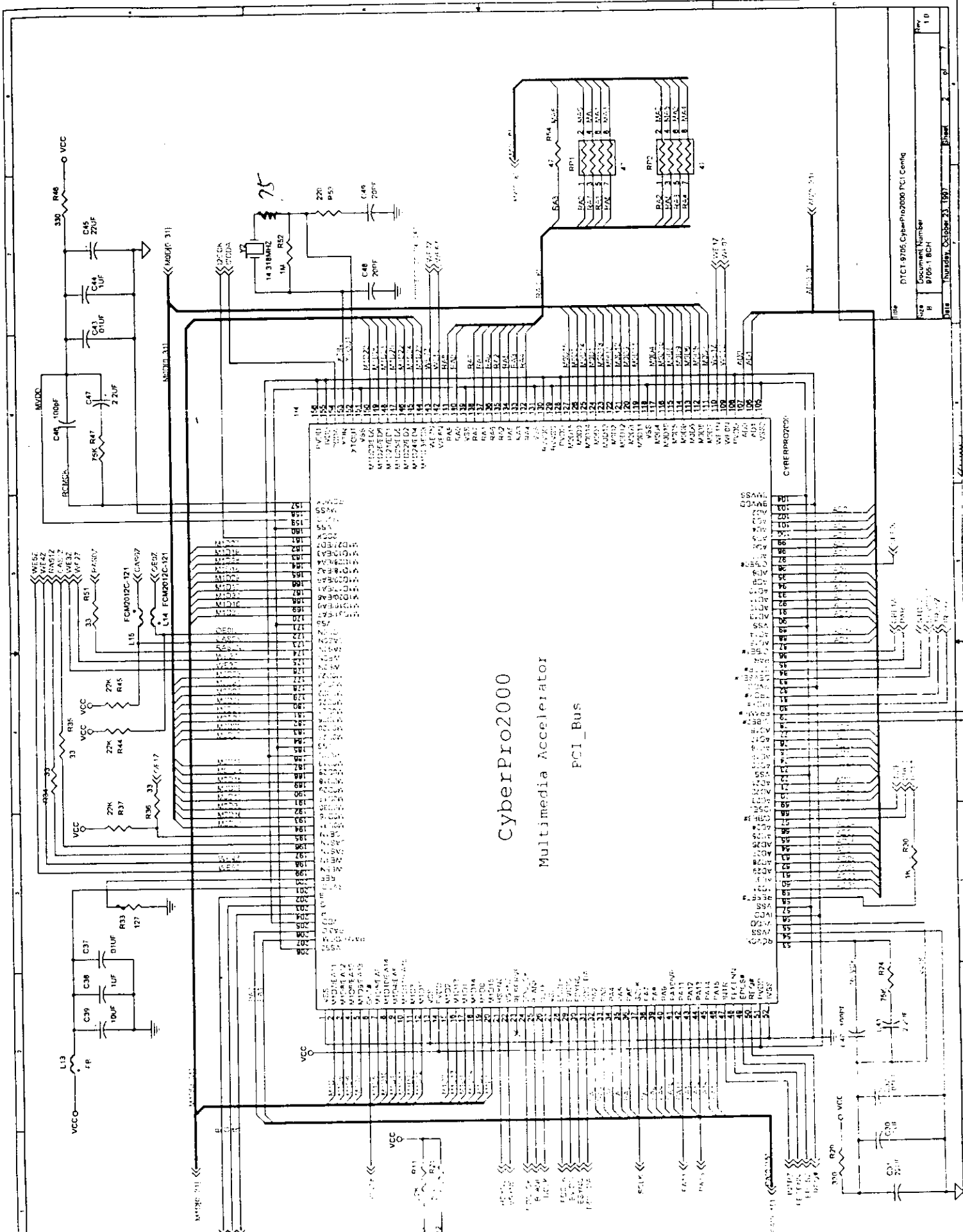
NOTE: LEAVE THE TAP PIN OF ASSEMBLY
IN PLACE. ASSEMBLY, SET & RE-TOGETHER
1.9. OPEN, RE- & INSTALL ASSEMBLY TO GET VOLTAGE

22K R42 22K R43



CRT Connector

Title	DTC1-9705, CRT & Feature Conn	
Size	Document Number	
B	9705-2 BCH	
Date	Tuesday, October 23, 1997	Rev. 0



CyberPro2000

Multimedia Accelerator

PCI_Bus

Doc: DTCT-9705 CyberPro2000 PCI Config

Document Number 9705-1 BCH

Date Thursday, October 23, 1997

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