I491xQ Series
Hardware Design

LTE Standard Module Series

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About the Document

Revision History

Version	Date	Description
-	2025-04-11	Creation of the document
1.0	2025-04-15	First official release

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1 Introduction

This document describes the I491xQ series features, performance, and air interfaces and hardware interfaces connected to your applications. The document provides a quick insight into interface specifications, RF performance, electrical and mechanical specifications, and other module information, as well.

This document is applicable to the following modules:

- I4915Q series: I4915Q-NA, I4915Q-AF
- I4916Q-GL

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.

2 Product Overview

I491xQ series are SMD modules with compact packaging, which also support GNSS to meet your specific application demands.

Table 2: Basic Information

Item	I4915Q Series	I4916Q-GL
Packaging type	LGA	LGA
Pin counts	126	126
Dimensions	(23.6 ±0.2) mm × (19.9 ±0.2) mm × (2.4 ±0.2) mm	(26.5 ±0.2) mm × (22.5 ±0.2) mm × (2.4 ±0.2) mm
Weight	Approx. 2.3 g	Approx. 2.9 g

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

Technology	I4915Q-NA	I4915Q-AF	I4916Q-GL
LTE-FDD	B2/B4/B5/B12/B13/ B66	B2/B4/B5/B12/B13/B14/ B66/B71	B1/B2/B3/B4/B5/B7/B8/B12/ B13/B18/B19/B20/B25/B26/ B28/B66
LTE-TDD	-	-	B34/B38/B39/B40/B41
GNSS (Optional)	GPS, GLONASS, BDS, Galileo, QZSS	GPS, GLONASS, BDS, Galileo, QZSS	GPS, GLONASS, BDS, Galileo, QZSS
Wi-Fi Scan	802.11b/g/n with 2.4G DSSS beacon	802.11b/g/n with 2.4G DSSS beacon	802.11b/g/n with 2.4G DSSS beacon

NOTE

Wi-Fi Scan function shares the same antenna interface with the main antenna. These two antennas should use TDM (Time Division Multiplexing) and cannot be used simultaneously. Wi-Fi Scan only supports receiving and does not support transmitting.

2.2. Key Features

Table 4: Key Features

Categories	Descriptions
Supply Voltage	● 3.3–4.3 V ● Typ.: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
USIM Interfaces	● Support 2 USIM interfaces: USIM1 interface and USIM2 interface ● Only support Dual SIM Single Standby ● USIM1: 1.8/3.0 V ● USIM2: 1.8 V ● When USIM1 and USIM2 are used at the same time, the power domain of USIM interfaces should be 1.8 V. Otherwise, USIM2 interface will be damaged. ● USIM2 interface and Camera SPI* cannot be used at the same time.
PCM Interface*	● Supports one digital audio interface: PCM interface ● Used for audio function with external Codec
I2C Interface*	● One I2C interface ● Complies with I2C-bus specification
Camera SPI *	● Supports one camera SPI ● Supports the SPI dual-wire data transmission ● USIM2 and Camera SPI cannot be used at the same time.
USB Interface	● Compliant with USB 2.0 specifications (only supports slave mode) ● Data transmission rate up to 480 Mbps ● Used for AT command communication, data transmission, GNSS NMEA sentence output (**All-in-one** solution only), software debugging, firmware upgrade and the output of partial logs ● The USB interface can be used to upgrade firmware only after the module entering download mode (Pulling up USB_BOOT to VDD_EXT before turning on the module, and then the module will enter download mode).

	● USB serial drivers: Windows 10/11, Linux 2.6–6.7, Android 4.x–14.x systems
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate: 115200 bps by default ● RTS and CTS hardware flow control **Debug UART:** ● Used for the output of partial logs ● Baud rate: 115200 bps, 3 Mbps (by default) **GNSS UART:** ● Used for outputting GNSS data or GNSS NMEA sentence output ● Baud rate: 921600 bps **GNSS debug UART:** ● Used for outputting GNSS system logs ● Baud rate: 3 Mbps
Network Indication	**NET_STATUS:** ● Used for indicating network connectivity status
AT Commands	● Complies with the AT commands defined in *3GPP TS 27.007* and *3GPP TS 27.005* ● Complies with Eagle enhanced AT commands
Antenna Interface	● Main antenna/Wi-Fi Scan antenna interface (ANT_MAIN) ● GNSS antenna interface (ANT_GNSS) ● 50 Ω characteristic impedance
Transmitting Power	● LTE bands: Class 3 (23 dBm ±2 dB)
LTE Features	● Complies with 3GPP Rel-14 FDD ● Max. LTE category: Cat1 bis ● 1.4/3/5/10/15/20 MHz RF bandwidth ● DL modulations: QPSK, 16QAM and 64QAM ● UL modulations: QPSK, 16QAM ● LTE-FDD Max. data rates: 10 Mbps (DL)/5 Mbps (UL) ● LTE-TDD Max. data rates: 8.96 Mbps (DL)/3.1 Mbps (UL)
Internet Protocol Features	● Complies with TCP/UDP/NTP/NITZ/FTP/HTTP/PING/HTTPS/FTPS/SSL/MQTT/CMUX/PPP/FILE/SMTP/SMTPS/MMS* protocols ● Complies with PPP protocol's PAP and CHAP authentication
Temperature Ranges	● Normal operating temperature [1]: -35 °C to +75 °C ● Extended operating temperature [2]: -40 °C to +85 °C ● Storage temperature: -40 °C to +90 °C
Firmware Upgrade	Via USB 2.0 interface or DFOTA

[1] Within this range, the module's indicators comply with 3GPP specification requirements.
[2] Within this range, the module retains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

RoHS	All hardware components fully comply with EU RoHS directive

NOTE

I491xQ series support SPI. If you need this function, please contact Eagle Technical Support.

2.3. Functional Diagram

The functional diagram illustrates the following major functional parts:

- Power management
- Baseband part
- Radio frequency part
- Peripheral interfaces
- GNSS part

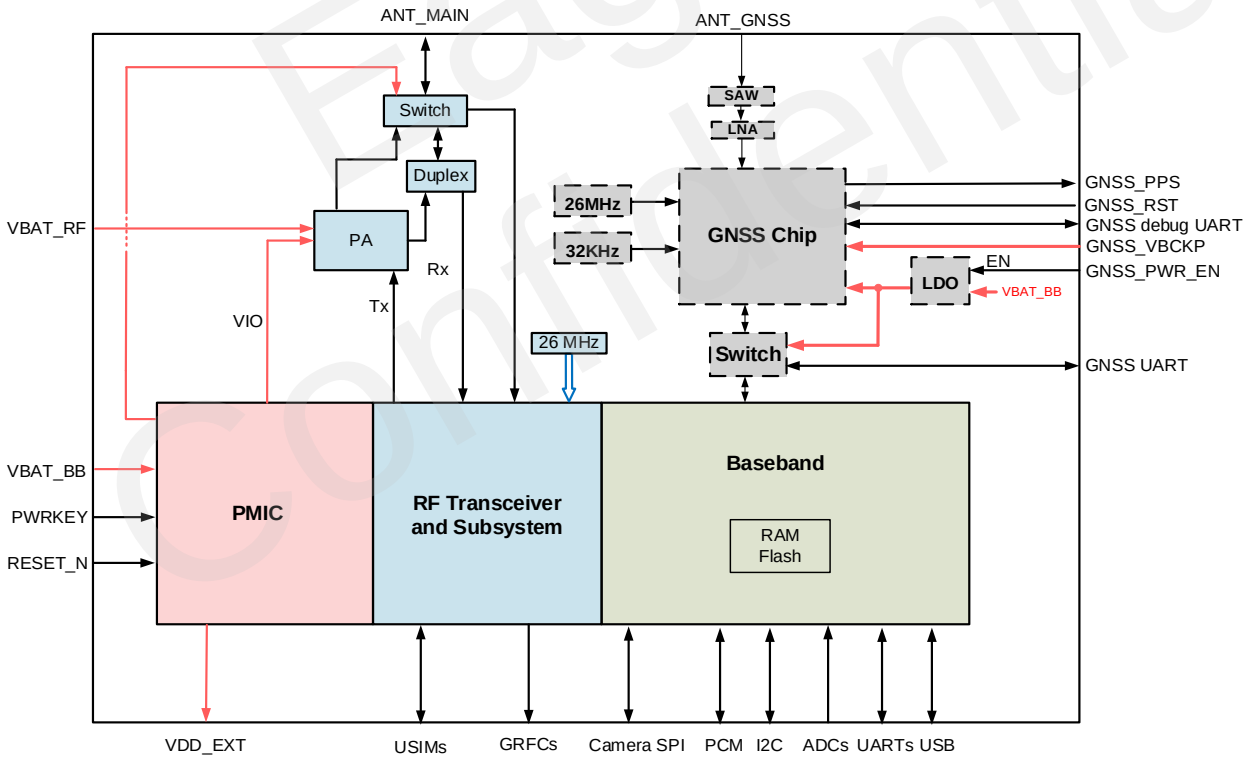


Figure 1: Functional Diagram

2.4. Pin Assignment

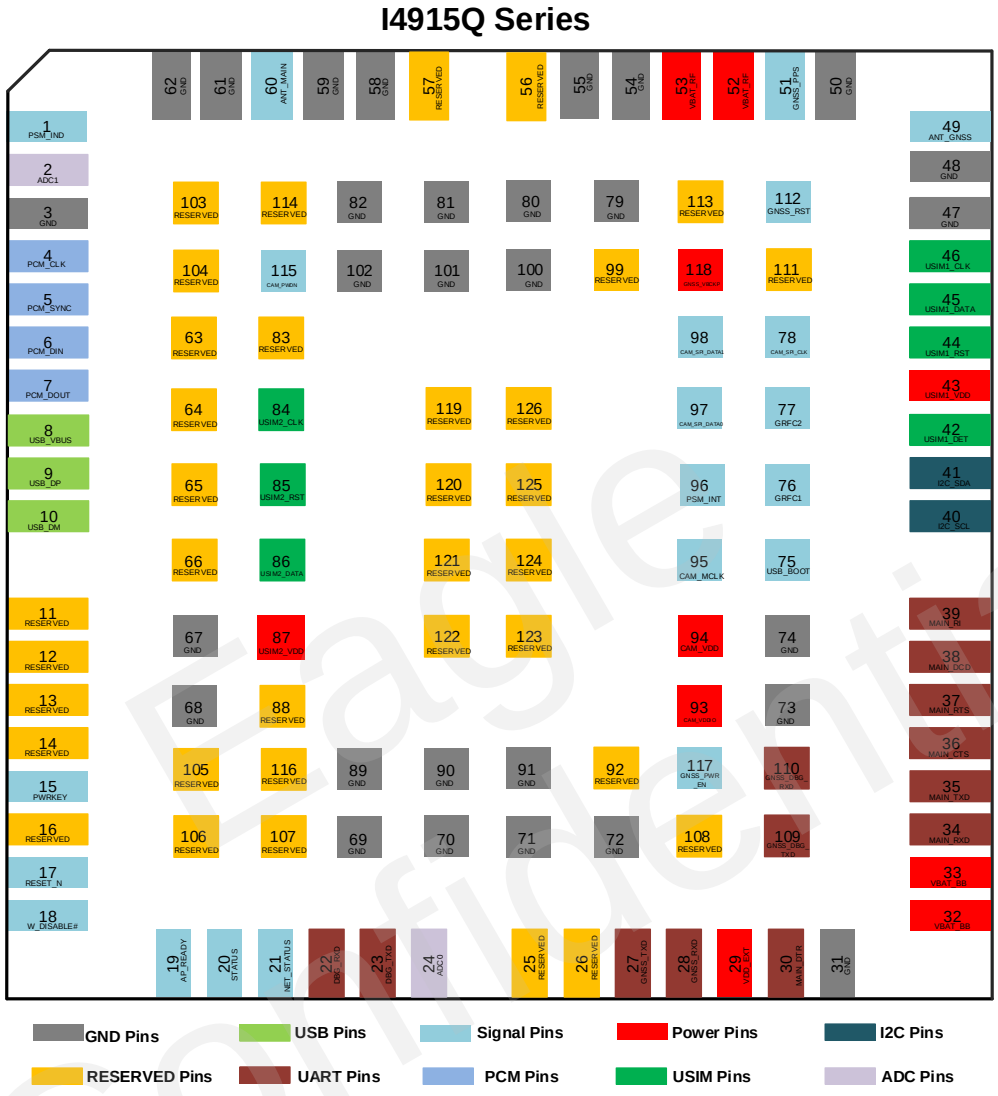


Figure 2: I4915Q Series Pin Assignment (Top View)

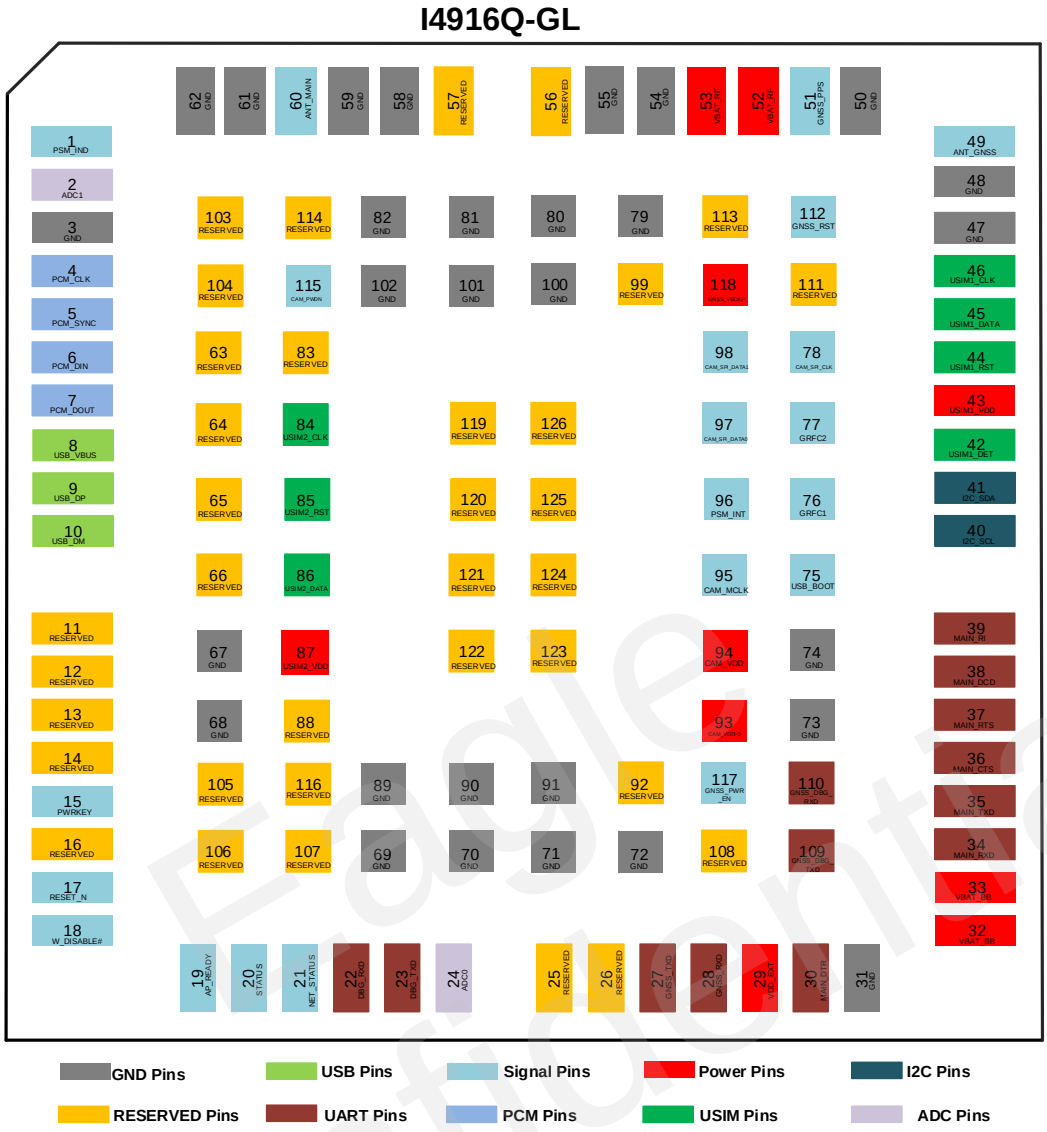


Figure 3: I4916Q-GL Pin Assignment (Top View)

NOTE

1. If the module does not need to enter download mode, USB_BOOT (pin 75) should not be pulled up to VDD_EXT before the module successfully starts up.
2. In sleep mode, pins 34–37 of the main UART interface, pins 22 and 23 of debug UART interface, USB_BOOT (pin 75), pins 4–7 of PCM interface*, pins 40 and 41 of I2C interface*, and pins 78, 93, 95, 97, 98 and 115 of Camera SPI* are powered down. The driving capacity will be lost and the functions of status indication and data transmission are disabled. Pay attention to it when designing circuits.
3. When USIM1 and USIM2 are used at the same time, the power domain of USIM interfaces should be 1.8 V. Otherwise, USIM2 interface will be damaged.
4. The module supports SPI. If you need this function, please contact Eagle Technical Support.

5. GNSS interface (pins 27, 28, 49, 51, 109, 110, 112, 117, 118) is optional. If you need this function, please contact Eagle Technical Support.
6. USIM2 interface and Camera SPI* cannot be used at the same time.
7. Keep all RESERVED pins and unused pins unconnected.

2.5. Pin Description

Table 5: Parameter Definition

Parameter	Description
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PI	Power Input
PO	Power Output
OD	Open Drain

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
VBAT_BB	32, 33	PI	Power supply for the module's BB part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	External power supply is recommended to provide with current of 0.3 A at least. A test point is recommended to be reserved.

VBAT_RF	52, 53	PI	Power supply for the module's RF part		External power supply is recommended to provide with current of 1.2 A at least. A test point is recommended to be reserved.
VDD_EXT	29	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. A test point is recommended to be reserved.
GNSS_ VBCKP [3]	118	PI	Power supply for GNSS RTC	Vmax = 3.6 V Vmin = 1.9 V Vnom = 3.3 V	If unused, keep it open.
GND	3, 31, 47, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102				
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
PWRKEY	15	DI	Turn on/off the module	V_{IL}max = 0.5 V	Active low. A test point is recommended to be reserved.
RESET_N	17	DI	Reset the module		Active low. A test point is recommended to be reserved if unused.
Indication Signals					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
STATUS	20	DO	Indicate the module's operation status	VDD_EXT	If unused, keep them open.
NET_STATUS	21	DO	Indicate the module's network activity status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**

[3] This pin is optional. If you need this function, please contact Eagle Technical Support.

USB_VBUS	8	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	A test point must be reserved.
USB_DP	9	AIO	USB differential data (+)		USB 2.0 compliant. Requires differential impedance of 90 Ω. Test points must be reserved.
USB_DM	10	AIO	USB differential data (-)		
USIM Interfaces [4]					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
USIM1_VDD	43	PO	USIM1 card power supply	$I_O$max = 50 mA **Low-voltage:** Vmax = 1.85 V Vmin = 1.75 V **High-voltage:** Vmax = 3.05 V Vmin = 2.95 V	Either 1.8 V or 3.0 V USIM1 card is supported and can be identified automatically by the module.
USIM1_DATA	45	DIO	USIM1 card data	USIM1_VDD	
USIM1_CLK	46	DO	USIM1 card clock		
USIM1_RST	44	DO	USIM1 card reset		
USIM1_DET	42	DI	USIM1 card hot-plug detect	VDD_EXT	If unused, keep it open.
USIM2_VDD [5]	87	PO	USIM2 card power supply	USIM1_VDD **(Low-voltage)**	Connected with USIM1_VDD inside the module. 1.8 V power domain is required for USIM2. Otherwise, this interface will be damaged.
USIM2_DATA [5]	86	DIO	USIM2 card data	VDD_EXT	Connected with pin 97 (CAM_SPI_DATA0) internally. 1.8 V power domain is required for

[4] When USIM1 and USIM2 are used at the same time, the power domain of USIM interfaces should be 1.8 V. Otherwise, USIM2 interface will be damaged.
[5] USIM2 and Camera SPI* cannot be used at the same time.

					USIM2. Otherwise, this interface will be damaged.
USIM2_RST [5]	85	DO	USIM2 card reset		Connected with pin 78 (CAM_SPI_CLK) internally. 1.8 V power domain is required for USIM2. Otherwise, this interface will be damaged.
USIM2_CLK [5]	84	DO	USIM2 card clock		Connected with pin 115 (CAM_PWDN) internally. 1.8 V power domain is required for USIM2. Otherwise, this interface will be damaged.
Main UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
MAIN_CTS	36	DO	Clear to send signal from the module	VDD_EXT	Connect to MCU's CTS. If unused, keep it open.
MAIN_RTS	37	DI	Request to send signal to the module		Connect to MCU's RTS. If unused, keep it open.
MAIN_RXD	34	DI	Main UART receive		If unused, keep them open.
MAIN_DCD	38	DO	Main UART data carrier detect		
MAIN_TXD	35	DO	Main UART transmit		
MAIN_RI	39	DO	Main UART ring indication		
MAIN_DTR	30	DI	Main UART data terminal ready		
Debug UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**

DBG_RXD	22	DI	Debug UART receive	VDD_EXT	Test points must be reserved.
DBG_TXD	23	DO	Debug UART transmit		
GNSS UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
GNSS_TXD [3]	27	DO	GNSS UART transmit	VDD_EXT	Test points are recommended to be reserved.
GNSS_RXD [3]	28	DI	GNSS UART receive		
GNSS debug UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
GNSS_DBG_TXD [3]	109	DO	GNSS debug UART transmit	VDD_EXT	Test points must be reserved.
GNSS_DBG_RXD [3]	110	DI	GNSS debug UART receive		
I2C Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
I2C_SCL	40	OD	I2C serial clock	VDD_EXT	External pull-up resistor is required. If unused, keep them open.
I2C_SDA	41	OD	I2C serial data		
PCM Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
PCM_SYNC	5	DO	PCM data frame sync	VDD_EXT	If unused, keep them open.
PCM_CLK	4	DO	PCM clock		
PCM_DIN	6	DI	PCM data input		
PCM_DOUT	7	DO	PCM data output		
RF Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
ANT_MAIN [6]	60	AIO	Main antenna/Wi-Fi Scan antenna interface		50 Ω impedance.

[6] ANT_MAIN only supports passive antennas.

ANT_GNSS [3]	49	AI	GNSS antenna interface		50 Ω impedance.
GRFC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
GRFC1	76	DO	Generic RF controller	VDD_EXT	If unused, keep them open.
GRFC2	77	DO	Generic RF controller		
Camera SPI* [5]					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
CAM_MCLK	95	DO	Master clock of the camera		If unused, keep it open.
CAM_SPI_CLK	78	DI	Camera SPI clock		Connected with pin 85 (USIM2_RST) internally. If unused, keep it open.
CAM_SPI_DATA0	97	DI	Camera SPI data bit 0	VDD_EXT	Connected with pin 86 (USIM2_DATA) internally. If unused, keep it open.
CAM_SPI_DATA1	98	DI	Camera SPI data bit 1		If unused, keep it open.
CAM_PWDN	115	DO	Power down of the camera		Connected with pin 84 (USIM2_CLK) internally. If unused, keep it open.
CAM_VDD	94	PO	Camera analog power supply	Vnom = 2.8 V	If unused, keep them open.
CAM_VDDIO	93	PO	Camera digital power supply	VDD_EXT	
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
ADC0	24	AI	General-purpose ADC interface	Voltage range: 0–1.2 V	If unused, keep them open.
ADC1	2	AI	General-purpose ADC interface		

Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
USB_BOOT	75	DI	Make the module enter download mode	VDD_EXT	Active high before power-up. A test point must be reserved.
W_DISABLE#*	18	DI	Airplane mode control		If unused, keep them open.
PSM_IND*	1	DO	Indicate the module's power saving mode		
PSM_INT*	96	DI	External interrupt; wake up the module from power saving mode		
AP_READY*	19	DI	Application processor ready		
GNSS_PPS [3]	51	DO	GNSS pulse per second output		
GNSS_RST [3]	112	DI	Reset the GNSS chip		A test point is recommended to be reserved.
GNSS_PWR_EN [3]	117	DI	GNSS power enabled		If unused, keep it open.
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	11–14, 16, 25, 26, 56, 57, 63–66, 83, 88, 92, 99, 103–108, 111, 113, 114, 116, 119–126				Keep these pins open.

2.6. EVB Kit

Eagle supplies an evaluation board (UMTS&LTE EVB) with accessories to develop or test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

The module integrates both LTE and GNSS [7] engines which can work as a whole (**All-in-one** solution) unit or work independently (**Stand-alone** solution) according to your demands.

3.1.1. Operating Modes of LTE Part

Table 7: Operating Modes Overview of LTE Part

Modes	Descriptions	
Full Functionality Mode	Idle	Software is active. The module is registered on the network but has no data interaction with the network.
	Data	Network connection is ongoing. Power consumption is decided by network setting and data rate.
Minimum Functionality Mode	● **AT+CFUN=0** can set the module to the minimum functionality mode when the power is on. ● Both RF function and USIM card will be invalid.	
Airplane Mode	● **AT+CFUN=4** or driving W_DISABLE#* low can set the module to airplane mode. ● RF function will be invalid.	
Sleep Mode	Power consumption of the module will be reduced to an ultra-low level. The module can still receive paging, SMS and TCP/UDP data from the network.	
PSM	The power consumption of the module will be reduced to an extremely low level. The network will be in a non-connected state, and no paging will be received.	
eDRX	The module and the network may negotiate the use of eDRX through non-access stratum signaling to reduce power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.	
Power Down Mode	The VBAT_BB and VBAT_RF pins are constantly turned on and the software stops working.	

[7] GNSS function is optional. If you need the function, please contact Eagle Technical Support.

NOTE

For more details about **AT+CFUN**, see ***document [2]***.

3.1.1.1. PSM

The module supports PSM. When the module works normally, you can enable PSM via **AT+CPSMS**. The module can be awakened from PSM by any of the following methods.

- Wake-up by TAU periodic request timer (T3412);
- Wake-up by PWRKEY pin;
- Wake-up by MAIN_DTR pin.

To minimize power consumption in PSM, AGPIO (including MAIN_DCD, MAIN_RI, PSM_IND and STATUS) should be disabled with **AT+QCFG="sleep/aon_cfg"**, and it is noted that VDD_EXT would be disabled simultaneously. Consequently, for pins with wakeup functions such as MAIN_DTR, AP_READY, W_DISABLE#, USB_VBUS, MAIN_RXD, PSM_INT and USIM1_DET, if VDD_EXT serves as the pull-up power supply, it must be replaced with an external power source. Failure to do this may lead to abnormalities in sleep mode.

NOTE

1. For details about AT commands, please refer to ***document [3]***.
2. Ensure the network supports PSM.

3.1.1.2. eDRX

The module supports eDRX mode. When the module is working normally, use **AT+CEDRXS** to enter eDRX mode and **AT+QSCLK=1** to enter sleep mode. The module can be awakened from eDRX by MAIN_DTR pin.

To minimize power consumption in eDRX, AGPIO (including MAIN_DCD, MAIN_RI, PSM_IND and STATUS) should be disabled with **AT+QCFG="sleep/aon_cfg"**, and it is noted that VDD_EXT would be disabled simultaneously. Consequently, for pins with wakeup functions such as MAIN_DTR, AP_READY, W_DISABLE#, USB_VBUS, MAIN_RXD, PSM_INT and USIM1_DET, if VDD_EXT serves as the pull-up power supply, it must be replaced with an external power source. Failure to do this may lead to abnormalities in sleep mode.

NOTE

1. For details about AT commands, please refer to ***document [2]*** and ***[3]***.
2. Ensure the network supports eDRX.

3.1.1.3. Sleep Mode

With DRX technology, power consumption of the module will be reduced to an ultra-low level.

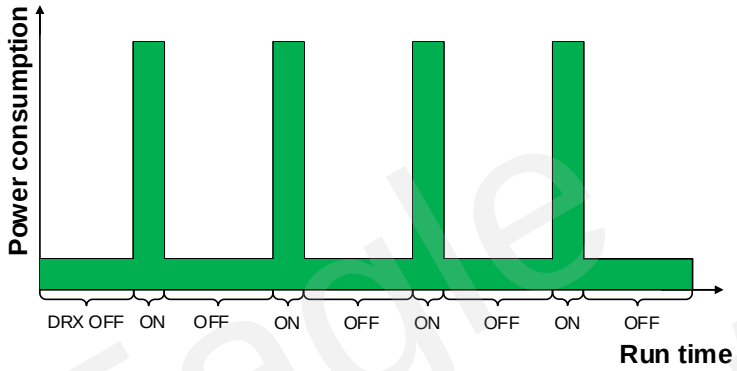


Figure 4: Power Consumption During Sleep Mode

NOTE

The DRX cycle values are transmitted sent over the wireless network.

3.1.1.4. UART Application Scenario

If the module communicates with the MCU via main UART, both the following preconditions should be met to set the module to sleep mode:

- Execute **AT+QSCLK=1**. For more details, see ***document [2]***.
- Ensure MAIN_DTR is held high or is kept unconnected.

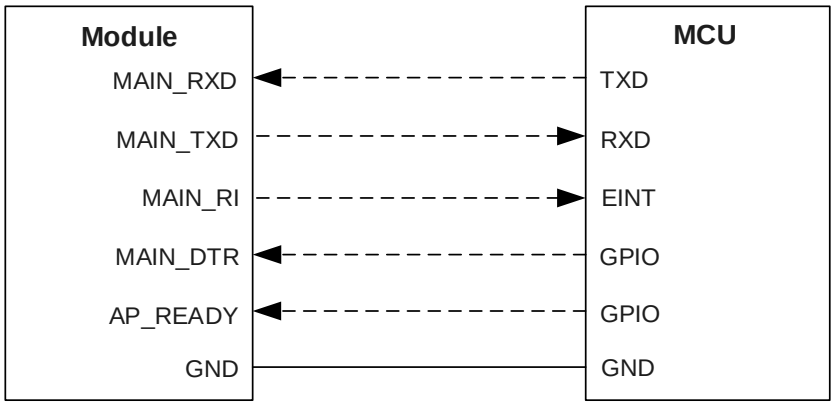


Figure 5: Sleep Mode Application via UART

- Driving MAIN_DTR low with the MCU will wake up the module.
- When the module has a URC to report, MAIN_RI signal will wake up the MCU. See ***Chapter 4.10.3*** for details about MAIN_RI.

NOTE

Pay attention to the level match shown in the dotted line between the module and the MCU.

3.1.1.5. USB Application with USB Remote Wakeup Function

If the host supports USB Suspend/Resume and remote wakeup functions, the following three preconditions must be met to set the module to sleep mode.

- Execute **AT+QSCLK=1**.
- Ensure MAIN_DTR is held high or is kept unconnected.
- Ensure the host's USB bus, which is connected to the module's USB interface, enters Suspend state.

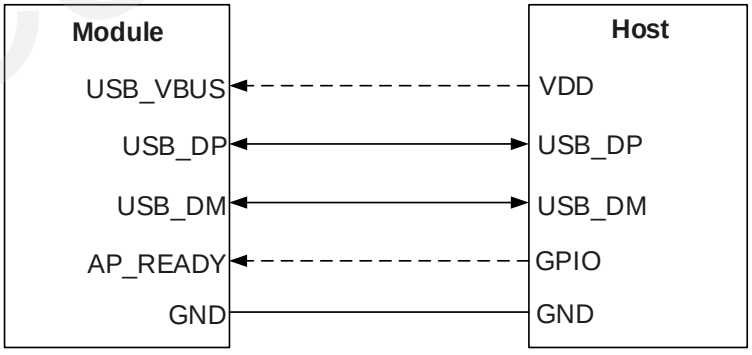


Figure 6:Sleep Mode Application with USB Suspend/Resume and Remote Wakeup

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will send remote wake-up signals through USB bus to wake up the host.

3.1.1.6. USB Application with USB Suspend/Resume and MAIN_RI Function

If the host supports USB Suspend/Resume, but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host. The following three preconditions must be met to set the module to sleep mode.

- Execute **AT+QSCLK=1**.
- Ensure MAIN_DTR is held high or is kept unconnected.
- Ensure the host's USB bus, which is connected to the module's USB interface, enters Suspend state.

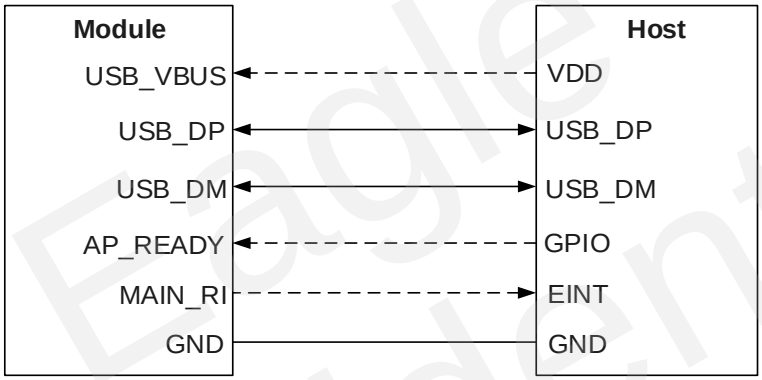


Figure 7: Sleep Mode Application with USB Suspend/Resume and MAIN_RI

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will wake up the host through MAIN_RI signal. See ***Chapter 4.10.3*** for details about MAIN_RI behavior.

3.1.1.7. USB Application without USB Suspend Function

If the host does not support USB Suspend function, the following three preconditions must be met to set the module to sleep mode:

- Execute **AT+QSCLK=1**.
- Ensure MAIN_DTR is held high or is kept unconnected.
- Ensure USB_VBUS is disconnected via the external control circuit.

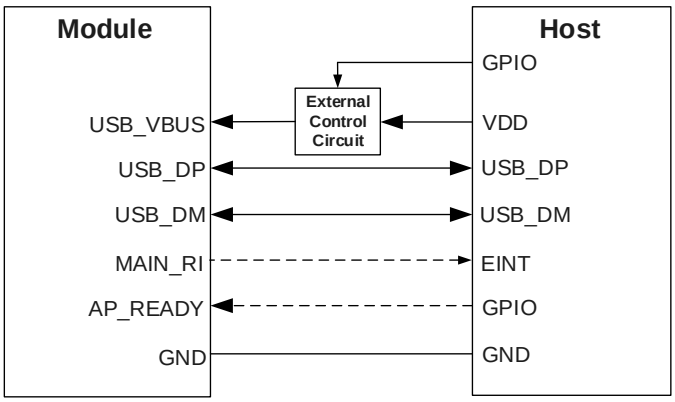


Figure 8: Sleep Mode Application without USB Suspend

Restore the power supply of USB_VBUS will wake up the module.

NOTE

Pay attention to the level match shown in the dotted line between the module and the host.

3.1.1.8. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands correlative with RF function will be inaccessible. This mode can be set via the following methods.

Hardware:

W_DISABLE#* is pulled up by default. Driving it low makes the module enter airplane mode.

Software:

AT+CFUN=<fun> provides choice of the functionality level via setting **<fun>** to 0, 1 or 4. For more details, see ***document [2]***.

- **AT+CFUN=0**: Minimum functionality mode (Both USIM and RF functions are disabled).
- **AT+CFUN=1**: Full functionality mode (By default).
- **AT+CFUN=4**: Airplane mode (RF function is disabled).

3.1.2. Operating Modes of GNSS Part

Table 8: Operating Modes Overview of GNSS Part

Modes	Descriptions
Continuous Mode	● GNSS starts to work. It can automatically locate, track, and continuously output positioning information. ● GNSS RF reception function is enabled. ● Entry conditions: GNSS_PWR_EN is at high-level and GNSS_VBCKP is powered on, the module will automatically enter the Continuous mode. ● Continuous mode includes acquisition mode and tracking mode. – **Acquisition mode**: The module starts to search satellites, and to determine visible satellites, coarse frequency, as well as the code phase of satellite signals. When the acquisition is completed, the module automatically switches to tracking mode. – **Tracking mode**: The module tracks satellites and demodulates the navigation data from specific satellites.
Backup Mode*	● Most system components will be shut down to save power consumption. ● Navigation data will be stored in the backup area for quick positioning next time.
Power Down Mode	● The power supply inside and outside the GNSS is cut off. ● The software stops working.

3.1.3. Summary of LTE and GNSS Parts' State in All-in-one Solution

In **All-in-one** solution, LTE part and GNSS part can be worked as a whole unit. The GNSS part can be regarded as a peripheral of the LTE part. Without an external power supply, the LTE part can internally control the LDO to supply power to the GNSS. If the LTE part is disabled, the GNSS will not work. This allows for convenient communication between LTE and GNSS parts, such as AT command sending for GNSS control, and AGPS data injection.

It should be noted that the UART of the GNSS part is switched by an analog switch inside the module. In **All-in-one** mode, the GNSS UART interface (pins 27 and 28) of the module is not connected inside and unavailable.

In **All-in-one** solution, GNSS NMEA sentences can be output through the debug UART or USB NMEA port (The output port can be selected by **AT+QGPSCFG**). For details about the AT command, see ***document [4]***.

The schematic diagram of **All-in-one** solution is shown below.

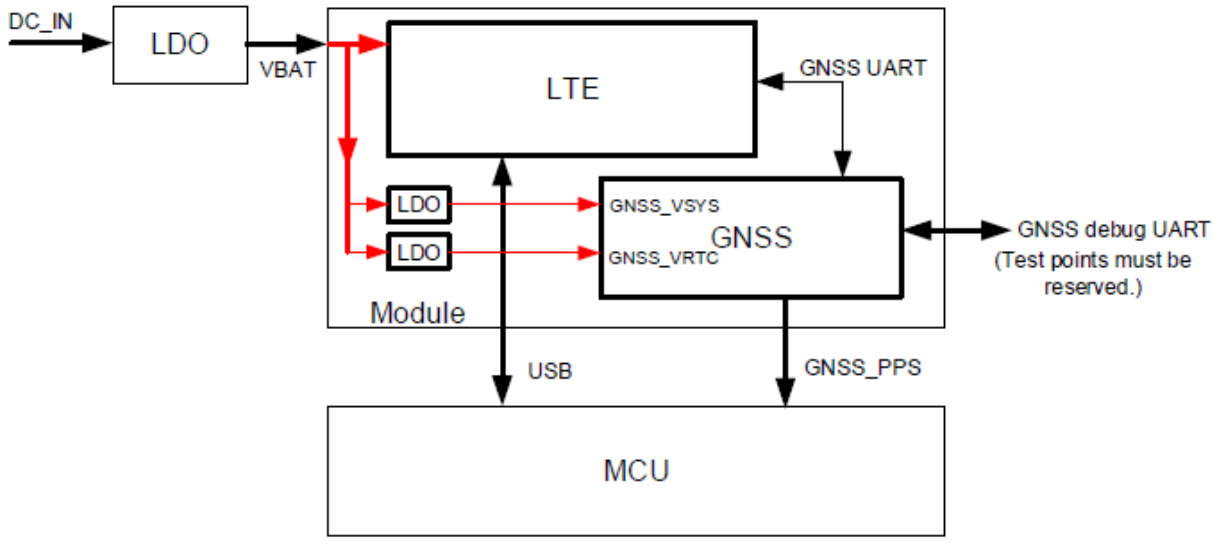


Figure 9: All-in-one Solution Schematic Diagram

3.1.4. Summary of LTE and GNSS Parts' State in Stand-alone Solution

In **Stand-alone** solution, LTE and GNSS parts work separately. Thus, they should be controlled separately by MCU. A lithium battery can be added externally to power GNSS_VBCKP independently. You can use MCU to control GNSS_VSYS to power on GNSS chip. At this time, the LTE part does not need to be enabled, and the GNSS part can still work.

In **Stand-alone** solution, GNSS NMEA sentences can be output through GNSS UART.

The schematic diagram of **Stand-alone** solution is shown below.

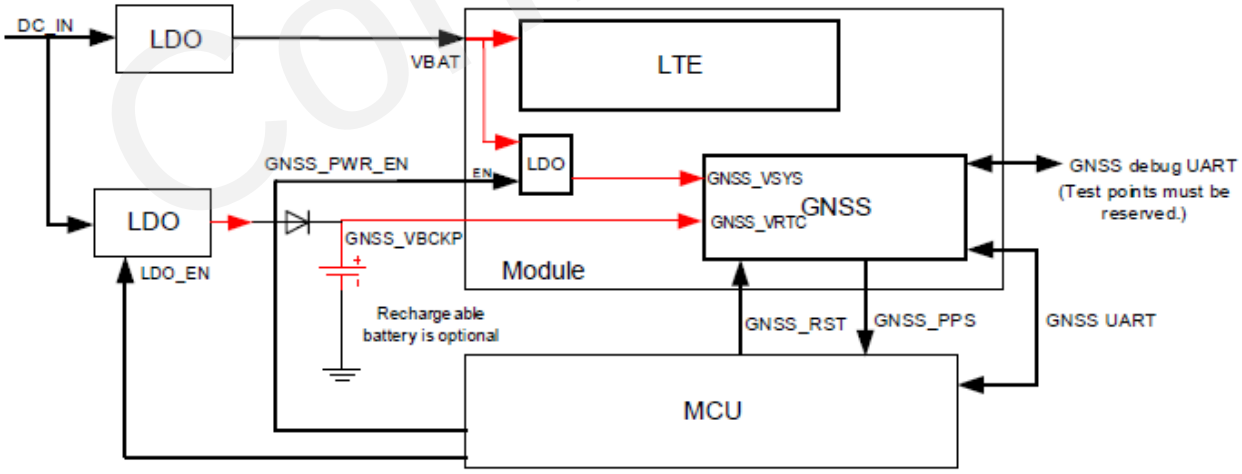


Figure 10: Stand-alone Solution Schematic Diagram

NOTE

1. In the **Stand-alone** or **All-in-one** solution, if the GNSS chip is powered externally, the GNSS firmware cannot be upgraded through the LTE network because LTE cannot reset the GNSS chip. If you want to upgrade the GNSS firmware through the LTE network, you need to disconnect GNSS_PWR_EN (pin 117) and GNSS_VBCKP (pin 118) from the outside or set both pins to low.
2. Whether in **Stand-alone** or **All-in-one** solution, to facilitate GNSS firmware upgrade, it is recommended to reserve test points for GNSS UART (pins 27 and 28), GNSS_VBCKP (pin 118), GNSS_PWR_EN (pin 117) and GNSS_RST (pin 112).

3.2. Power Supply

3.2.1. Power Supply Pins

The module provides four VBAT pins dedicated to connecting with the external power supply:

Table 9: Pin Description of Power Supply Interface

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Units
VBAT_BB	32, 33	PI	Power supply for the module's BB part	3.3	3.8	4.3	V
VBAT_RF	52, 53	PI	Power supply for the module's RF part	3.3	3.8	4.3	V
GNSS_VBCKP [8]	118	PI	Power supply for GNSS RTC	1.9	3.3	3.6	V
GND	3, 31, 47, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102						

3.2.2. Reference Design for Power Supply

Power design for the module is essential.

For LTE part, it is recommended to use a power supply that can provide the module with at least 1.5 A current. If the voltage difference between input voltage and the supply voltage is small, it is suggested to use an LDO; if the voltage difference is big, a buck converter is recommended.

The following figure shows a reference design for +5 V input power supply.

[8] This pin is optional. If you need this function, please contact Eagle Technical Support.

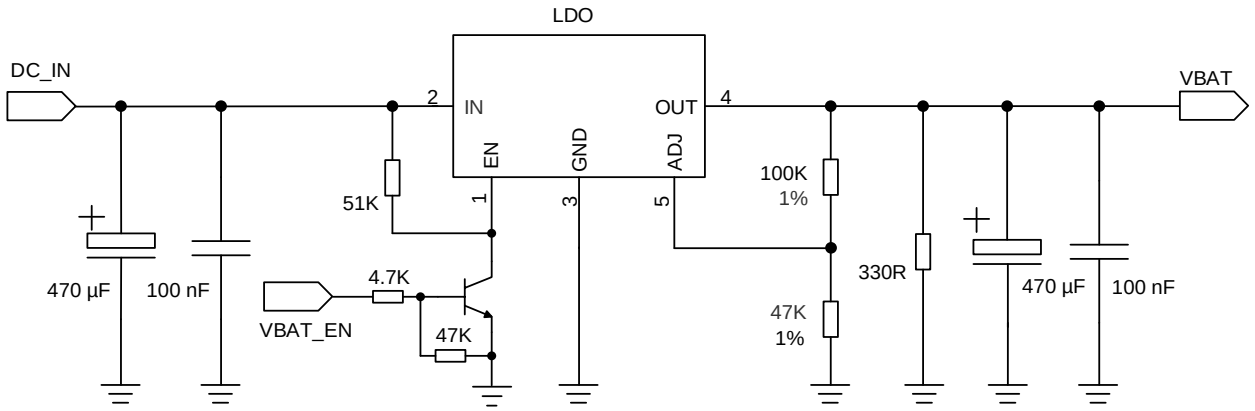


Figure 11: Reference Design of Power Input

NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.

For the power supply of GNSS part:

- In **All-in-one** solution, the power supply of GNSS part is controlled by the LTE part internally.
- In **Stand-alone** solution, the power supply of GNSS part is controlled independently by MCU.

For more information about **All-in-one** solution and **Stand-alone** solution, see ***Chapter 3.1.3 & 3.1.4***.

3.2.3. Voltage Stability Requirements

The power supply range of the module is 3.3–4.3 V. Ensure the input voltage never drops below 3.3 V.

To decrease the voltage drop, use a bypass capacitor of about 100 µF with low ESR for VBAT_BB and VBAT_RF respectively and reserve a multi-layer ceramic chip (MLCC) capacitor array with ultra-low ESR. Use three ceramic capacitors (100 nF, 33 pF and 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT pins. The main power supply from an external application should be a single voltage source and can be expanded to two sub paths with the star configuration. The width of VBAT_BB trace and VBAT_RF trace should be at least 1 mm and 2 mm respectively. In principle, the longer the VBAT trace is, the wider it should be.

To avoid the ripple and surge and to ensure the stability of the power supply to the module, it is recommended to add a TVS with V_{RWM} = 4.7 V, low clamping voltage and high reverse peak pulse current Ipp at the front end of the power supply.

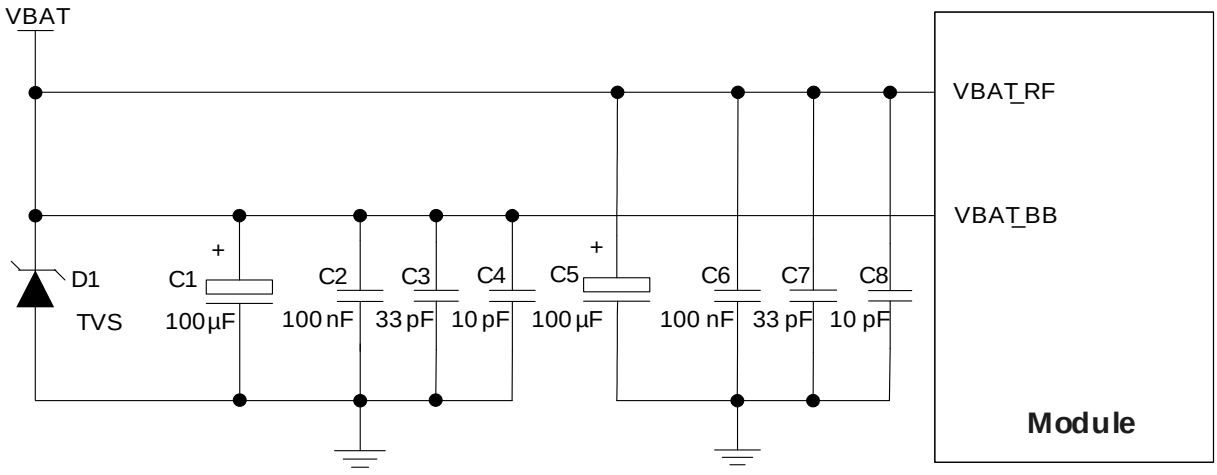


Figure 12: Reference Design of Power Supply

3.3. Turn On

3.3.1. Turn On with PWRKEY

Table 10: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turn on/off the module	Active low. A test point is recommended to be reserved.

When the module is in power-down mode, it can be turned on by driving the PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY.

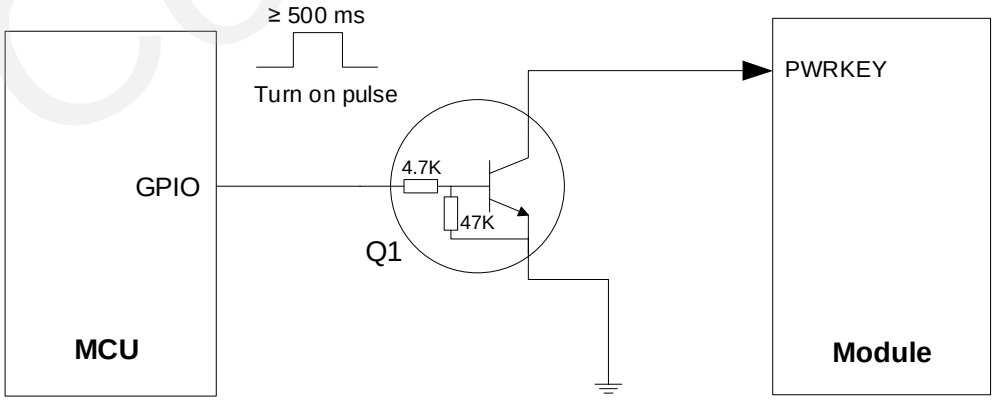


Figure 13: Reference Design of Turn On with Driving Circuit

Another way to control the PWRKEY is using a keystroke directly. When pressing the keystroke, an electrostatic strike may be generated from finger. Therefore, you should place a TVS component near the keystroke for ESD protection.

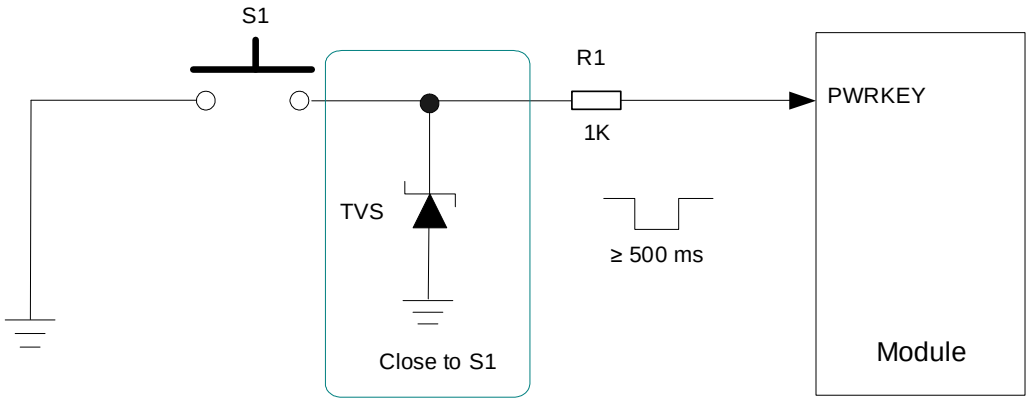


Figure 14: Reference Design of Turn On with Keystroke

The power-up timing is illustrated in the following figure.

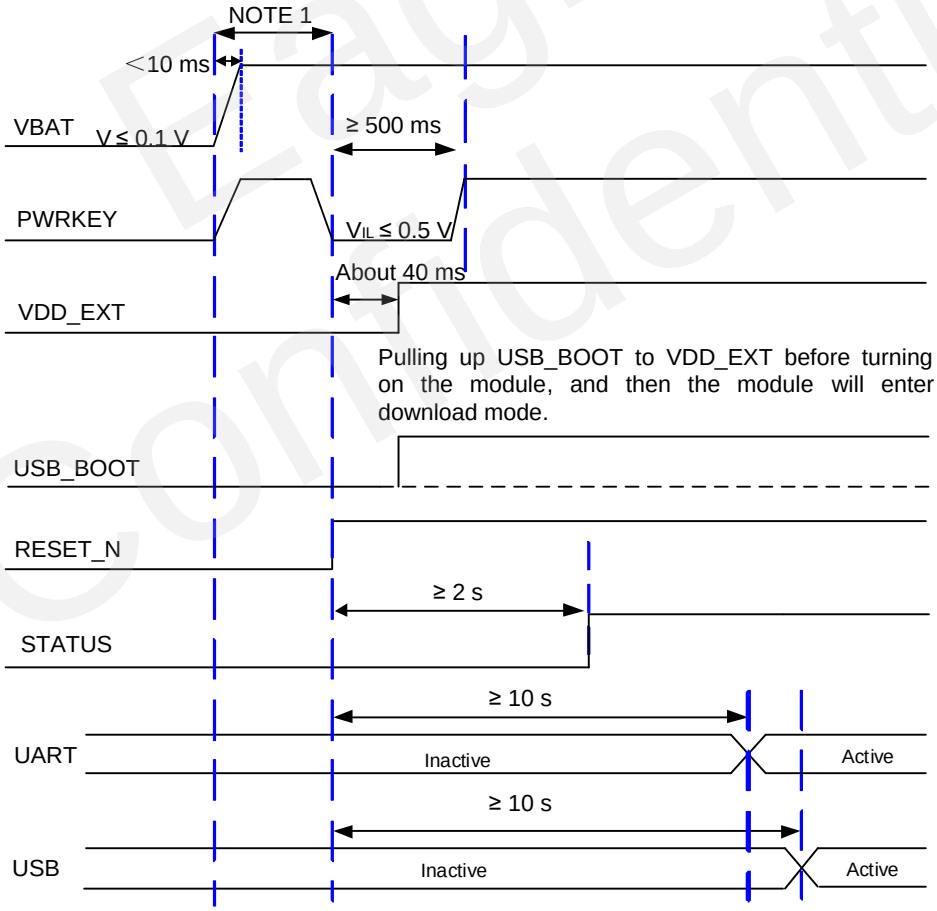


Figure 15: Power-up Timing with PWRKEY

NOTE

1. Ensure the voltage of VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. If the module needs to turn on automatically but does not need the turn-off function, PWRKEY can be driven low directly to ground with a recommended 4.7 kΩ resistor.

3.4. Turn Off

The following procedures can be used to turn off the module normally.

3.4.1. Turn Off with PWRKEY

Drive the PWRKEY low for at least 650 ms and then release it. Then, the module will execute the turn-off procedure.

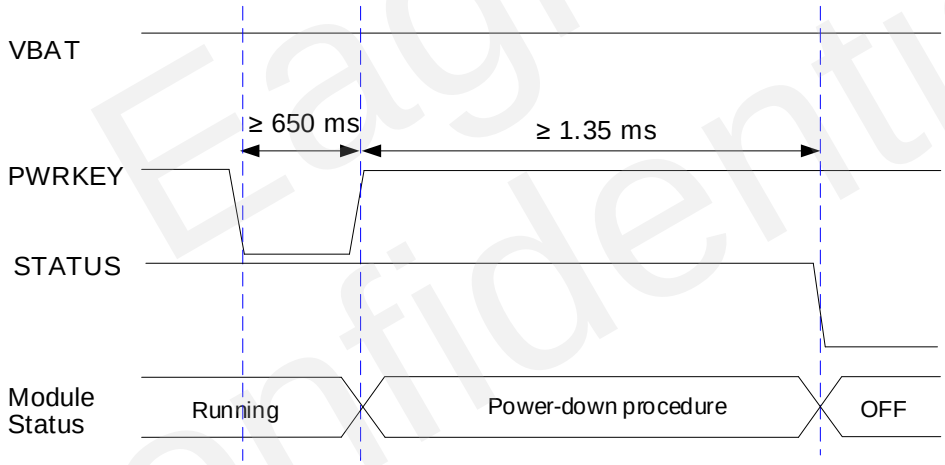


Figure 16: Power-down Timing with PWRKEY

3.4.2. Turn Off with AT Command

For proper shutdown procedure, execute **AT+QPOWD**, which is similar to turning off the module via the PWRKEY pin. See ***document [2]*** for details about **AT+QPOWD**.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.

2. If the module is turned on by connecting the PWRKEY to ground for a long time, **AT+QPOWD** cannot be used to turn off the module.
3. When turning off the module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module cannot be turned off successfully.

3.5. Reset

The reset function requires the PWRKEY and RESET_N pins to work together to complete. Pulling down PWRKEY when RESET_N is at low level can reset the module. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 11: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	17	DI	Reset the module	Active low. A test point is recommended to be reserved if unused.

The recommended circuit for reset function is similar to the PWRKEY control circuit. You can use an open drain/collector driver or a button to control RESET_N and PWRKEY pins.

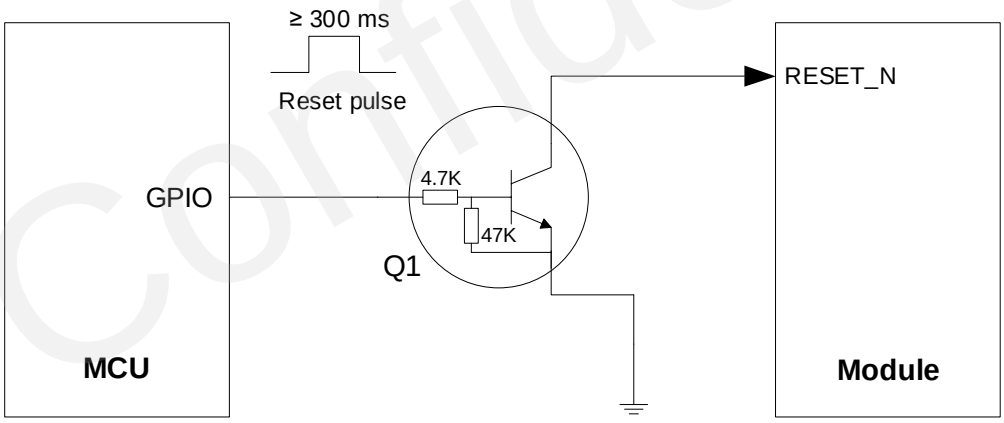


Figure 17: Reference Design of Reset with Driving Circuit

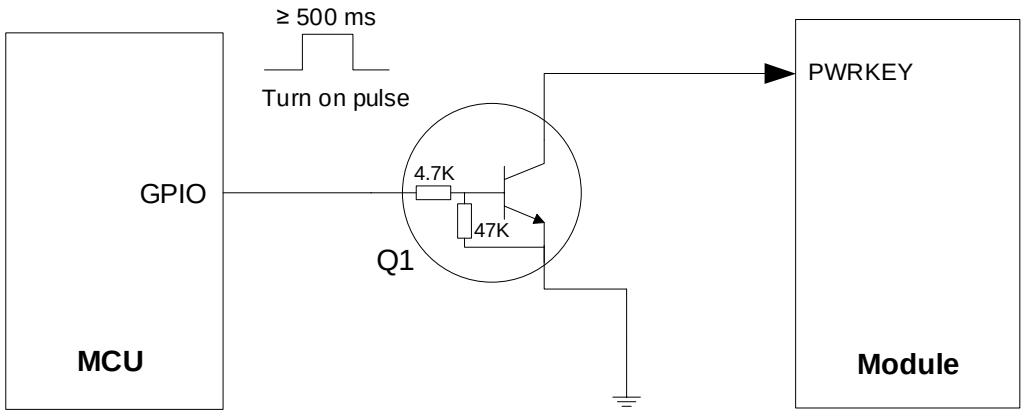


Figure 18: Reference Design of PWRKEY with Driving Circuit

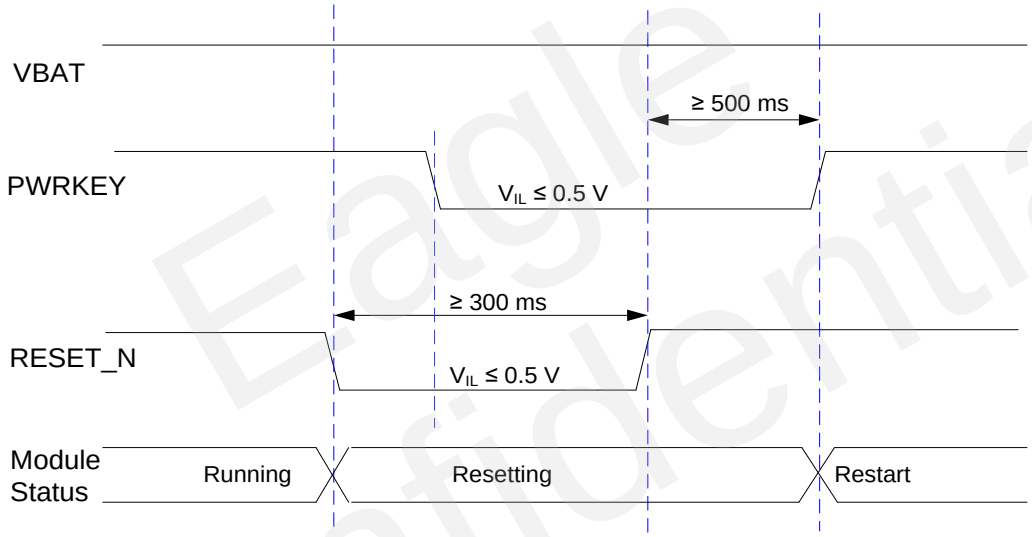


Figure 19: Reset Timing

NOTE

1. In reset timing, pull down PWRKEY when RESET_N is at low level.
2. Ensure the capacitance on PWRKEY and RESET_N does not exceed 10 nF.

4 Application Interfaces

4.1. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specifications and supports high-speed (480 Mbps) and full-speed (12 Mbps) for USB 2.0. The module only supports USB slave mode. The USB interface can be used for AT command communication, data transmission, GNSS NMEA sentence output (**All-in-one** mode only), software debugging, firmware upgrade and the output of partial logs.

Table 12: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	A test point must be reserved.
USB_DP	9	AIO	USB differential data (+)	USB 2.0 compliant. Requires differential impedance of 90 Ω. Test points must be reserved.
USB_DM	10	AIO	USB differential data (-)	

Test points of USB 2.0 interface must be reserved, which can be used for firmware upgrading. Only in download mode, the module supports firmware upgrade over USB 2.0 interface.

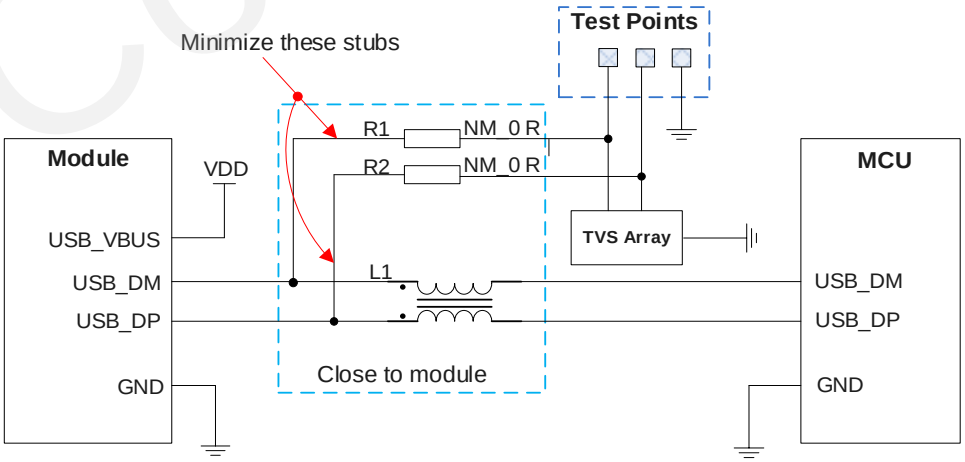


Figure 20: Reference Design of USB 2.0 Interface

It is recommended to add a common-mode choke L1 in series between MCU and the module to suppress EMI. Meanwhile, it is also suggested to add R1 and R2 in series between the module and test points for debugging. These resistors are not mounted by default. To ensure the signal integrity of USB 2.0 data transmission, you should place L1, R1 and R2 close to the module, and keep these resistors close to each other. Moreover, keep extra stubs of trace as short as possible.

To ensure performance, you should follow the following principles when designing USB interface:

- Route USB signal traces as differential pairs with surrounded ground. The impedance of USB 2.0 differential trace is 90 Ω.
- Route USB differential traces at the inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below. For signal traces, provide clearance from power supply traces, crystal-oscillators, magnetic devices, sensitive signals like RF signals, analog signals, noise signals generated by clock and DC-DC.
- Pay attention to the impact caused by stray capacitance of the ESD protection component on USB data lines. Typically, the stray capacitance should be less than 2 pF for USB 2.0.
- Keep the ESD protection components as close to the USB port as possible.

For more details about the USB specifications, visit http://www.usb.org/home.

4.2. USB_BOOT

The module provides a USB_BOOT pin for download. Pulling up USB_BOOT to VDD_EXT before turning on the module, and then the module will enter download mode. Only in this mode, the module supports firmware upgrade over USB 2.0 interface.

Table 13: Pin Description of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Make the module into download mode	Active high before power-up. A test point must be reserved.

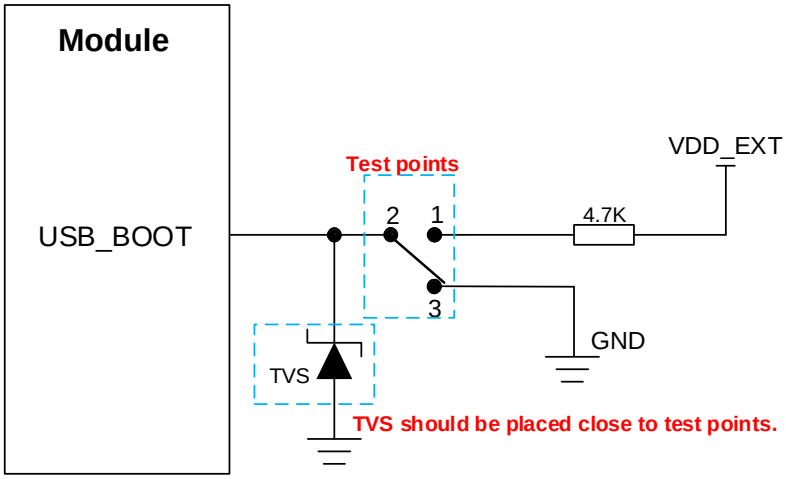


Figure 21: Reference Design of USB_BOOT

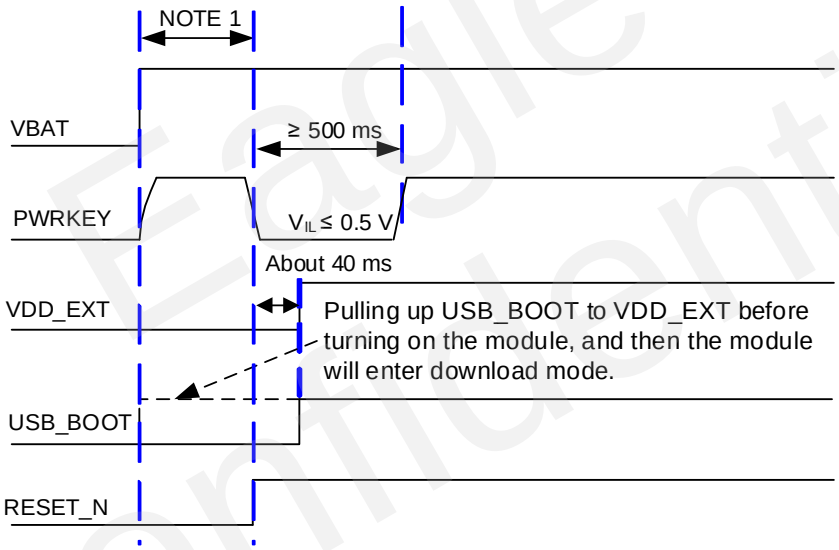


Figure 22: Timing of Entering Download Mode

NOTE

1. Ensure VBAT is stable before driving PWRKEY low.
2. Follow the above timing when using MCU control the module to enter the forced download mode.
3. If you need to manually force the module to enter download mode, directly connect the test points shown in ***Figure 21***.
4. The firmware upgrade function of USB interface can only be used in download mode. It is strongly recommended to lead out USB_BOOT and VDD_EXT together with the USB interface.

4.3. USIM Interfaces

The USIM interfaces meets ETSI and IMT-2000 requirements.

- USIM1 interface supports 1.8 V or 3.0 V power domain.
- USIM2 interface only supports 1.8 V power domain.
- When USIM1 and USIM2 are used at the same time, the power domain of USIM interfaces should be 1.8 V. Otherwise, USIM2 interface will be damaged.
- USIM interfaces support Dual SIM Single Standby.
- USIM2 and Camera SPI* cannot be used at the same time.

Table 14: Pin Description of USIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	43	PO	USIM1 card power supply	Either 1.8 V or 3.0 V USIM1 card is supported and can be identified automatically by the module.
USIM1_DATA	45	DIO	USIM1 card data	
USIM1_CLK	46	DO	USIM1 card clock	
USIM1_RST	44	DO	USIM1 card reset	
USIM1_DET	42	DI	USIM1 card hot-plug detect	If unused, keep it open.
USIM2_VDD	87	PO	USIM2 card power supply	Connected with USIM1_VDD inside the module. 1.8 V power domain is required for USIM2. Otherwise, this interface will be damaged.
USIM2_DATA	86	DIO	USIM2 card data	Connected with pin 97 (CAM_SPI_DATA0) internally. 1.8 V power domain is required for USIM2. Otherwise, this interface will be damaged.
USIM2_RST	85	DO	USIM2 card reset	Connected with pin 78 (CAM_SPI_CLK) internally. 1.8 V power domain is required for USIM2. Otherwise, this interface will be damaged.
USIM2_CLK	84	DO	USIM2 card clock	Connected with pin 115 (CAM_PWDN) internally. 1.8 V power domain is required for USIM2. Otherwise, this interface will be damaged.

The module supports USIM1 card hot-plug via the USIM1_DET, and both high-level and low-level detections are supported. Hot-plug function is disabled by default and you can use **AT+QSIMDET** to configure this function. See ***document [2]*** for more details. Only USIM1 supports hot-plug detection.

The following figure illustrates a reference design for USIM1 card interface with an 8-pin USIM card connector.

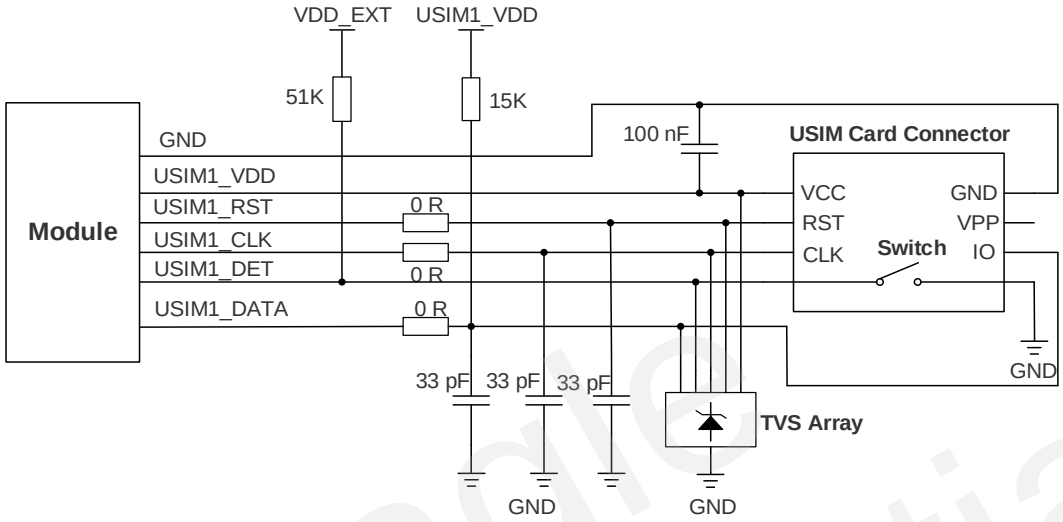


Figure 23: Reference Design of USIM1 Interface with an 8-pin USIM Card Connector

If the function of USIM1 card hot-plug is not needed, keep USIM1_DET disconnected. A reference design for USIM interfaces with a 6-pin USIM card connector is illustrated in the following figure.

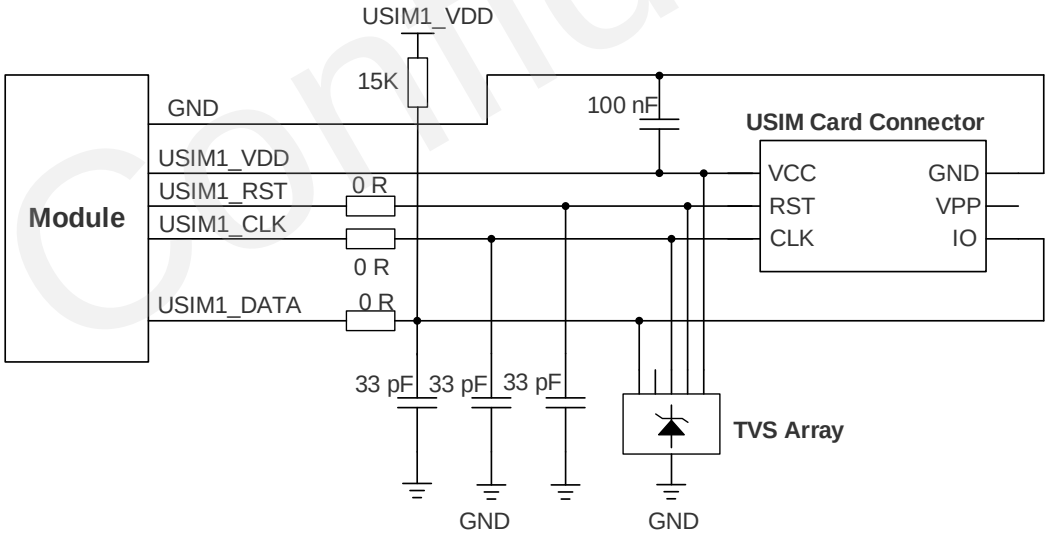


Figure 24: Reference Design of USIM1 Interface with a 6-pin USIM Card Connector

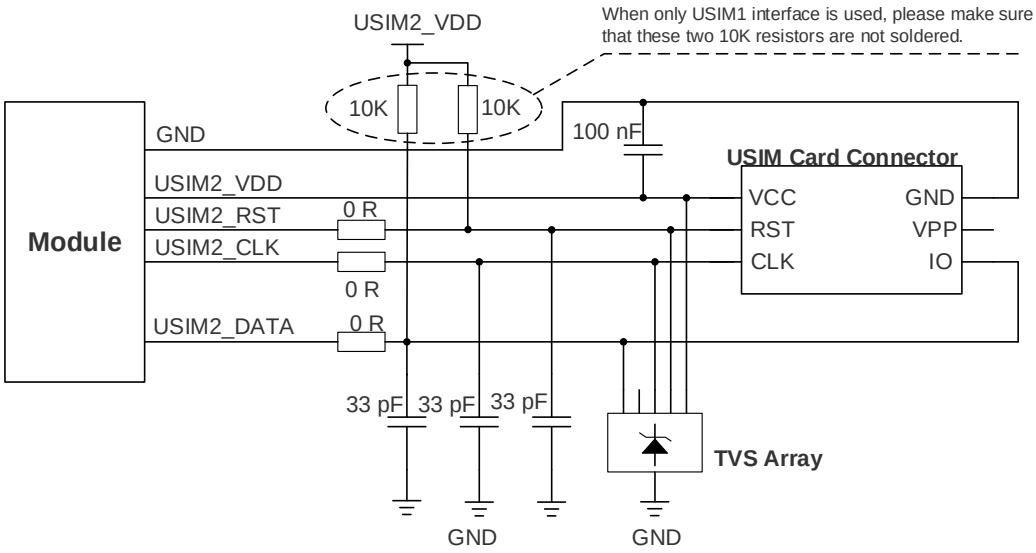


Figure 25: Reference Design of USIM2 Interface with a 6-pin USIM Card Connector

To enhance the reliability and availability of the USIM cards in applications, follow the principles below in the USIM circuit design:

- Place the USIM card connector close to the module. Keep the trace length as short as possible and at most 200 mm.
- Route USIM card traces at the inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below. For signal traces, provide spacing from power supply traces, crystal-oscillators, magnetic devices, sensitive signals such as RF signals, analog signals, and noise signals generated by clock, DC-DC.
- Ensure the tracing between the USIM card connector and the module is short and wide. Keep the trace width of ground and USIM_VDD at least 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep the traces away from each other and shield them with surrounded ground.
- To offer good ESD protection, it is recommended to add a TVS array of which parasitic capacitance should be less than 15 pF. Add 0 Ω resistors in series between the module and the USIM card connector to facilitate debugging. The 33 pF capacitors are used for filtering out RF interference. Additionally, keep the USIM peripheral circuit close to the USIM card connector.
- The pull-up resistor on USIM1_DATA trace, USIM2_DATA and USIM2_RST can improve anti-jamming capability when long layout trace and sensitive occasions are applied, and should be placed close to the USIM card connector.

4.4. UART

The module provides four UARTs.

Table 15: UART Information (Unit: bps)

UART Types	Supported Baud Rates	Default Baud Rates	Functions
Main UART	4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600	115200	● AT command communication ● data transmission ● RTS and CTS hardware flow control
Debug UART	115200, 3000000	3000000	● Partial logs output
GNSS UART	921600	921600	● GNSS data output ● GNSS NMEA sentence output
GNSS debug UART	3000000	3000000	● GNSS system logs output

Table 16: Pin Description of UART

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	36	DO	Clear to send signal from the module	Connect to MCU's CTS. If unused, keep it open.
MAIN_RTS	37	DI	Request to send signal to the module	Connect to MCU's RTS. If unused, keep it open.
MAIN_RXD	34	DI	Main UART receive	If unused, keep them open.
MAIN_DCD	38	DO	Main UART data carrier detect	
MAIN_TXD	35	DO	Main UART transmit	
MAIN_RI	39	DO	Main UART ring indication	
MAIN_DTR	30	DI	Main UART data terminal ready	
DBG_RXD	22	DI	Debug UART receive	Test points must be reserved.
DBG_TXD	23	DO	Debug UART transmit	
GNSS_TXD [9]	27	DO	GNSS UART transmit	Test points are

[9] This pin is optional. If you need this function, please contact Eagle Technical Support.

GNSS_RXD [9]	28	DI	GNSS UART receive	recommended to be reserved.
GNSS_DBG_TXD [9]	109	DO	GNSS debug UART transmit	Test points must be reserved.
GNSS_DBG_RXD [9]	110	DI	GNSS debug UART receive	

The module provides 1.8 V UART interfaces. You can use a level-shifting chip between the module and MCU's UART if the MCU is equipped with a 3.3 V UART.

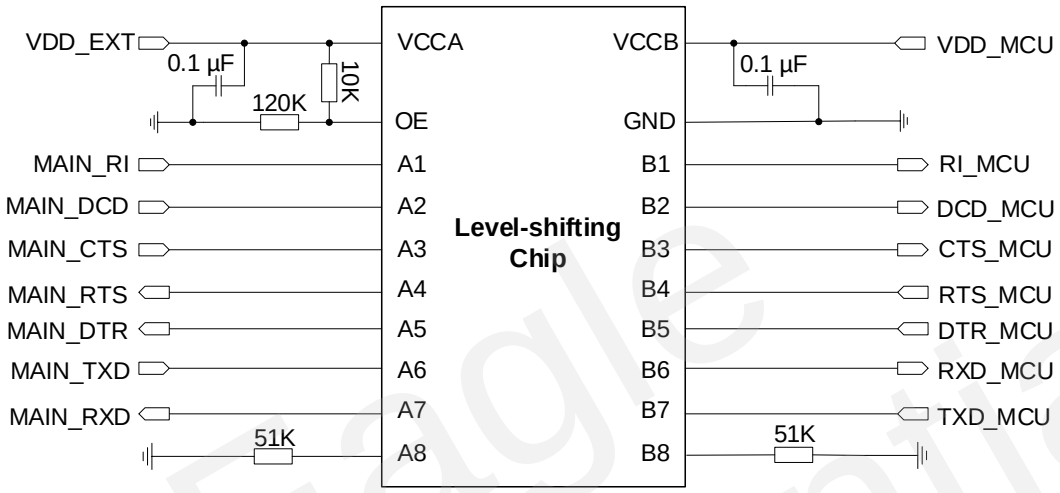


Figure 26: Reference Design of UART with Level-shifting Chip (Main UART)

Another example of level-shifting circuit is shown as below. For the design of circuits in dotted lines, see that shown in solid lines, but pay attention to the direction of the connection.

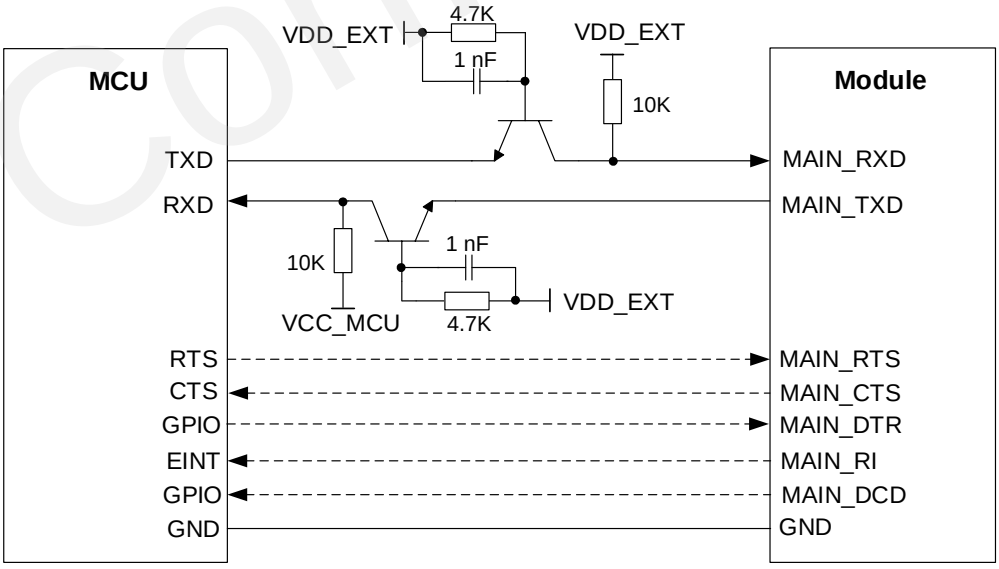


Figure 27: Reference Design of UART with Transistor Level-shifting Circuit (Main UART)

NOTE

1. Transistor circuit solution above is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to MCU's CTS, and the module's RTS is connected to MCU's RTS.
3. The level-shifting circuits (***Figure 26*** and ***Figure 27***) take the main UART as an example. The circuits of debug UART, GNSS UART and GNSS debug UART are connected in the same way as the main UART.
4. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

4.5. PCM and I2C Interfaces*

The module provides one Pulse Code Modulation (PCM) digital interface and one I2C interface.

Table 17: Pin Description of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	5	DO	PCM data frame sync	If unused, keep them open.
PCM_CLK	4	DO	PCM clock	
PCM_DIN	6	DI	PCM data input	
PCM_DOUT	7	DO	PCM data output	
I2C_SCL	40	OD	I2C serial clock	External pull-up resistor is required. If unused, keep them open.
I2C_SDA	41	OD	I2C serial data	

The reference design is illustrated as follows.

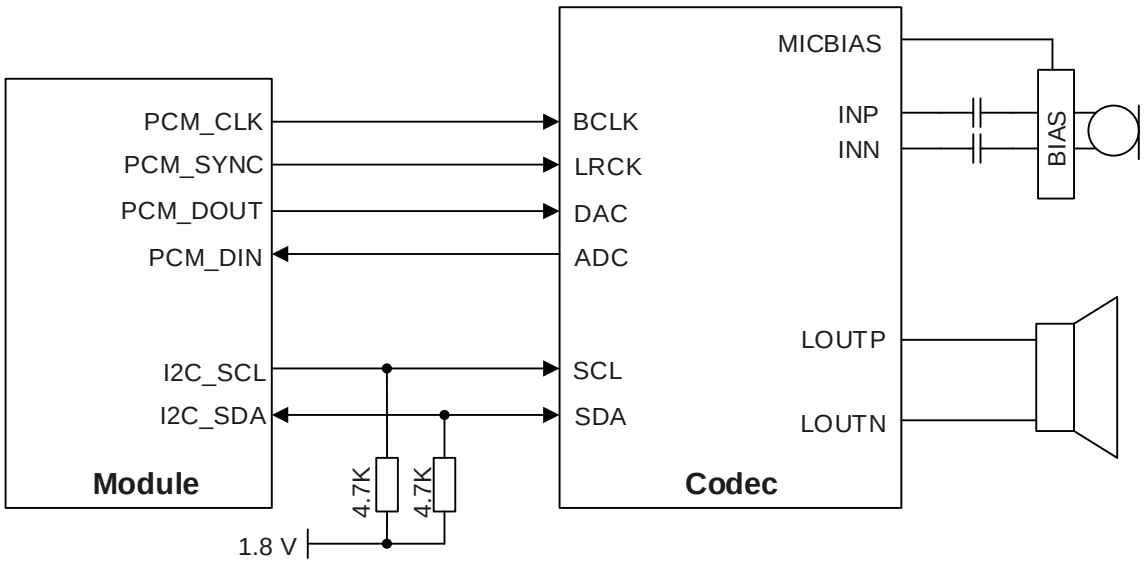


Figure 28: Reference Design of PCM and I2C Interfaces

NOTE

1. It is recommended to reserve RC circuits (R = 22 Ω, C = 22 pF) on the PCM signal traces, especially on the PCM_CLK pin.
2. The module can only be used as a master device in applications related to both the PCM interface and the I2C interface.

4.6. ADC Interfaces

The module provides two Analog-to-Digital Converter (ADC) interfaces. To improve the accuracy of ADC, surround the trace of ADC with ground.

Table 18: Pin Description of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	General-purpose ADC interface	If unused, keep them open.
ADC1	2	AI	General-purpose ADC interface	

With **AT+QADC=<port>**, you can:

- **AT+QADC=0**: read the voltage value on ADC0

- **AT+QADC=1**: read the voltage value on ADC1

For more details about the AT command, see ***document [2]***.

Table 19: Characteristics of ADC Interfaces

Parameters	Min.	Typ.	Max.	Units
ADC0 input voltage range	0	-	1.2	V
ADC input resistance	0.26	-	0.75	MΩ
ADC resolution	-	12	-	bits

NOTE

1. The input voltage of every ADC interface should not exceed 1.2 V.
2. It is prohibited to directly supply any voltage to ADC Interfaces when the module is not powered by the VBAT.
3. It is recommended to use resistor divider circuit for ADC interface application. Resistance of the external resistor divider should not exceed 100 kΩ, and the divider resistor accuracy should not higher than 1 %, otherwise the measurement accuracy of ADC would be significantly reduced. It is recommended to reserve a 100 nF capacitor for the design.

4.7. Camera SPI*

The module provides one camera SPI supporting SPI dual-wire data transmission. USIM2 and Camera SPI cannot be used at the same time.

Table 20: Pin Description of Camera SPI

Pin Name	Pin No.	I/O	Description	Comment
CAM_MCLK	95	DO	Master clock of the camera	If unused, keep it open.
CAM_SPI_CLK	78	DI	Camera SPI clock	Connected with pin 85 (USIM2_RST) internally. If unused, keep it open.
CAM_SPI_DATA0	97	DI	Camera SPI data bit 0	Connected with pin 86 (USIM2_DATA) internally. If unused, keep it open.

CAM_SPI_DATA1	98	DI	Camera SPI data bit 1	If unused, keep it open.
CAM_PWDN	115	DO	Power down of the camera	Connected with pin 84 (USIM2_CLK) internally. If unused, keep it open.
CAM_VDD	94	PO	Camera analog power supply	If unused, keep them open.
CAM_VDDIO	93	PO	Camera digital power supply	

4.8. GRFC Interfaces

The module provides two GRFC (generic RF control) interfaces for the control of external antenna tuners.

Table 21: Pin Description of GRFC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GRFC1	76	DO	Generic RF controller	If unused, keep them open.
GRFC2	77	DO	Generic RF controller	

4.9. Control Signals

Table 22: Pin Description of Control Signals

Pin Name	Pin No.	I/O	Description	Comment
W_DISABLE#*	18	DI	Airplane mode control	If unused, keep them open.
PSM_IND*	1	DO	Indicate the module's power saving mode	
PSM_INT*	96	DI	External interrupt; wake up the module from power saving mode	
AP_READY*	19	DI	Application processor ready	

4.9.1. W_DISABLE#*

The module provides W_DISABLE# to enable or disable RF function. When the voltage level of W_DISABLE# is high, you can send **AT+CFUN=<fun>** to set the module's operating mode. For the details of this command, see ***document [2]***. Driving W_DISABLE# low will set the module to airplane mode.

Table 23: W_DISABLE# AT Command Configuration Information

Level Status	AT Command	RF Function	Operating Mode
High level	**AT+CFUN=1**	Enabled	Full functionality mode
	AT+CFUN=0	Disabled	Minimum functionality mode
	AT+CFUN=4	Disabled	Airplane mode
Low level	**AT+CFUN=0** **AT+CFUN=1** **AT+CFUN=4**	Disabled	Airplane mode

4.10. Indication Signals

Table 24: Pin Description of Indication Signals

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module's operation status	If unused, keep them open.
NET_STATUS	21	DO	Indicate the module's network activity status	
GNSS_PPS [10]	51	DO	GNSS pulse per second output	

4.10.1. Network Status Indication

The module provides one network status indication pin: the NET_STATUS for the module's network operation status indication, which can drive corresponding LEDs.

[10] This pin is optional. If you need this function, please contact Eagle Technical Support.

Table 25: Network Status Indication Pin Level and Module Network Status

Pin Name	NET_STATUS Level Status	Module Network Status
NET_STATUS	Blink slowly (200 ms High/1800 ms Low)	Network searching
	Blink slowly (1800 ms High/200 ms Low)	Idle
	Blink quickly (125 ms High/125 ms Low)	Data transmission is ongoing

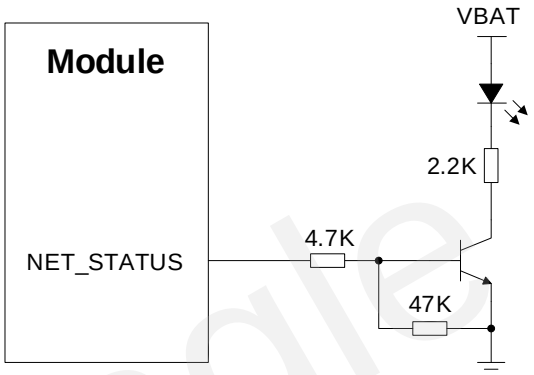


Figure 29: Reference Design of NET_STATUS Indication

4.10.2. STATUS

The STATUS is used for indicating the module's operation status. It will output high level when the module is turned on.

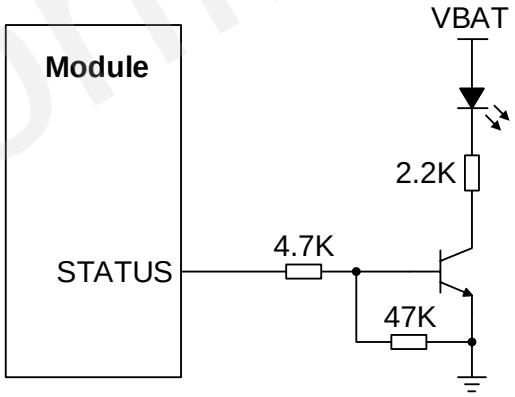


Figure 30: Reference Design of STATUS

4.10.3. MAIN_RI

AT+QCFG= "risignaltype", "physical" can be used to configure MAIN_RI behavior. No matter on which port a URC information is presented, the URC information will trigger the behavior of the MAIN_RI. For the details of **AT+QCFG**, see ***document [2]***.

NOTE

The **AT+QURCCFG** allows you to set the main UART, USB AT port or USB modem port as the URC information output port. The USB AT port is the URC output port by default. For more details about **AT+QURCCFG**, see ***document [2]***.

You can configure MAIN_RI behaviors flexibly. The default behaviors of the MAIN_RI are shown as below.

Table 26: MAIN_RI Level and Module Status

Module Status	MAIN_RI Level Status
Idle	High level
When a new URC information returns	MAIN_RI will output a low level for at least 120 ms. After this pin changes to a high level, the module starts to output data.

Indication behavior for MAIN_RI can be configured via **AT+QCFG="urc/ri/ring"**.

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. LTE/Wi-Fi Scan Antenna Interface

5.1.1. Antenna Interface & Frequency Bands

Table 27: Pin Description of LTE/Wi-Fi Scan Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN [11]	60	AIO	Main antenna/Wi-Fi Scan antenna interface	50 Ω impedance.

NOTE

Wi-Fi Scan function shares the same antenna interface with the main antenna. These two antennas should use TDM (Time Division Multiplexing) and cannot be used simultaneously. Wi-Fi Scan only supports receiving and does not support transmitting.

Table 28: Operating Frequency of I4915Q-NA (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE-FDD B2	1850–1910	1930–1990
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894
LTE-FDD B12	699–716	729–746

[11] ANT_MAIN only supports passive antennas.

LTE-FDD B13	777–787	746–756
LTE-FDD B66	1710–1780	2110–2180

Table 29: Operating Frequency of I4915Q-AF (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE-FDD B2	1850–1910	1930–1990
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894
LTE-FDD B12	699–716	729–746
LTE-FDD B13	777–787	746–756
LTE-FDD B14	788-798	758-768
LTE-FDD B66	1710–1780	2110–2180
LTE-FDD B71	663-698	617-652

Table 30: Operating Frequency of I4916Q-GL (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B2	1850–1910	1930–1990
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B12	699–716	729–746
LTE-FDD B13	777–787	746–756
LTE-FDD B18	815–830	860–875

LTE-FDD B19	830–845	875–890
LTE-FDD B20	832–862	791–821
LTE-FDD B25	1850–1915	1930–1995
LTE-FDD B26	814–849	859–894
LTE-FDD B28	703–748	758–803
LTE-TDD B34	2010–2025	2010–2025
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B39	1880–1920	1880–1920
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2496–2690	2496–2690
LTE-FDD B66	1710–1780	2110–2180

5.1.2. Tx Power

Table 31: RF Transmitting Power

Frequency Bands	Max.	Min.
LTE bands	23 dBm ±2 dB	< -39 dBm

5.1.3. Rx Sensitivity

Table 32: Conducted RF Receiver Sensitivity of I4915Q-NA (Unit: dBm)

Frequency Bands	Receiver Sensitivity (Typ.)	3GPP
	Primary	
LTE-FDD B2 (10 MHz)	-98 dBm	-91.3 dBm
LTE-FDD B4 (10 MHz)	-98.5 dBm	-93.3 dBm
LTE-FDD B5 (10 MHz)	-99 dBm	-91.8 dBm
LTE-FDD B12 (10 MHz)	-98.5 dBm	-90.3 dBm

LTE-FDD B13 (10 MHz)	-98.5dBm	-90.3 dBm
LTE-FDD B66 (10 MHz)	-98.5 dBm	-92.8 dBm

Table 33: Conducted RF Receiver Sensitivity of I4915Q-AF (Unit: dBm)

Frequency Bands	Receiver Sensitivity (Typ.)	3GPP
	Primary	
LTE-FDD B2 (10 MHz)	-98 dBm	-91.3 dBm
LTE-FDD B4 (10 MHz)	-98.5 dBm	-93.3 dBm
LTE-FDD B5 (10 MHz)	-99 dBm	-91.8 dBm
LTE-FDD B12 (10 MHz)	-98.5 dBm	-90.3 dBm
LTE-FDD B13 (10 MHz)	-98.5 dBm	-90.3 dBm
LTE-FDD B14 (10 MHz)	-98.5 dBm	-90.3 dBm
LTE-FDD B66 (10 MHz)	-98.5 dBm	-92.8 dBm
LTE-FDD B71 (10 MHz)	-98 dBm	-90.5 dBm

Table 34: Conducted RF Receiver Sensitivity of I4916Q-GL (Unit: dBm)

Frequency Bands	Receiver Sensitivity (Typ.)	3GPP
	Primary	
LTE-FDD B1 (10 MHz)	-98.6 dBm	-93.3 dBm
LTE-FDD B2 (10 MHz)	-99.4 dBm	-91.3 dBm
LTE-FDD B3 (10 MHz)	-98.9 dBm	-90.3 dBm
LTE-FDD B4 (10 MHz)	-98.6 dBm	-93.3 dBm
LTE-FDD B5 (10 MHz)	-99.1 dBm	-91.8 dBm
LTE-FDD B7 (10 MHz)	-97.4 dBm	-91.3 dBm
LTE-FDD B8 (10 MHz)	-99.3 dBm	-90.8 dBm
LTE-FDD B12 (10 MHz)	-99.5 dBm	-90.3 dBm

LTE-FDD B13 (10 MHz)	-98.3 dBm	-90.3 dBm
LTE-FDD B18 (10 MHz)	-99.3 dBm	-93.8 dBm
LTE-FDD B19 (10 MHz)	-99.1 dBm	-93.3 dBm
LTE-FDD B20 (10 MHz)	-99.8 dBm	-90.8 dBm
LTE-FDD B25 (10 MHz)	-99.4 dBm	-89.8 dBm
LTE-FDD B26 (10 MHz)	-98.9 dBm	-91.3 dBm
LTE-FDD B28 (10 MHz)	-98.6 dBm	-92.3 dBm
LTE-TDD B34 (10 MHz)	-99.2 dBm	-93.8 dBm
LTE-TDD B38 (10 MHz)	-97.6 dBm	-93.3 dBm
LTE-TDD B39 (10 MHz)	-99.8 dBm	-93.8 dBm
LTE-TDD B40 (10 MHz)	-98 dBm	-93.8 dBm
LTE-TDD B41 (10 MHz)	-97.7 dBm	-91.8 dBm
LTE-FDD B66 (10 MHz)	-98.6 dBm	-92.8 dBm

5.1.4. Reference Design

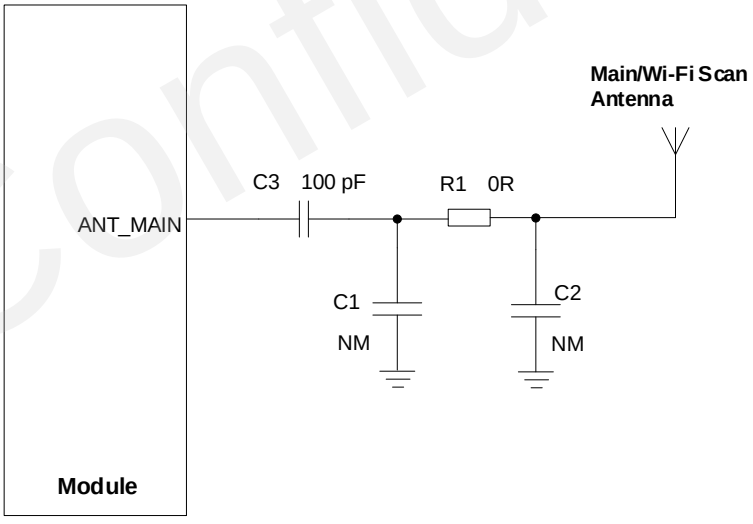


Figure 31: Reference Design of Main/Wi-Fi Scan Antenna

NOTE

1. Use a dual L-type matching circuit for the antenna interface for better cellular performance and for the ease of debugging.
2. Capacitors C1 and C2 are not mounted by default.
3. Place the dual L-type matching components (R1 & C1 & C2 & C3) to the antenna as close as possible.
4. Notes on C3:
   1) If there is DC power at the antenna ports, place capacitor on C3 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
   2) If there is no DC power in the peripheral design:
      a) Do not reserve C3.
      b) If C3 has already been reserved, it should be mounted with components, and it is recommended to use 0 Ω resistors. You can also match the component according to the debugging results.

5.2. GNSS (Optional)

5.2.1. Antenna Interface & Frequency Bands

The GNSS part of the module supports GPS, GLONASS, BDS, Galileo, and QZSS systems.

Table 35: Pin Description of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	49	AI	GNSS antenna interface	50 Ω impedance.

Table 36: GNSS Frequency (Unit: MHz)

GNSS Constellation Type	Frequency
GPS	1575.42 ±1.023 (L1)
GLONASS	1597.5–1605.8 (L1)
BDS	1561.098 ±2.046 (B1I)
Galileo	1575.42 ±2.046 (E1)

QZSS	1575.42 ±1.023 (L1)

5.2.2. GNSS Performance

Table 37: GNSS Performance of I4915Q Series

Parameter	Description	Conditions	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-145	dBm
	Reacquisition		-157	
	Tracking		-166	
TTFF	Cold start @ open sky	Autonomous	27.43	s
		AGPS enabled	5.6	
	Warm start @ open sky	Autonomous	27.37	
	Hot start @ open sky	Autonomous	2.56	
Accuracy	CEP-50	Autonomous @ open sky	2.5	m

Table 38: GNSS Performance of I4916Q-GL

Parameter	Description	Conditions	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-146	dBm
	Reacquisition		-159	
	Tracking		-166	
TTFF	Cold start @ open sky	Autonomous	24.96	s
		AGPS enabled	11.3	
	Warm start @ open sky	Autonomous	24.36	
	Hot start @ open sky	Autonomous	2.22	
Accuracy	CEP-50	Autonomous @ open sky	2.5	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.3. Reference Design

In any case, it is recommended to use a passive antenna. However, if an active antenna is needed in your application, it is recommended to reserve a π-type attenuation circuit and use a high-performance LDO in the power system design.

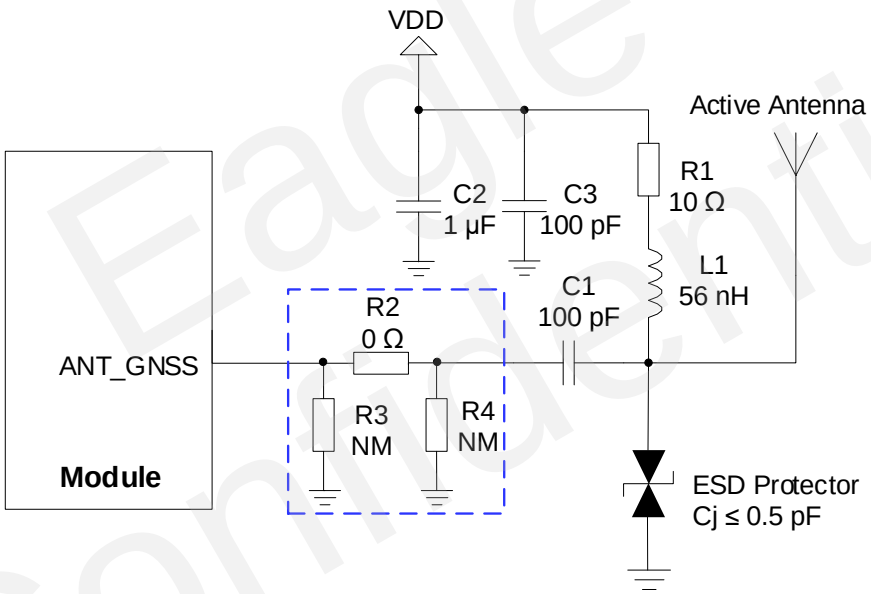


Figure 32: Reference Design of GNSS Antenna

NOTE

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.
3. Notes on C1:
   1) If there is DC power at the antenna ports, place capacitor on C1 to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to the debugging results.
   2) If there is no DC power in the peripheral design:

a) Do not reserve C1.
b) If C1 has already been reserved, it should be mounted with components, and it is recommended to use 0 Ω resistors. You can also match the component according to the debugging results.

5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

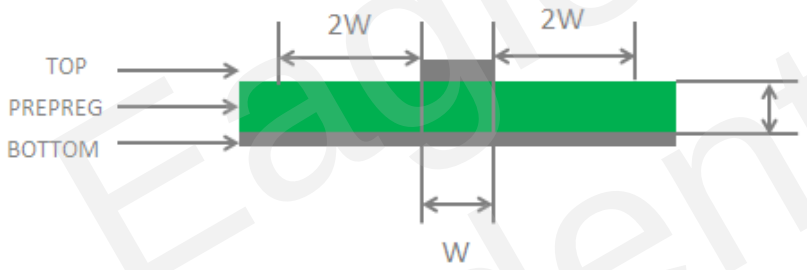


Figure 33: Microstrip Design on a 2-layer PCB

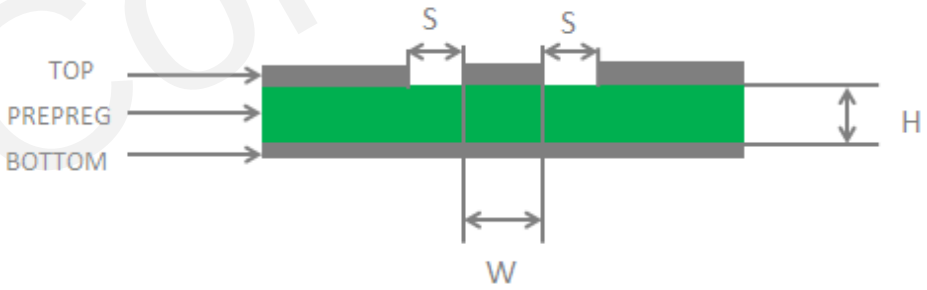


Figure 34: Coplanar Waveguide Design on a 2-layer PCB

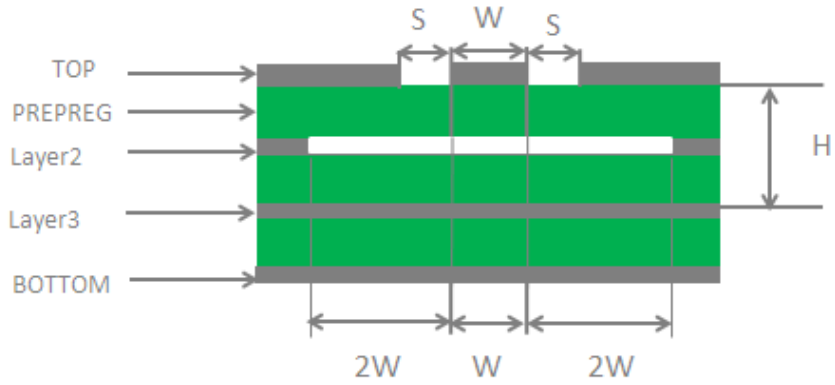


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

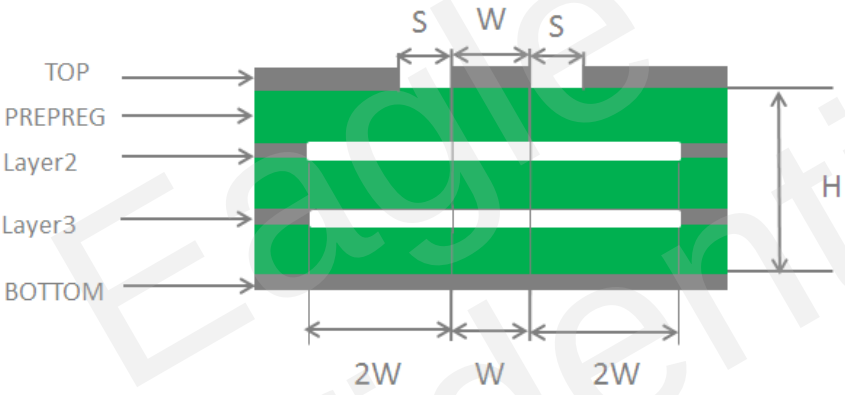


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
  Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [5]***.

5.4. Antenna Design Requirements

Table 39: Requirements for Antenna Design

Antenna Types	Requirements
GNSS (Optional)	● Frequency range: 1559–1609 MHz ● Polarization: RHCP or linear ● VSWR: ≤ 2 (Typ.)
	For passive antenna usage: ● Passive antenna gain: > 0 dBi
	For active antenna usage: ● Active antenna noise figure: < 1.5 dB ● Active antenna embedded LNA gain: < 17 dB
Cellular/Wi-Fi Scan	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Gain: 1 dBi ● Max. input power: 50 W ● Input impedance: 50 Ω ● Vertical polarization ● Cable insertion loss: **< 1 dB:** LB (<1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)

NOTE

It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

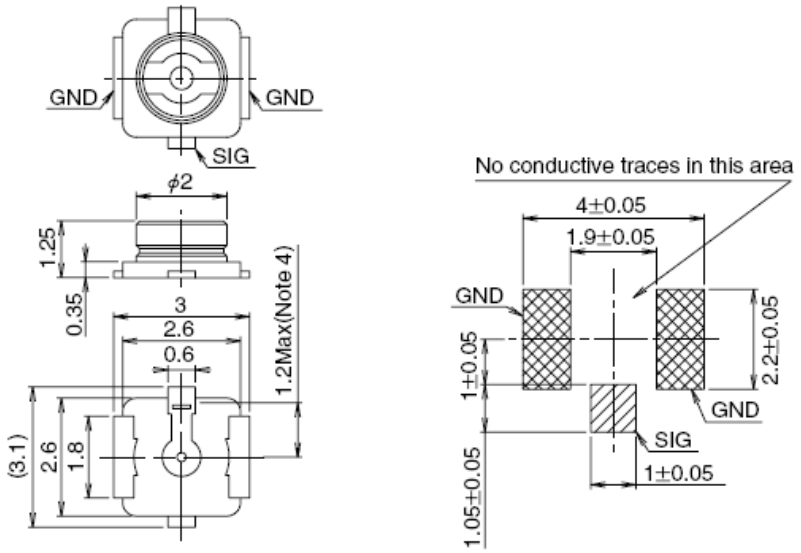


Figure 37: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

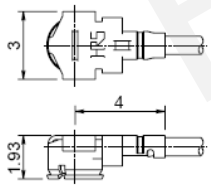
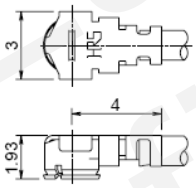
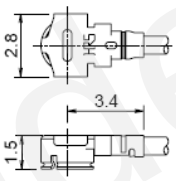
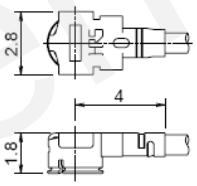
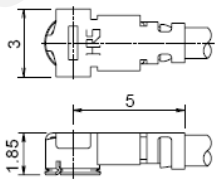
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 38: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors.

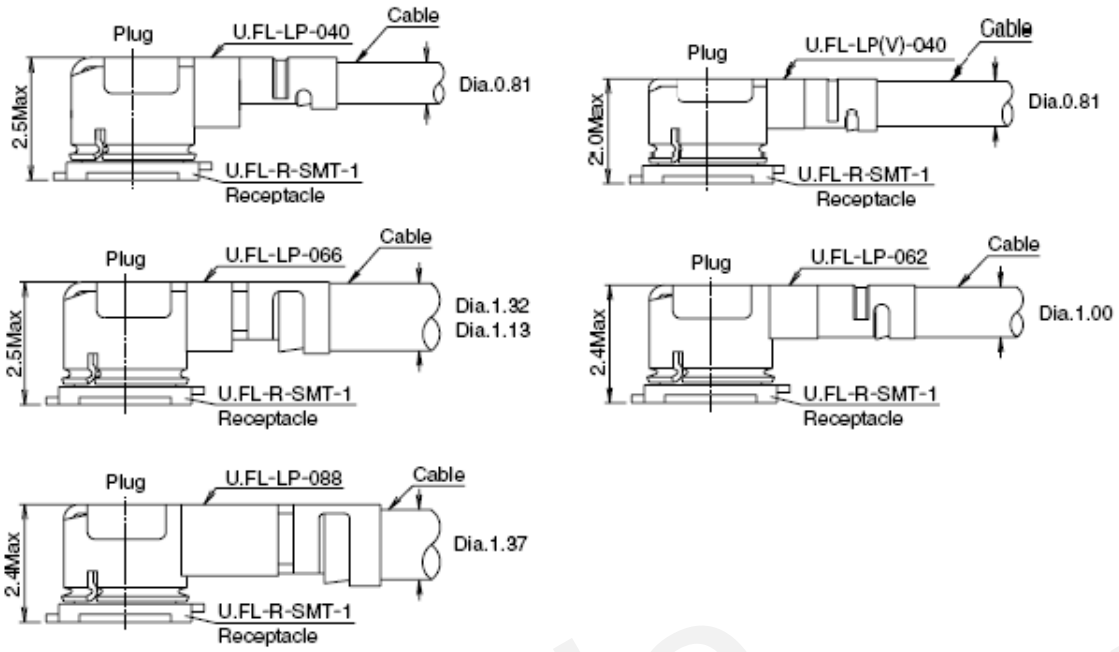


Figure 39: Space Factor of Mated Connectors (Unit: mm)

For more details, please visit http://www.hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Table 40: Absolute Maximum Ratings

Parameters	Min.	Max.	Unit
Voltage at VBAT_RF & VBAT_BB	-0.3	5	V
Voltage at USB_VBUS	-0.3	5.25	V
Voltage at GNSS_VBCKP	-0.3	3.63	V
Voltage at digital pins	-0.3	2.3	V

6.2. Power Supply Ratings

Table 41: Power Supply Ratings

Parameters	Descriptions	Conditions	Min.	Typ.	Max.	Units
VBAT	VBAT_BB & VBAT_RF	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V
GNSS_ VBCKP	Power supply for GNSS RTC		1.9	3.3	3.6	V
I_{VBAT}	Peak power consumption	At maximum power control level	-	-	1.0	A
USB_VBUS	USB connection detection	-	3.0	5.0	5.25	V

6.3. Power Consumption

Table 42: Power Consumption of I4915Q-NA LTE Part (GNSS Part Off)

Description	Conditions	Typ.	Units
OFF state	Power down	0.4	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	54	μA
	AT+CFUN=4 (USB disconnected)	130	μA
	LTE-FDD @ PF = 32 (USB disconnected)	1.24	mA
	LTE-FDD @ PF = 64 (USB disconnected)	0.68	mA
	LTE-FDD @ PF = 128 (USB disconnected)	0.41	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.3	mA
Idle state	LTE-FDD @ PF = 64 (USB disconnected)	4.55	mA
	LTE-FDD @ PF = 64 (USB connected)	25.31	mA
LTE data transmission	LTE-FDD B2	629	mA
	LTE-FDD B4	570	mA
	LTE-FDD B5	544	mA
	LTE-FDD B12	571	mA
	LTE-FDD B13	657	mA
	LTE-FDD B66	543	mA

Table 43: Power Consumption of I4915Q-AF LTE Part (GNSS Part Off)

Description	Conditions	Typ.	Units
OFF state	Power down	0.5	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	61	μA
	AT+CFUN=4 (USB disconnected)	139	μA

	LTE-FDD @ PF = 32 (USB disconnected)	1.12	mA
	LTE-FDD @ PF = 64 (USB disconnected)	0.61	mA
	LTE-FDD @ PF = 128 (USB disconnected)	0.35	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.24	mA
Idle state	LTE-FDD @ PF = 64 (USB disconnected)	4.31	mA
	LTE-FDD @ PF = 64 (USB connected)	24.75	mA
LTE data transmission	LTE-FDD B2	629	mA
	LTE-FDD B4	570	mA
	LTE-FDD B5	544	mA
	LTE-FDD B12	571	mA
	LTE-FDD B13	606	mA
	LTE-FDD B14	548	mA
	LTE-FDD B66	543	mA
	LTE-FDD B71	584	mA

Table 44: Power Consumption of I4916Q-GL LTE Part (GNSS Part Off)

Description	Conditions	Typ.	Units
OFF state	Power down	0.5	μA
PSM	Power Saving Mode	2.2	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	54	μA
	AT+CFUN=4 (USB disconnected)	135	μA
	LTE-FDD @ PF = 32 (USB disconnected)	1.23	mA
	LTE-FDD @ PF = 64 (USB disconnected)	0.68	mA
	LTE-FDD @ PF = 128 (USB disconnected)	0.41	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.31	mA

	LTE-TDD @ PF = 32 (USB disconnected)	1.27	mA
	LTE-TDD @ PF = 64 (USB disconnected)	0.70	mA
	LTE-TDD @ PF = 128 (USB disconnected)	0.42	mA
	LTE-TDD @ PF = 256 (USB disconnected)	0.32	mA
	LTE-FDD @ eDRX Cycle Length 40.96 s PTW = 10.24 s PF = 32 (USB disconnected)	0.28	mA
	LTE-FDD @ eDRX Cycle Length 40.96 s PTW = 10.24s PF = 64 (USB disconnected)	0.15	mA
	LTE-FDD @ eDRX Cycle Length 40.96 s PTW = 10.24s PF = 128 (USB disconnected)	0.09	mA
	LTE-FDD @ eDRX Cycle Length 40.96 s PTW = 10.24s PF = 256 (USB disconnected)	0.07	mA
	LTE-TDD @ eDRX Cycle Length 40.96 s PTW = 10.24s PF = 32 (USB disconnected)	0.29	mA
	LTE-TDD @ eDRX Cycle Length 40.96 s PTW = 10.24s PF = 64 (USB disconnected)	0.16	mA
	LTE-TDD @ eDRX Cycle Length 40.96 s PTW = 10.24s PF = 128 (USB disconnected)	0.09	mA
	LTE-TDD @ eDRX Cycle Length 40.96 s PTW = 10.24s PF = 256 (USB disconnected)	0.07	mA
Idle state	LTE-FDD @ PF = 64 (USB disconnected)	4.56	mA
	LTE-FDD @ PF = 64 (USB connected)	25.80	mA
	LTE-TDD @ PF = 64 (USB disconnected)	4.58	mA
	LTE-TDD @ PF = 64 (USB connected)	25.51	mA
LTE data transmission	LTE-FDD B1	616.3	mA
	LTE-FDD B2	529.6	mA
	LTE-FDD B3	630.0	mA
	LTE-FDD B4	572.3	mA
	LTE-FDD B5	506.0	mA
	LTE-FDD B7	722.3	mA
	LTE-FDD B8	581.2	mA
	LTE-FDD B12	520.1	mA

	LTE-FDD B13	559.8	mA
	LTE-FDD B18	480.0	mA
	LTE-FDD B19	474.9	mA
	LTE-FDD B20	550.9	mA
	LTE-FDD B25	546.5	mA
	LTE-FDD B26	493.8	mA
	LTE-FDD B28	580.5	mA
	LTE-TDD B34	246.8	mA
	LTE-TDD B38	258.6	mA
	LTE-TDD B39	249.8	mA
	LTE-TDD B40	216.3	mA
	LTE-TDD B41	259.46	mA
	LTE-FDD B66	574.4	mA

6.4. Digital I/O Characteristics

Table 45: VDD_EXT I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	1.2	2
V_{IL}	Low-level input voltage	-0.3	0.6
V_{OH}	High-level output voltage	1.35	-
V_{OL}	Low-level output voltage	-	0.45

Table 46: USIM Low-voltage I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	1.2	-
V_{IL}	Low-level input voltage	-	0.6
V_{OH}	High-level output voltage	1.35	-
V_{OL}	Low-level output voltage	-	0.45

Table 47: USIM High-voltage I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	1.95	-
V_{IL}	Low-level input voltage	-	1.0
V_{OH}	High-level output voltage	2.55	-
V_{OL}	Low-level output voltage	-	0.45

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 48: ESD Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %; Unit: kV)

Test Points	Contact Discharge	Air Discharge
VBAT & GND	±8	±12
Antenna interface	±5	±10
Other interfaces	±0.5	±1

6.6. Operating and Storage Temperatures

Table 49: Operating and Storage Temperatures (Unit: °C)

Parameters	Min.	Typ.	Max.
Normal Operating Temperature [12]	-35	+25	+75
Extended Operating Temperature [13]	-40	-	+85
Storage Temperature	-40	-	+90

[12] Within this range, the module's indicators comply with 3GPP specification requirements.

[13] Within this range, the module retains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

7.1.1. Mechanical Dimensions of I4915Q Series

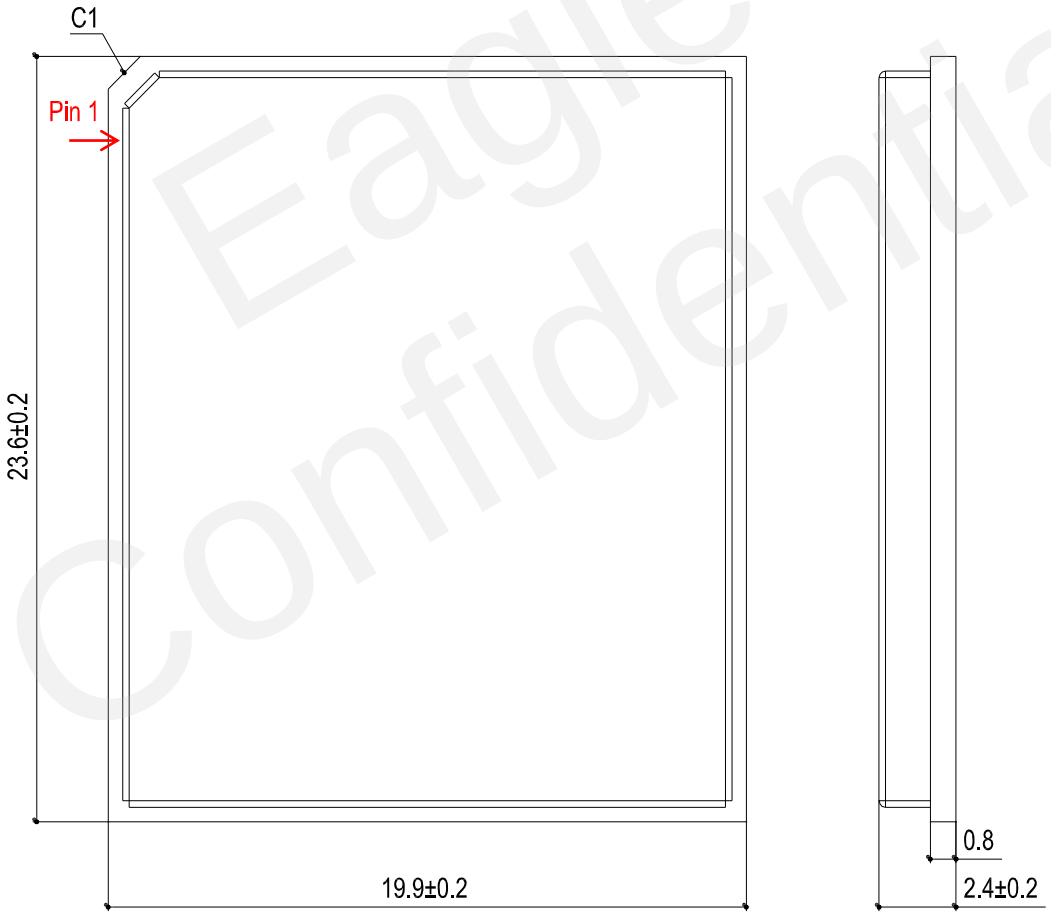


Figure 40: I4915Q Series Top and Side Dimensions (Unit: mm)

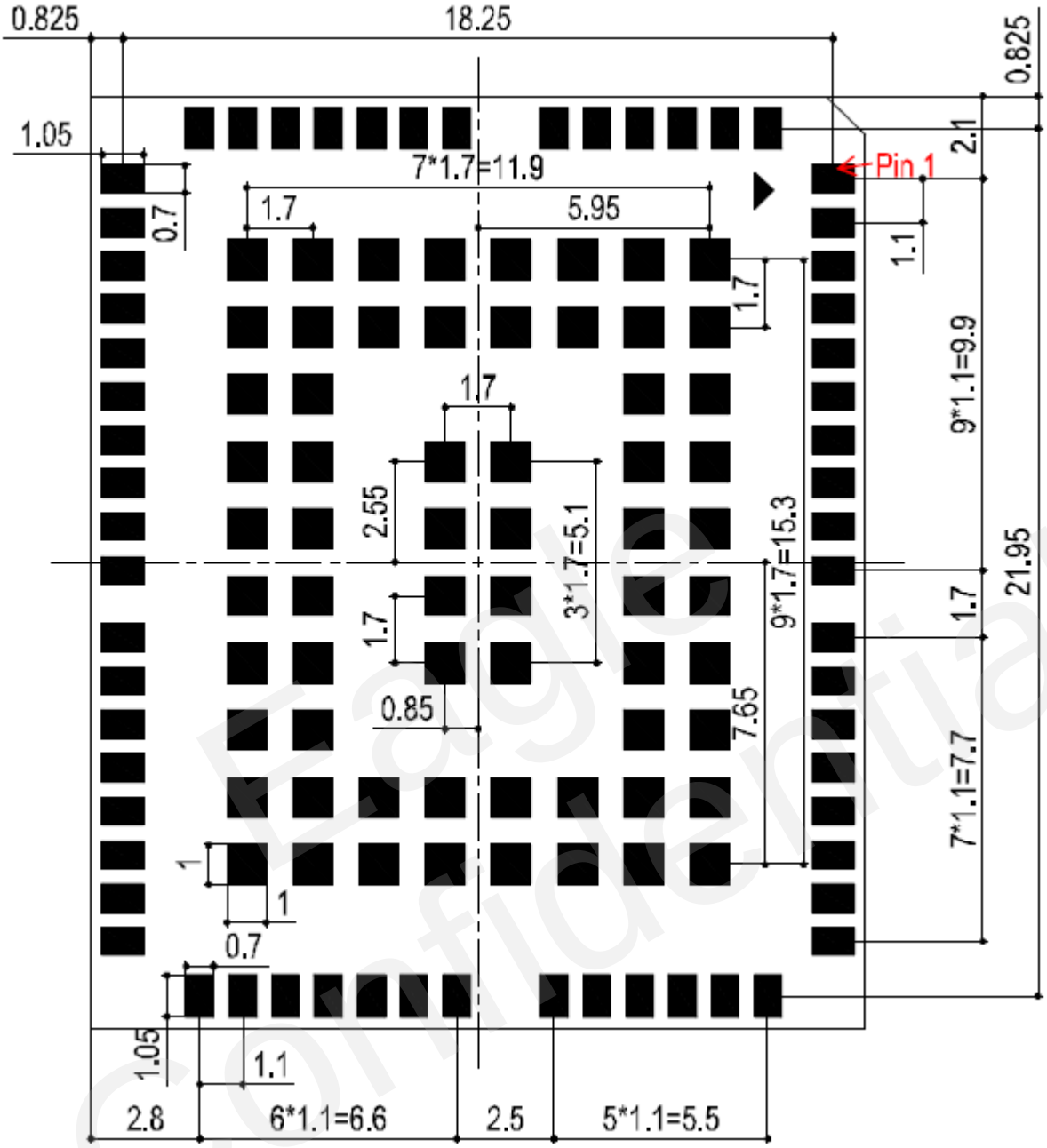


Figure 41: I4915Q Series Bottom Dimension (Bottom View, Unit: mm)

NOTE

The module's coplanarity standard: ≤ 0.13 mm.

7.1.2. Mechanical Dimensions of I4916Q-GL

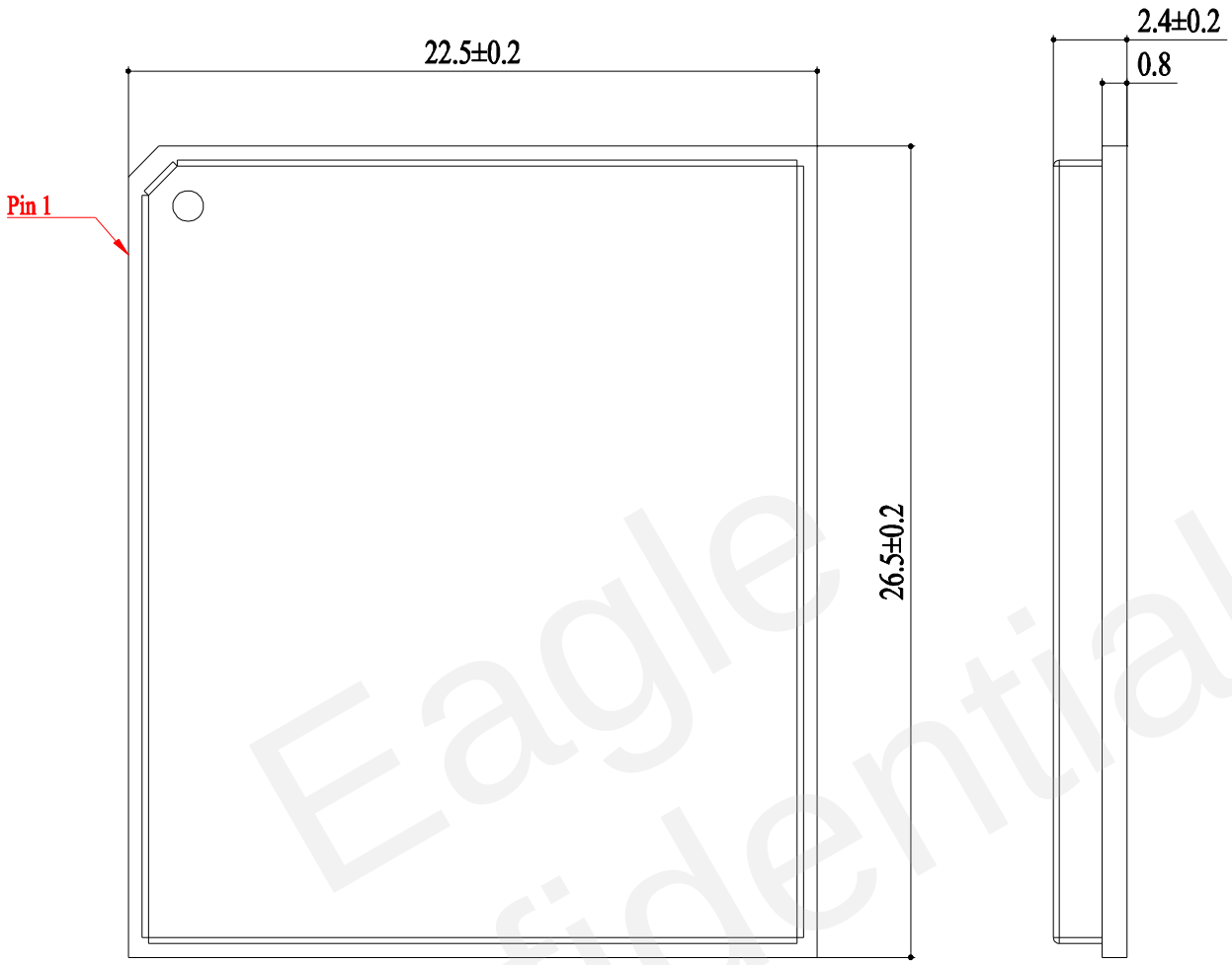


Figure 42: I4916Q-GL Top and Side Dimensions (Unit: mm)

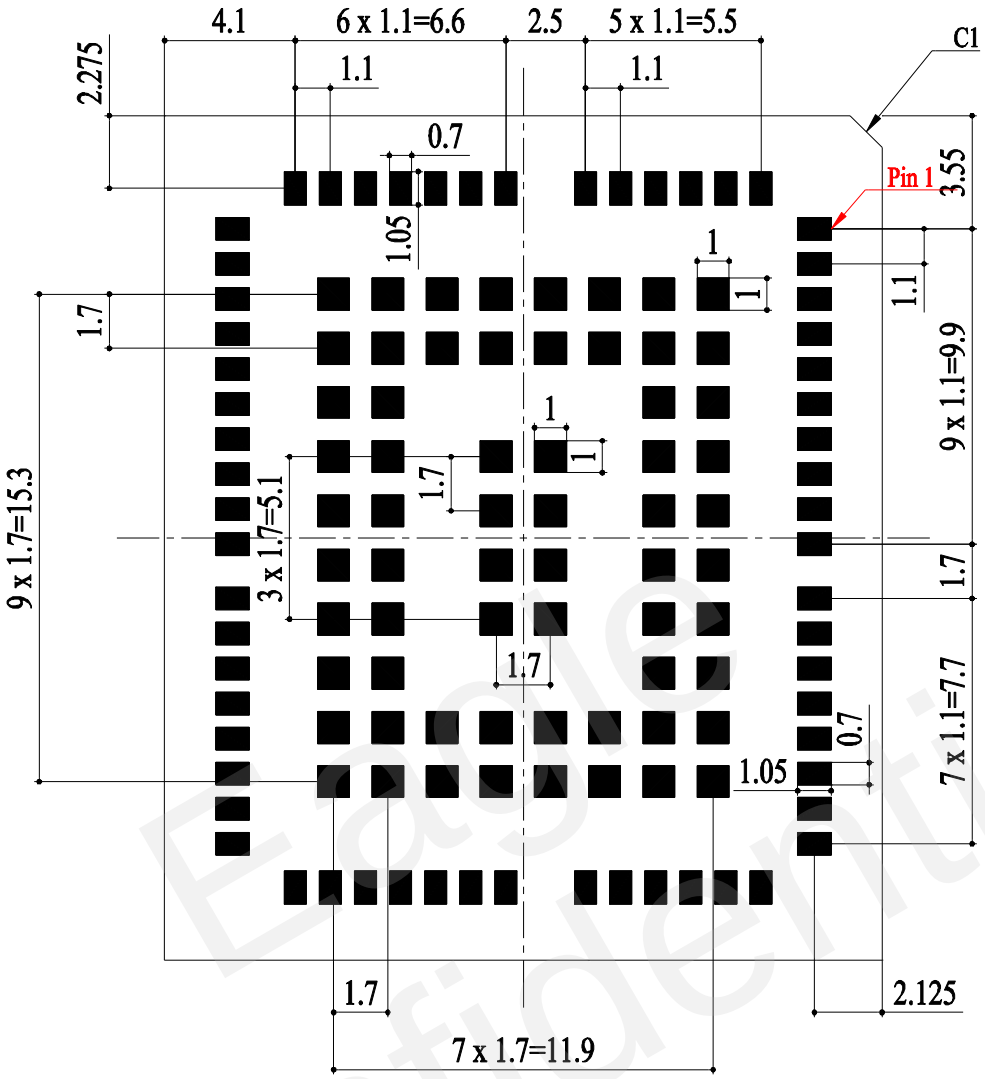


Figure 43: I4916Q-GL Bottom Dimension (Bottom View, Unit: mm)

NOTE

The module's coplanarity standard: ≤ 0.13 mm.

7.2. Recommended Footprint

7.2.1. Recommended Footprint of I4915Q Series

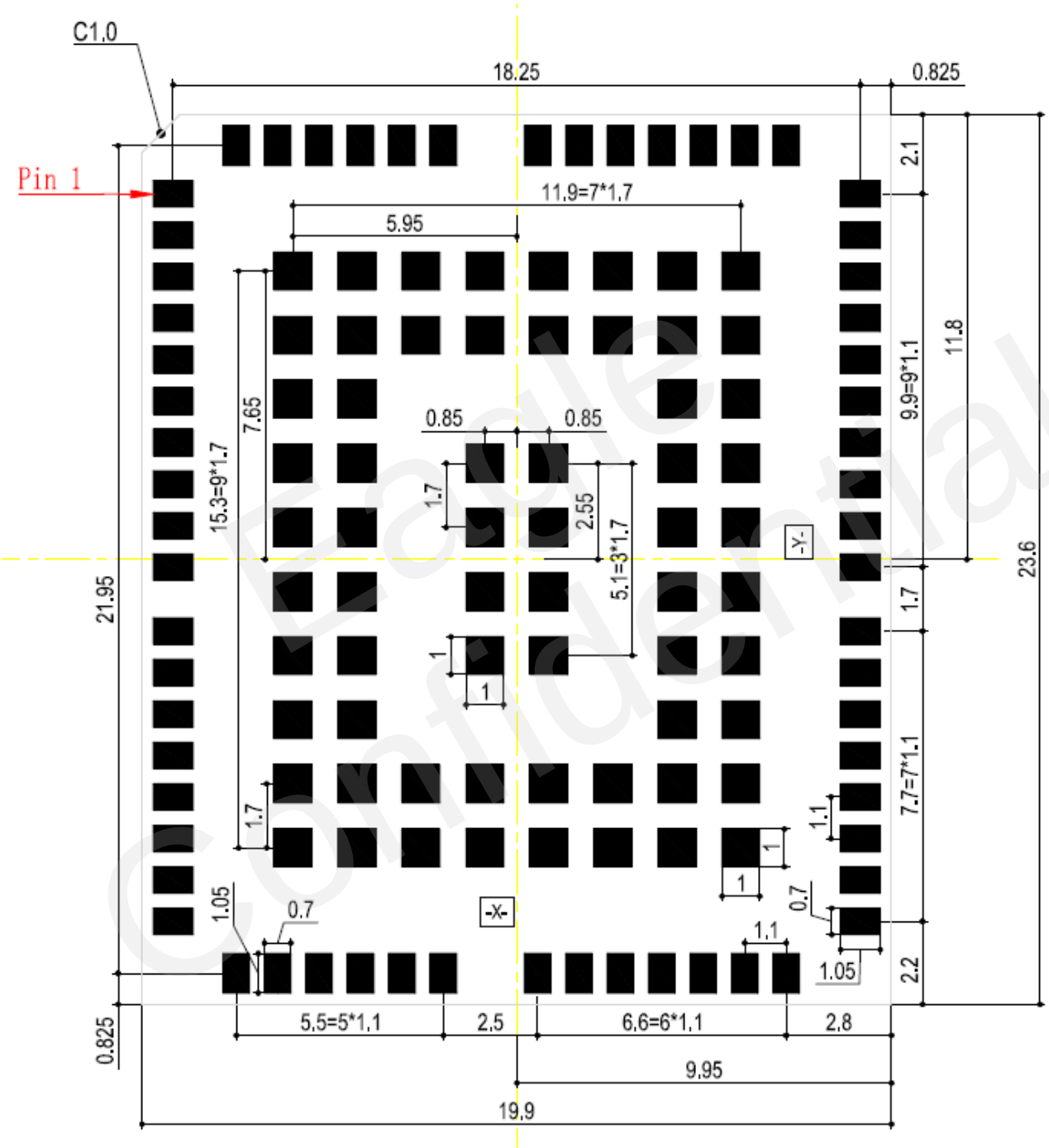


Figure 44: I4915Q Series Recommended Footprint (Unit: mm)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.2.2. Recommended Footprint of I4916Q-GL

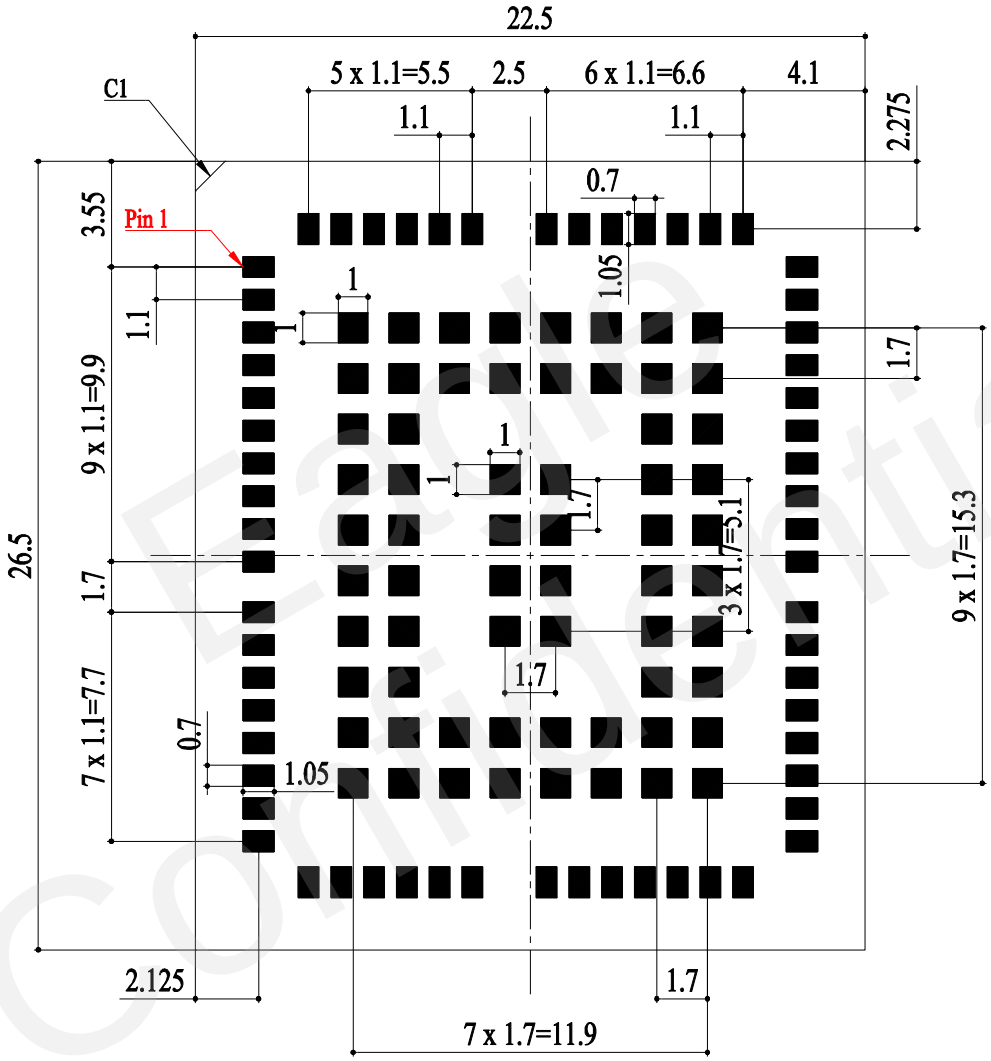


Figure 45: I4916Q-GL Recommended Footprint (Unit: mm)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

7.3.1. Top and Bottom Views of I4915Q Series

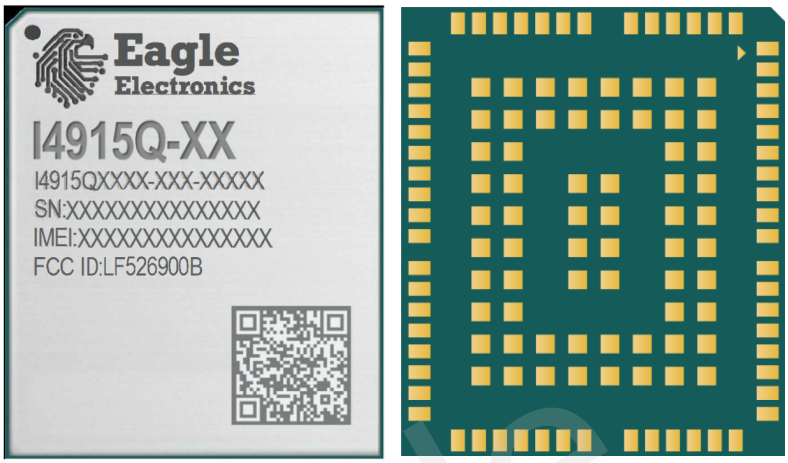


Figure 46: I4915Q Series Top and Bottom Views

7.3.2. Top and Bottom Views of I4916Q-GL

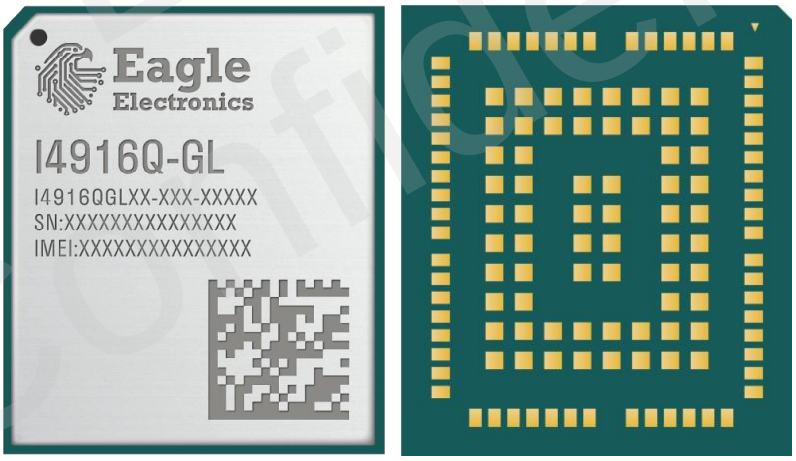


Figure 47: I4916Q-GL Top and Bottom Views

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Eagle.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [14] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 24 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[14] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [6]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

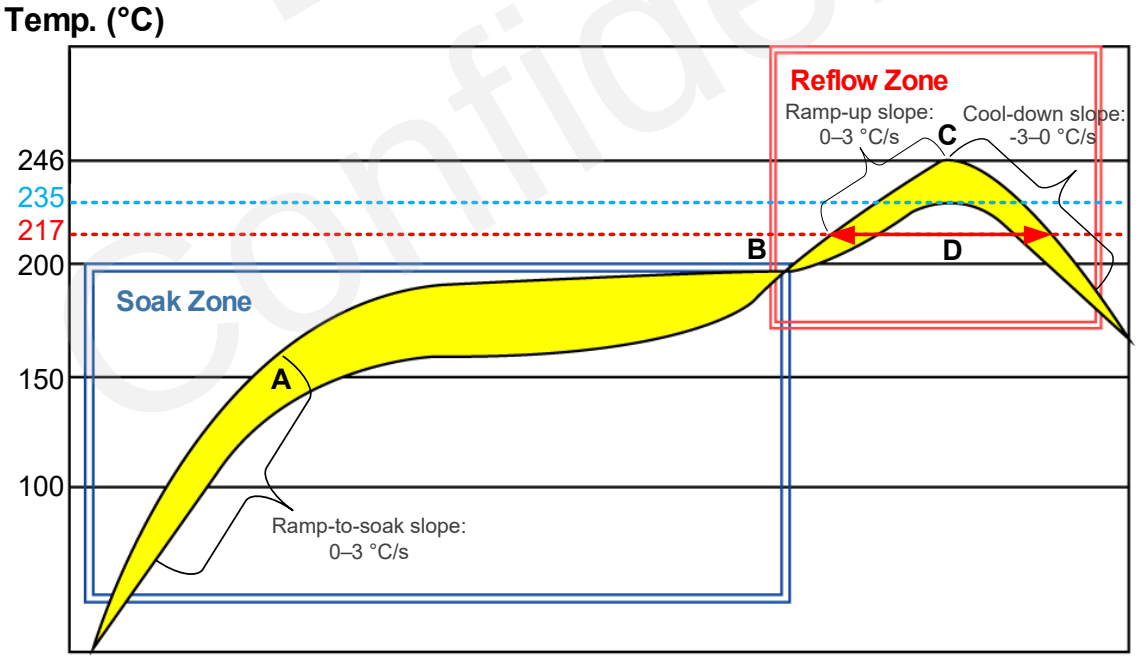


Figure 48: Recommended Reflow Soldering Thermal Profile

Table 50: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, never wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol and trichloroethylene. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do not use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.
8. Due to the complexity of the SMT process, contact Eagle Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective wave soldering, ultrasonic

soldering) that is not mentioned in ***document [7]***.

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

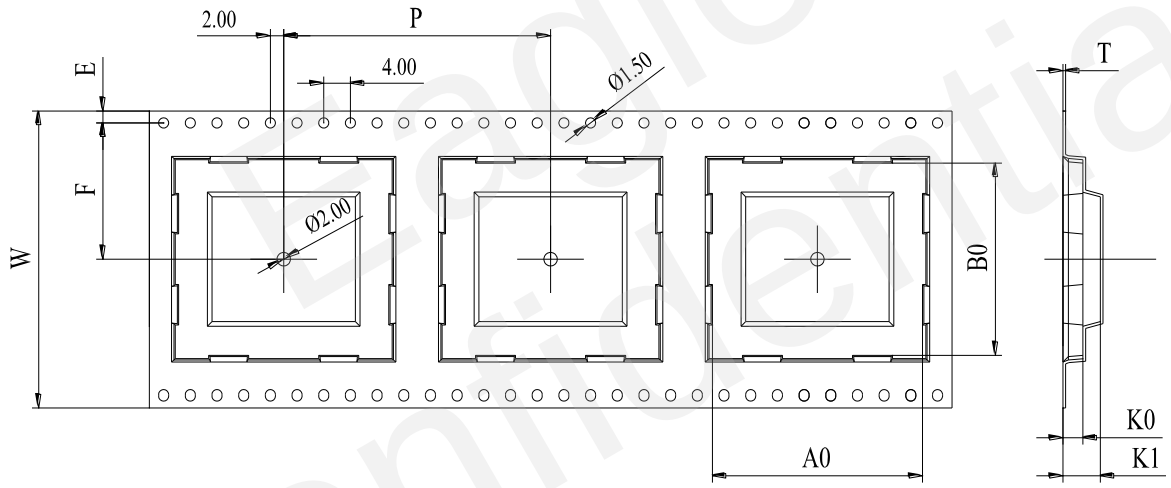


Figure 49: Carrier Tape Dimension Drawing (Unit: mm)

Table 51: Carrier Tape Dimension Table (Unit: mm)

Module Name	W	P	T	A0	B0	K0	K1	F	E
I4915Q Series	44	32	0.35	20.2	24	3.15	6.65	20.2	1.75
I4916Q-GL	44	32	0.35	22.8	26.8	3.1	6.9	20.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

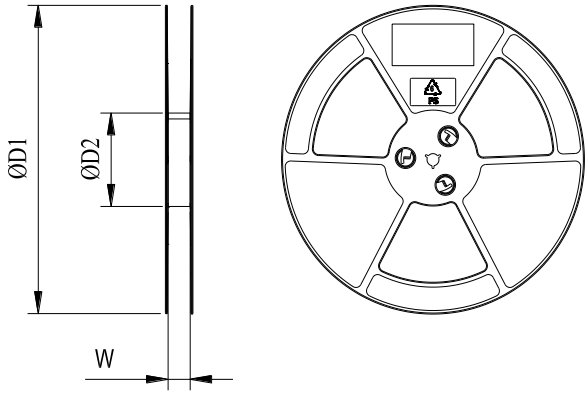


Figure 50: Plastic Reel Dimension Drawing

Table 52: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

8.3.3. Mounting Direction

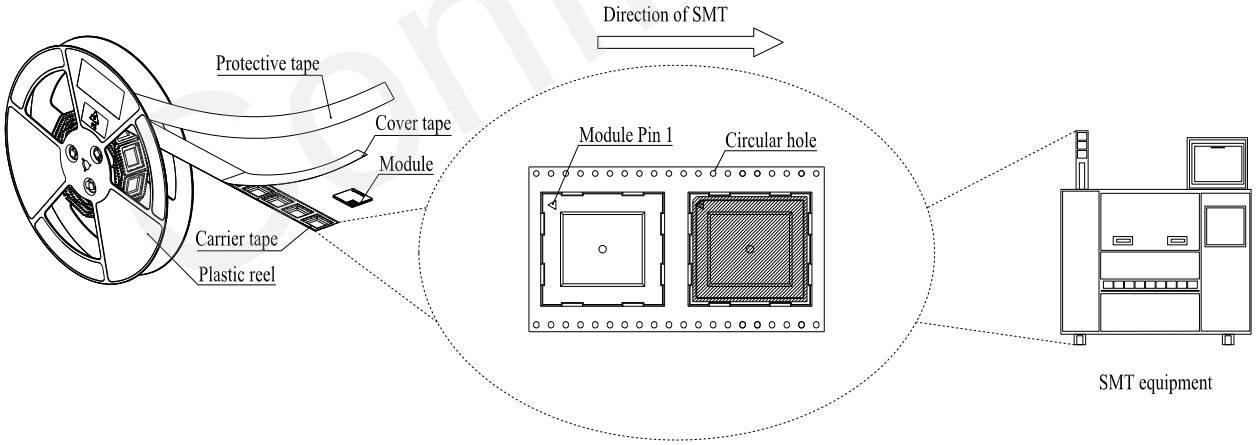
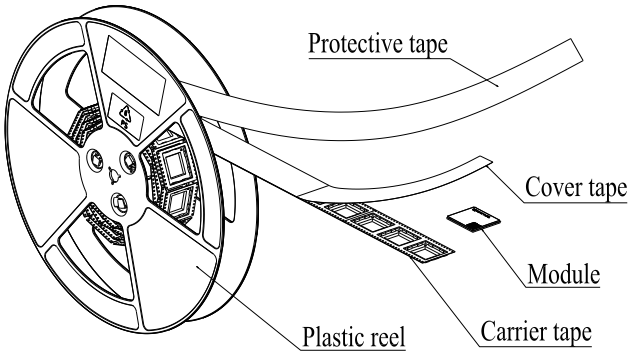


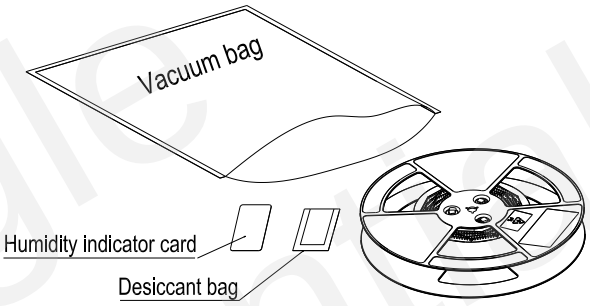
Figure 51: Mounting Direction

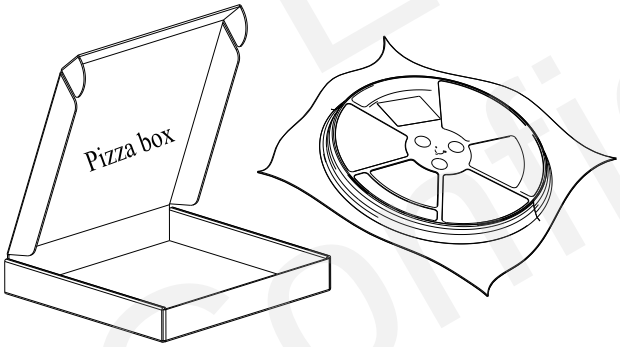
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 1000 modules.

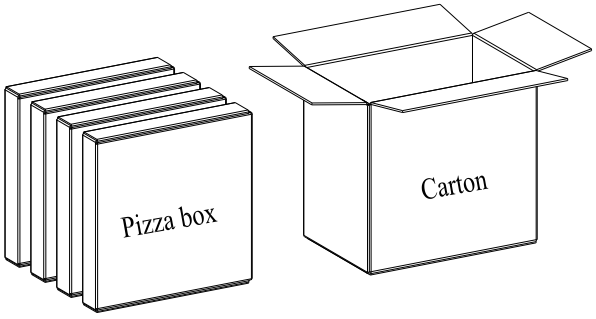


Figure 52: Packaging Process

9 Appendix References

Table 53: Related Documents

Document Name
[1] Eagle_UMTS&LTE_EVB_User_Guide
[2] Eagle_I491xQ_Series_AT_Commands_Manual
[3] Eagle_I491xQ_Series_PSM&eDRX_Application_Note
[4] Eagle_I491xQ_Series_GNSS_Application_Note
[5] Eagle_RF_Layout_Application_Note
[6] Eagle_Module_Stencil_Design_Requirements
[7] Eagle_Module_SMT_Application_Note

Table 54: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
ADC	Analog-to-Digital Converter
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection MUX
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over the Air
DL	Downlink
DRX	Discontinuous Reception

DSSS	direct-sequence spread spectrum
DTR	Data Terminal Ready
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FILE	File Protocol
FTP	File Transfer Protocol
FTPS	FTP over SSL
GRFC	General RF Control
HB	High Band
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
I2C	Inter-Integrated Circuit
I/O	Input/Output
IMT-2000	International Mobile Telecommunications 2000
LB	Low Band
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
MB	Middle Band
MCU	Microcontroller Unit
MO	Mobile Originated
MQTT	Message Queuing Telemetry Transport
MT	Mobile Terminated
NITZ	Network Identity and Time Zone
NTP	Network Time Protocol

PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PING	Packet Internet Groper
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RI	Ring Indicator
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTS	Request To Send
Rx	Receive
SMD	Surface Mount Device
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SPI	Serial Peripheral Interface
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TVS	Transient Voltage Suppressor
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UL	Uplink

UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
USIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
V_{IH}	High-level input voltage
V_{IL}	Low-level input voltage
V_{OH}	High-level output voltage
V_{OL}	Low-level output voltage
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{RWM}	Working Peak Reverse Voltage
VSWR	Voltage Standing Wave Ratio

A1 Addendum

Product Marketing Name: Quectel I4915Q-NA
FCC Certification Requirements.
According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.
And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based timeaveraging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.
2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.
3. A label with the following statements must be attached to the host end product: This device contains FCC ID: LF526900B
4. To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

radiation, maximum antenna gain (including cable loss) must not exceed: Operating Band	FCC Max Antenna Gain dBi
LTE Band 2	8.00
LTE Band 4	5.00
LTE Band 5	9.41
LTE Band 12	8.70
LTE Band 13	9.16
LTE Band 14	9.23
LTE Band 66	5.00
LTE Band 71	8.48

5. This module must not transmit simultaneously with any other antenna or transmitter
6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.
For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093
If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.
For this device, OEM integrators must be provided with labeling instructions of finished products.
Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:
A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above).
The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).
For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: LF526900B" or "Contains FCC ID: LF526900B" must be used.
The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.
The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.
The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.
This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.
To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier's Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.