FCC ID: LU9331223

Technical Description :

The brief circuit description is listed as follows :
- ANT1, ANT2 and ANT3 and associated circuit act as Loop Antennas and Matching Circuit for the tag reader.
- U1 W55MID50, XTAL1 and associated circuit act as RFID Reader & 13.56 MHz Oscillator.
- U2 RSC-4128 and associated circuit act as Speech Recognition Processor.
- U3 74HC374 and associated circuit act as 3-State Octal d-type Flip-Flop.
- U4 MR27V802F and associated circuit act as Programmed ROM.
- U5 SPY0030A and associated circuit act as Amplifier for Speaker.
- Q2(9014D), Q3(9014D), Q4(WPTS-565WC) and associated circuit act as Light Detector.
- S1 – S9, BZ1 and BZ2 act as Control Keys.
- Q4(9014D), Q5(8550D) and associated circuit act as Eye Motor Driver.
- Q1(3904), Q2(3904), Q3(8550D), Q4(8050D), Q5(8550D), Q6(8050D), Q7(3904) and associated circuit act as Body Motor Driver.
- Q1(9014D), Q2(A928) and associated circuit act as Lip Motor Driver.
- L1 and C1 act as Loop Antenna and Matching Circuit for the tag.
- U1 W55MID15 and associated circuit act as RFID Tag.

Antenna Used :

Loop antennas have been used.

General Description

Winbond *MFID*^{WB} (Magnetic Field Identification) series is used in all areas of automatic data capture allowing contactless identification of objects using magnetic field. From ticketing to industrial automation and access control, the applications of MFID are burgeoning. In recent years automatic identification procedures have become very popular in many service industries, purchasing and distribution logistics, industry, manufacturing companies and material flow systems.

W55MID50 is one of series in Winbond *MFID*^{WB} family that supports multi-functional Reader solution and especially focus on toy, security, and consumer related applications. The applications with Winbond *MFID*^{WB} Tag series such as W55MID10 that provides read-only mask ROM-ID version transponder for mass production solution in toy industrial, meanwhile W55MID15 provides the other solution for manufacture option, which is 243 bonding-ID selection transponder. Besides the single tag transponder application, W55MID35 offers multi-transponder recognition function for intelligent and smart toy applications.

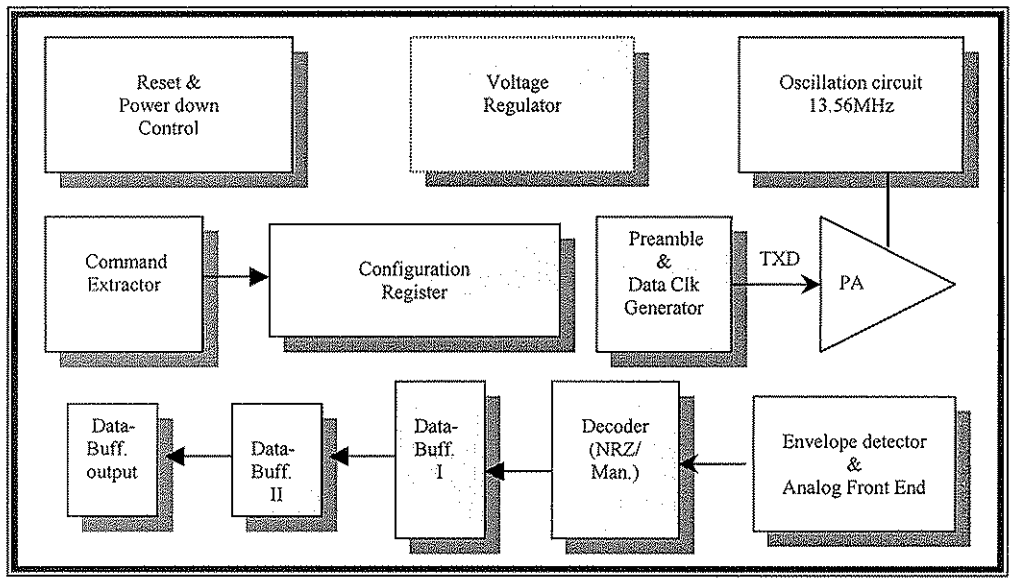
W55MID50 provides a wide variety of applications for toy, security, and consumer market meanwhile the W55MID50 is the most cost effective solution on current *MFID*^{WB} related application market.

1.1 W55MID50 Features

- Magnetic field resonance frequency: 13.56MHz
- Data clock: 22 ~ 66KHz
- Inductive coupled power supplies for transponder's no battery operation
- On-chip rectifier, voltage limiter, clock extraction, power management, uC interface
- Provides NRZ and Manchester coding data format
- Adjustable 4-level of Reader transmission power selection
- Provides serial and parallel mode uC interface
- uC data output rate ≥ 1Mbps
- Low power, low voltage operation
- Supports power-down mode ≤ 1uA
- Operating distance: 0 ~ 10cm
- Operating voltage: 2.4V ~ 5.5V
- Operating temperature: 0 ~ 70 °C
- Package: Dice form, PDIP-20, SOP-20
- Reference design PC board Size: 2.0x2.0cm^2 (without PCB antenna)
- Winbond patented "Automatic Reader Transmission Power Adjustment" for Reader optimum transmission power adjust
- Minimize external components

System Description

2.1 W55MID50 System Block Diagram



2.2 W55MID50 Functional Description

Transmission Power Amplifier (PA)

It provides 4 different selectable transmission power for Reader chip to support *MFID*^{WB} Tag's radiation power supply. The external inductor coupling circuit is designed for 13.56MHz magnetic field resonance. The coupled center frequency will depend on equivalent value of external PCB inductor and capacitor.

Envelope Detector & Analog Front End

The major function of this unit provides *MFID*^{WB} Tag's data can be extracted.

Voltage Regulator

The voltage regulator generates the system needs of device power supply.

Configuration Register

System configuration register controls the all functional settings of W55MID50 such as Tag data

format, Tag detection cycle, output data format, and PA transmission power selection.

Reset and Power-down Control

The function of system power-down control mode is normally used for power consumption saving.

Crystal Oscillation

The 13.56MHz system clock generator generates the need of device system clock.

Decoder NRZ/Manchester

This unit is in charge of Tag data format decoder, which can provide Tag-ID data format decoding of NRZ or Manchester.

Data Buffer and Output

This unit buffers the Tag-ID data, which is under de-frame processing.

General Description

MFID^{WB} (Magnetic Field Identification) is used in all areas of automatic data capture allowing contactless identification of objects using magnetic field. From ticketing to industrial automation and access control, the applications of MFID are burgeoning. In recent years automatic identification procedures have become very popular in many service industries, purchasing and distribution logistics, industry, manufacturing companies and material flow systems.

W55MID15 is one of Winbond *MFID*^{WB} (Magnetic Field Identification) series in *WinRF*^{WB} family that focus on toy and consumer related applications meanwhile W55MID15 provides manufacture bonding-ID transponder. Regarding the *MFID*^{WB} Reader series, the W55MID50 supports multi-functional *MFID*^{WB} Reader solution. Besides the single transponder application, W55MID35 offers multi-transponder recognition function for intelligent and smart toy applications.

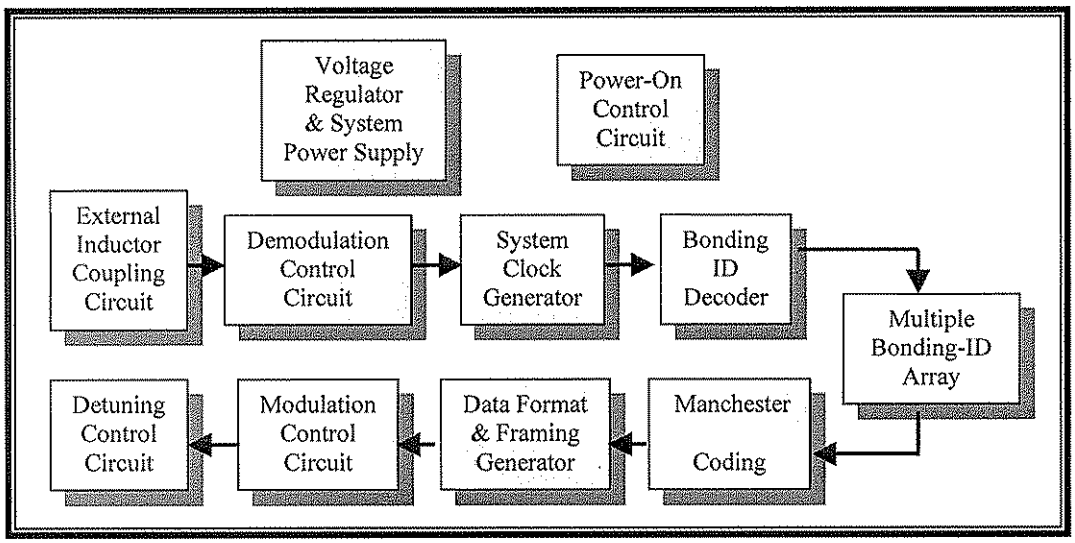
W55MID15 provides total 243 different bonding-IDs in manufacture and 10bit ID length in each ID. That can extremely save customer's design investment in consumer MFID related products.

1.1 W55MID15 Features

- Magnetic field resonance frequency: 13.56MHz
- Data clock: 32KHz
- Read-only bonding-ID transponder
- Inductive coupled power supply for no battery operation
- On-chip rectifier, voltage limiter, clock extraction
- 10bit bonding-ID length
- Provides Manchester coding data format
- RS0, RS1, RS2, RS3, and RS4 the 3-state bonding finger for the total 243 bonding-ID option in manufacture
- Low power, low voltage operation
- Operating distance: 0 ~ 5cm
- Operating temperature: 0 ~ 70 °C
- Package: Dice form
- Reference design PC board Size: 1.0x1.0cm^2 (with PCB antenna)
- Winbond patented "3-state Bonding Finger" for multiple bonding-ID option
- Minimize external component: capacitor and PCB antenna only

System Description

2.1 W55MID15 System Block Diagram



2.2 W55MID15 Functional Description

External Inductor Coupling Circuit

The external inductor coupling circuit is designed for 13.56MHz magnetic field resonance. The coupled center frequency will depend on equivalent inductor of external PCB inductor and a paralleled capacitor.

Voltage Regulator & System Power Supply

The voltage regulator generates the need of device power supply.

Power-On Control Circuit

System power-on control circuit initiates the device to get into initial state.

Demodulation Control Circuit

The demodulation control circuit demodulates the signal of command, which is magnetic field coupling from W55MID50 *MFID*^{WB} Reader system.

System Clock Generator

The system clock generator generates the need of device system clock.

Bonding-ID Decoder

The memory array decoder circuit decodes the mapping location of memory array, which indicates by external RS0, RS1, RS2, RS3, and RS4 the 3-state Bonding Finger (Winbond patented).

Multiple Bonding-ID Arrays

The multiple Bonding-IDs array provides total up to 243 different bonding-ID and 10bit in each ID.

Data Format and Framing Generator

The data format and framing generator is in charge of the entire bonding-ID and command data into a Winbond defined *MFID*^{WB} tag format.

Modulation Control Circuit

The modulation control circuit modulates the Winbond defined *MFID*^{WB} transponder format into the magnetic field resonation.

Electronic Characteristics

3.1 W55MID15 Absolute Maximum Ratings

Parameter	Rating	Unit
Maximum Current in COIL	10	mA
Power Dissipation (T_a = 70°C)	100	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-40 to +85	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

3.2 W55MID15 DC Characteristics

(VDD-VSS = 4.5 V, Ta = 25°C; unless otherwise specified)

Parameter	Sym.	Conditions	Min.	Typ.	Max.	Unit
Operating Magnetic Field	f_{OP}	Field in resonation	-	13.56	-	MHz
Operating Voltage	V_{DD}	Field in resonation	3	-	5.5	V
Operating Temperature	Tamb	Ambient operating temp	0	25	70	°C
Operating Current	I_{OP}	f_{OP} = 13.56MHz	-	2	-	uA
Magnetic Resonat Voltage	V_M		6	-	9	V

SENSORY®

RSC-4128
Speech Recognition Processor

Data Sheet

General Description

The RSC-4128 represents Sensory's next generation speech and analog I/O mixed signal processor. The RSC-4128 is designed to bring advanced speech I/O features to cost sensitive embedded and consumer products. Based on an 8-bit microcontroller, the RSC-4128 integrates speech-optimized digital and analog processing blocks into a single chip solution capable of accurate speech recognition; high quality, low data-rate compressed speech; and advanced music. Products can use one or all features in a single application.

The RSC-4128 supports Sensory Speech™ 7 technology, which includes advanced speech algorithms that add features and improve performance. Capable of running both new HMM and enhanced neural network technologies, accuracy in all kinds of noise is dramatically improved. New Speaker Verification technology is perfect for voice password security applications that must work in noisy environments. New high quality compressed speech technology reduces data rates by 5 times. New 8 voice MIDI-compatible music includes drum tracks, effectively increasing instruments beyond 8. Simultaneous music and speech rounds out the Sensory Speech™ 7 technology.

The RSC-4128 also supports the revolutionary capability of creating speaker independent recognition sets by simply typing in the desired recognition vocabulary! A few keystrokes creates a recognition set in seconds without the wait or cost of recording sessions to train the recognizer, speeding time to sales.

A new and unique Audio Wakeup feature listens while the RSC-4128 is in power down mode. When an audio event such as a clap or whistle occurs, Audio Wakeup will wakeup the RSC-4128 for speech or application tasks. Audio Wakeup is perfect for battery applications that require continuous listening and long battery life.

In addition to improved recognition performance, the RSC-4128 provides further on-chip integration of features. A complete speech I/O application can be built with as few additional parts as a clock crystal, speaker, microphone, and few resistors and capacitors.

Moreover, the RSC-4128 provides an unprecedented level of cost effective system-on-chip (SOC) integration, enabling many applications that require DSP and/or audio processing. The RSC-4128 may be used as a general-purpose mixed signal processor platform for custom algorithms, technologies and applications.

Features

Full Range of Sensory Speech™ 7 Capabilities

- Enhanced Word Spotting capability (10 SI or 4 SD words) in parallel
- Noise robust Speaker Independent, Dependent & Continuous Listening recognition
- Speaker Verification (SVWS) – Noise robust voice biometric security
- High quality, 3.7-7.8 kbps speech synthesis & sound effects with Sensory "SX" synthesis technology
- 8 voice MIDI-compatible music synthesis coincident with speech; drum track feature enables additional voices
- Voice record & playback
- Audio Wakeup from sleep

Integrated Single-Chip Solution

- 8-bit microcontroller
- ROMless, 128KByte and 256KByte ROM options
- 16 bit ADC, 10 bit DAC and microphone pre-amplifier
- Independent, programmable Digital Filter engine
- 4.8 KBytes total RAM (256Bytes "user" application RAM)
- Five timers (3 GP, 1 Watchdog, 1 Multi Tasking)
- Twin-DMA, Vector Math accelerator, and Multiplier
- Built-in Analog Comparator Unit (4 inputs)
- External memory bus: 20-bit Address(1Mbyte), 8-bit Data
- On chip storage for SD, SV, templates (10 templates)
- Code security through no ROM dump capability
- Uses low cost 3.58MHz crystal (internal PLL)
- Low EMI design for FCC and CE requirements
- 24 configurable I/O lines with 10 mA (typical) outputs
- Fully nested interrupt structure with up to 8 sources
- Optional Real Time Clock

Long Battery Life

- 2.4 – 3.6V operation
- 12mA (typical) operating current at 3V
- 2 low power modes; 1 µA typical sleep current

Full Suite of Quick & Powerful Tools

- Quick Text-to-SI (T2SI) text entry to build noise robust SI recognition sets – low cost & push-button – no recording!
- Quick Synthesis for push-button speech compression
- Integrated Development Environment, C Compiler, Debugger & In Circuit Emulator from Phyton, Inc.

RSC-4128 Overview

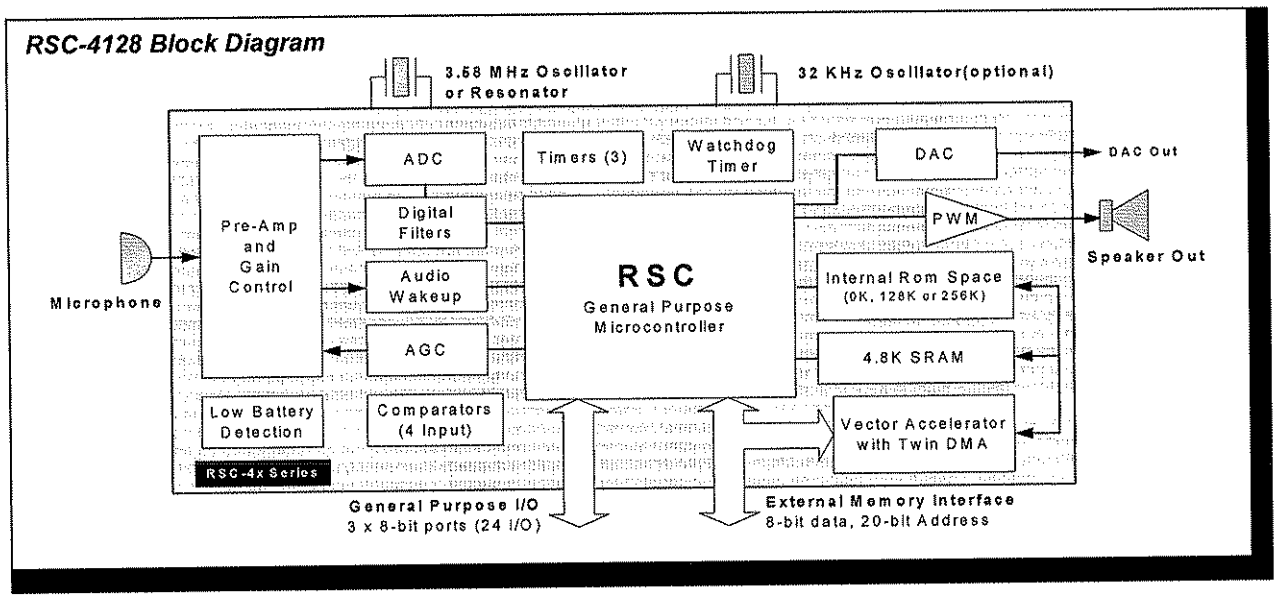
The RSC-4128 is a member of the Interactive Speech™ line of products from Sensory. It features a high-performance 8-bit microcontroller with on-chip ADC, DAC, preamplifier, RAM, ROM (except on ROM-less version), and optimized audio processing blocks. The RSC-4128 is designed to bring a high degree of integration and versatility into low-cost, power-sensitive applications. Various functional units have been integrated onto the CPU core in order to reduce total system cost and increase system reliability.

The RSC-4128 operates in tandem with Sensory Speech™ 7 firmware, an ultra compact suite of recognition and synthesis technologies. This reduced software footprint enables, for example, products with over 150 seconds of compressed speech, multiple speaker dependent and independent vocabularies, speaker verification, and all application code built into the RSC-4128 as a single chip solution. Revolutionary Text-to-Speaker-Independent (T2SI) technology allows the creation of SI recognition sets by simply entering text.

The CPU core embedded in the RSC-4128 is an 8-bit, variable-length-instruction microcontroller. The instruction set is similar to the 8051 microcontroller, and has a variety of addressing mode, *MOV* and 16 bit instructions. The RSC-4128 processor avoids the limitations of dedicated A, B, and DPTR registers by having completely symmetrical sources and destinations for all instructions.

The RSC-4128 provides a high level of on-chip features and special DSP engines, providing a very cost effective mixed signal platform for general-purpose applications and development of custom algorithms. The full suite of industry standard tools for easy product development makes the RSC-4128 an ideal platform for consumer electronics.

RSC-4128 Block Diagram



RSC-4128 Architecture

The RSC-4128 is a highly integrated speech and analog I/O mixed signal processor that combines:

- 8-bit microcontroller with enhanced instructions and interrupt control, superior register architecture, independent Digital Filter engine and "L1" Vector Math Accelerator
- On-chip ROM and RAM (4.8 Kbytes), and the ability to address off-chip RAM, ROM, EPROM or Flash.
- Input microphone preamp and 16 bit Analog-to-Digital Converter (ADC) for speech and audio/analog input
- 10 bit Digital-to-Analog Converter (DAC), and 10 bit Pulse Width Modulator (PWM) to directly drive a speaker or other analog device
- Low power Audio Wakeup from power down mode, when a selected audio event, such as clap or whistle, occurs

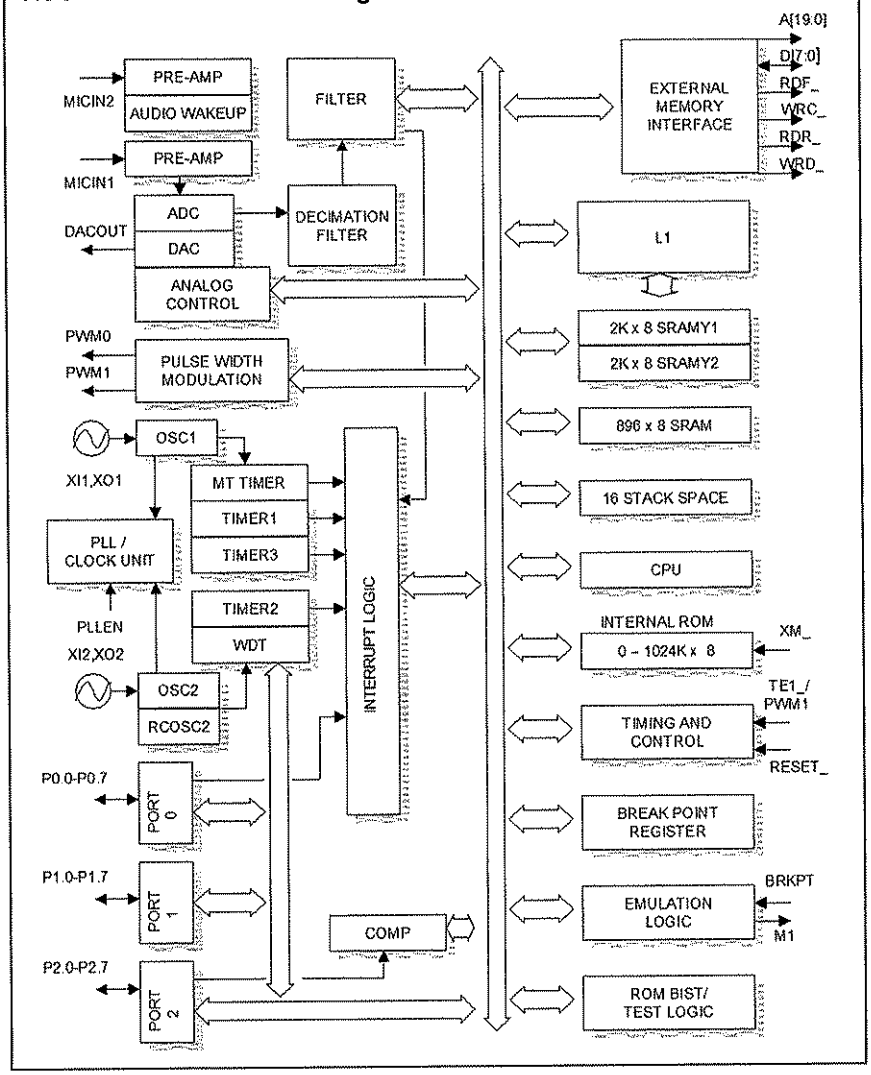
The RSC-4128 has 20-bit address and 8-bit data busses for interfacing with external memory. It includes an -XM input pin capable of enabling or disabling the internal ROM.

NOTE: Neither the -XM input pin nor the extended memory busses are available on 64-lead LQFP packaged versions of the RSC-4128 with internal ROM. These are available on the die and 100 LQFP versions.

Three bi-directional ports provide 24 configurable, general-purpose I/O pins to communicate with or control external devices with a variety of source and sink currents. Up to 4 of these I/O may be used as programmable Analog Comparator inputs. 16 may be used as I/O wakeup.

The RSC-4128 has a high frequency (14.32 MHz) clock as well as a low frequency (32,768 Hz) clock. The processor clock can be selected from either source, with a selectable divider value. The device performs speech recognition when running at 14.32 MHz. The RSC-4128 also supports programmable wait states to allow the use of slower memory.

RSC-4128 Internal Block Diagram



OSC1 is a very low-cost 3.58 MHz crystal oscillator which is used by a 4X PLL to generate the 14.32MHz clock. The OSC2 oscillator provides the options of using an external crystal or its own internal RC devices (no external components required for the internal RC mode).

There are three programmable, general-purpose 8-bit counters / timers – Timers 1 and 3 are derived from OSC1, and Timer2 from OSC2. There is also a Watchdog timer that may be used to exit an undesired condition in program flow, and Multi-tasking timer to allow chip operations to share resources in parallel.

A single chip speech I/O solution may be created with the RSC-4128. An external microphone passes an audio signal to the preamplifier and ADC to convert the incoming speech signal into digital data. Speech features are extracted using the Digital Filter engine. The microcontroller CPU processes these speech features using speech recognition algorithms in firmware, with the help of the "L1" Vector Accelerator and enhanced instruction set. The resulting speech recognition results may be used to control the consumer product application code, or to output speech or audio in the form of a dialog with the user of the consumer product. If desired, the output speech or audio signal from the RSC-4128 is generated by a DAC for external amplification into a speaker, or a PWM capable of directly driving a speaker at typical consumer product volumes. A typical product will require about $0.30 - $1.00 (in high volume) of additional components, in addition to the RSC-4128.

The RSC-4128 also provides a very cost effective mixed signal platform for general-purpose applications and development of custom algorithms. A typical general purpose application will require about $0.30 - $0.50 (in high volume) of additional components, in addition to the RSC-4128.

Octal D-type flip-flop; positive edge-trigger; 3-state

74HC/HCT374

FEATURES

- 3-state non-inverting outputs for bus oriented applications
- 8-bit positive, edge-triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT374 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT374 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CP) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The "374" is functionally identical to the "534", but has non-inverting outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay CP to Q_n	C_L = 15 pF; V_{CC} = 5 V	15	13	ns
f_{max}	maximum clock frequency		77	48	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	17	17	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

Octal D-type flip-flop; positive edge-trigger; 3-state

74HC/HCT374

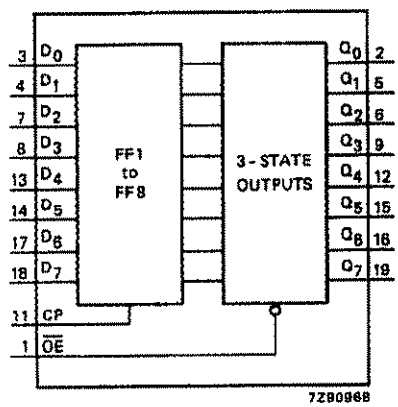


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 to Q_7
load and read register	L	↑	l	L	L
	L	↑	h	H	H
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

Notes

1. H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
   Z = high impedance OFF-state
   ↑ = LOW-to-HIGH CP transition

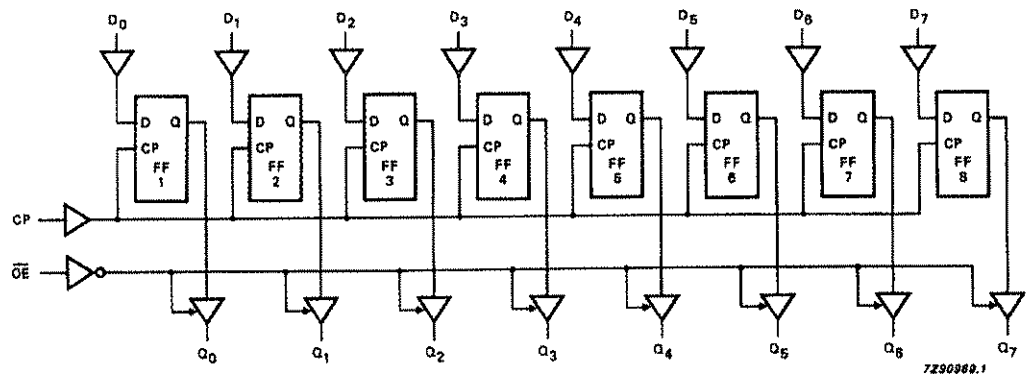


Fig.5 Logic diagram.

OKI

Oki, Network Solutions for a Global Society

OKI Semiconductor

FEDR27V802F-02-03
Issue Date: Jul. 9, 2004

MR27V802F

512k-Word × 16-Bit or 1M-Word × 8-Bit P2ROM

FEATURES

·512k-word × 16-bit / 1M-word × 8-bit electrically switchable configuration
· +3.0 V to 3.6 V power supply
· Access time 70 ns MAX
· Operating current 18 mA MAX(5MHz)
· Standby current 5 µA MAX
· Input/Output TTL compatible
· Three-state output

PACKAGES

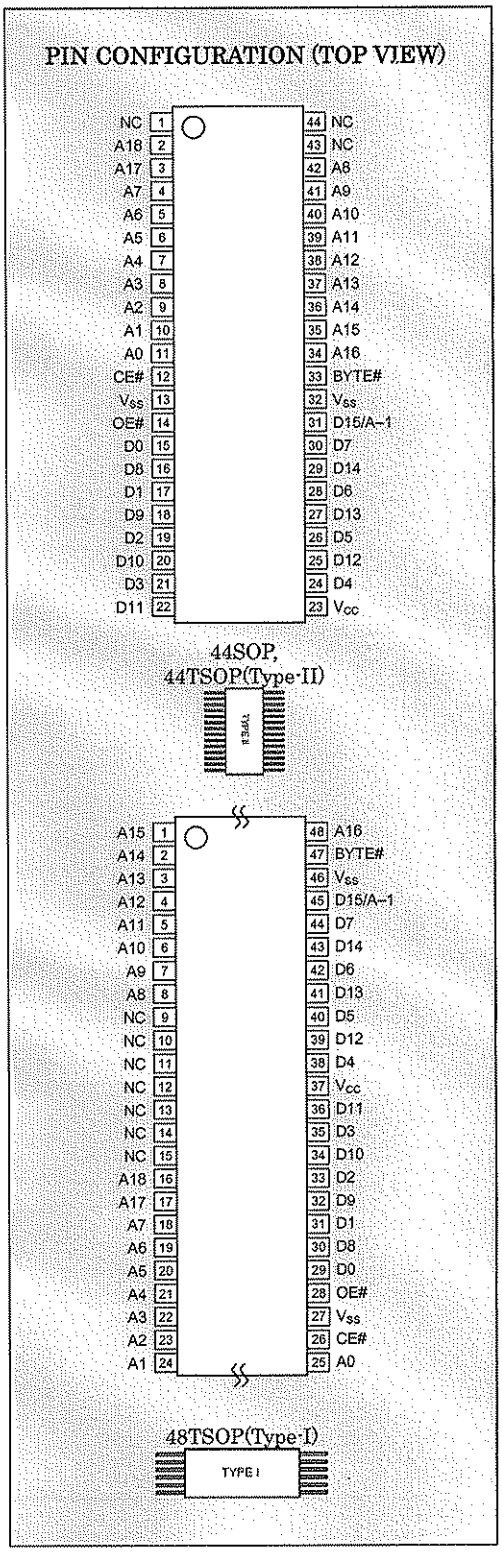
· MR27V802F-xxxTN
  48-pin plastic TSOP (TSOP I 48-P-1220-0.50-1K)
· MR27V802F-xxxMA
  44-pin plastic SOP (SOP44-P-600-1.27-K)
· MR27V802F-xxxTP
  44-pin plastic TSOP (TSOP II 44-P-400-0.80-K)

P2ROM ADVANCED TECHNOLOGY

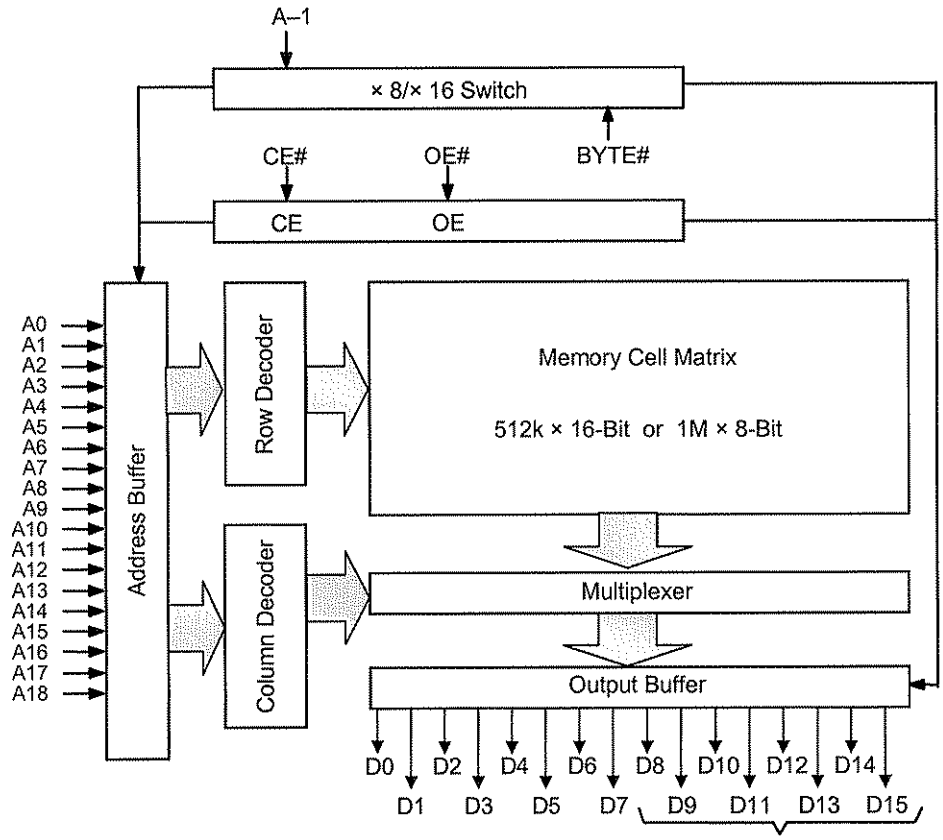
P2ROM stands for Production Programmed ROM. This exclusive Oki technology utilizes factory test equipment for programming the customers code into the P2ROM prior to final production testing. Advancements in this technology allows production costs to be equivalent to MASKROM and has many advantages and added benefits over the other non-volatile technologies, which include the following;

- **Short lead time,** since the P2ROM is programmed at the final stage of the production process, a large P2ROM inventory "bank system" of un-programmed packaged products are maintained to provide an aggressive lead-time and minimize liability as a custom product.
- **No mask charge,** since P2ROMs do not utilize a custom mask for storing customer code, no mask charges apply.
- **No additional programming charge,** unlike Flash and OTP that require additional programming and handling costs, the P2ROM already has the code loaded at the factory with minimal effect on the production throughput. The cost is included in the unit price.
- **Custom Marking is** available at no additional charge.
- **Pin Compatible with Mask ROM** and some FLASH products.

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



In 8-bit output mode, these pins are placed in a high-Z state and pin D15 functions as the A-1 address pin.

PIN DESCRIPTIONS

Pin name	Functions
D15 / A–1	Data output / Address input
A0 to A18	Address inputs
D0 to D14	Data outputs
CE#	Chip enable input
OE#	Output enable input
BYTE#	Word / Byte select input
V_{CC}	Power supply voltage
V_{SS}	Ground
NC	No connect