PAWN 101 -400
Service Manual

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MADE IN ISRAEL
by HEAD CONNECTION SYSTEMS LTD.

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SPECIFICATIONS

1) General

8 CH. Within 462.56-465.71 MHz (PAWN101-460)

Modulation:	FM (F3E)
DC Power Source:	3.6V ~ 4.5 Volts (internal battery)
Current Consumption:	TX/approx. 100mA (Low Power @4.5VDC)
	500mA (Hi Power @4.5VDC)
	RX/approx. 33mA (squelched)
Weight:	Approx. 400 gr. (inc. batteries)
Speaker:	internal speakers 220Ω X 2 (parallel)
Microphone	Noise canceling gooseneck microphone 200Ω.

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2) Transmitter (per transceiver)

Output Power:	500mW (Hi Power with 4.5V DC) (PAWN101-460)
Modulator:	variable Reactance
Max. Deviation:	±5KHz (PAWN101-433)
	±2.5KHz (PAWN101-460)

3) Receiver

Configuration:	Double Conversion Superheterodyne
Intermediate Frequency:	First: 21.7MHz / Second: 450KHz
Sensitivity:	Better than –15dBμ (12dB SINAD)
AF output:	Not less than 100mW(@10% distortion@110Ω)

PAWN-101 460 - Antenna description

Helical Antenna
Frequency coverage 430-470 MHz
Omni-Directional
Sizes - 95 mm in length
6 mm in diameter

Note: Specifications are subject to change without notice or obligation.

CIRCUIT DESCRIPTION (per transceiver)

1) Receiver System

The receiver system is a double superheterodyne.
The first IF is 21.7MHz and the second is 450KHz.

1. Front End

The signal from the antenna is passed through a low-pass filter and input to RF coil L108.
The signal from L108 is amplified by Q104, Q103 and led to the band pass filter, from there to the first mixer base of Q101.

2. First mixer

The amplified signal (f0) by Q104, Q103 is mixed with the first local oscillator signal (f0-21.7MHz) from PLL circuit by the first stage mixer Q101 and so is converted into the first IF signal.
The unwanted frequency band of the first IF signal is eliminated by the monolithic crystal filter FL101, and led to the IF amplifier Q201.

3. IF circuit

The first IF signal is amplified by Q201, and input to pin 16 of IC203 where it is mixed with the second local oscillator signal (21.25MHz) and so is converted into second IF signal (450KHz).
The second IF signal is output from pin 3 of IC203, and the unwanted frequency band of second IF signal is eliminated by ceramic filter FL102.
The resulting signal is than amplified by the second IF limiting amplifier, and detected by quadrature circuit
The audio signal if output from pin 9 of IC203.

4. Audio circuit

The detected signal from IC203 (the active receiver) is passed through low-pass active filter in U10 and output (U10 pin 5) to main volume SW1 than led to the power amplifier U4, which is, switched ON/OFF by CD signal from U1.

5. C.T.C.S.S circuit

While the RX signal passes through U10 it is being tested to carry a sub-tone signal (77Hz). when it is detected it causes U10 pin 14 (TSQD) to become low.

6. Carrier detect

The signal comes from the receiver delayed for 50ms to ensure that the signal is real and not temporary noise.

2) PLL, Synthesizer

Output frequency of PLL circuit is set by the serial data from the C.P.U PLL circuit consists of VCO Q401, buffer amplifier Q301.

The pulse wave output of charge pump is converted to DC voltage by PLL loop filter circuit, and supplied to D402, D401 of varicap diode in VCO unit. The frequency modulation is executed when audio signal voltage is supplied to the varicap D403. When PLL is unlocked, pin 7 of IC201 goes “high”.

3) Transmitter system

1. Microphone amplifier

The voice from the microphone is led to the pre-emphasis circuit, and then input to the microphone amplifier U7, which is consist of two operation amplifier. The output from the amplified microphone is passed through variable resistor VR1 for modulation adjustment to varicap diode of the VCO.

2. Power amplifier

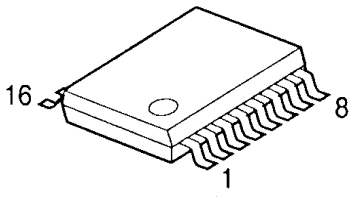
The signal from VCO is passed through TX/RX switch circuit D201. The signal is than amplified by IC202 and input to power amplifier Q202 and then passed through the low-pass filter, the antenna switch circuit and the output low-pass filter. The unwanted harmonics frequency signal is eliminated by low-pass filter and input to the antenna.

SEMICONDUCTOR DATA

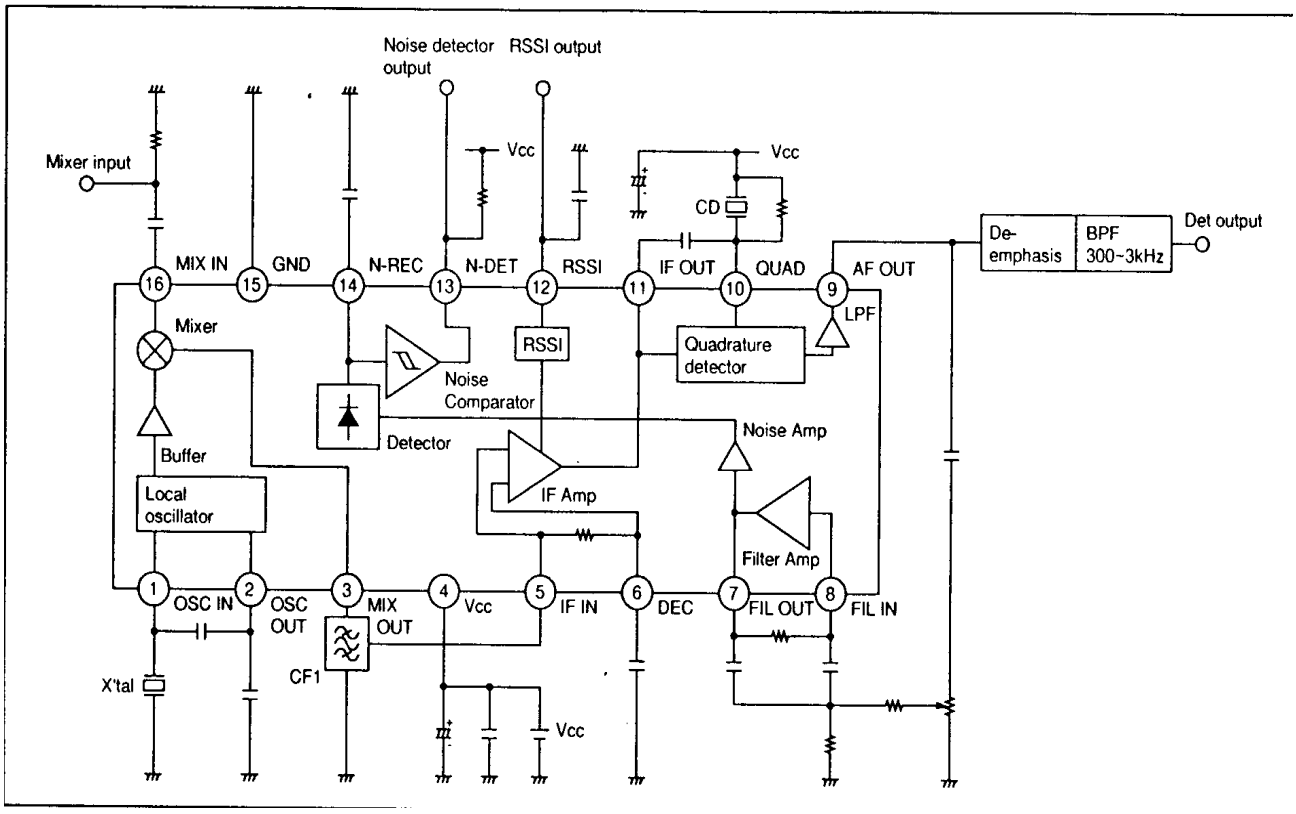
1) TA31136FN Receiver

TA31136FN

Low Power FM IF



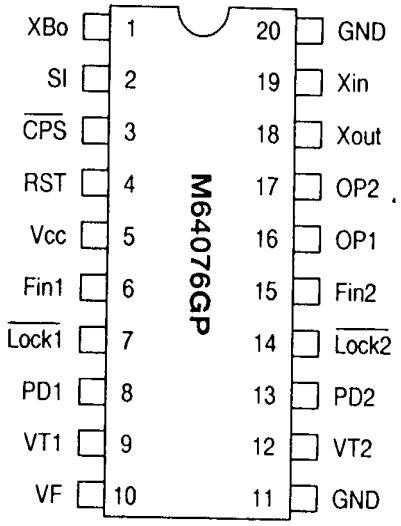
Block Diagram



2) M64076GP Synthesizer

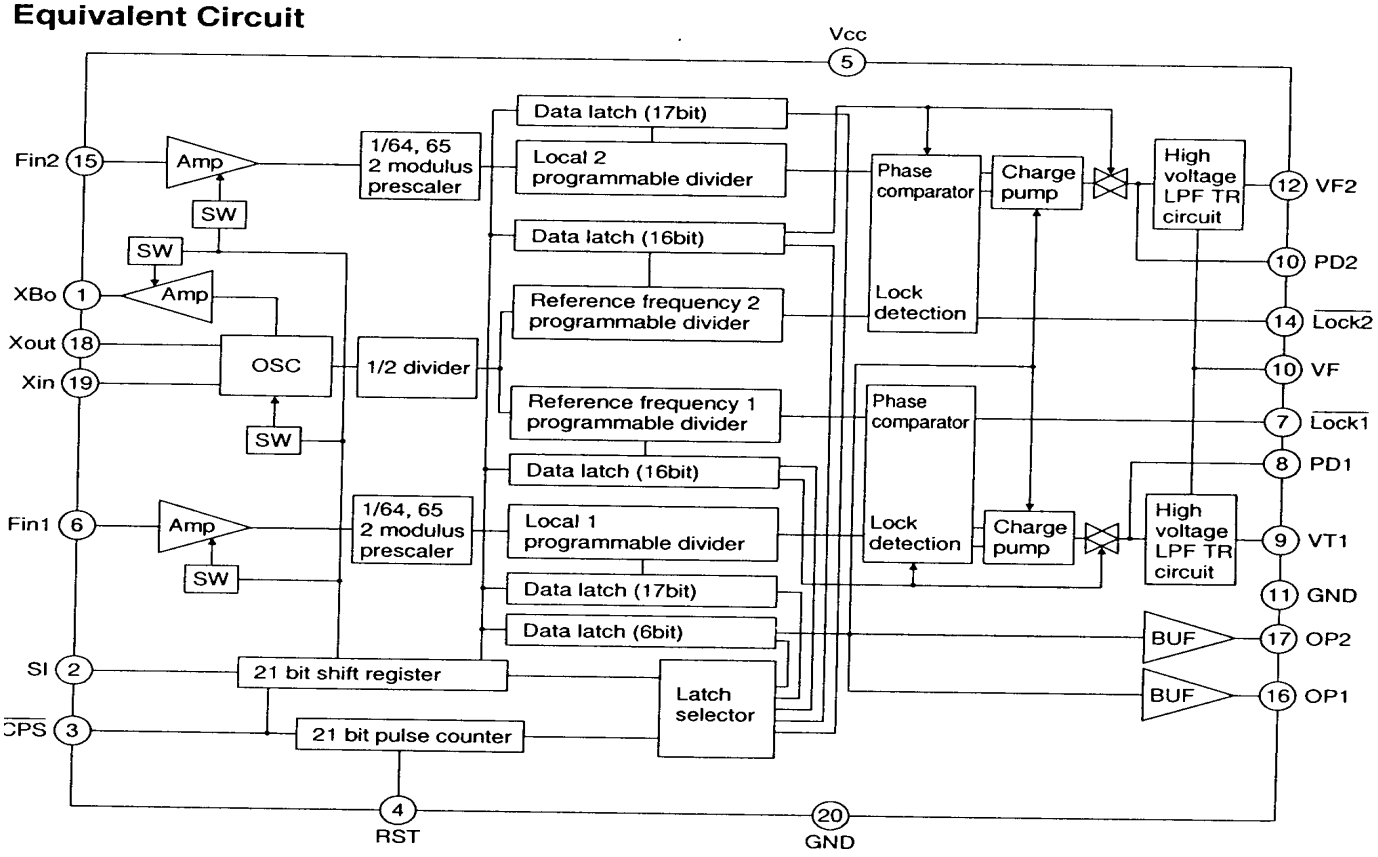
M64076GP

Dual PLL Synthesizer



Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	Vcc	Fin=80~520MHz Vin=– 10dBm	2.7	-	5.5	V
LPF supply voltage	VF		-	9	12	V
Local oscillator input level	Vin	Fin=80~520MHz Vcc=2.7~5.5V	– 20	-	– 4	dBm
Local oscillator input frequency	Fin	Vin=-20~– 4dBm Vcc=2.7~5.5V	80	-	520	MHz
Xin input level	Vxin	Vcc=2.7~5.5V Fxin=10~25MHz Sine wave	0.4	-	1.4	Vp-p
Xin input frequency	Fxin	Vcc=2.7~5.5V Vxin=0.4~1.4Vp-p	10	-	25	MHz

Equivalent Circuit



3) MC34119D
AUDIO POWER AMPLIFIER

MC34119

Low Power Audio Amplifier
Silicon Monolithic Integrated Circuit

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The MC34119 is a low power audio amplifier integrated circuit intended (primarily) for telephone applications, such as in speakerphones. It provides differential speaker outputs to maximize output swing at low supply voltages (2.0 volts minimum). Coupling capacitors to the speaker are not required. Open loop gain is 80 dB, and the closed loop gain is set with two external resistors. A Chip Disable pin permits powering down and/or muting the input signal. The MC34119 is available in a standard 8–pin DIP or a surface mount package.

- Wide Operating Supply Voltage Range (2 – 16 Volts) — Allows Telephone Line Powered Applications
- Low Quiescent Supply Current (2.7 mA Typical) for Battery Powered Applications
- Chip Disable Input to Power Down the IC
- Low Power–Down Quiescent Current (65 µA Typical)
- Drives a Wide Range of Speaker Loads (8 Ohms and Up)
- Output Power Exceeds 250 mW with 32 Ohm Speaker
- Low Total Harmonic Distortion (0.5% Typical)
- Gain Adjustable from < 0 dB to > 46 dB for Voice Band
- Requires Few External Components

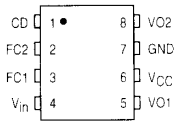
P SUFFIX
PLASTIC DIP
CASE 626

D SUFFIX
SOIC PACKAGE
CASE 751

ORDERING INFORMATION

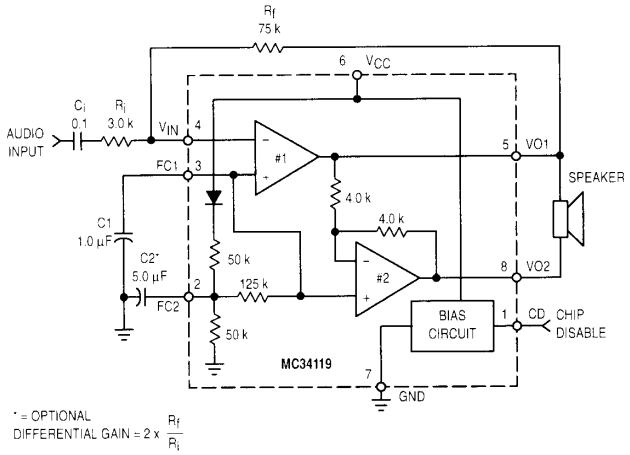
MC34119P	Plastic DIP
MC34119D	Plastic SOIC

PIN ASSIGNMENT



(TOP VIEW)

BLOCK DIAGRAM AND TYPICAL APPLICATION CIRCUIT



* = OPTIONAL
DIFFERENTIAL GAIN = $2 \times \frac{R_f}{R_i}$

4) LMC662 AMPLIFIER

National Semiconductor

LMC662 CMOS Dual Operational Amplifier

General Description

The LMC662 CMOS Dual operational amplifier is ideal for operation from a single supply. It operates from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain into realistic loads (2 kΩ and 600Ω) are all equal to or better than widely accepted bipolar equivalents.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC660 datasheet for a Quad CMOS operational amplifier with these same features.

Features

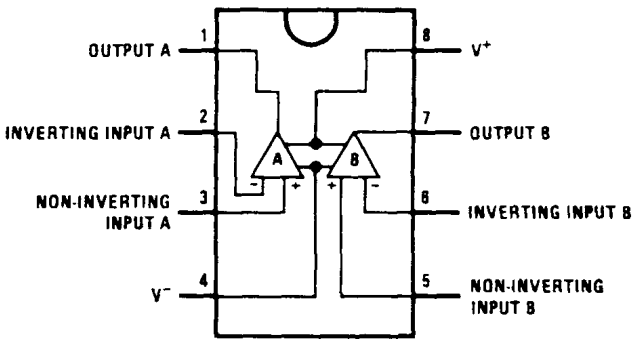
- Rail-to-rail output swing
- Specified for 2 kΩ and 600Ω loads
- High voltage gain 126 dB
- Low input offset voltage 3 mV
- Low offset voltage drift 1.3 μV/°C
- Ultra low input bias current 2 fA
- Input common-mode range includes V^-
- Operating range from +5V to +15V supply
- I_{SS} = 400 μA/amplifier; independent of V^+
- Low distortion 0.01% at 10 kHz
- Slew rate 1.1 V/μs
- Available in extended temperature range (−40°C to +125°C); ideal for automotive applications
- Available to a Standard Military Drawing specification

Applications

- High-impedance buffer or preamplifier
- Precision current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls
- Automotive sensors

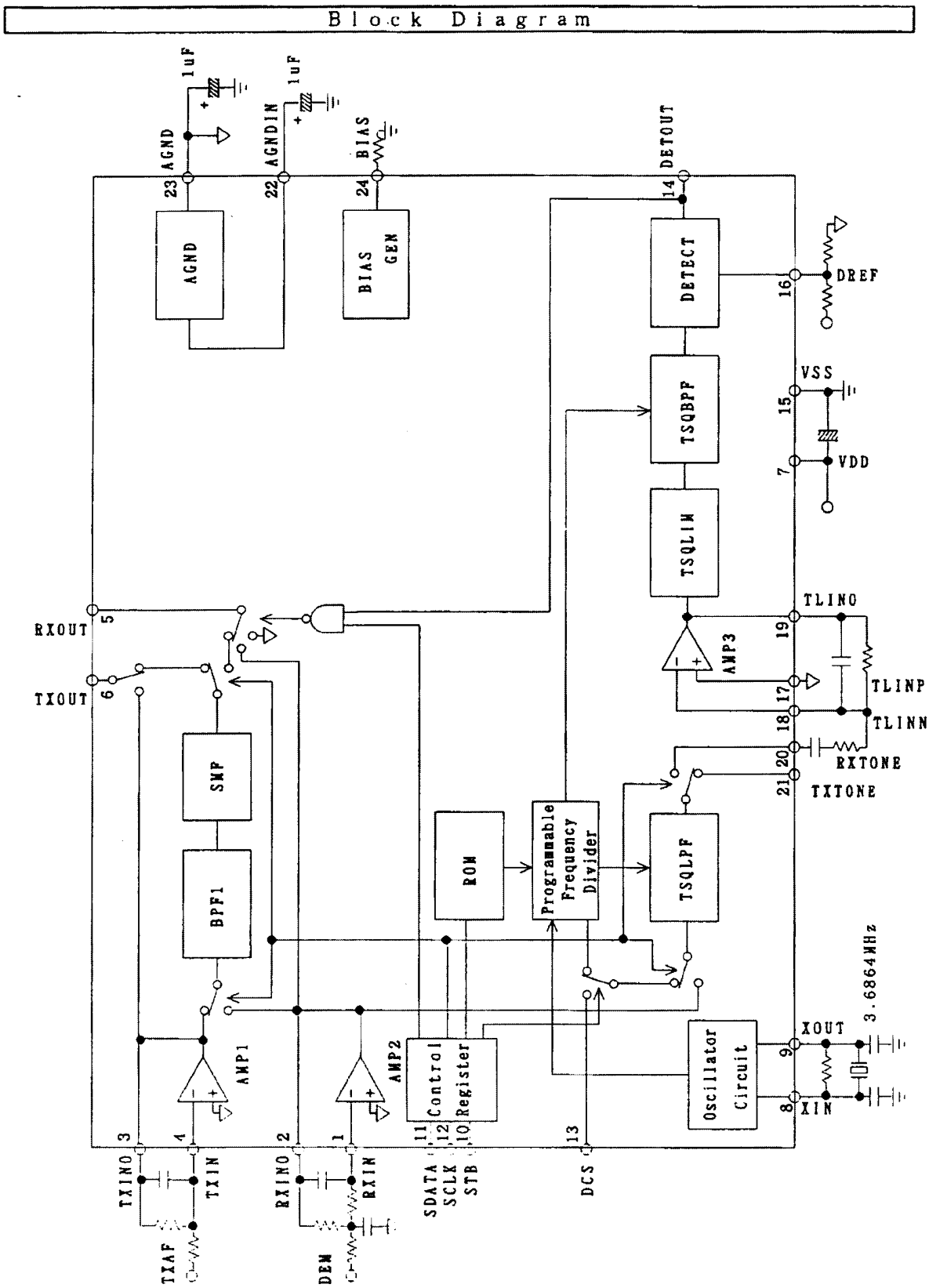
Connection Diagram

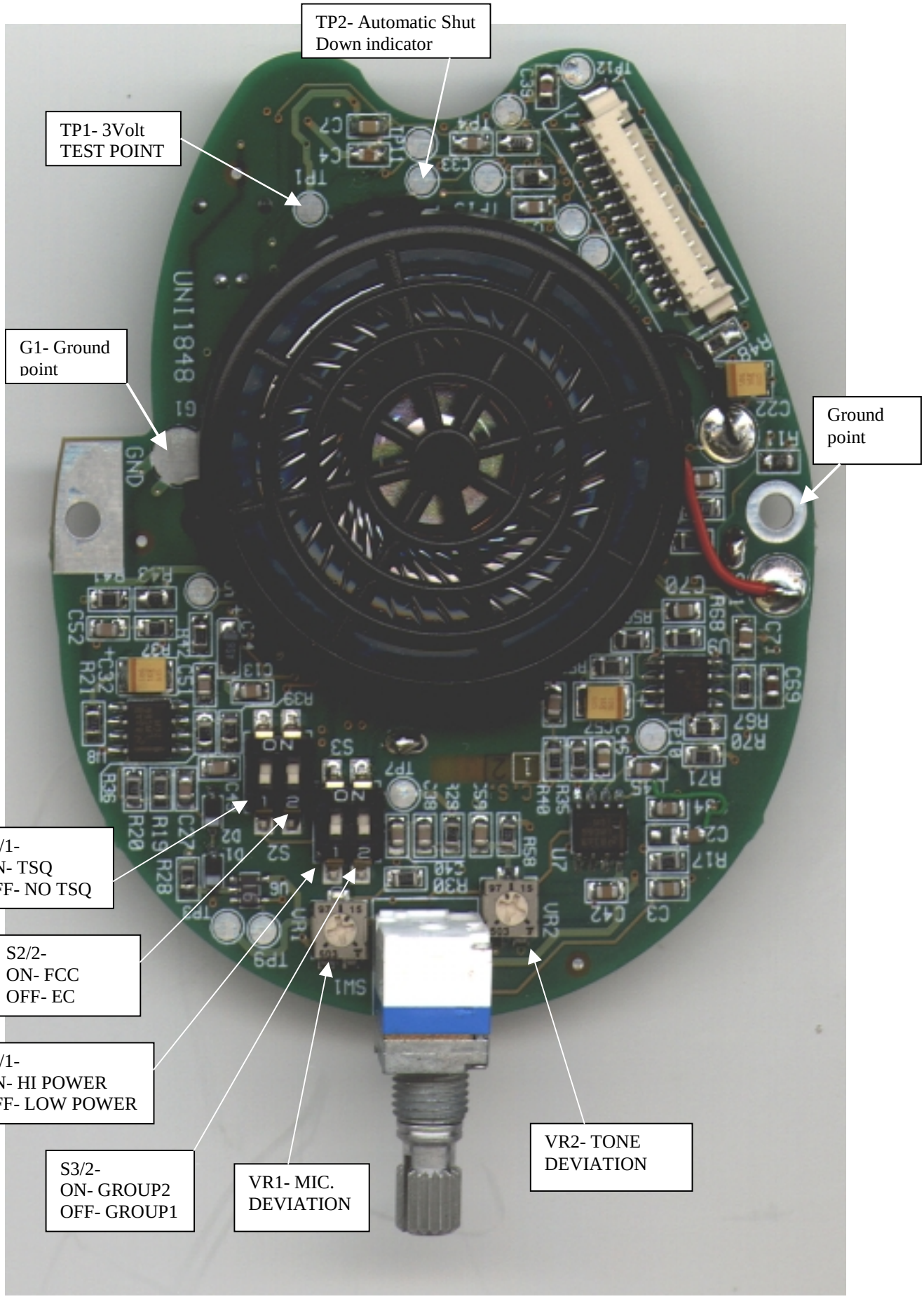
8-Pin DIP/SO

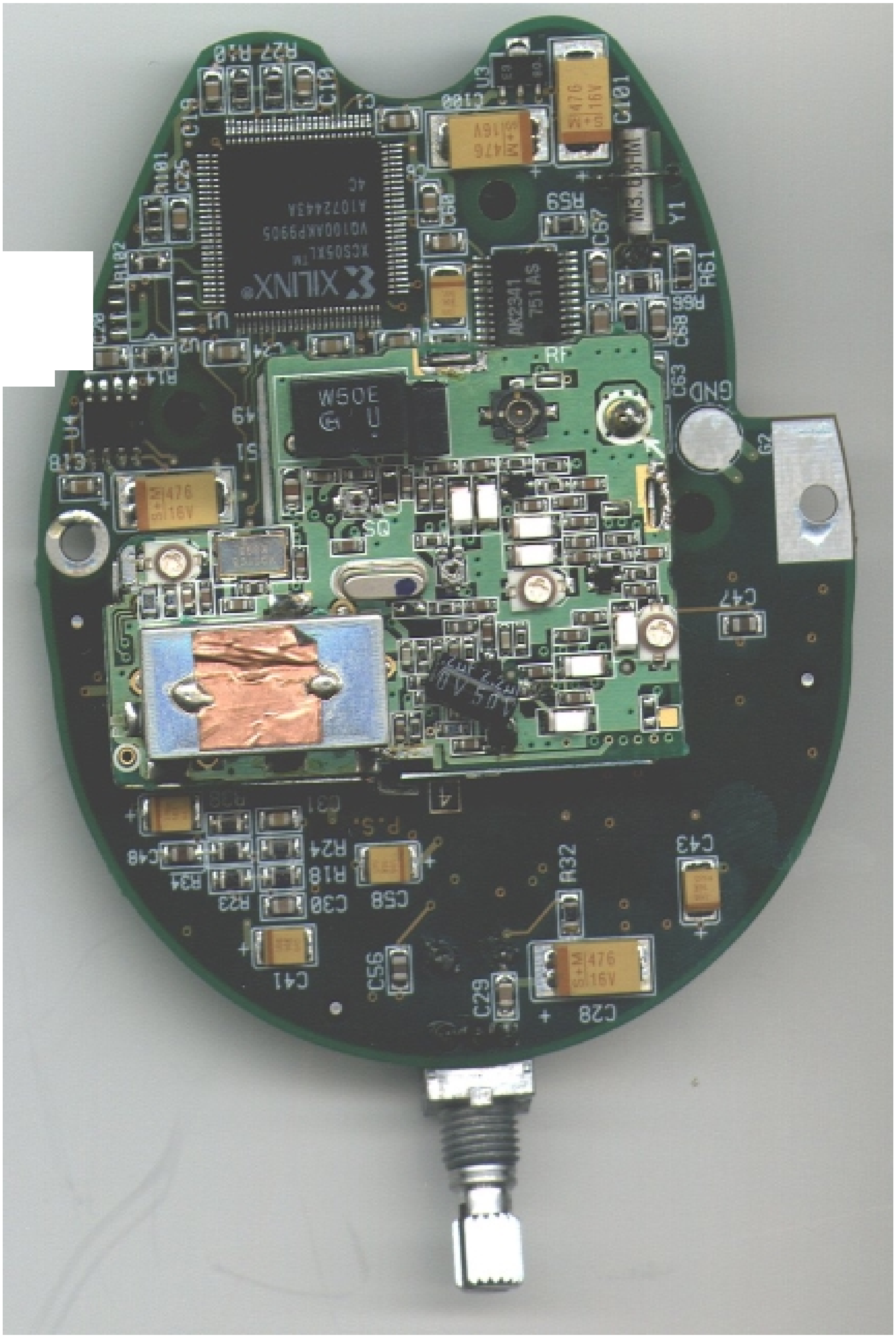


TL/H/9763–1

5) AK2341 C.T.C.S.S TONE ENCODER/DECODER




TP2- Automatic Shut Down indicator
TP1- 3Volt TEST POINT
G1- Ground point
Ground point
S2/1-
ON- TSQ
OFF- NO TSQ
S2/2-
ON- FCC
OFF- EC
S3/1-
ON- HI POWER
OFF- LOW POWER
S3/2-
ON- GROUP2
OFF- GROUP1
VR1- MIC. DEVIATION
VR2- TONE DEVIATION


XILINX
RF
GND
SQ
C47
C43
R32
C28
C41
P.S.
476
16V